ESD2CANFD24 24-V, 2-Channel ESD Protection Diode for In-Vehicle Networks

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±25-kV contact discharge
  - ±25-kV air-gap discharge
- Tested in compliance to IEC 61000-4-5
- 24 V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 2.5 pF (typical)
- SOT-23 (DBZ) small, standard, common footprint
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- Industrial control networks:
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4

3 Description

The ESD2CANFD24 is a bidirectional ESD protection diode for Controller Area Network (CAN) interface protection. The ESD2CANFD24 is rated to dissipate contact ESD strikes beyond the maximum level specified in the IEC 61000-4-2 standard (±25-kV Contact, ±25-kV Airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key as systems require a high level of robustness and reliability for safety applications.

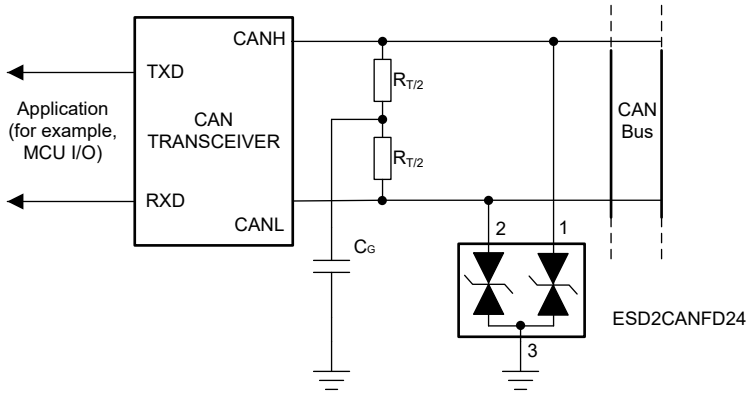
This device features a low IO capacitance per channel and a pin-out to suit two CAN bus lines (CANH and CANL) from the damage caused by ElectroStatic Discharge (ESD) and other transients. Additionally, the 2.5 pF (typical) or less line capacitance of the ESD2CANFD24 is suitable for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10 Mbps.

The ESD2CANFD24 is offered in a leaded package for easy flow through routing.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD2CANFD24	DBZ (SOT-23, 3)	2.92 mm × 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



ESD2CANFD24 Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
November 2022	*	Initial Release

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5 Pin Configuration and Functions

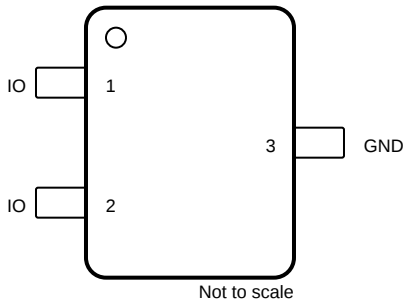


Figure 5-1. DBZ Package, 3-Pin SOT-23 (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C	ESD2CANFD24		133	W
I_{PP}	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C			3.5	A
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	
T_{stg}	Storage temperature		-65	155	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002 (2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufactuuring with a standard ESD control proccess.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufactuuring with a standard ESD control proccess.

6.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

Parameter		Test Conditions	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD2CANFD24	±25000	V
		IEC 61000-4-2 Air-gap Discharge, all pins		±25000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD2CANFD24 DBZ (SOT-23) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	316.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	170.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	156.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	155.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		ESD2CANFD24	–24		24	V
V_{BRF}	Breakdown voltage(2)	I_{IO} = 10 mA, IO to GND	ESD2CANFD24	25.5		35.5	V
V_{BRR}	Breakdown voltage(2)	I_{IO} = –10 mA, IO to GND	ESD2CANFD24	–35.5		–25.5	V
V_{CLAMP}	Clamping voltage(3)	I_{PP} = 3.5 A, t_p = 8/20 µs, IO to GND	ESD2CANFD24		37		V
V_{CLAMP}	Clamping voltage(4)	I_{PP} = 16 A, TLP, IO to GND or GND to IO	ESD2CANFD24		36		V
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND	ESD2CANFD24	-50	5	50	nA
R_{DYN}	Dynamic resistance(4)	IO to GND or GND to IO	ESD2CANFD24		0.45		Ω
C_L	Line capacitance(5)	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV	ESD2CANFD24		2.5	4.2	pF
V_{Hold}	Holding voltage after snapback	TLP	ESD2CANFD24		30		V

(1) Measurements made on each IO channel
(2) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive and negative going direction respectively, before the device latches into the snapback state
(3) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5
(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008
(5) Measured from IO to GND on each channel

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6.7 Typical Characteristics – ESD2CANFD24

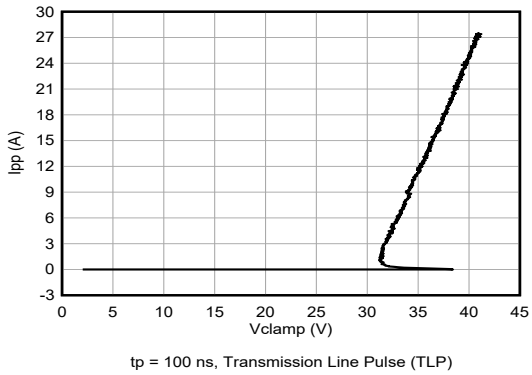


Figure 6-1. Positive TLP Curve

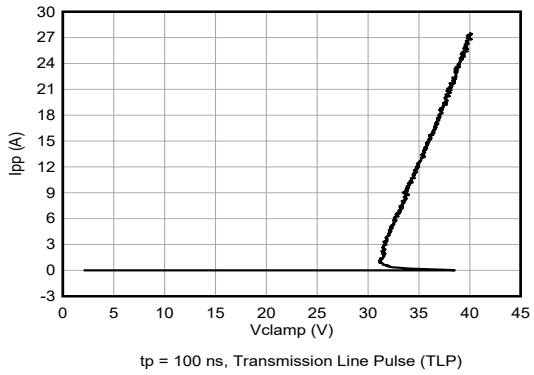


Figure 6-2. Negative TLP Curve

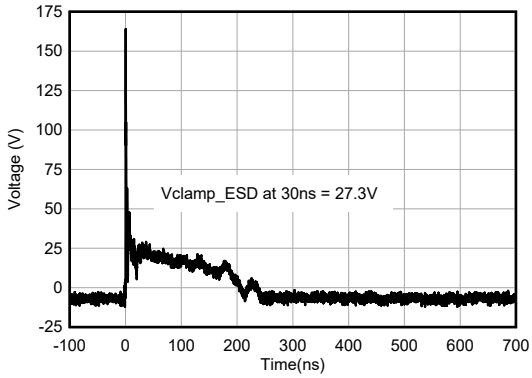


Figure 6-3. +8-kV Clamped IEC Waveform

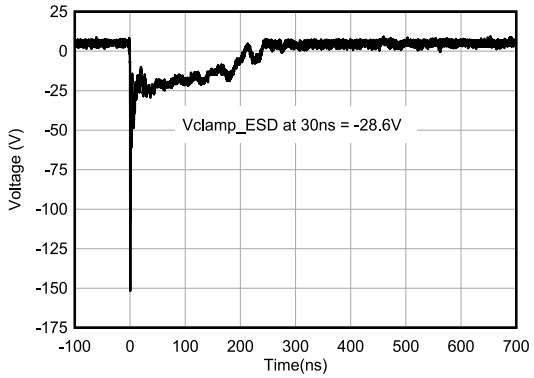


Figure 6-4. −8-kV Clamped IEC Waveform

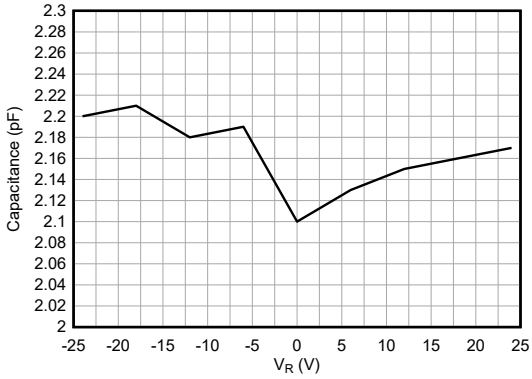


Figure 6-5. Capacitance vs. Bias Voltage

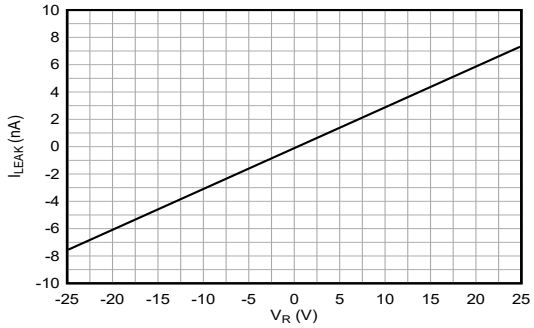


Figure 6-6. Leakage Current vs. Bias Voltage Across Temperature

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6.7 Typical Characteristics – ESD2CANFD24 (continued)

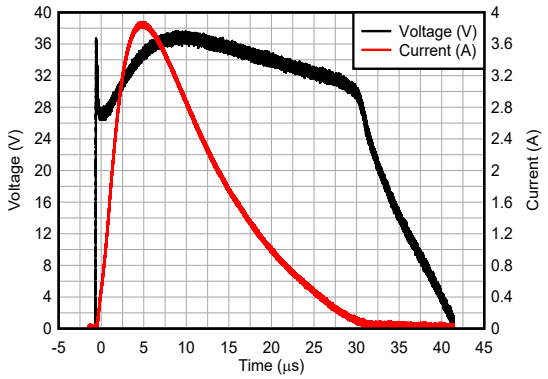


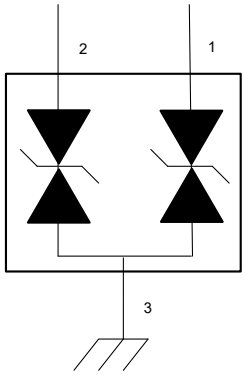
Figure 6-7. 8/20 µs Surge Response at 3.5 A

7 Detailed Description

7.1 Overview

The ESD2CANFD24 is a dual-channel ESD TVS diode in SOT-23 leaded package which is convenient for automatic optical inspection. This product offers IEC 61000-4-2 ±25-kV air-gap, ±25-kV contact ESD protection, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support. The 2.5 pF (typical) or less line capacitance of this ESD protection diode is suitable for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 10 Mbps. A typical application for this product is ESD circuit protection for CAN transceivers.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD2CANFD24 is a bidirectional TVS with a high ESD protection level. This device protects the circuit from ESD strikes up to ±25-kV contact and ±25-kV air-gap specified in the IEC 61000-4-2 standard. The device can also handle up to 3.5 A surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 2.5-pF (typical) supports a data rate up to 10 Mbps. This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 37 V when the device is taking 3.5 A transient surge current. The breakdown is bidirectional so this protection device is a good fit for CAN which is a differential signal. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 package is good for applications requiring automatic optical inspection (AOI).

7.3.1 Temperature Range

This device is qualified to operate from –55°C to +150°C.

7.3.2 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events of at least ±25-kV contact and ±25-kV air-gap in the leaded SOT-23 package according to the IEC 61000-4-2 standard. An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3.5 A (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between the I/O pins is 2.5 pF (typical) or less. This capacitance supports data rates for CAN, CANFD, CAN SiC, and CAN-XL up to 10 Mbps.

7.3.5 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.45 Ω (Pin 1 or Pin 2 to Pin 3) and 0.45 Ω (Pin 3 to Pin 1 or Pin 2) or less which prevents system damage during ESD events.

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7.3.6 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of ± 25.5 V. This protects sensitive equipment from surges above the reverse standoff voltage of ± 24 V.

7.3.7 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of ± 50 nA (maximum) with a bias of ± 24 V.

7.3.8 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V (I_{PP} = 3.5 A) and 36 V (I_{PP} = 16 A for TLP).

7.3.9 Industry Standard Leaded Packages

This device features an industry standard SOT-23 (DBZ) leaded package for automatic optical inspection (AOI).

7.4 Device Functional Modes

The ESD2CANFD24 is a dual channel passive clamp that has low leakage during normal operation when the voltage between pin 1 or pin 2 and pin 3 is below V_{RWM}, and activates when the voltage between pin 1 or pin 2 and pin 3 goes above V_{BR}. During IEC 61000-4-2 ESD events, transient voltages as high as ±25 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD2CANFD24 is a dual channel TVS diode which is used to provide a path to ground for dissipating ESD events on differential CAN signal lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

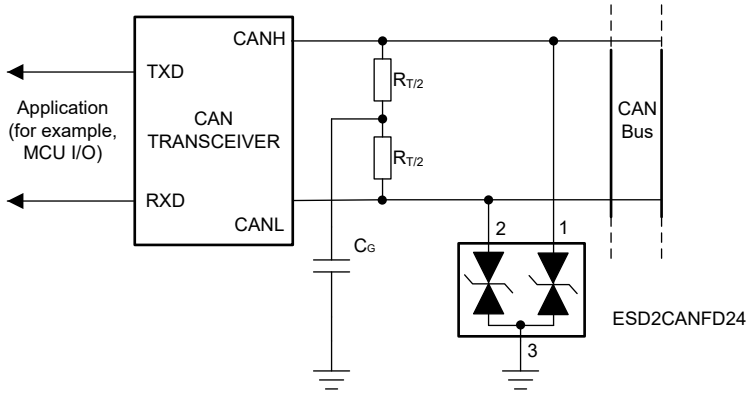


Figure 8-1. ESD2CANFD24 Typical Application

8.2.1 Design Requirements

For this design example, the ESD2CANFD24 is used to provide ESD protection for a CAN transceiver. Table 8-1 lists the known design parameters for this application.

Table 8-1. Design Parameters for the ESD2CANFD24 Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} differential signal range	> ±1.5 V
V_{RWM}	±24 V
Data rate	Up to 10 Mbps
RT/2	60 Ω

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8.2.2 Detailed Design Procedure

The ESD2CANFD24 has a V_{RWM} of ±24 V. The bidirectional characteristic enables the signal integrity of the differential CAN lines to not be impacted by the diode. The low capacitance of 2.5 pF (typical) or less enables data rates up to 10 Mbps, which allows the designer to meet the requirements for CAN, CANFD, CAN SiC, and CAN-XL. The 60 Ω split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

8.2.3 Application Curves

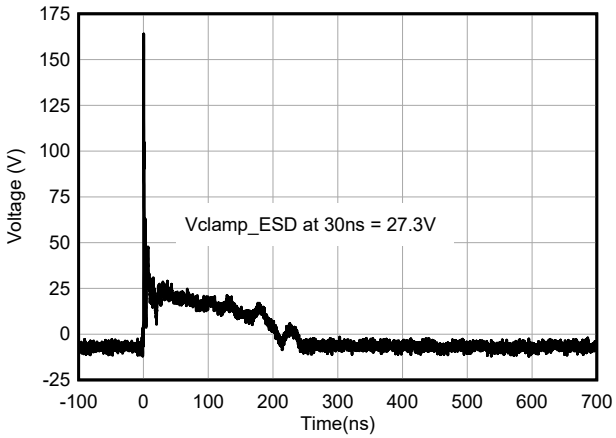


Figure 8-2. +8-kV Clamped IEC Waveform

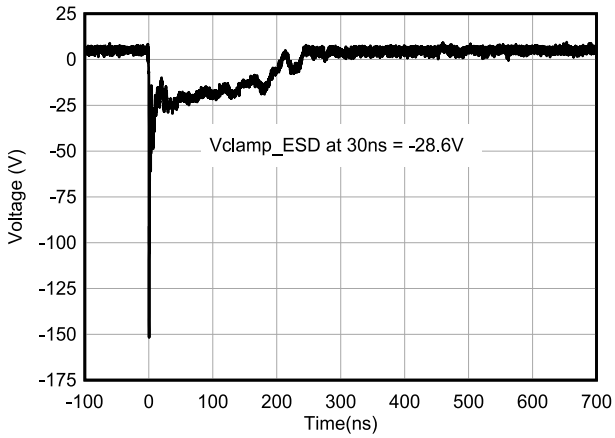


Figure 8-3. −8-kV Clamped IEC Waveform

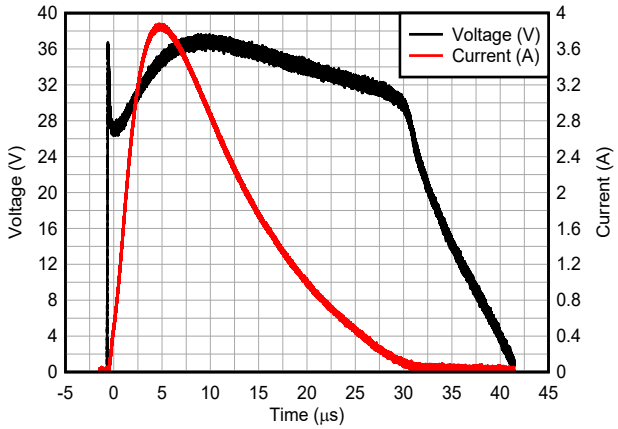


Figure 8-4. 8/20 µs Surge Response at 3.5 A

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9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

This example is typical of a dual channel differential data pair application, such as CAN.

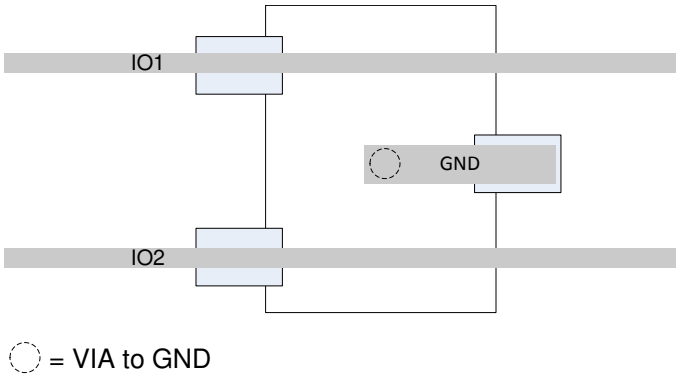


Figure 10-1. Routing with DBZ Package

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD2CANFD24DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2QO8
ESD2CANFD24DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2QO8

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ESD2CANFD24 :

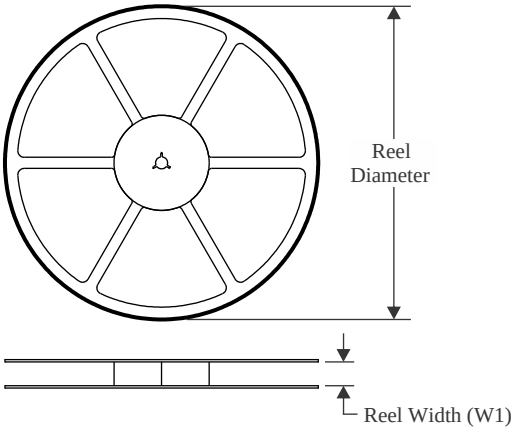
- Automotive : ESD2CANFD24-Q1

NOTE: Qualified Version Definitions:

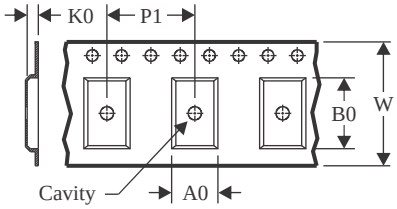
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

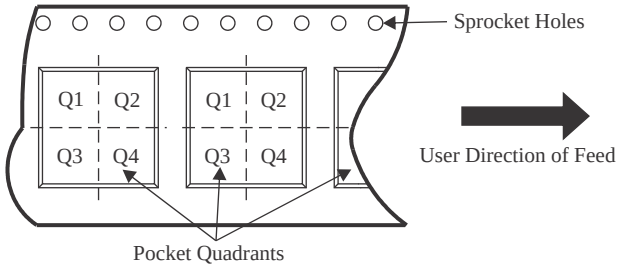


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

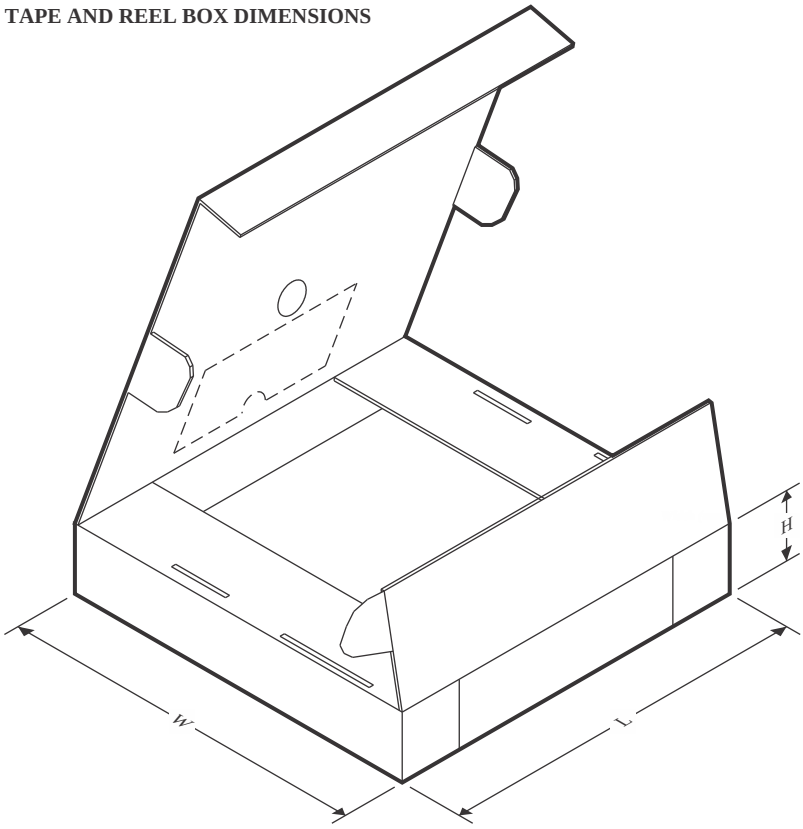
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CANFD24DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CANFD24DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

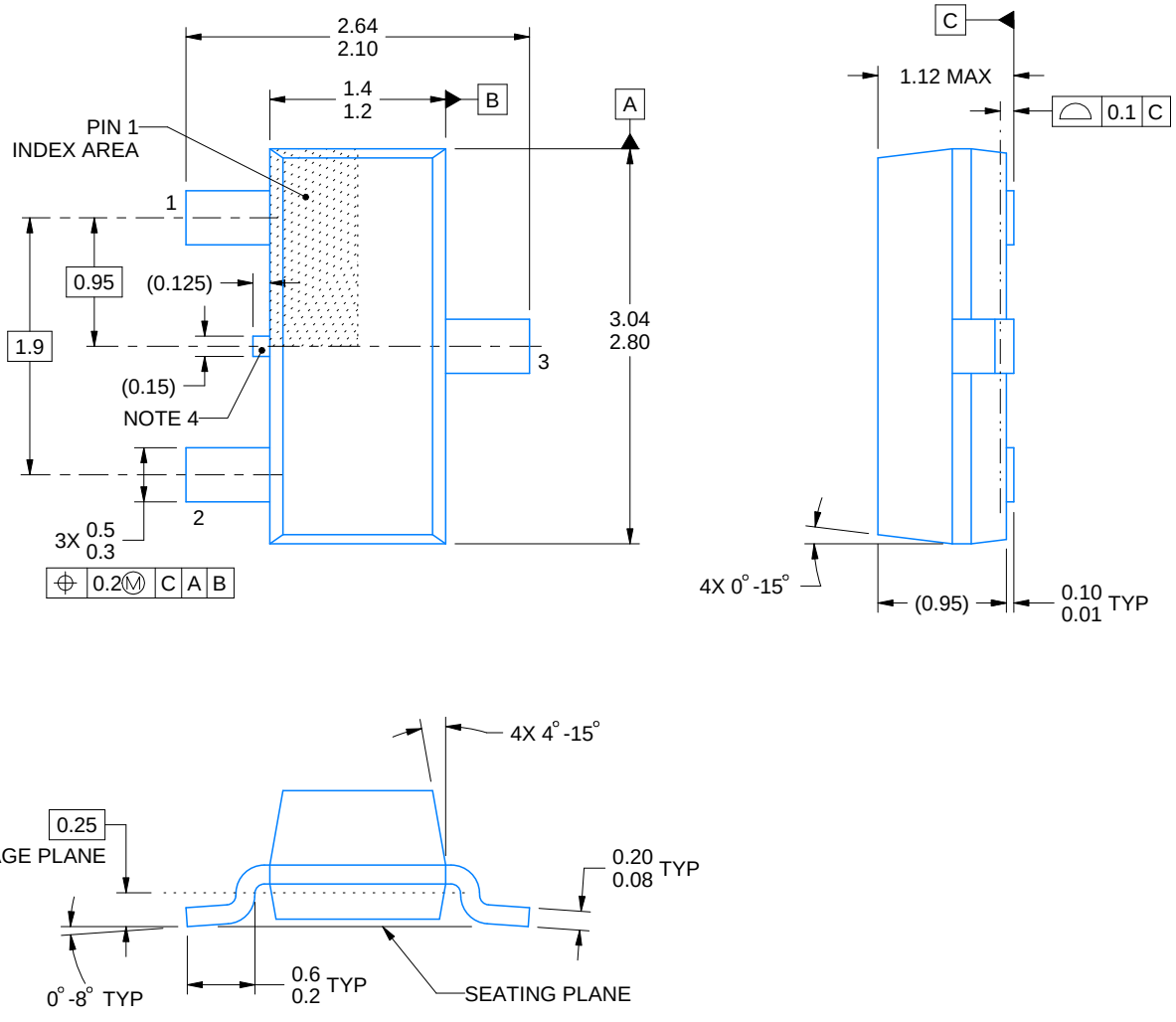
PACKAGE OUTLINE

DBZ0003A



SOT-23 - 1.12 mm max height

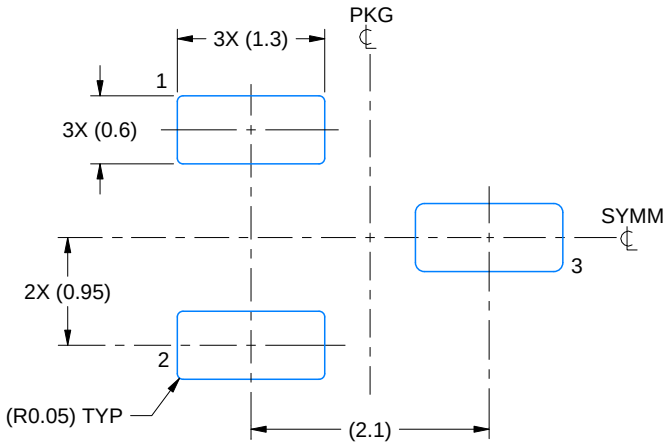
SMALL OUTLINE TRANSISTOR



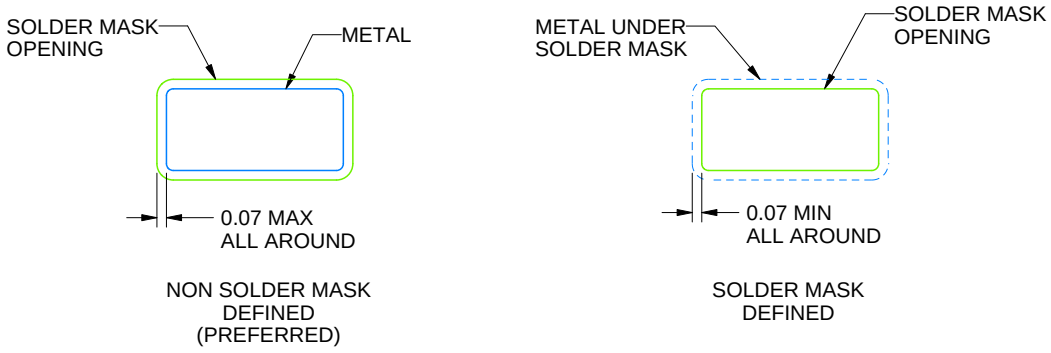
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

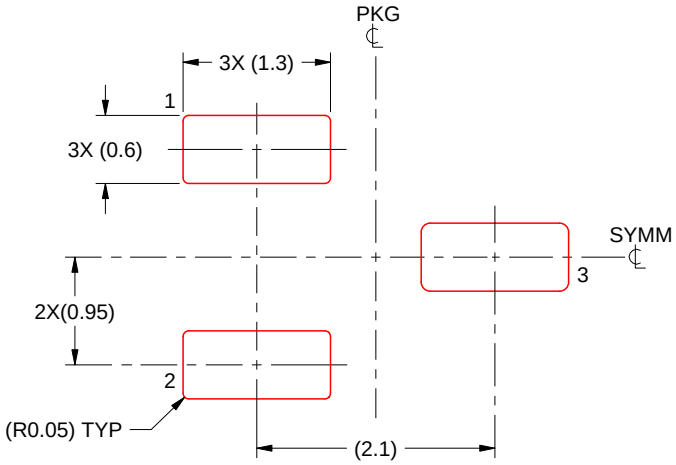


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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