Digital Transistors (BRT) R1 = 4.7 kΩ, R2 = 4.7 kΩ

NPN Transistors with Monolithic Bias Resistor Network

MUN2232, MMUN2232L, MUN5232, DTC143EE, DTC143EM3, NSBC143EF3

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

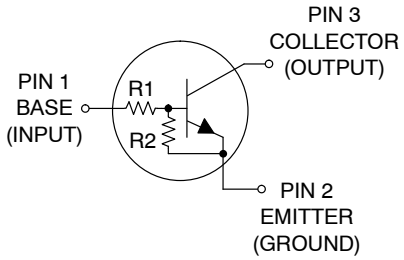
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25 °C)

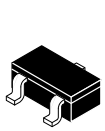
Symbol	Rating	Max	Unit
V_{CBO}	Collector-Base Voltage	50	Vdc
V_{CEO}	Collector-Emitter Voltage	50	Vdc
I_C	Collector Current-Continuous	100	mAdc
$V_{IN(fwd)}$	Input Forward Voltage	30	Vdc
$V_{IN(rev)}$	Input Reverse Voltage	10	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

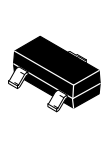
PIN CONNECTIONS



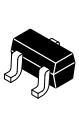
MARKING DIAGRAMS



SC-59
CASE 318D
STYLE 1



SOT-23
CASE 318
STYLE 6



SC-70/SOT-323
CASE 419
STYLE 3



SC-75
CASE 463
STYLE 1



SOT-723
CASE 631AA
STYLE 1



SOT-1123
CASE 524AA
STYLE 1

XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

* Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking, and shipping information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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Table 1. THERMAL CHARACTERISTICS

Symbol	Characteristic		Max	Unit
THERMAL CHARACTERISTICS (SC-59) (MUN2232)				
P_D	Total Device Dissipation T_A = 25 °C	(Note 1)	230	mW
		(Note 2)	338	
	Derate above 25 °C	(Note 1)	1.8	mW/°C
		(Note 2)	2.7	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1)	540	°C/W
		(Note 2)	370	
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	(Note 1)	264	°C/W
		(Note 2)	287	
T_J, T_{stg}	Junction and Storage Temperature Range		−55 to +150	°C
THERMAL CHARACTERISTICS (SOT-23) (MMUN2232L)				
P_D	Total Device Dissipation T_A = 25 °C	(Note 1)	246	mW
		(Note 2)	400	
	Derate above 25 °C	(Note 1)	2.0	mW/°C
		(Note 2)	3.2	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1)	508	°C/W
		(Note 2)	311	
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	(Note 1)	174	°C/W
		(Note 2)	208	
T_J, T_{stg}	Junction and Storage Temperature Range		−55 to +150	°C
THERMAL CHARACTERISTICS (SC-70/SOT-323) (MUN5232)				
P_D	Total Device Dissipation T_A = 25 °C	(Note 1)	202	mW
		(Note 2)	310	
	Derate above 25 °C	(Note 1)	1.6	mW/°C
		(Note 2)	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1)	618	°C/W
		(Note 2)	403	
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	(Note 1)	280	°C/W
		(Note 2)	332	
T_J, T_{stg}	Junction and Storage Temperature Range		−55 to +150	°C
THERMAL CHARACTERISTICS (SC-75) (DTC143EE)				
P_D	Total Device Dissipation T_A = 25 °C	(Note 1)	200	mW
		(Note 2)	300	
	Derate above 25 °C	(Note 1)	1.6	mW/°C
		(Note 2)	2.4	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1)	600	°C/W
		(Note 2)	400	
T_J, T_{stg}	Junction and Storage Temperature Range		−55 to +150	°C
THERMAL CHARACTERISTICS (SOT-723) (DTC143EM3)				
P_D	Total Device Dissipation T_A = 25°C	(Note 1)	260	mW
		(Note 2)	600	
	Derate above 25 °C	(Note 1)	2.0	mW/°C
		(Note 2)	4.8	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1)	480	°C/W
		(Note 2)	205	
T_J, T_{stg}	Junction and Storage Temperature Range		−55 to +150	°C
THERMAL CHARACTERISTICS (SOT-1123) (NSBC143EF3)				
P_D	Total Device Dissipation T_A = 25 °C	(Note 3)	254	mW
		(Note 4)	297	
	Derate above 25 °C	(Note 3)	2.0	mW/°C
		(Note 4)	2.4	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 3)	493	°C/W
		(Note 4)	421	

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Table 1. THERMAL CHARACTERISTICS

Symbol	Characteristic		Max	Unit
THERMAL CHARACTERISTICS (SOT-1123) (NSBC143EF3)				
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	(Note 3)	193	°C/W
T_J, T_{stg}	Junction and Storage Temperature Range		−55 to +150	°C

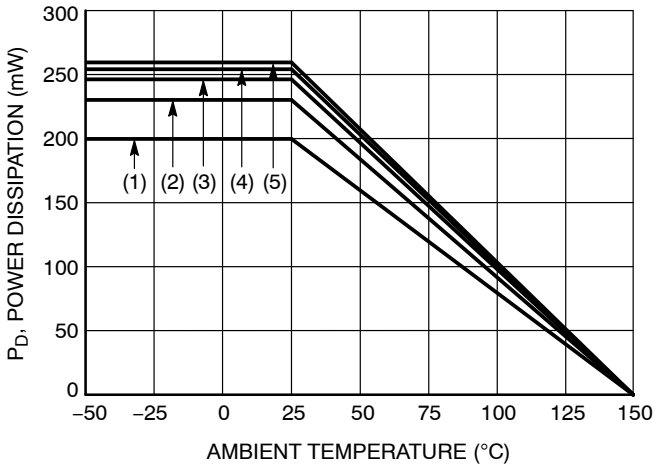
1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 Inch Pad.
3. FR-4 @ 100 mm^2, 1 oz. copper traces, still air.
4. FR-4 @ 500 mm^2, 1 oz. copper traces, still air.

Table 2. ELECTRICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
I_{CBO}	Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)			100	nAdc
I_{CEO}	Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)			500	nAdc
I_{EBO}	Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)			1.5	mAdc
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	50			Vdc
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (Note 5) (I_C = 2.0 mA, I_B = 0)	50			Vdc
ON CHARACTERISTICS					
h_{FE}	DC Current Gain (Note 5) (I_C = 5.0 mA, V_{CE} = 10 V)	15	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (Note 5) (I_C = 10 mA, I_B = 1.0 mA)			0.25	Vdc
$V_{i(off)}$	Input Voltage (off) (V_{CE} = 5.0 V, I_C = 100 μA)		1.2	0.5	Vdc
$V_{i(on)}$	Input Voltage (on) (V_{CE} = 0.3 V, I_C = 20 mA)	2.5	2.0		Vdc
V_{OL}	Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)			0.2	Vdc
V_{OH}	Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	4.9			Vdc
R1	Input Resistor	3.3	4.7	6.1	kΩ
R_1/R_2	Resistor Ratio	0.8	1.0	1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.



(1) SC-75 and SC-70/SOT323; Minimum Pad
(2) SC-59; Minimum Pad
(3) SOT-23; Minimum Pad
(4) SOT-1123; 100 mm^2, 1 oz. copper trace
(5) SOT-723; Minimum Pad

Figure 1. Derating Curve

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TYPICAL CHARACTERISTICS
MUN2232, MMUN2232L, MUN5232, DTC143EE, DTC143EM3

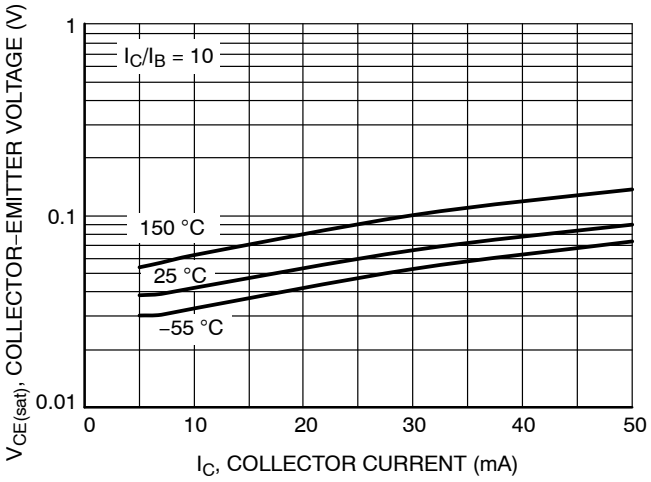


Figure 2. $V_{CE(sat)}$, vs. I_C

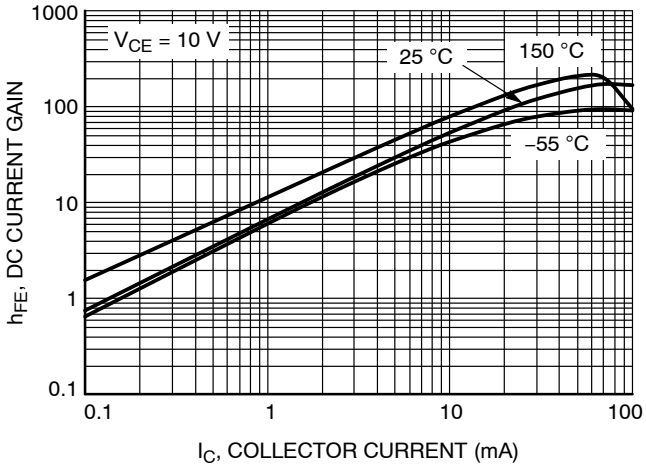


Figure 3. DC Current Gain

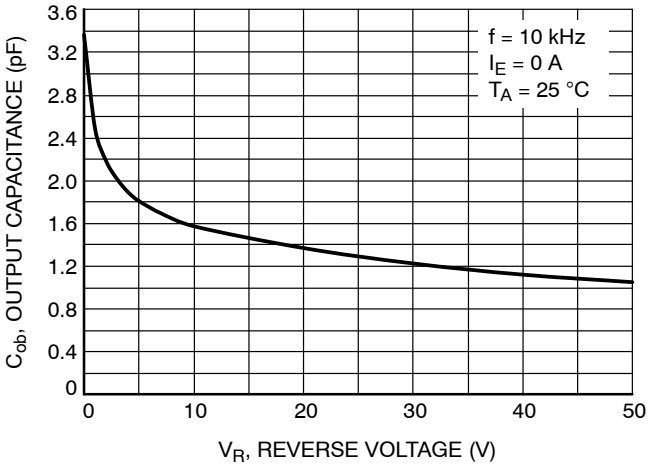


Figure 4. Output Capacitance

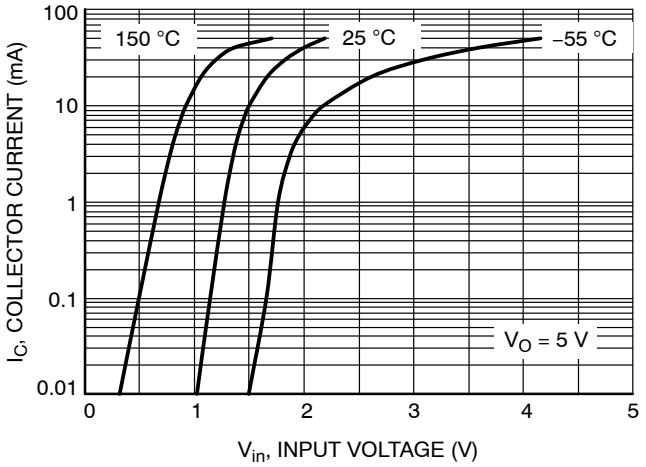


Figure 5. Output Current vs. Input Voltage

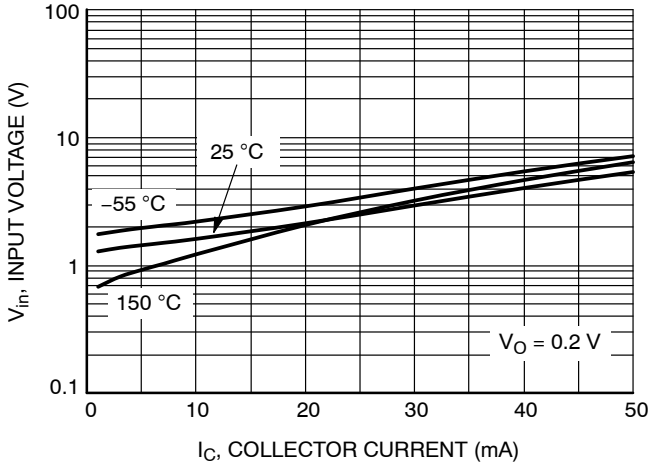


Figure 6. Input Voltage vs. Output Current

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TYPICAL CHARACTERISTICS – NSBC143EF3

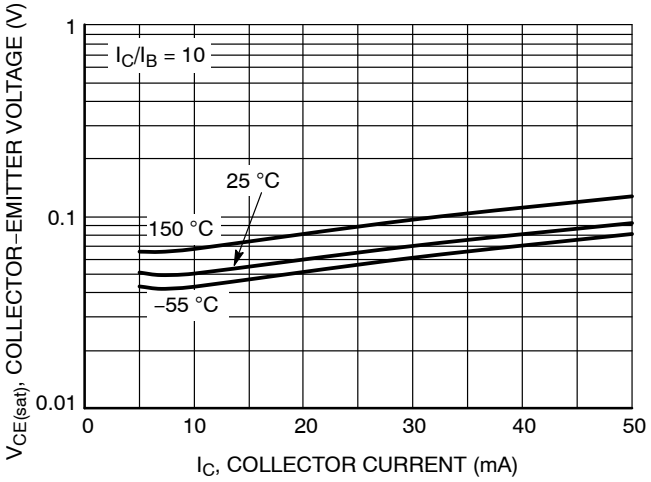


Figure 7. $V_{CE(sat)}$, vs. I_C

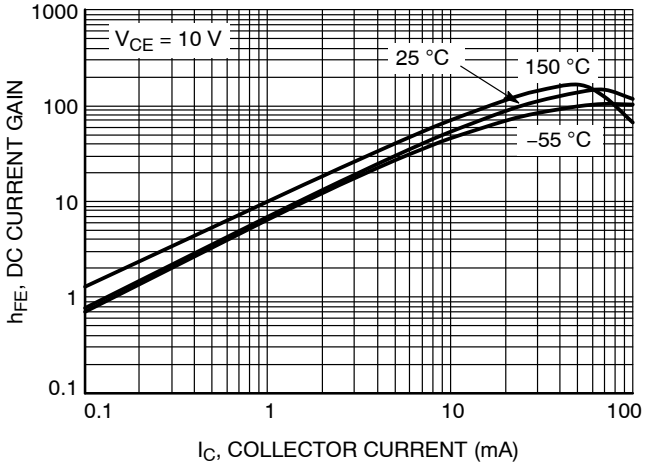


Figure 8. DC Current Gain

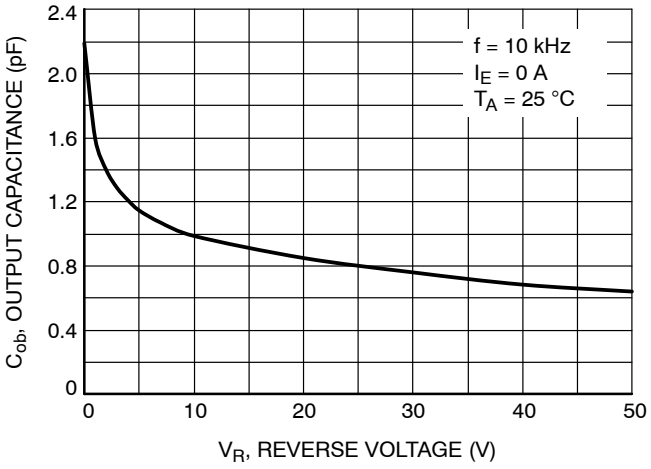


Figure 9. Output Capacitance

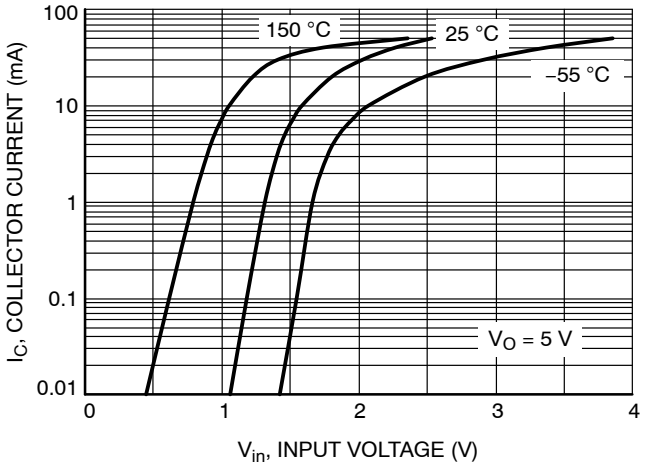


Figure 10. Output Current vs. Input Voltage

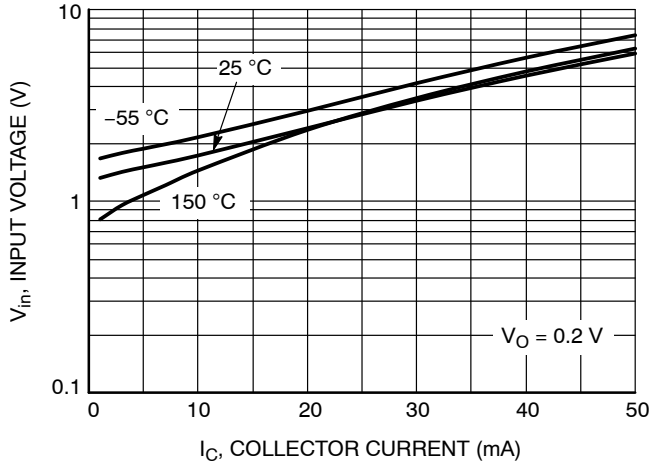


Figure 11. Input Voltage vs. Output Current

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Table 3. ORDERING INFORMATION

Device	Part Marking	Package	Shipping†
MUN2232T1G, SMUN2232T1G*	8J	SC-59 (Pb-Free)	3000 / Tape & Reel
MMUN2232LT1G, MMUN2232LT1G-NC NSVMMUN2232LT1G* NSVMMUN2232LT1G-NC*	A8J	SOT-23 (Pb-Free)	3000 / Tape & Reel
NSVMMUN2232LT3G* NSVMMUN2232LT3G-NC*			10000 / Tape & Reel
MUN5232T1G MUN5232T1G-NC SMUN5232T1G* SMUN5232T1G-NC*	8J	SC-70/SOT-323 (Pb-Free)	3000 / Tape & Reel
DTC143EET1G DTC143EET1G-NC (Under Development)	8J	SC-75 (Pb-Free)	3000 / Tape & Reel
DTC143EM3T5G DTC143EM3T5G-NC (Under Development)	8J	SOT-723 (Pb-Free)	8000 / Tape & Reel

DISCONTINUED (Note 6)

NSBC143EF3T5G	P	SOT-1123 (Pb-Free)	8000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

6. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

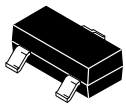
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REVISION HISTORY

Revision	Description of Changes	Date
5	Adding OPN's device on ordering information table and update the datasheet to follow our latest formatting guidelines	10/8/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

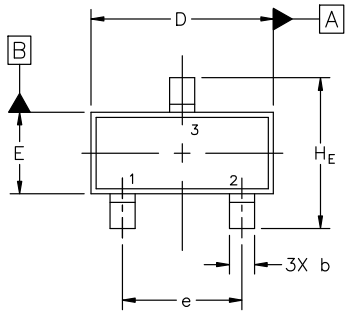
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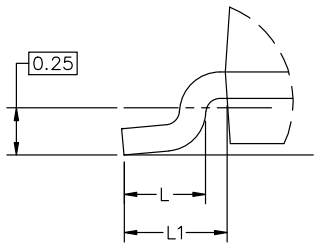
SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

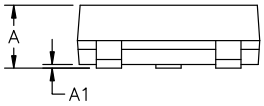
DATE 14 AUG 2024



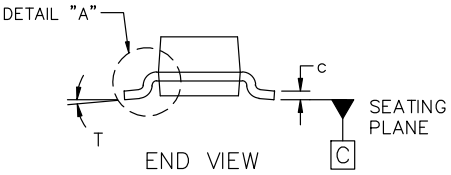
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

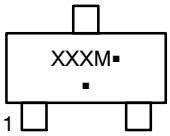


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

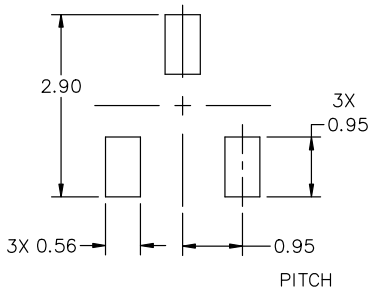
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**		**PAGE 1 OF 2**

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SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
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2. CATHODE
3. GATE

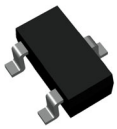
STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

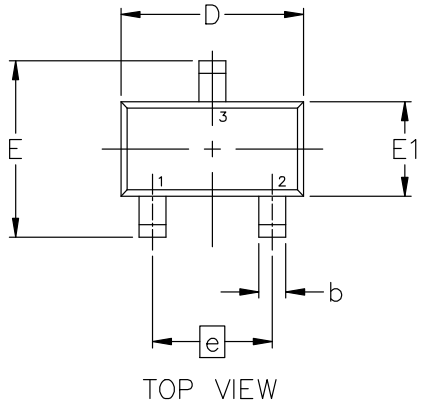
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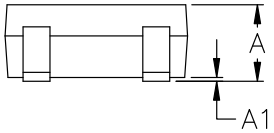


SC−59−3 2.90x1.50x1.15, 1.90P
CASE 318D
ISSUE J

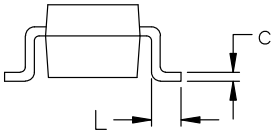
DATE 15 FEB 2024



TOP VIEW



SIDE VIEW

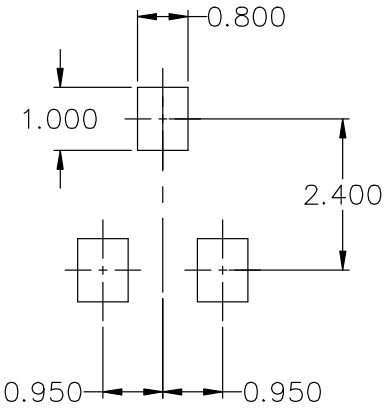


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

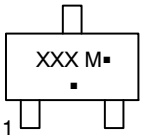
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.15	1.30
A1	0.01	0.06	0.10
b	0.35	0.43	0.50
c	0.09	0.14	0.18
D	2.70	2.90	3.10
E	2.50	2.80	3.00
E1	1.30	1.50	1.70
e	1.90 BSC		
L	0.20	0.40	0.60



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package*

(*Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. N.C.
3. ANODE

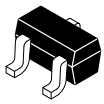
STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE/CATHODE

DOCUMENT NUMBER:	**98ASB42664B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−59−3 2.90x1.50x1.15, 1.90P**	**PAGE 1 OF 1**

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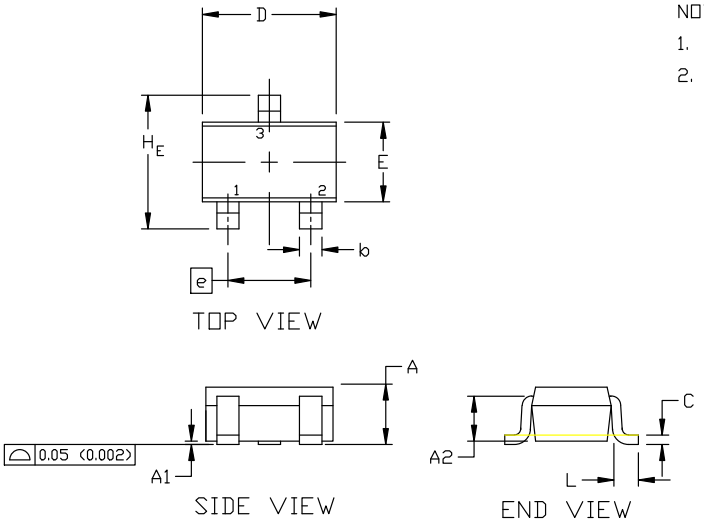
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SCALE 4:1

SC−70 (SOT−323)
CASE 419
ISSUE R

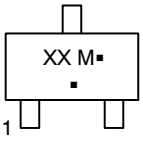
DATE 11 OCT 2022



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

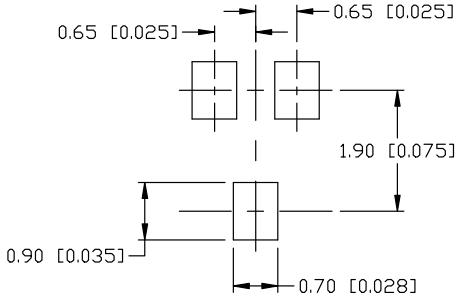
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

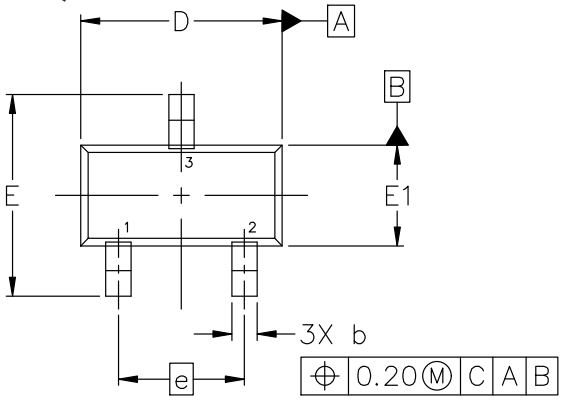
DOCUMENT NUMBER:	**98ASB42819B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−70 (SOT−323)**	**PAGE 1 OF 1**

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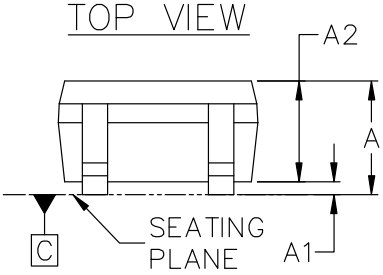
SC75−3 1.60x0.80x0.80, 1.00P
CASE 463
ISSUE H

DATE 01 FEB 2024

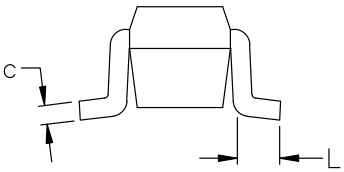




TOP VIEW



SIDE VIEW



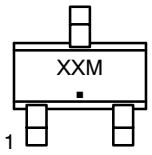
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.05	0.10
A2		0.80 REF.	
b	0.15	0.20	0.30
c	0.10	0.15	0.25
D	1.55	1.60	1.65
E	1.50	1.60	1.70
E1	0.70	0.80	0.90
e		1.00 BSC	
L	0.10	0.15	0.20

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

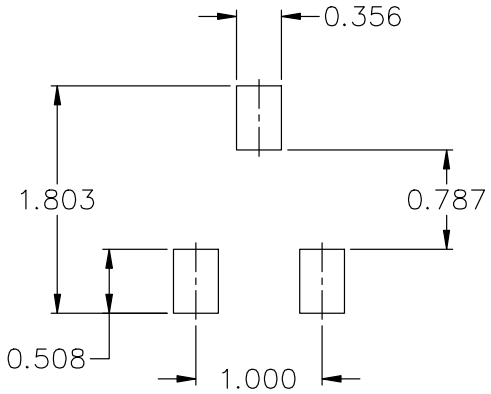
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN



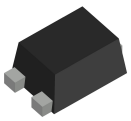
RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	SC75−3 1.60x0.80x0.80, 1.00P	PAGE 1 OF 1

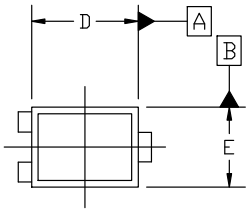
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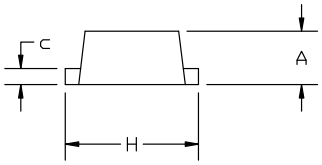


SOT−1123 0.80x0.60x0.37, 0.35P
CASE 524AA
ISSUE D

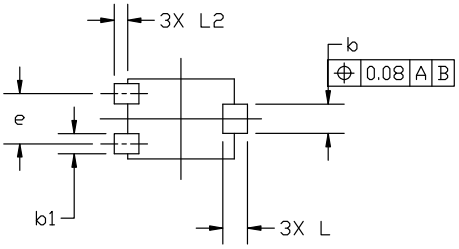
DATE 18 JAN 2024



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

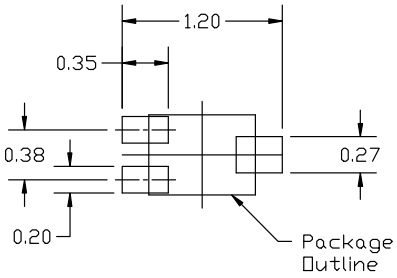
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.15	0.22	0.28
b1	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
e	0.35	0.38	0.40
H	0.950	1.000	1.050
L	0.185 REF		
L2	0.05	0.10	0.15

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

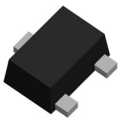
STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

DOCUMENT NUMBER:	**98AON23134D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−1123 0.80x0.60x0.37, 0.35P**		**PAGE 1 OF 1**

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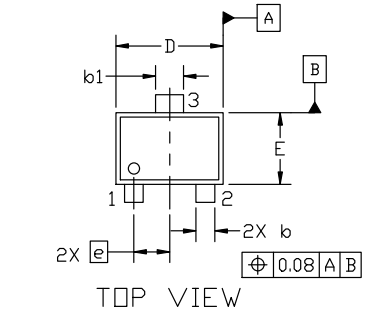


SOT−723 1.20x0.80x0.50, 0.40P
CASE 631AA
ISSUE E

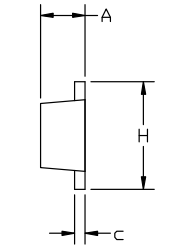
DATE 24 JAN 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

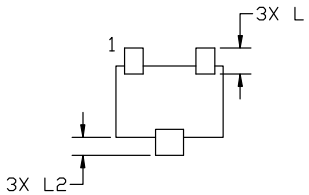
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
b	0.15	0.21	0.27
b1	0.25	0.31	0.37
c	0.07	0.12	0.17
D	1.15	1.20	1.25
E	0.75	0.80	0.85
e	0.40 BSC		
H	1.15	1.20	1.25
L	0.29 REF		
L2	0.15	0.20	0.25



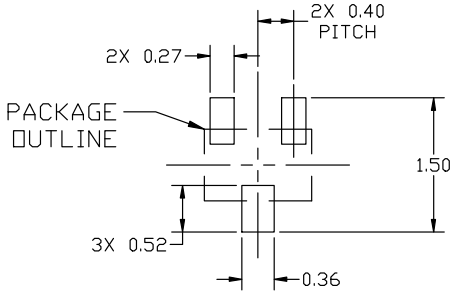
TOP VIEW



SIDE VIEW



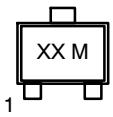
BOTTOM VIEW



RECOMMENDED MOUNTING
FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

DOCUMENT NUMBER:	**98AON12989D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT−723 1.20x0.80x0.50, 0.40P**	**PAGE 1 OF 1**

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