Surface Mount Schottky Power Rectifier

MBR120VLSF, NRVB120VLSF

Plastic SOD−123 Package

This device uses the Schottky Barrier principle with a large area metal−to−silicon power diode. Ideally suited for low voltage, high frequency rectification or as free wheeling and polarity protection diodes in surface mount applications where compact size and weight are critical to the system. This package also provides an easy to work with alternative to leadless 34 package style. Because of its small size, it is ideal for use in portable and battery powered products such as cellular and cordless phones, chargers, notebook computers, printers, PDAs and PCMCIA cards. Typical applications are AC−DC and DC−DC converters, reverse battery protection, and "Oring" of multiple supply voltages and any other application where performance and size are critical.

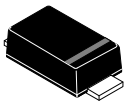
Features

- Guardring for Stress Protection
- Optimized for Very Low Forward Voltage
- 125°C Operating Junction Temperature
- Epoxy Meets UL 94 V−0 @ 0.125 in
- Package Designed for Optimal Automated Board Assembly
- ESD Ratings: Machine Model, C;
  Human Body Model, 3B
- NRVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Mechanical Characteristics

- Reel Options: MBR120VLSFT1G = 3,000 per 7″ reel/8 mm tape
  MBR120VLSFT3G = 10,000 per 13″ reel/8 mm tape
- Device Marking: L2V
- Polarity Designator: Cathode Band
- Weight: 11.7 mg (approximately)
- Case: Epoxy, Molded
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Device Meets MSL 1 Requirements

SCHOTTKY BARRIER RECTIFIER 1.0 AMPERES 20 VOLTS



SOD−123FL
CASE 498

MARKING DIAGRAM



L2V = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MBR120VLSFT1G	SOD−123FL (Pb−Free)	3000 / Tape & Reel
NRVB120VLSFT1G	SOD−123FL (Pb−Free)	3000 / Tape & Reel
MBR120VLSFT3G	SOD−123FL (Pb−Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	V
Average Rectified Forward Current (Rated V_R) T_L = 119°C	$I_{F(AV)}$	1.0	A
Non−Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions, Halfwave, Single Phase, 60 Hz)	I_{FSM}	45	A
Storage Temperature Range	T_{stg}	−65 to +125	°C
Operating Junction Temperature	T_J	−65 to +125	°C
Voltage Rate of Change (Rated V_R)	dv/dt	1000	V/μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Lead (Note 1) Thermal Resistance − Junction−to−Lead (Note 2) Thermal Resistance − Junction−to−Ambient (Note 1) Thermal Resistance − Junction−to−Ambient (Note 2)	$R_{\theta jl}$ $R_{\theta jl}$ $R_{\theta ja}$ $R_{\theta ja}$	26 21 325 82	°C/W

1. Mounted with minimum recommended pad size, PC Board FR4.
2. Mounted with 1 in. copper pad (Cu area 700 mm^2).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	T_J = 25°C	T_J = 85°C	Unit
Maximum Instantaneous Forward Voltage (Note 3) (I_F = 0.1 A) (I_F = 0.5 A) (I_F = 1.0 A)	V_F	 0.275 0.315 0.340	 0.205 0.270 0.300	V
Maximum Instantaneous Reverse Current (Note 3) (Rated DC Voltage)	I_R	 0.60	 15	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

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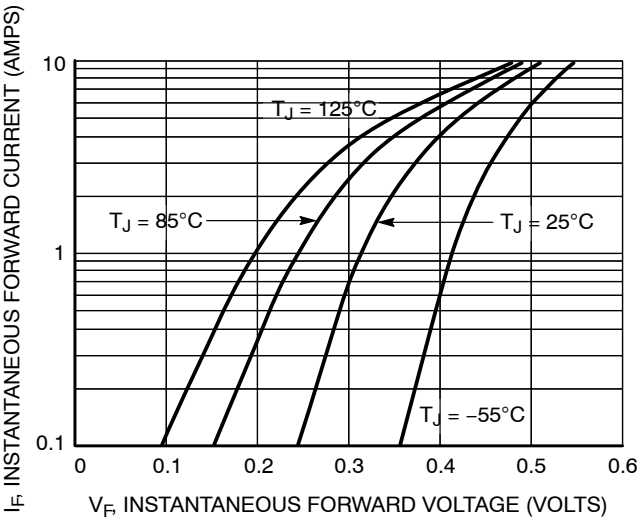


Figure 1. Typical Forward Voltage

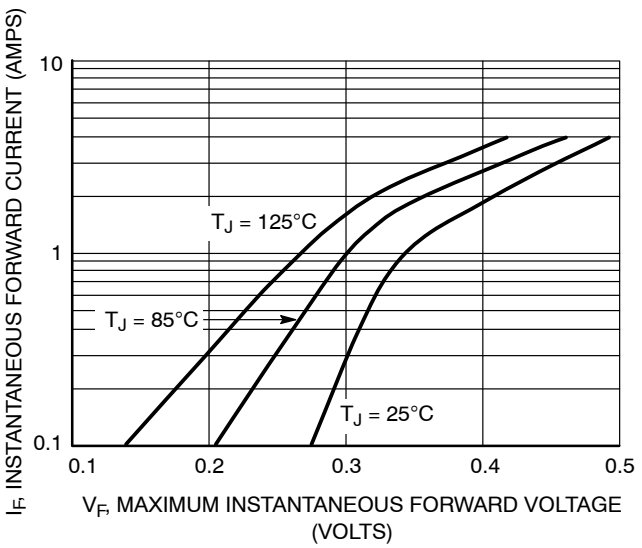


Figure 2. Maximum Forward Voltage

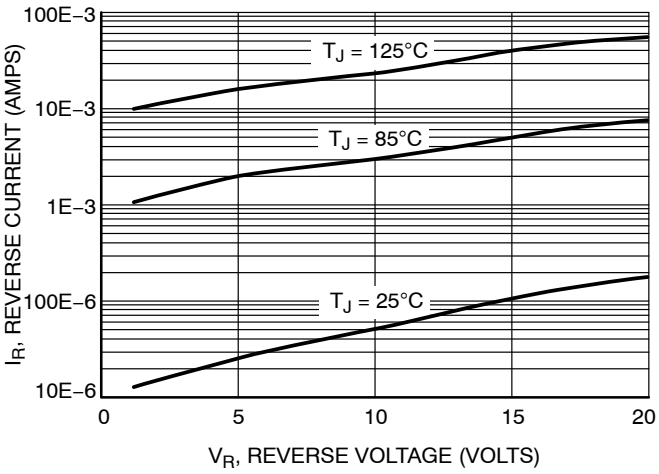


Figure 3. Typical Reverse Current

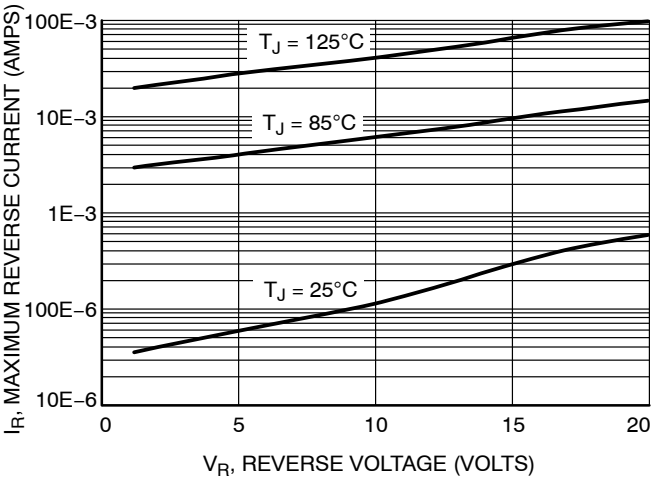


Figure 4. Maximum Reverse Current

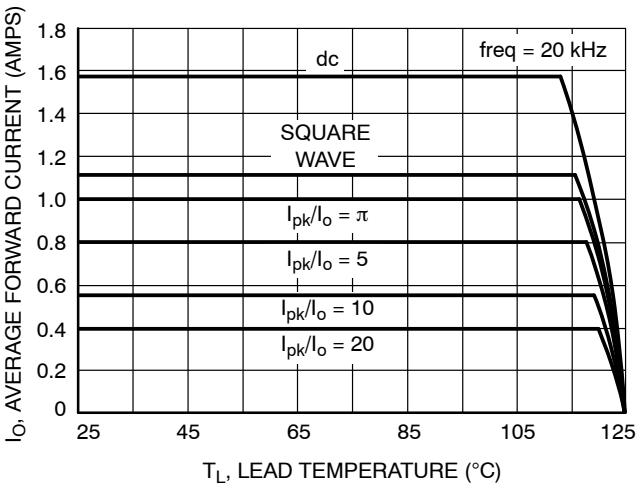


Figure 5. Current Derating

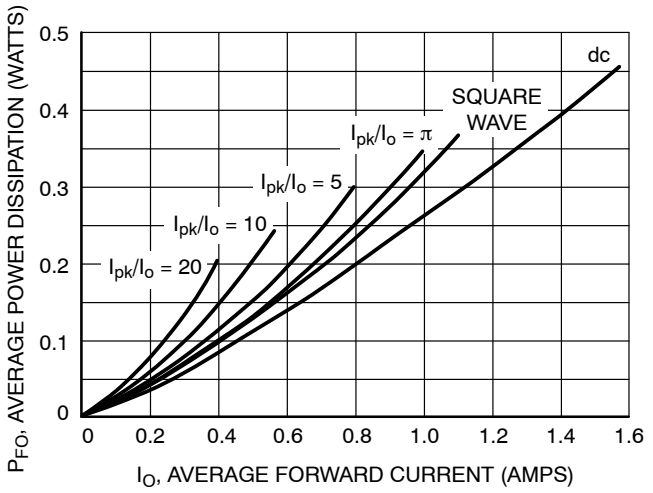


Figure 6. Forward Power Dissipation

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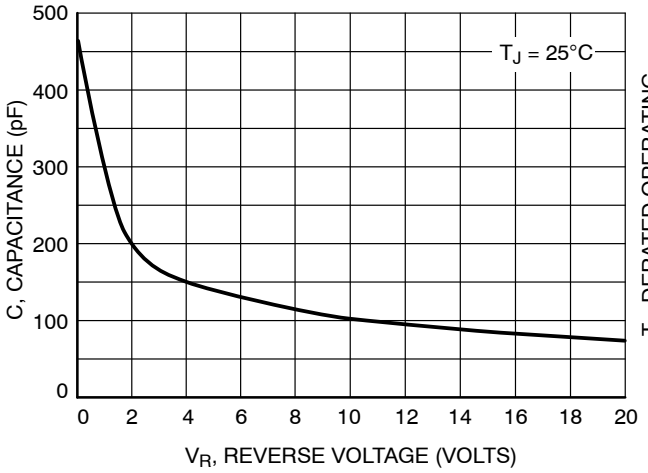


Figure 7. Capacitance

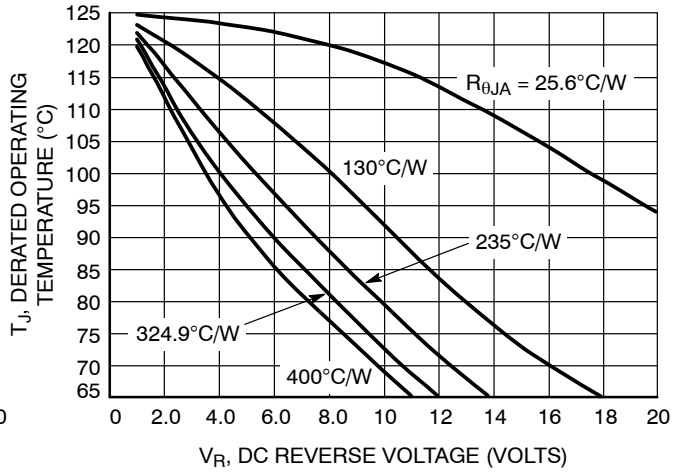


Figure 8. Typical Operating Temperature Derating*

* Reverse power dissipation and the possibility of thermal runaway must be considered when operating this device under any reverse voltage conditions. Calculations of T_J therefore must include forward and reverse power effects. The allowable operating T_J may be calculated from the equation: $T_J = T_{Jmax} - r(t)(Pf + Pr)$ where
$r(t)$ = thermal impedance under given conditions,
Pf = forward power dissipation, and
Pr = reverse power dissipation
This graph displays the derated allowable T_J due to reverse bias under DC conditions only and is calculated as $T_J = T_{Jmax} - r(t)Pr$, where r(t) = Rthja. For other power applications further calculations must be performed.

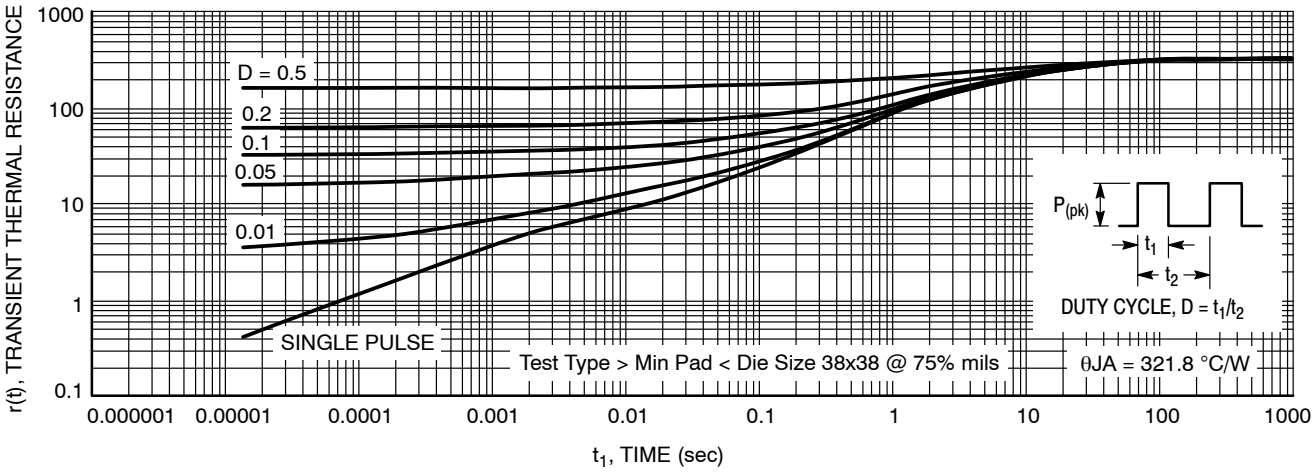


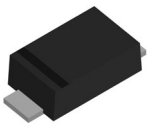
Figure 9. Thermal Response

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REVISION HISTORY

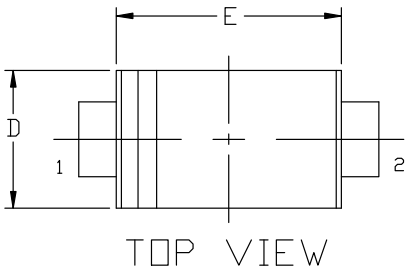
Revision	Description of Changes	Date
4	Rebranded the Data Sheet to onsemi format	6/23/2025

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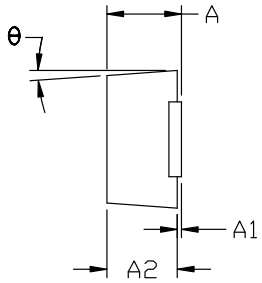


SOD−123−2 1.65x2.70x0.90
CASE 498
ISSUE E

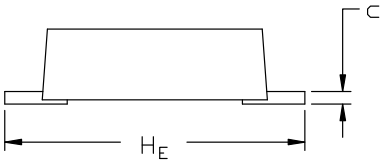
DATE 22 AUG 2023



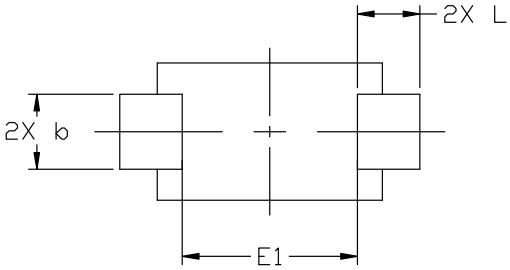
TOP VIEW



END VIEW



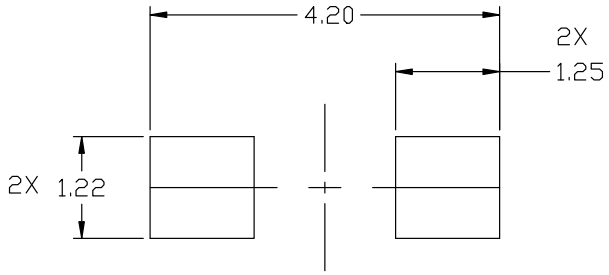
SIDE VIEW



BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	0.95	0.98
A1	0.00	0.05	0.10
A2	0.85	0.90	0.95
b	0.70	0.90	1.10
c	0.10	0.15	0.20
D	1.50	1.65	1.80
E	2.50	2.70	2.90
E1	1.70	2.10	2.50
H_E	3.40	3.60	3.80
L	0.55	0.75	0.95
θ	0°	---	8°

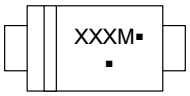
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND L ARE TO BE MEASURED ON A FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH PROTRUSIONS, OR GATE BURRS.
5. FLAT LEAD.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOD−123−2 1.65x2.70x0.90**		**PAGE 1 OF 1**

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