# Single Supply Dual Operational Amplifiers

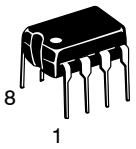
# LM258, LM358, LM358A, LM358E, LM2904, LM2904A, LM2904E, LM2904V, NCV2904

Utilizing the circuit designs perfected for Quad Operational Amplifiers, these dual operational amplifiers feature low power drain, a common mode input voltage range extending to ground/$V_{EE}$, and single supply or split supply operation. The LM358 series is equivalent to one−half of an LM324.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one−fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

### Features

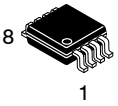
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation:  3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant




**PDIP−8**
**N, AN, VN SUFFIX**
**CASE 626**

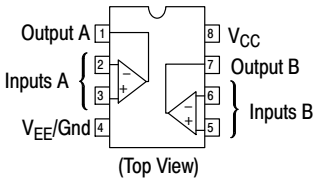



**SOIC−8**
**D, VD SUFFIX**
**CASE 751**




**Micro8™**
**DMR2 SUFFIX**
**CASE 846A**

### PIN CONNECTIONS



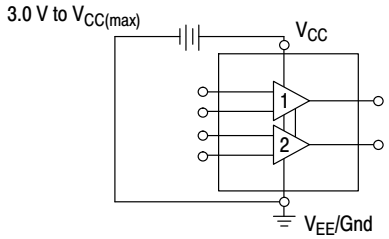

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

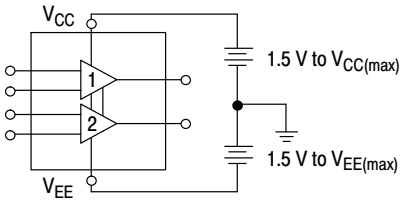
### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.

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Single Supply




Split Supplies

**Figure 1.**

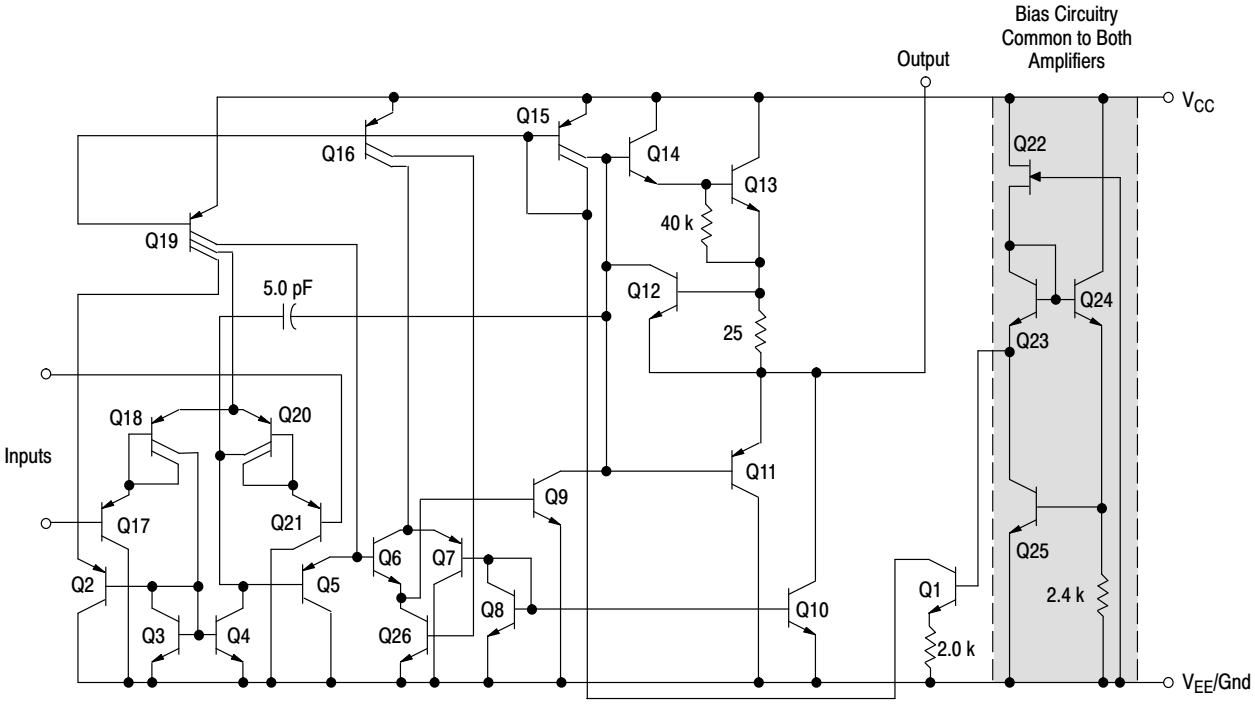



**Figure 2. Representative Schematic Diagram**
(One−Half of Circuit Shown)



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**MAXIMUM RATINGS** ($T_A$ = +25°C, unless otherwise noted.)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Power Supply Voltages<br>Single Supply<br>Split Supplies | | <br>$V_{CC}$<br>$V_{CC}$, $V_{EE}$ | <br>32<br>±16 | Vdc |
| Input Differential Voltage Range (Note 1) | | $V_{IDR}$ | ±32 | Vdc |
| Input Common Mode Voltage Range | | $V_{ICR}$ | −0.3 to 32 | Vdc |
| Output Short Circuit Duration | | $t_{SC}$ | Continuous | |
| Junction Temperature | | $T_J$ | 150 | °C |
| Thermal Resistance, Junction−to−Air (Note 2) | Case 846A<br>Case 751<br>Case 626 | $R_{\theta JA}$ | 238<br>212<br>161 | °C/W |
| Thermal Resistance, Junction−to−Case | Case 751 | $R_{\theta JC}$ | 72 | °C/W |
| Thermal Resistance, Junction−to−Board | Case 751 | $R_{\theta JB}$ | 74 | °C/W |
| Storage Temperature Range | | $T_{stg}$ | −65 to +150 | °C |
| Operating Ambient Temperature Range | <br>LM258<br>LM358, LM358A, LM358E<br>LM2904, LM2904A, LM2904E<br>LM2904V, NCV2904 (Note 3) | $T_A$ | <br>−25 to +85<br>0 to +70<br>−40 to +105<br>−40 to +125 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Split Power Supplies.
2. All $R_{\theta JA}$ measurements made on evaluation board with 1 oz. copper traces of minimum pad size. All device outputs were active.
3. *NCV2904 is qualified for automotive use.*

**ESD RATINGS**

| Rating | HBM | MM | Unit |
|---|---|---|---|
| ESD Protection at any Pin (Human Body Model − HBM, Machine Model − MM) | | | |
| NCV2904 (Note 3) | 2000 | 200 | V |
| LM358E, LM2904E | 2000 | 200 | V |
| LM358DG/DR2G, LM2904DG/DR2G | 250 | 100 | V |
| All Other Devices | 2000 | 200 | V |



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**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = GND, $T_A$ = 25°C, unless otherwise noted.)

| Characteristic | Symbol | LM258 | | | LM358, LM358E | | | LM358A | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>$V_{CC}$ = 5.0 V to 30 V, $V_{IC}$ = 0 V to $V_{CC}$ −1.7 V, $V_O \simeq$ 1.4 V, $R_S$ = 0 Ω | $V_{IO}$ | | | | | | | | | | mV |
| $T_A$ = 25°C | | – | 2.0 | 5.0 | – | 2.0 | 7.0 | – | 2.0 | 3.0 | |
| $T_A$ = $T_{high}$ (Note 4) | | – | – | 7.0 | – | – | 9.0 | – | – | 5.0 | |
| $T_A$ = $T_{low}$ (Note 4) | | – | – | 7.0 | – | – | 9.0 | – | – | 5.0 | |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | $\Delta V_{IO}/\Delta T$ | – | 7.0 | – | – | 7.0 | – | – | 7.0 | – | μV/°C |
| Input Offset Current | $I_{IO}$ | – | 3.0 | 30 | – | 5.0 | 50 | – | 5.0 | 30 | nA |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | | – | – | 100 | – | – | 150 | – | – | 75 | |
| Input Bias Current | $I_{IB}$ | – | −45 | −150 | – | −45 | −250 | – | −45 | −100 | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | | – | −50 | −300 | – | −50 | −500 | – | −50 | −200 | |
| Average Temperature Coefficient of Input Offset Current<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | $\Delta I_{IO}/\Delta T$ | – | 10 | – | – | 10 | – | – | 10 | – | pA/°C |
| Input Common Mode Voltage Range (Note 5), $V_{CC}$ = 30 V | $V_{ICR}$ | 0 | – | 28.3 | 0 | – | 28.3 | 0 | – | 28.5 | V |
| $V_{CC}$ = 30 V, $T_A$ = $T_{high}$ to $T_{low}$ | | 0 | – | 28 | 0 | – | 28 | 0 | – | 28 | |
| Differential Input Voltage Range | $V_{IDR}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | V |
| Large Signal Open Loop Voltage Gain | $A_{VOL}$ | | | | | | | | | | V/mV |
| $R_L$ = 2.0 kΩ, $V_{CC}$ = 15 V, For Large $V_O$ Swing, | | 50 | 100 | – | 25 | 100 | – | 25 | 100 | – | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | | 25 | – | – | 15 | – | – | 15 | – | – | |
| Channel Separation<br>1.0 kHz ≤ f ≤ 20 kHz, Input Referenced | CS | – | −120 | – | – | −120 | – | – | −120 | – | dB |
| Common Mode Rejection<br>$R_S$ ≤ 10 kΩ | CMR | 70 | 85 | – | 65 | 70 | – | 65 | 70 | – | dB |
| Power Supply Rejection | PSR | 65 | 100 | – | 65 | 100 | – | 65 | 100 | – | dB |
| Output Voltage−High Limit<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | $V_{OH}$ | | | | | | | | | | V |
| $V_{CC}$ = 5.0 V, $R_L$ = 2.0 kΩ, $T_A$ = 25°C | | 3.3 | 3.5 | – | 3.3 | 3.5 | – | 3.3 | 3.5 | – | |
| $V_{CC}$ = 30 V, $R_L$ = 2.0 kΩ | | 26 | – | – | 26 | – | – | 26 | – | – | |
| $V_{CC}$ = 30 V, $R_L$ = 10 kΩ | | 27 | 28 | – | 27 | 28 | – | 27 | 28 | – | |
| Output Voltage−Low Limit<br>$V_{CC}$ = 5.0 V, $R_L$ = 10 kΩ,<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | $V_{OL}$ | – | 5.0 | 20 | – | 5.0 | 20 | – | 5.0 | 20 | mV |
| Output Source Current | $I_{O+}$ | | | | | | | | | | mA |
| $V_{ID}$ = +1.0 V, $V_{CC}$ = 15 V | | 20 | 40 | – | 20 | 40 | – | 20 | 40 | – | |
| $T_A$ = $T_{high}$ to $T_{low}$ (LM358A Only) | | | | | | | | 10 | – | – | |
| Output Sink Current | $I_{O-}$ | | | | | | | | | | |
| $V_{ID}$ = −1.0 V, $V_{CC}$ = 15 V | | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | mA |
| $T_A$ = $T_{high}$ to $T_{low}$ (LM358A Only) | | | | | | | | 5.0 | – | – | mA |
| $V_{ID}$ = −1.0 V, $V_O$ = 200 mV | | 12 | 50 | – | 12 | 50 | – | 12 | 50 | – | μA |
| Output Short Circuit to Ground (Note 6) | $I_{SC}$ | – | 40 | 60 | – | 40 | 60 | – | 40 | 60 | mA |
| Power Supply Current (Total Device)<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 4) | $I_{CC}$ | | | | | | | | | | mA |
| $V_{CC}$ = 30 V, $V_O$ = 0 V, $R_L$ = ∞ | | – | 1.5 | 3.0 | – | 1.5 | 3.0 | – | 1.5 | 2.0 | |
| $V_{CC}$ = 5 V, $V_O$ = 0 V, $R_L$ = ∞ | | – | 0.7 | 1.2 | – | 0.7 | 1.2 | – | 0.7 | 1.2 | |

4. LM258: $T_{low}$ = −25°C, $T_{high}$ = +85°C
   LM2904/A/E: $T_{low}$ = −40°C, $T_{high}$ = +105°C
   *NCV2904 is qualified for automotive use.*
   LM358, LM358A, LM358E: $T_{low}$ = 0°C, $T_{high}$ = +70°C
   LM2904V & NCV2904: $T_{low}$ = −40°C, $T_{high}$ = +125°C
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is $V_{CC}$ − 1.7 V, but either or both inputs can go to +32 V without damage, independent of the magnitude of $V_{CC}$.
6. Short circuits from the output to $V_{CC}$ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.



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**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5.0 V, $V_{EE}$ = Gnd, $T_A$ = 25°C, unless otherwise noted.)

| Characteristic | Symbol | LM2904/LM2904E | | | LM2904A | | | LM2904V, NCV2904 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage<br>$V_{CC}$ = 5.0 V to 30 V, $V_{IC}$ = 0 V to $V_{CC}$ −1.7 V, $V_O \simeq$ 1.4 V, $R_S$ = 0 Ω | $V_{IO}$ | | | | | | | | | | mV |
| $T_A$ = 25°C | | – | 2.0 | 7.0 | – | 2.0 | 7.0 | – | – | 7.0 | |
| $T_A$ = $T_{high}$ (Note 7) | | – | – | 10 | – | – | 10 | – | – | 13 | |
| $T_A$ = $T_{low}$ (Note 7) | | – | – | 10 | – | – | 10 | – | – | 10 | |
| Average Temperature Coefficient of Input Offset Voltage<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | $\Delta V_{IO}/\Delta T$ | – | 7.0 | – | – | 7.0 | – | – | 7.0 | – | μV/°C |
| Input Offset Current | $I_{IO}$ | – | 5.0 | 50 | – | 5.0 | 50 | – | 5.0 | 50 | nA |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | | – | 45 | 200 | – | 45 | 200 | – | 45 | 200 | |
| Input Bias Current | $I_{IB}$ | – | −45 | −250 | – | −45 | −100 | – | −45 | −250 | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | | – | −50 | −500 | – | −50 | −250 | – | −50 | −500 | |
| Average Temperature Coefficient of Input Offset Current<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | $\Delta I_{IO}/\Delta T$ | – | 10 | – | – | 10 | – | – | 10 | – | pA/°C |
| Input Common Mode Voltage Range (Note 8), $V_{CC}$ = 30 V | $V_{ICR}$ | 0 | – | 28.3 | 0 | – | 28.3 | 0 | – | 28.3 | V |
| $V_{CC}$ = 30 V, $T_A$ = $T_{high}$ to $T_{low}$ | | 0 | – | 28 | 0 | – | 28 | 0 | – | 28 | |
| Differential Input Voltage Range | $V_{IDR}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | – | – | $V_{CC}$ | V |
| Large Signal Open Loop Voltage Gain | $A_{VOL}$ | | | | | | | | | | V/mV |
| $R_L$ = 2.0 kΩ, $V_{CC}$ = 15 V, For Large $V_O$ Swing, | | 25 | 100 | – | 25 | 100 | – | 25 | 100 | – | |
| $T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | | 15 | – | – | 15 | – | – | 15 | – | – | |
| Channel Separation<br>1.0 kHz ≤ f ≤ 20 kHz, Input Referenced | CS | – | −120 | – | – | −120 | – | – | −120 | – | dB |
| Common Mode Rejection<br>$R_S$ ≤ 10 kΩ | CMR | 50 | 70 | – | 50 | 70 | – | 50 | 70 | – | dB |
| Power Supply Rejection | PSR | 50 | 100 | – | 50 | 100 | – | 50 | 100 | – | dB |
| Output Voltage−High Limit<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | $V_{OH}$ | | | | | | | | | | V |
| $V_{CC}$ = 5.0 V, $R_L$ = 2.0 kΩ, $T_A$ = 25°C | | 3.3 | 3.5 | – | 3.3 | 3.5 | – | 3.3 | 3.5 | – | |
| $V_{CC}$ = 30 V, $R_L$ = 2.0 kΩ | | 26 | – | – | 26 | – | – | 26 | – | – | |
| $V_{CC}$ = 30 V, $R_L$ = 10 kΩ | | 27 | 28 | – | 27 | 28 | – | 27 | 28 | – | |
| Output Voltage−Low Limit<br>$V_{CC}$ = 5.0 V, $R_L$ = 10 kΩ, $T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | $V_{OL}$ | – | 5.0 | 20 | – | 5.0 | 20 | – | 5.0 | 20 | mV |
| Output Source Current<br>$V_{ID}$ = +1.0 V, $V_{CC}$ = 15 V | $I_{O+}$ | 20 | 40 | – | 20 | 40 | – | 20 | 40 | – | mA |
| Output Sink Current | $I_{O-}$ | | | | | | | | | | |
| $V_{ID}$ = −1.0 V, $V_{CC}$ = 15 V | | 10 | 20 | – | 10 | 20 | – | 10 | 20 | – | mA |
| $V_{ID}$ = −1.0 V, $V_O$ = 200 mV | | – | – | – | – | – | – | – | – | – | μA |
| Output Short Circuit to Ground (Note 9) | $I_{SC}$ | – | 40 | 60 | – | 40 | 60 | – | 40 | 60 | mA |
| Power Supply Current (Total Device)<br>$T_A$ = $T_{high}$ to $T_{low}$ (Note 7) | $I_{CC}$ | | | | | | | | | | mA |
| $V_{CC}$ = 30 V, $V_O$ = 0 V, $R_L$ = ∞ | | – | 1.5 | 3.0 | – | 1.5 | 3.0 | – | 1.5 | 3.0 | |
| $V_{CC}$ = 5 V, $V_O$ = 0 V, $R_L$ = ∞ | | – | 0.7 | 1.2 | – | 0.7 | 1.2 | – | 0.7 | 1.2 | |

7. LM258: $T_{low}$ = −25°C, $T_{high}$ = +85°C
   LM358, LM358A, LM358E: $T_{low}$ = 0°C, $T_{high}$ = +70°C
   LM2904/A/E: $T_{low}$ = −40°C, $T_{high}$ = +105°C
   LM2904V & NCV2904: $T_{low}$ = −40°C, $T_{high}$ = +125°C
   *NCV2904 is qualified for automotive use.*
8. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is $V_{CC}$ − 1.7 V, but either or both inputs can go to +32 V without damage, independent of the magnitude of $V_{CC}$.
9. Short circuits from the output to $V_{CC}$ can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



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## CIRCUIT DESCRIPTION

The LM358 series is made using two internally compensated, two−stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single−ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal−voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

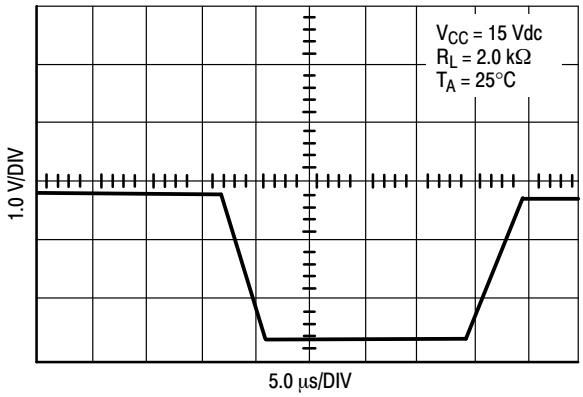



**Figure 3. Large Signal Voltage Follower Response**

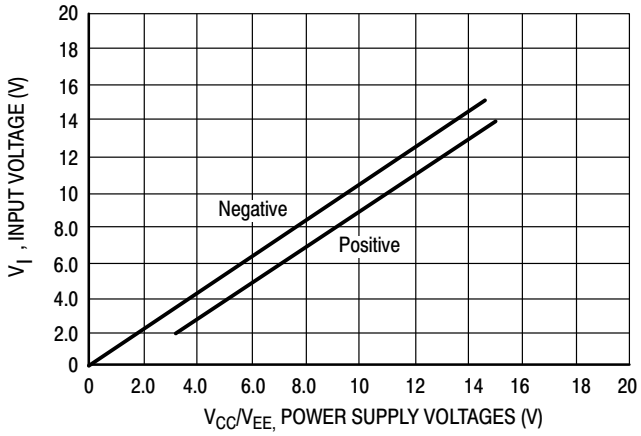



**Figure 4. Input Voltage Range**

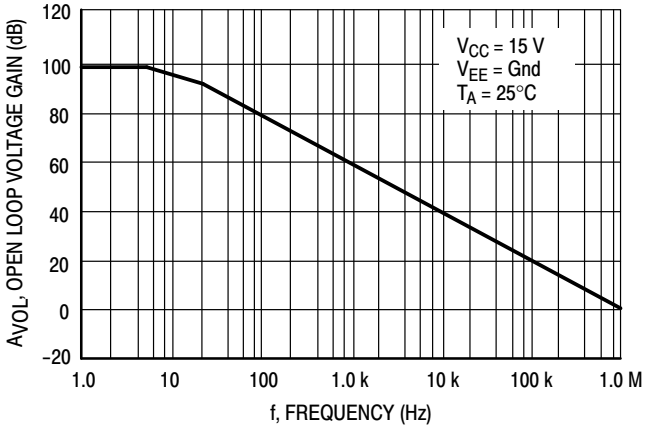



**Figure 5. Large−Signal Open Loop Voltage Gain**



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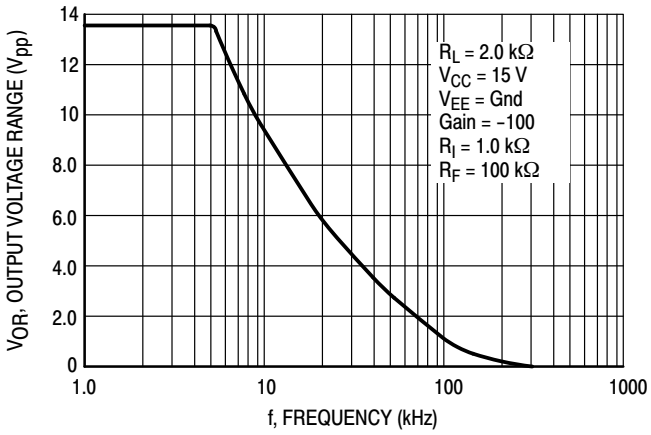



**Figure 6. Large−Signal Frequency Response**

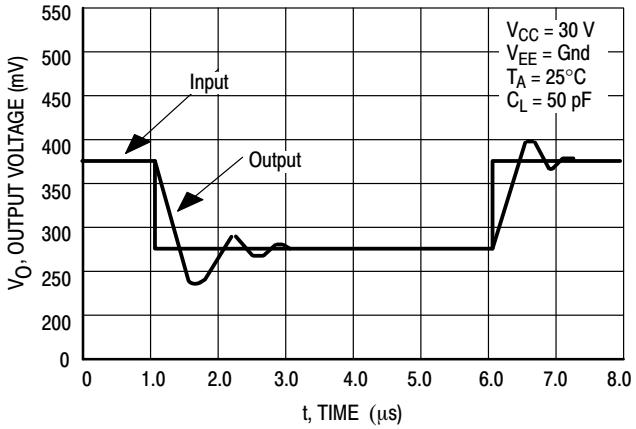



**Figure 7. Small Signal Voltage Follower Pulse Response (Noninverting)**

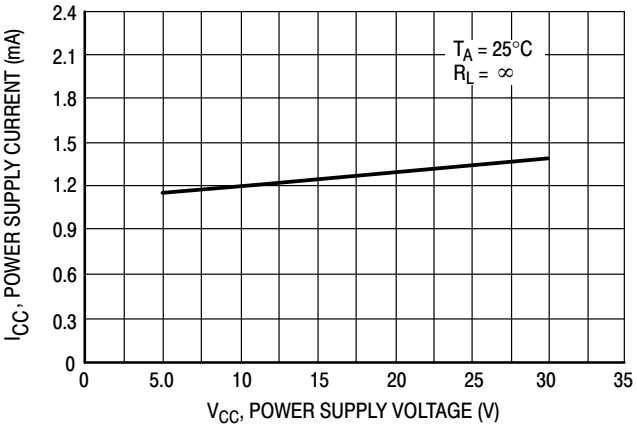



**Figure 8. Power Supply Current versus Power Supply Voltage**

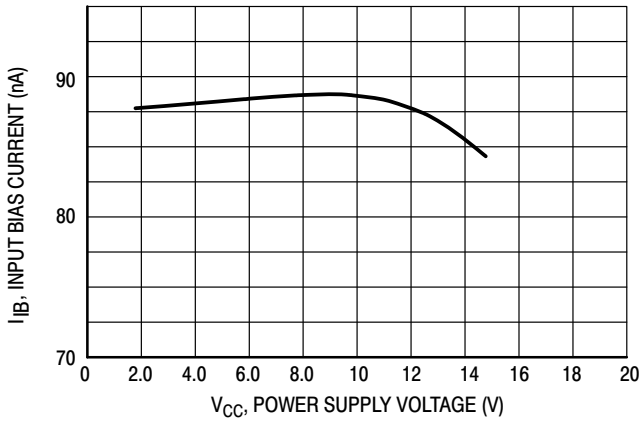



**Figure 9. Input Bias Current versus Supply Voltage**



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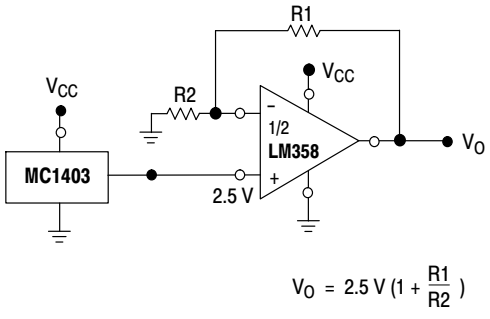



Figure 10. Voltage Reference

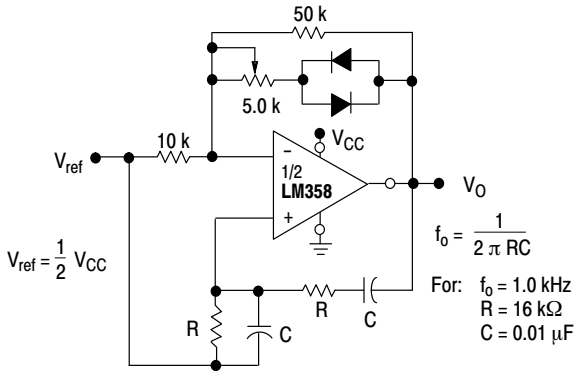



Figure 11. Wien Bridge Oscillator

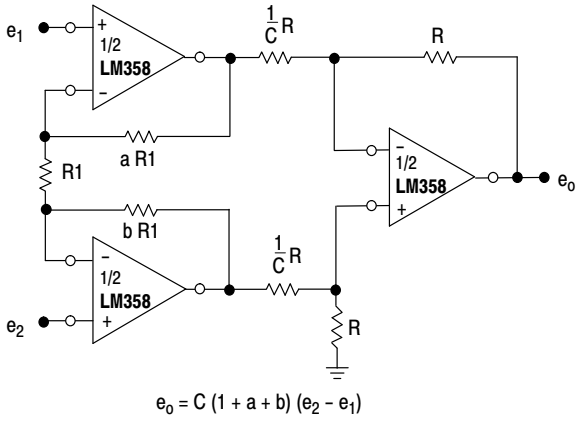



Figure 12. High Impedance Differential Amplifier

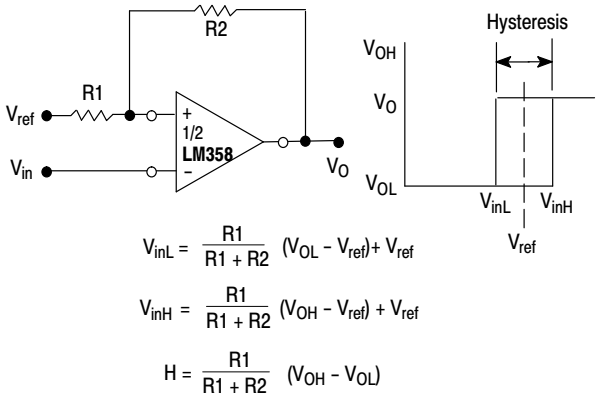



Figure 13. Comparator with Hysteresis

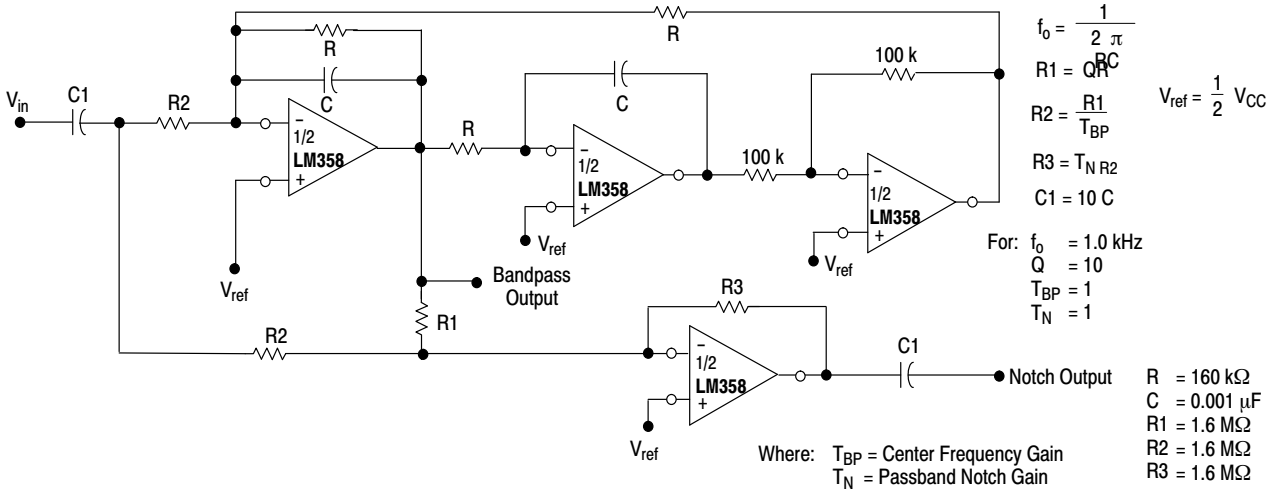
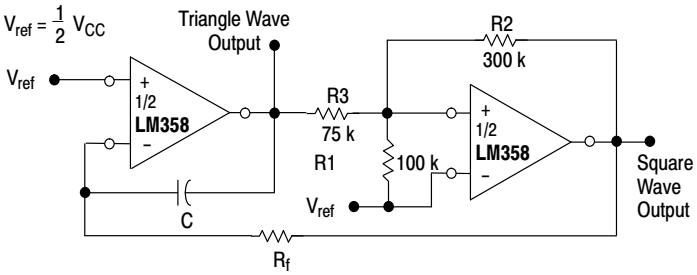



Figure 14. Bi−Quad Filter

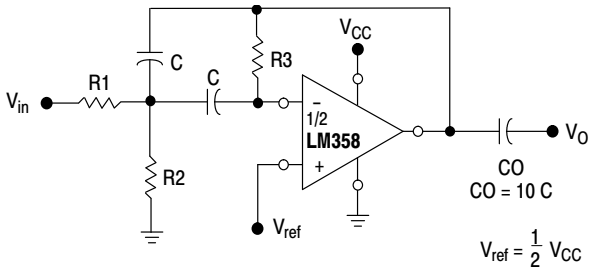


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$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if,} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

**Figure 15. Function Generator**




Given: $f_o$ = center frequency
$A(f_o)$ = gain at center frequency

Choose value $f_o$, C

Then: $R3 = \frac{Q}{\pi\, f_o\, C}$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier. $\frac{Q_o\, f_o}{BW} < 0.1$

Where $f_o$ and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

**Figure 16. Multiple Feedback Bandpass Filter**



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## ORDERING INFORMATION

| Device | Operating Temperature Range | Package | Shipping† |
|---|---|---|---|
| LM358ADR2G | 0°C to +70°C | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| LM358DG | | | 98 Units / Rail |
| LM358DR2G | | | 2500 / Tape & Reel |
| LM358EDR2G | | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| LM358DMR2G | | Micro8 (Pb−Free) | 4000 / Tape & Reel |
| LM358NG | | PDIP−8 (Pb−Free) | 50 Units / Rail |
| LM258DG | −25°C to +85°C | SOIC−8 (Pb−Free) | 98 Units / Rail |
| LM258DR2G | | | 2500 / Tape & Reel |
| LM258DMR2G | | Micro8 (Pb−Free) | 4000 / Tape & Reel |
| LM258NG | | PDIP−8 (Pb−Free) | 50 Units / Rail |
| LM2904DG | −40°C to +105°C | SOIC−8 (Pb−Free) | 98 Units / Rail |
| LM2904DR2G | | | 2500 / Tape & Reel |
| LM2904EDR2G | | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| LM2904DMR2G | | Micro8 (Pb−Free) | 2500 / Tape & Reel |
| LM2904NG | | PDIP−8 (Pb−Free) | 50 Units / Rail |
| LM2904ADMG | | Micro8 (Pb−Free) | 4000 / Tape & Reel |
| LM2904ADMR2G | | | 4000 / Tape & Reel |
| LM2904ANG | | PDIP−8 (Pb−Free) | 50 Units / Rail |
| LM2904VDG | −40°C to +125°C | SOIC−8 (Pb−Free) | 98 Units / Rail |
| LM2904VDR2G | | | 2500 / Tape & Reel |
| LM2904VDMR2G | | Micro8 (Pb−Free) | 4000 / Tape & Reel |
| LM2904VNG | | PDIP−8 (Pb−Free) | 50 Units / Rail |
| NCV2904DR2G* | | SOIC−8 (Pb−Free) | 2500 / Tape & Reel |
| NCV2904DMR2G* | | Micro8 (Pb−Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

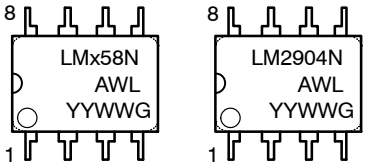
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.



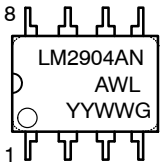
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## MARKING DIAGRAMS

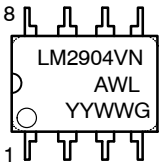
**PDIP−8**
**N SUFFIX**
**CASE 626**



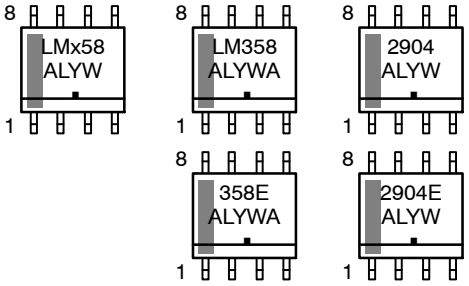

**PDIP−8**
**AN SUFFIX**
**CASE 626**



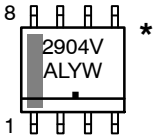

**PDIP−8**
**VN SUFFIX**
**CASE 626**



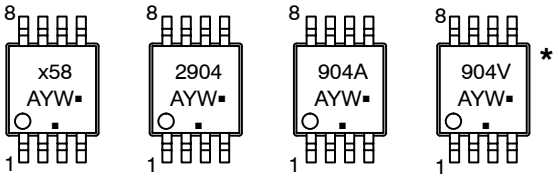

**SOIC−8**
**D SUFFIX**
**CASE 751**




**SOIC−8**
**VD SUFFIX**
**CASE 751**




**Micro8**
**DMR2 SUFFIX**
**CASE 846A**




*This diagram also applies to NCV2904

x = 2 or 3
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package
▪ = Pb−Free Package − (Note: Microdot may be in either location)



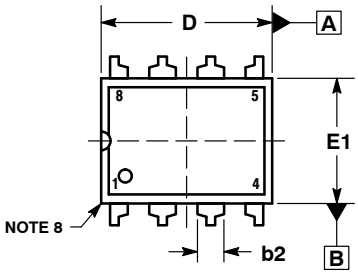
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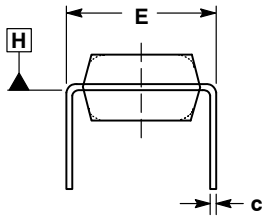
**SCALE 1:1**

**PDIP–8**
CASE 626–05
ISSUE P

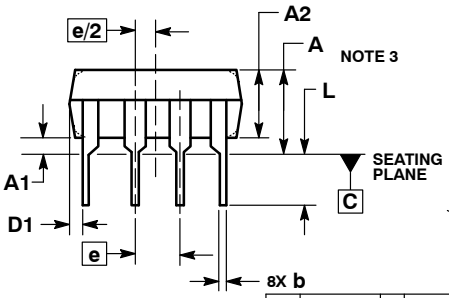
DATE 22 APR 2015



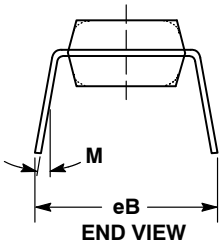

**TOP VIEW**




**END VIEW**
**WITH LEADS CONSTRAINED**
**NOTE 5**




**SIDE VIEW**



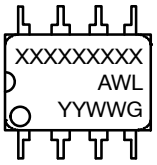

**END VIEW**
**NOTE 6**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | ---- | 0.210 | --- | 5.33 |
| A1 | 0.015 | ---- | 0.38 | --- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.355 | 0.400 | 9.02 | 10.16 |
| D1 | 0.005 | ---- | 0.13 | --- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | ---- | 0.430 | --- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | ---- | 10° | --- | 10° |

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. $V_{CC}$

**GENERIC**
**MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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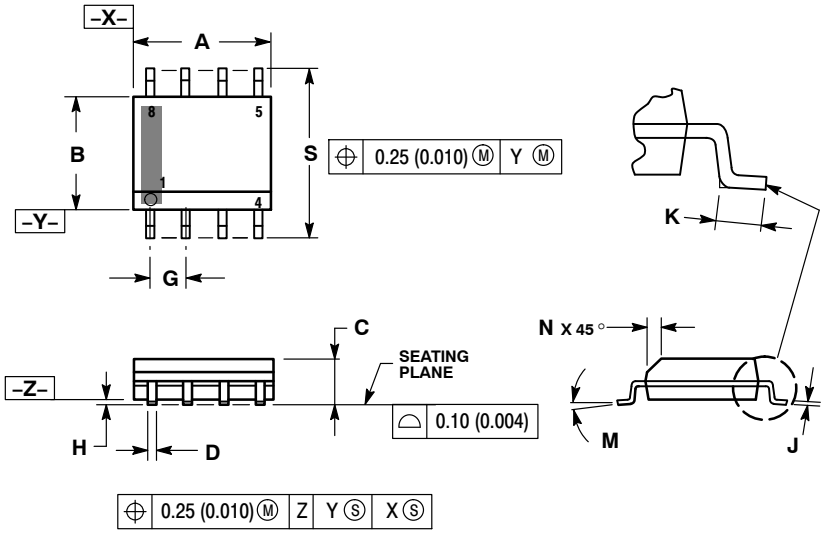
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**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

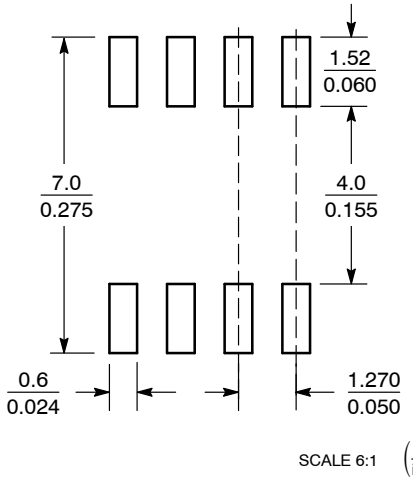
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

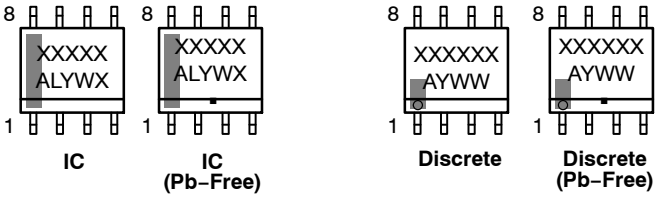
## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

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**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

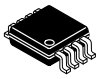
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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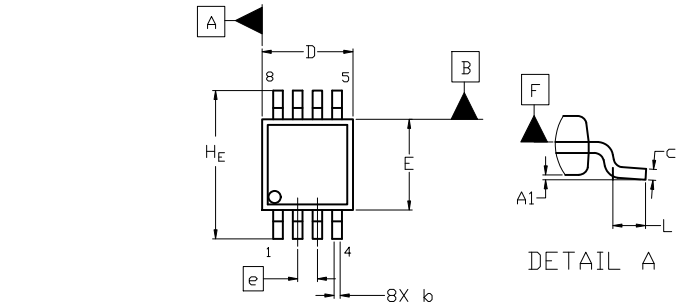
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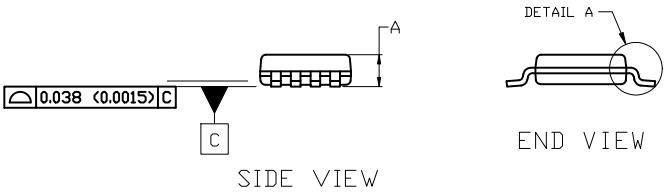


**SCALE 2:1**

**Micro8**
CASE 846A–02
ISSUE K

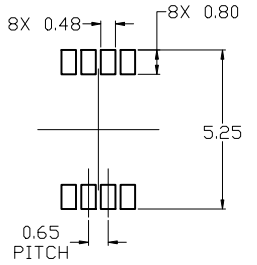
DATE 16 JUL 2020




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

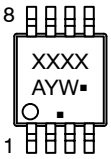



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.10 |
| A1 | 0.05 | 0.08 | 0.15 |
| b | 0.25 | 0.33 | 0.40 |
| c | 0.13 | 0.18 | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| e | 0.65 BSC | | |
| $H_E$ | 4.75 | 4.90 | 5.05 |
| L | 0.40 | 0.55 | 0.70 |

## GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

| | | |
|---|---|---|
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| **DESCRIPTION:** | **MICRO8** | **PAGE 1 OF 1** |

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