ESD Protection Diode Array

Ultra Low Capacitance ESD Protection for High Speed Data Line Protection

ESDR0502N

The ESDR0502N ultra low capacitance surge protection array is designed to protect high speed data lines from ESD. Ultra−low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 applications.

Features

- Low Capacitance (0.3 pF Typical Between I/O Lines and Ground)
- IEC 61000−4−2 Level 4
- UL Flammability Rating of 94 V−0
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

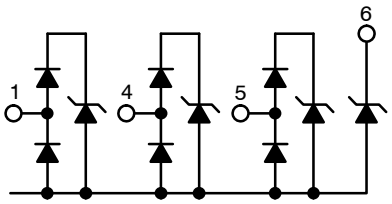
- High Speed Communication Line Protection
- USB 2.0 High Speed Data Line and Power Line Protection
- Monitors and Flat Panel Displays
- MP3
- Gigabit Ethernet

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−40 to +125	°C
Peak Power Dissipation 8x20 μs @ T_A = 25°C (Note 1)	P_{pk}	100	W
Peak Power Current 8x20 μs @ T_A = 25°C (Note 1)	I_{pp}	3.0	A
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD)	ESD	8.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Nonrepetitive current pulse (pin 6 to pin 1).





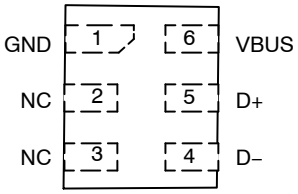
UDFN6
MU SUFFIX
CASE 517AA

MARKING DIAGRAM



D = Specific Device Code*
(Rotated 90° clockwise)
M = Date Code & Assembly Location

PINOUT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
ESDR0502NMUTAG	UDFN6 (Pb−Free)	3000 / Tape & Reel
ESDR0502NMUTBG	UDFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

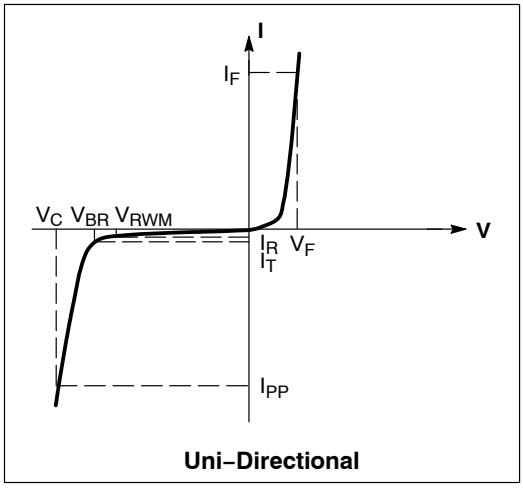
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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 2)			5.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, (Note 3)	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5.5 V			1.0	μA
ESD Clamping Voltage	V_C	Per IEC61000−4−2 (Note 4)	See Figures 1 & 2			
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.3	0.6	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		0.3	0.6	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V_{BR} is measured at pulse test current I_T.
4. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

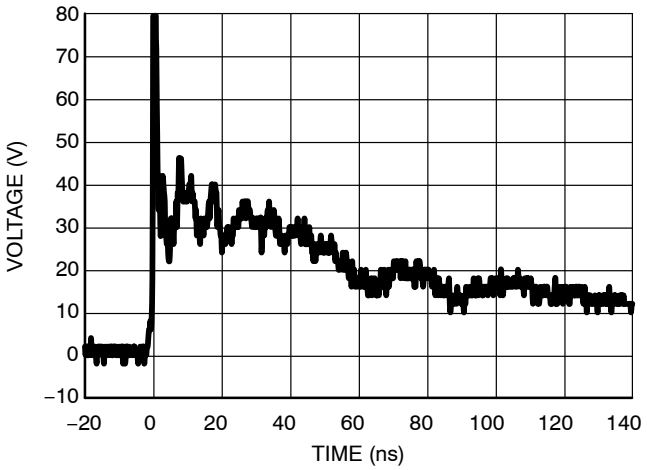


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

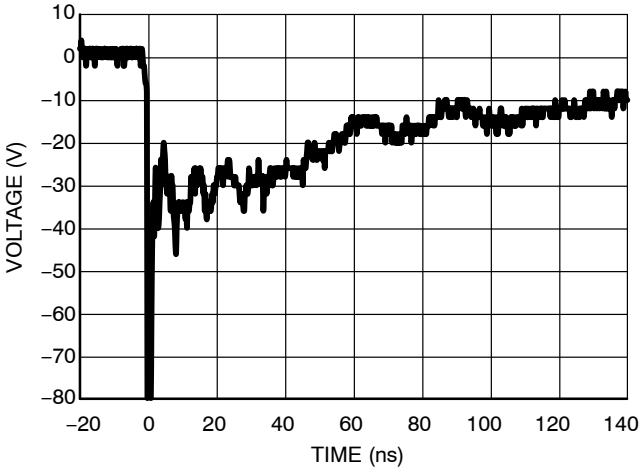


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

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IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

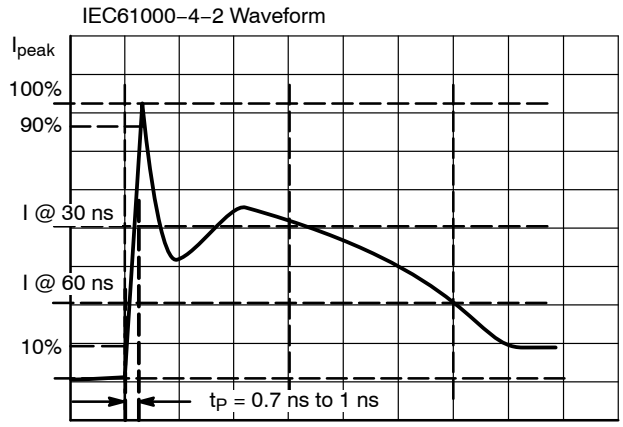


Figure 3. IEC61000−4−2 Spec

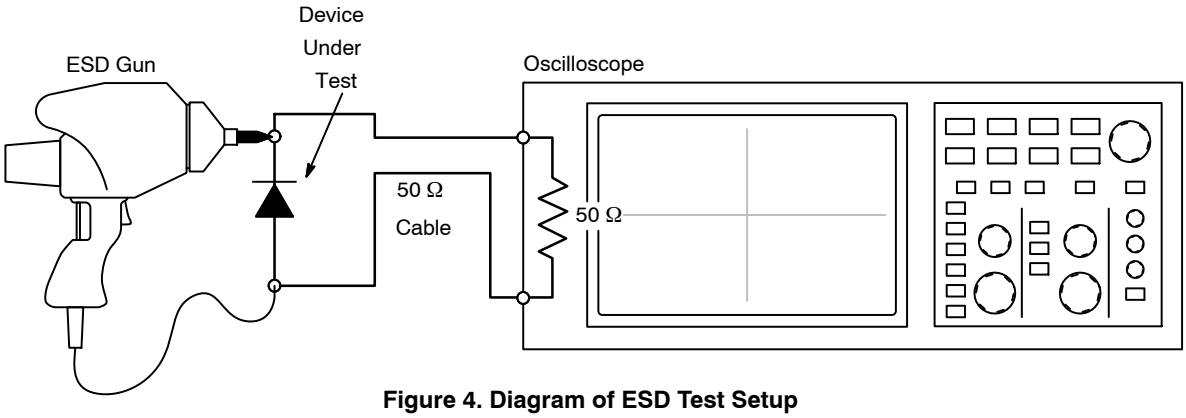


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

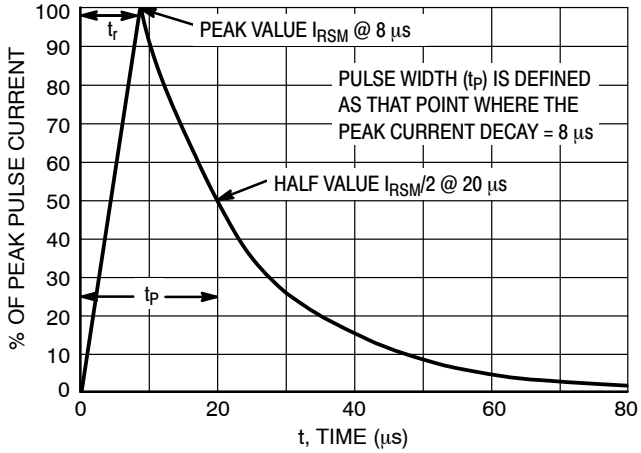


Figure 5. 8 x 20 μs Pulse Waveform

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APPLICATION INFORMATION

Protecting USB 2.0 Interfaces

The USB interface consists of Data (D− and D+) lines and a 5.5 V bus, which are all vulnerable to ESD and cable discharge events. Each ESDR0502N device will protect the four USB connections (V_{CC}, D+, D−, and GND) of one USB port. When the voltage on the data lines exceed the breakdown voltage of the protection device, the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The surge protection diode suppresses ESD strikes directly on the voltage bus and directs the surge to ground, protecting both the power and data pins.

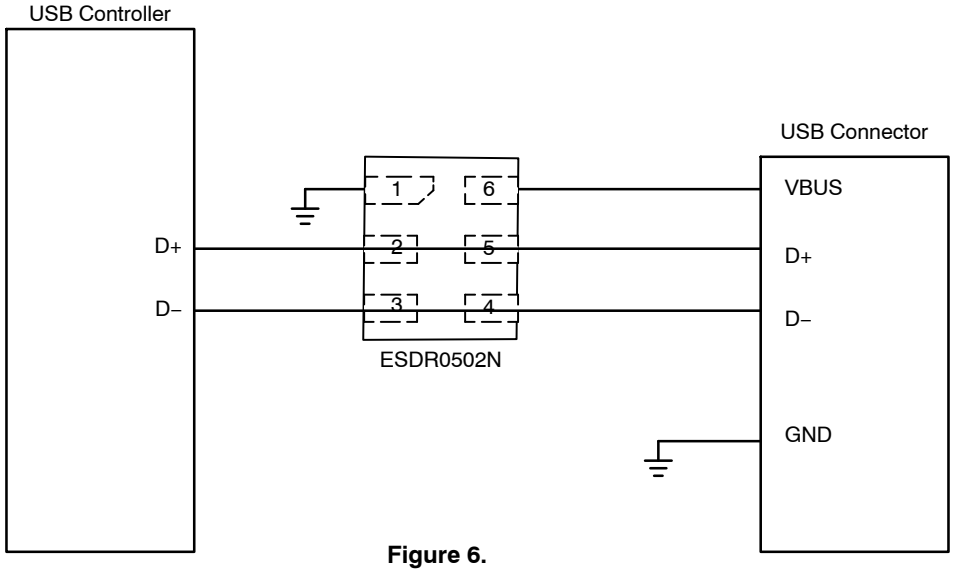
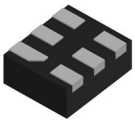


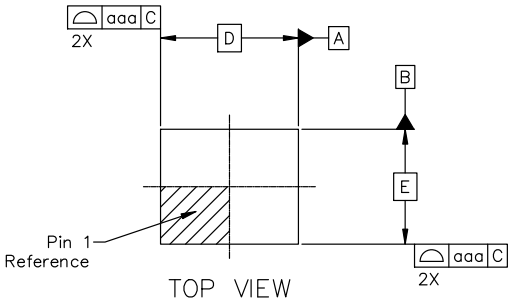
Figure 6.

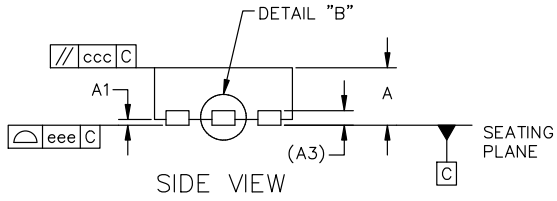
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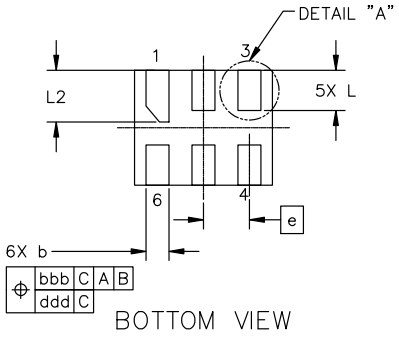


UDFN−6, 1.20x1.00x0.50, 0.40P
CASE 517AA
ISSUE F

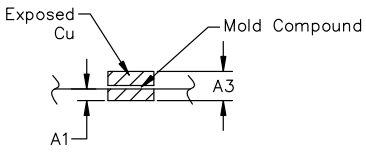
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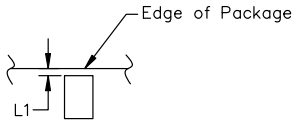




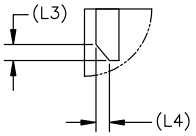
NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO TH EXPOSED PAD AS WELL AS THE TERMINALS.



DETAIL "B"
Scale 2:1
Side View
(Optional)



DETAIL "A"
Scale 2:1
Bottom View
(Optional)



PIN 1
Chamfer Dimension

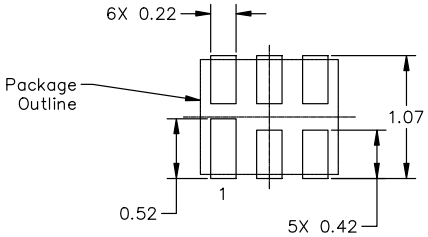
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	−−−	0.05
A3		0.127 REF	
b	0.15	0.20	0.25
D		1.20 BSC	
E		1.00 BSC	
e		0.40 BSC	
L	0.30	0.35	0.40
L1	0.00	−−−	0.15
L2	0.40	0.45	0.50
L3		0.14 REF	
L4		0.116 REF	
TOLERANCE FORM & POSITION			
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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