# TRS3253E RS-232 Transceiver With Split Supply Pin for Logic Side

## 1 Features

- $V_L$ Pin for Compatibility With Mixed-Voltage Systems Down to 1.8 V on Logic Side
- Enhanced ESD Protection on RIN Inputs and DOUT Outputs
  - ±15-kV IEC 61000-4-2 Air-Gap Discharge
  - ±8-kV IEC 61000-4-2 Contact Discharge
  - ±15-kV Human Body Model
- Low 300-μA Supply Current
- Specified 1000-kbps Data Rate
- Auto Powerdown Plus Feature

## 2 Applications

- Hand-Held Equipment
- Cell Phones
- Battery-Powered Equipment
- Data Cables
- POS Equipment
- HDMI Switch Matrix
- Debug Ports

## 3 Description

The TRS3253E device is a three-driver and five-receiver RS-232 interface device, with split supply pins for mixed-signal operations without needing an external voltage translator. All RS-232 inputs and outputs are protected to ±15 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human Body Model.

The charge pump requires only four capacitors for operation from a single 3.3-V or 5-V supply. The TRS3253E is capable of running at data rates up to 1000 kbps, while maintaining RS-232 compliant output levels.

The TRS3253E is available in a space-saving VQFN package (4-mm × 4-mm RSM).

Auto-powerdown-plus automatically powers down drivers to reduce power after 30 seconds of inactivity. In powerdown state supply current is 10 μA maximum.

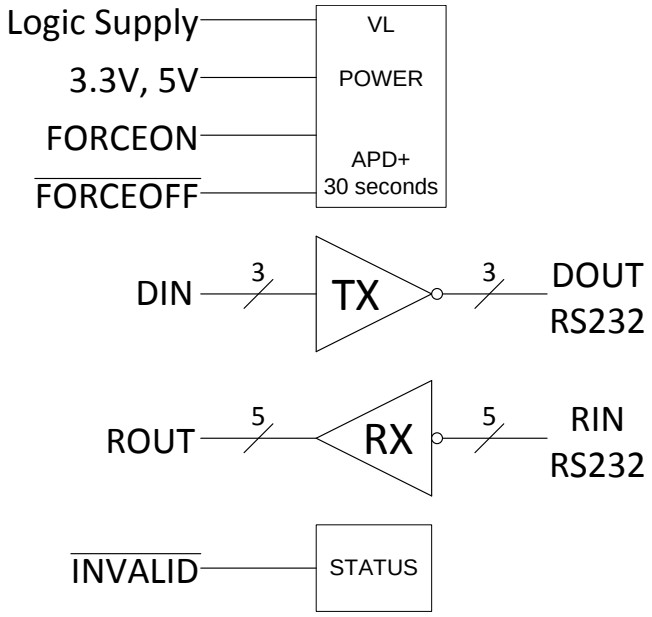
Receiver input voltage status is available on $\overline{\text{INVALID}}$ logic output even when the device is in powerdown state.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TRS3253ERSM | VQFN (32) | 4.00 mm × 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Diagram**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (June 2015) to Revision D | Page |
|---|---|
| • Changed "IEC61000-4-2, Contact Discharge" from "8 kV" to "15 kV" in *Features*, *Description*, *Overview* and *ESD Ratings* | 5 |

| Changes from Revision B (December 2013) to Revision C | Page |
|---|---|
| • Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |


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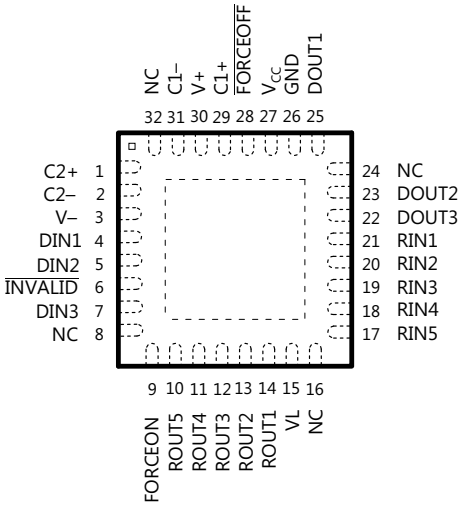
# 5 Pin Configuration and Functions

**RSM Package**
**32-Pin VQFN**
**Top View**




Power pad can be connected to GND or floating.

NC – No internal connection.

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| C1+ | 29 | — | Positive terminals of the voltage-doubler charge-pump capacitors |
| C2+ | 1 | | |
| C1– | 31 | — | Negative terminals of the voltage-doubler charge-pump capacitors |
| C2– | 2 | | |
| DIN1 | 4 | I | Driver inputs |
| DIN2 | 5 | | |
| DIN3 | 7 | | |
| DOUT1 | 25 | O | RS-232 driver outputs |
| DOUT2 | 23 | | |
| DOUT3 | 22 | | |
| $\overline{\text{FORCEOFF}}$ | 28 | I | Auto-powerdown-plus control input |
| FORCEON | 9 | I | Auto-powerdown-plus control input |
| GND | 26 | — | Ground |
| $\overline{\text{INVALID}}$ | 6 | O | Invalid output pin. Active low when all RIN inputs are unpowered |
| NC | 8 | — | No connect pins (do not connect to these pins) |
| | 16 | | |
| | 24 | | |
| | 32 | | |
| RIN1 | 21 | I | RS-232 receiver inputs |
| RIN2 | 20 | | |
| RIN3 | 19 | | |
| RIN4 | 18 | | |
| RIN5 | 17 | | |

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## Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ROUT1 | 14 | O | Receiver outputs. Swing between 0 and $V_L$ |
| ROUT2 | 13 | | |
| ROUT3 | 12 | | |
| ROUT4 | 11 | | |
| ROUT5 | 10 | | |
| $V_{CC}$ | 27 | — | 3-V to 5.5-V supply voltage |
| $V_L$ | 15 | — | Logic-level supply. All CMOS inputs and outputs are referenced to this supply |
| V+ | 30 | O | 5.5-V supply generated by the charge pump |
| V– | 3 | O | –5.5-V supply generated by the charge pump |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $V_{CC}$ to GND | | –0.3 | 6 | V |
| | $V_L$ to GND | | –0.3 | $V_{CC}$ + 0.3 | |
| | V+ to GND | | –0.3 | 7 | |
| | V– to GND | | 0.3 | –7 | |
| | V+ + \|V–\|[2] | | | 13 | |
| $V_I$ | Input voltage | DIN, $\overline{\text{FORCEOFF}}$, and FORCEON to GND | –0.3 | 6 | V |
| | | RIN to GND | | ±25 | |
| $V_O$ | Output voltage | DOUT to GND | | ±13.2 | V |
| | | ROUT to GND | –0.3 | $V_L$ + 0.3 | |
| | Continuous power dissipation | $T_A$ = 85°C, 32-pin RSM ($R_{\theta JA}$ = 37.2°C/W)[3] | | 1747 | mW |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability..
(2) V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.
(3) Maximum power dissipation is a function of $T_J$(max), $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / R_{\theta JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | All pins except 17 to 23 and 25 | ±2000 | V |
| | | | Pins 17 to 23 and 25 | ±15000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | All pins | ±1500 | |
| | | IEC61000-4-2, Contact discharge | Pins 17 to 23 and 25 | ±8000 | |
| | | IEC61000-4-2, Air-gap discharge | Pins 17 to 23 and 25 | ±15000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 3 | 5.5 | V |
| $V_L$ | Supply voltage | | | 1.65 | $V_{CC}$ | V |
| | Input logic low | DIN, $\overline{\text{FORCEOFF}}$, FORCEON | $V_L$ = 3 V or 5.5 V | 0 | 0.8 | V |
| | | | $V_L$ = 2.3 V | 0 | 0.6 | |
| | | | $V_L$ = 1.65 V | 0 | 0.5 | |
| | Input logic high | DIN, $\overline{\text{FORCEOFF}}$, FORCEON | $V_L$ = 5.5 V | 2.4 | $V_L$ | V |
| | | | $V_L$ = 3 V | 2 | $V_L$ | |
| | | | $V_L$ = 2.7 V | 1.4 | $V_L$ | |
| | | | $V_L$ = 1.95 V | 1.25 | $V_L$ | |
| | Operating temperature | | TRS3253EIRSMR | –40 | 85 | °C |
| | Receiver input voltage | | | –25 | 25 | V |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TRS3253E RSM (VQFN) 32 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 37.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 30.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 7.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 7.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics—Power

over operating free-air temperature range, $V_{CC} = V_L$ = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%) (unless otherwise noted)[1]

| PARAMETER | | | TEST CONDITIONS | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_I$ | Input leakage current | $\overline{\text{FORCEOFF}}$, FORCEON | | | ±0.01 | ±1 | µA |
| $I_{CC}$ | Supply current ($T_A$ = 25°C) | Auto-powerdown plus disabled | No load, $\overline{\text{FORCEOFF}}$ and FORCEON at $V_{CC}$ | | 0.5 | 1 | mA |
| | | Powered off | No load, $\overline{\text{FORCEOFF}}$ at GND | | 1 | 10 | µA |
| | | Auto-powerdown plus active | No load, $\overline{\text{FORCEOFF}}$ at $V_{CC}$, FORCEON at GND, All RIN are open or grounded | | 1 | 10 | |

(1) Testing supply conditions are C1–C4 = 0.1 µF at $V_{CC}$ = 3.3 V ± 0.15 V; C1–C4 = 0.22 µF at $V_{CC}$ = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2–C4 = 0.33 µF at $V_{CC}$ = 5 V ± 0.5 V. (See Figure 8)
(2) All typical values are at $V_{CC}$ = 3.3 V or $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## 6.6 Electrical Characteristics—Driver

over operating free-air temperature range, $V_{CC} = V_L$ = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to $T_{MAX}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output voltage swing | All driver outputs loaded with 3 kΩ to ground, $V_{CC}$= 3.1V to 5.5V | ±5 | ±5.4 | | V |
| $r_O$ | Output resistance | $V_{CC}$ = V+ = V– = 0, Driver output = ±2 V | 300 | 10M | | Ω |
| $I_{OS}$ | Output short-circuit current | $V_{T_OUT}$ = 0 | | | ±60 | mA |
| $I_{OZ}$ | Output leakage current | $V_{T_OUT}$ = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, $V_{CC}$ = 3 V to 3.6 V | | | ±25 | µA |
| | | $V_{T_OUT}$ = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, $V_{CC}$ = 4.5 V to 5.5 V | | | | |
| | Driver input hysteresis | | | | 0.5 | V |
| | Input leakage current | DIN, $\overline{\text{FORCEOFF}}$, FORCEON | | ±0.01 | ±1 | µA |

(1) Typical values are at $V_{CC} = V_L$ = 3.3 V, $T_A$ = 25°C

## 6.7 Electrical Characteristics—Receiver

over operating free-air temperature range, $V_{CC} = V_L$ = 3 V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to $T_{MAX}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{off}$ | Output leakage current | ROUT, receivers disabled | | ±0.05 | ±10 | µA |
| $V_{OL}$ | Output voltage low | $I_{OUT}$ = 1.6 mA | | | 0.4 | V |
| $V_{OH}$ | Output voltage high | $I_{OUT}$ = –1 mA | $V_L$ – 0.6 | $V_L$ – 0.1 | | V |

(1) Typical values are at $V_{CC} = V_L$ = 3.3 V, $T_A$ = 25°C


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## Electrical Characteristics—Receiver (continued)

over operating free-air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to $T_{MAX}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT-}$ | Input threshold low | $T_A = 25°C$ | $V_L = 5$ V | 0.8 | 1.2 | | V |
| | | | $V_L = 3.3$ V | 0.6 | 1.5 | | |
| $V_{IT+}$ | Input threshold high | $T_A = 25°C$ | $V_L = 5$ V | | 1.8 | 2.4 | V |
| | | | $V_L = 3.3$ V | | 1.5 | 2.4 | |
| $V_{hys}$ | Input hysteresis | | | | 0.5 | | V |
| | Input resistance | $T_A = 25°C$ | | 3 | 5 | 7 | kΩ |

## 6.8 Electrical Characteristics—Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IT+(valid)}$ | Receiver input threshold for $\overline{INVALID}$ high-level output voltage | FORCEON = GND, $\overline{FORCEOFF} = V_L$ | | 2.7 | V |
| $V_{IT-(valid)}$ | Receiver input threshold for $\overline{INVALID}$ high-level output voltage | FORCEON = GND, $\overline{FORCEOFF} = V_L$ | –2.7 | | V |
| $V_{T(invalid)}$ | Receiver input threshold for $\overline{INVALID}$ low-level output voltage | FORCEON = GND, $\overline{FORCEOFF} = V_L$ | –0.3 | 0.3 | V |
| $V_{OH}$ | $\overline{INVALID}$ high-level output voltage | $I_{OH} = –1$ mA, FORCEON = GND, $\overline{FORCEOFF} = V_L$ | $V_L – 0.6$ | | V |
| $V_{OL}$ | $\overline{INVALID}$ low-level output voltage | $I_{OL} = 1.6$ mA, FORCEON = GND, $\overline{FORCEOFF} = V_L$ | | 0.4 | V |

## 6.9 Switching Characteristics—Driver

over operating free-air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to $T_{MAX}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Maximum data rate | $R_L = 3$ kΩ, $C_L = 200$ pF, one driver switching | | 1000 | | | kbps |
| | Time-to-exit powerdown | $\|V_{T_OUT}\| > 3.7$ V | | | 100 | | μs |
| $\|t_{PHL} – t_{PLH}\|$ | Driver skew(2) | | | | 100 | | ns |
| | Transition-region slew rate | $V_{CC} = 3.3$ V, $T_A = 25°C$, $R_L = 3$ kΩ to 7 kΩ, Measured from 3 V to –3 V or –3 V to 3 V | $C_L = 150$ pF to 1000 pF | 15 | | 150 | V/μs |

(1) Typical values are at $V_{CC} = V_L = 3.3$ V, $T_A = 25°C$.
(2) Driver skew is measured at the driver zero crosspoint.

## 6.10 Switching Characteristics—Receiver

over operating free-air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%), $T_A = T_{MIN}$ to $T_{MAX}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Receiver propagation delay | Receiver input to receiver output, $C_L = 150$ pF | | 0.15 | | μs |
| $t_{PLH}$ | | | | 0.15 | | |
| $t_{PHL} – t_{PLH}$ | Receiver skew | | | 50 | | ns |
| $t_{en}$ | Receiver output enable time | From $\overline{FORCEOFF}$ | | 200 | | |
| $t_{dis}$ | Receiver output disable time | From $\overline{FORCEOFF}$ | | 200 | | |

(1) Typical values are at $V_{CC} = V_L = 3.3$ V, $T_A = 25°C$.

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## 6.11 Switching Characteristics—Power and Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 7)

| PARAMETER | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{valid}$ | Propagation delay time, low- to high-level output | | 0.1 | | µs |
| $t_{invalid}$ | Propagation delay time, high- to low-level output | | 50 | | |
| $t_{en}$ | Supply enable time | | 25 | | |
| $t_{dis}$ | Receiver or driver edge to auto-powerdown plus | 15 | 30 | 60 | s |

(1) All typical values are at $V_{CC}$ = $V_L$ = 3.3 V and TA = 25°C.


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## 6.12 Typical Characteristics

$V_{CC}$ = 3.3 V

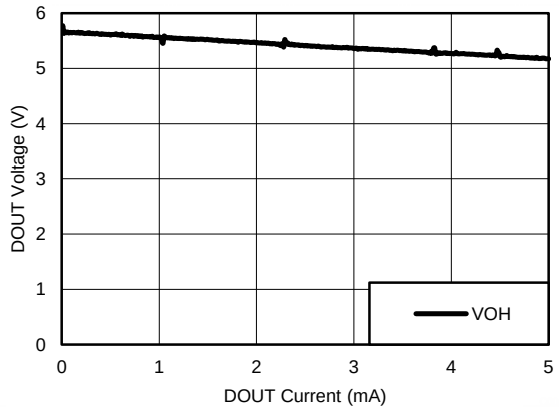



**Figure 1. DOUT $V_{OH}$ vs Load Current Other Drivers 3-kΩ Load**

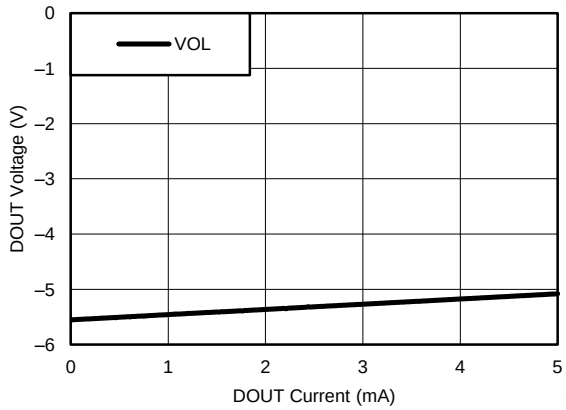
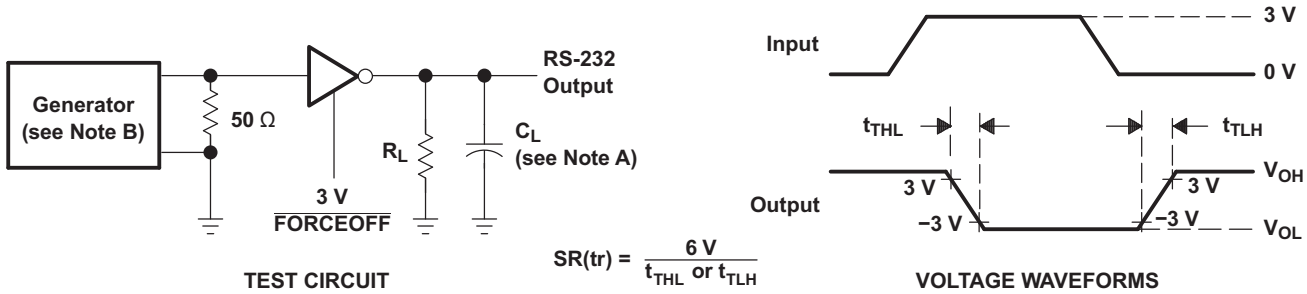



**Figure 2. DOUT $V_{OL}$ vs Load Current Other Drivers 3-kΩ Load**

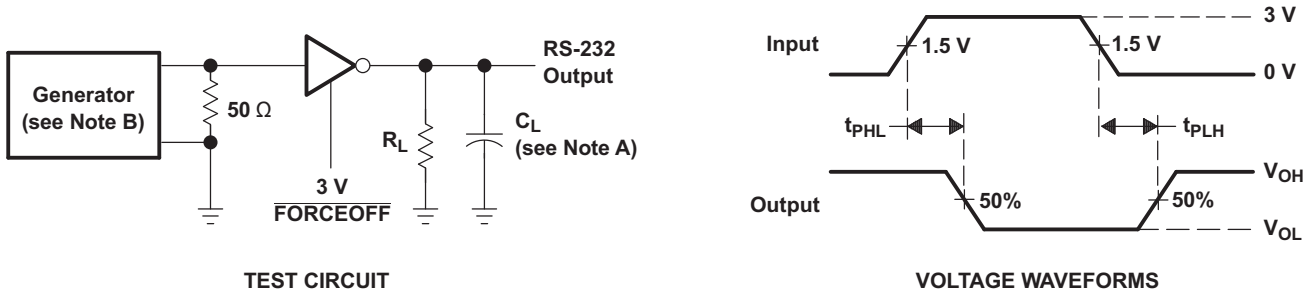
# 7 Parameter Measurement Information




A. $C_L$ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r$ ≤ 10 ns, $t_f$ ≤ 10 ns.

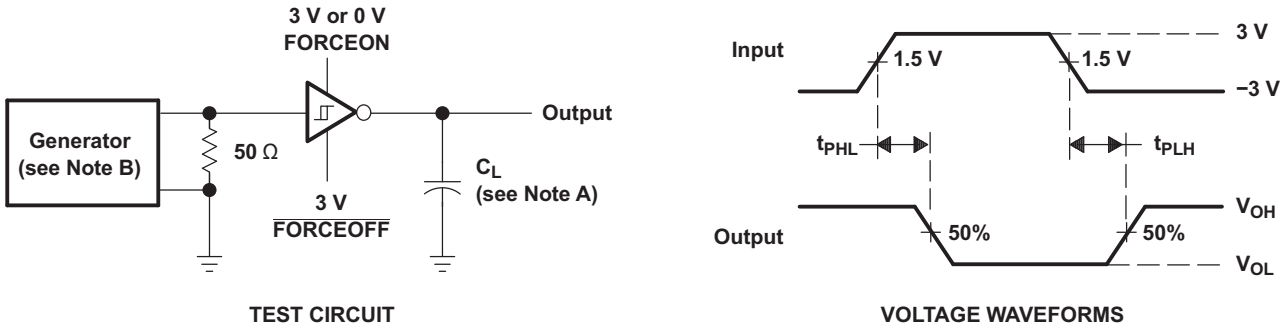
**Figure 3. Driver Slew Rate**




A. $C_L$ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O$ = 50 Ω, 50% duty cycle, $t_r$ ≤ 10 ns, $t_f$ ≤ 10 ns.

**Figure 4. Driver Pulse Skew**




A. $C_L$ includes probe and jig capacitance.

B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r$ ≤ 10 ns, $t_f$ ≤ 10 ns.

**Figure 5. Receiver Propagation Delay Times**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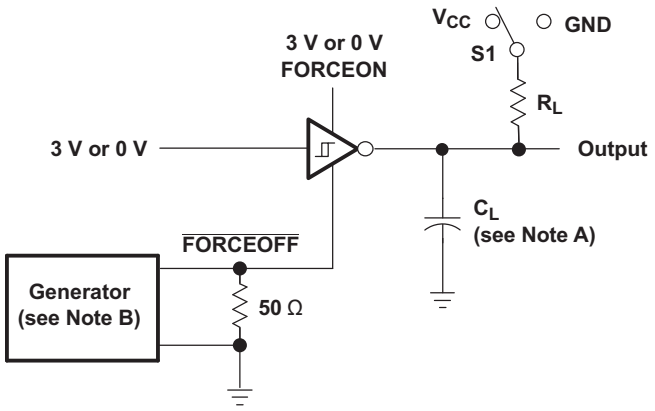
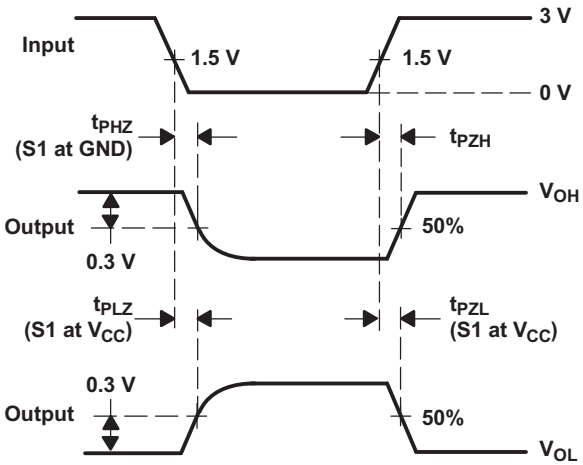
## Parameter Measurement Information (continued)




TEST CIRCUIT




VOLTAGE WAVEFORMS

A. $C_L$ includes probe and jig capacitance.

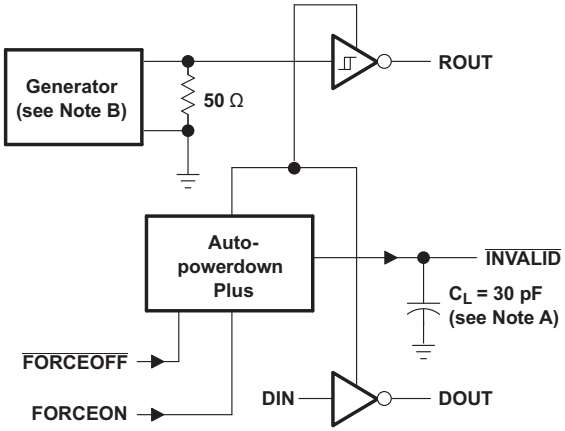
B. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, 50% duty cycle, $t_r$ ≤ 10 ns, $t_f$ ≤ 10 ns.

C. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

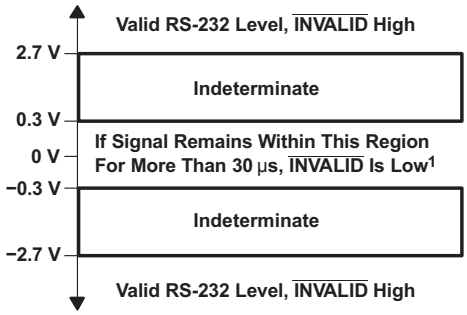
D. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

**Figure 6. Receiver Enable and Disable Times**

## Parameter Measurement Information (continued)

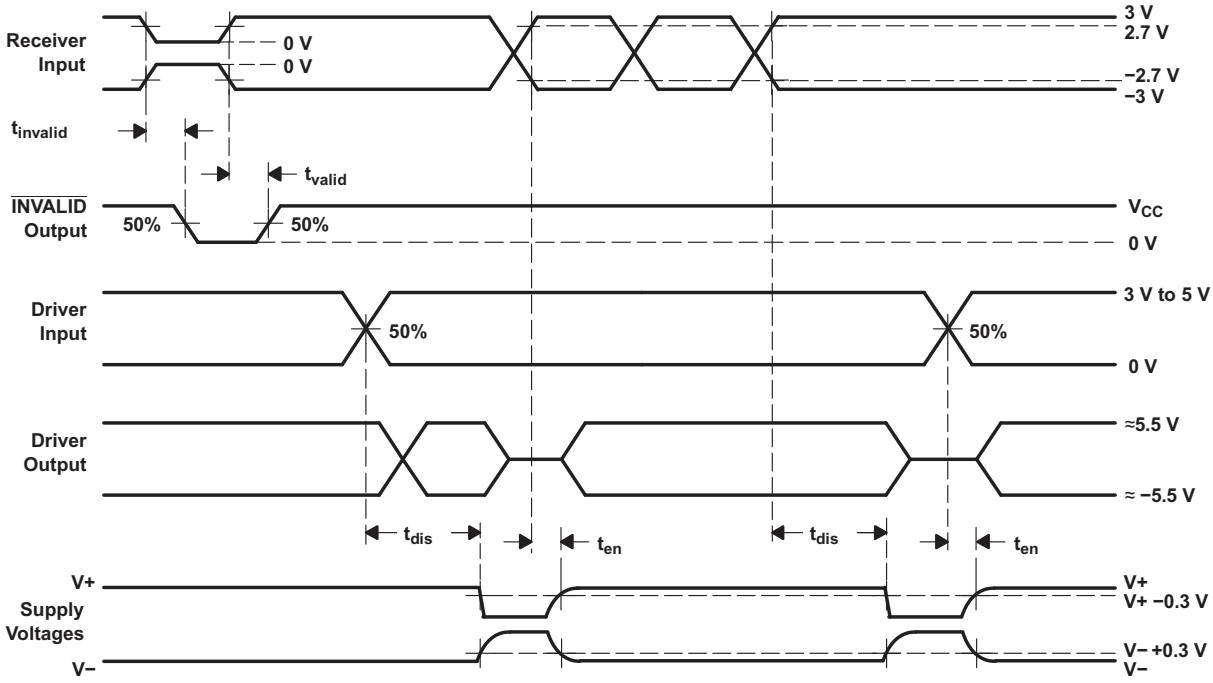



TEST CIRCUIT




† Auto-powerdown plus disables drivers and reduces supply current to 1 µA.

NOTES: A. $C_L$ includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O$= 50 Ω, 50% duty cycle, $t_r$ ≤ 10 ns, $t_f$ ≤ 10 ns.




Voltage Waveforms and Timing Diagrams

**Figure 7. INVALID Propagation-Delay Times and Supply-Enabling Time**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# 8 Detailed Description

## 8.1 Overview

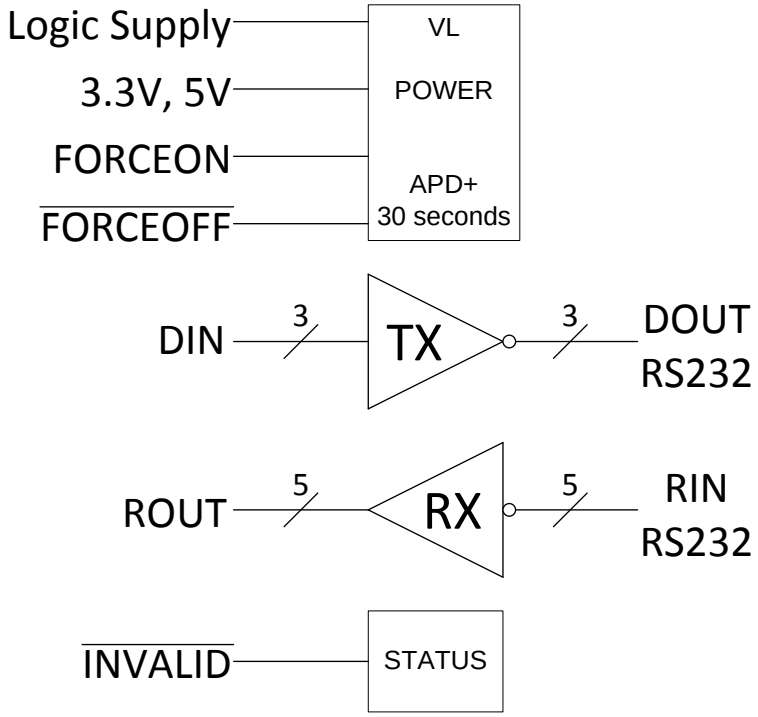
The TRS3253E is a three-driver and five-receiver RS-232 interface device, with split-supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to ±15 kV using the IEC 61000-4-2 Air-Gap Discharge method, ±8 kV using the IEC 61000-4-2 Contact Discharge method, and ±15 kV using the Human-Body Model. The charge pump requires only four small 0.1-µF capacitors for operation from a 3.3-V supply. The TRS3253E is capable of running at data rates up to 1000 kbps, while maintaining RS-232-compliant output levels. The TRS3253E is available in a space-saving VQFN package (4-mm × 4-mm RSM).

The TRS3253E has a unique $V_L$ pin that allows operation in mixed-logic voltage systems. Both driver input (DIN) and receiver output (ROUT) logic levels are pin programmable through the $V_L$ pin. This eliminates the need for additional voltage level shifter while interfacing with low-voltage microcontroller or UARTs.

Auto-powerdown plus can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown plus enabled, the device activates automatically when a valid signal change is applied to any receiver or driver input. After 30 seconds of inactivity the device will automatically power down to save power.

$\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 7 for receiver input levels.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors. Logic voltage translation is controlled by voltage provided to $V_L$ pin. Auto-powerdown-plus feature is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. See Table 1 and Table 2.

When TRS3253E is unpowered, it can be safely connected to an active remote RS232 device.

## Feature Description (continued)

### 8.3.2 RS232 Driver

Three drivers interface standard logic level to RS232 levels. All DIN inputs must be valid high or low.

### 8.3.3 RS232 Receiver

Five receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

### 8.3.4 RS232 Status

The $\overline{\text{INVALID}}$ output goes low when all RIN inputs are unpowered for more than 30 µs. The $\overline{\text{INVALID}}$ output goes high when any receiver has a valid input. The $\overline{\text{INVALID}}$ output is active when $V_L$ is powered irregardless of FORCEON and $\overline{\text{FORCEOFF}}$ inputs. See Table 3.

## 8.4 Device Functional Modes

**Table 1. Each Driver(1)**

| INPUTS | | | | OUTPUT | DRIVER STATUS |
|---|---|---|---|---|---|
| DIN | FORCEON | $\overline{\text{FORCEOFF}}$ | TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION | DOUT | |
| X | X | L | X | Z | Powered off |
| L | H | H | X | H | Normal operation with auto-powerdown plus disabled |
| H | H | H | X | L | |
| L | L | H | <30 s | H | Normal operation with auto-powerdown plus enabled |
| H | L | H | <30 s | L | |
| L | L | H | >30 s | Z | Powered off by auto-powerdown plus feature |
| H | L | H | >30 s | Z | |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance.

**Table 2. Each Receiver(1)**

| INPUTS | | | OUTPUT | RECEIVER STATUS |
|---|---|---|---|---|
| RIN | $\overline{\text{FORCEOFF}}$ | TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION | ROUT | |
| X | L | X | Z | Powered off |
| L | H | <30 s | H | Normal operation with auto-powerdown plus disabled/enabled |
| H | H | <30 s | L | |
| Open | H | <30 s | H | |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off.

**Table 3. $\overline{\text{INVALID}}$(1)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| RIN1 – RIN5 | FORCEON | $\overline{\text{FORCEOFF}}$ | TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION | $\overline{\text{INVALID}}$ |
| Any L or H | X | X | X | H |
| All Open | X | X | X | L |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off.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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

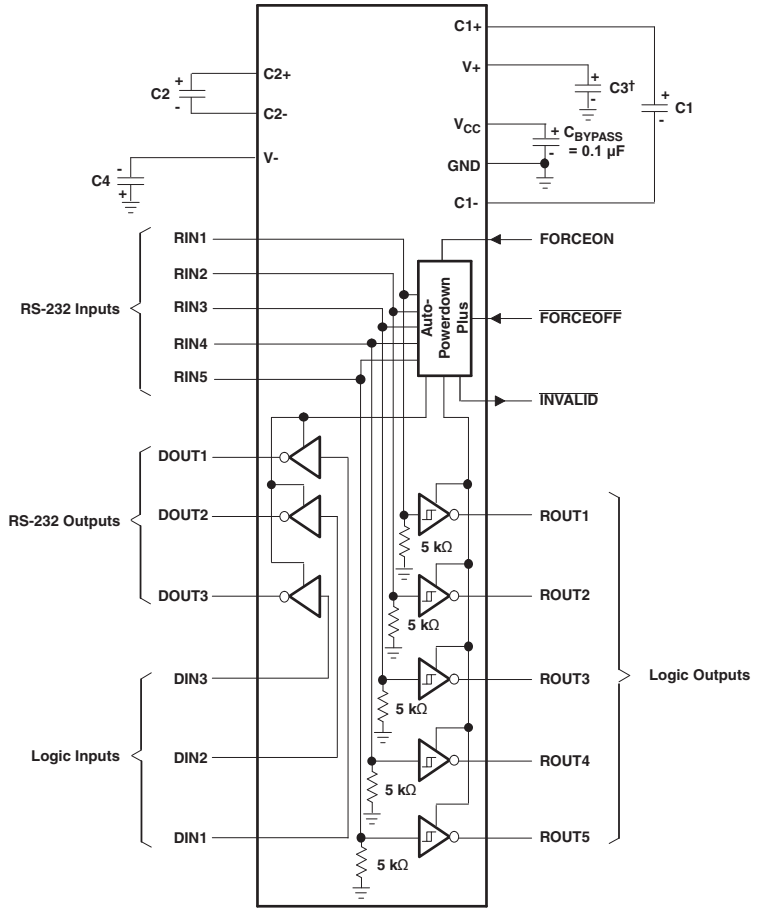
## 9.1 Application Information

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector.

## 9.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or $V_L$. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected. For proper operation, add capacitors as shown in Figure 8.

## Typical Application (continued)




† C3 can be connected to $V_{CC}$ or GND.

NOTES: A. Resistor values shown are nominal.
B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

$V_{CC}$ vs CAPACITOR VALUES

| $V_{CC}$ | C1 | C2, C3, and C4 |
|---|---|---|
| 3.3 V ± 0.3 V | 0.1 µF | 0.1 µF |
| 5 V ± 0.5 V | 0.047 µF | 0.33 µF |
| 3 V to 5.5 V | 0.1 µF | 0.47 µF |

**Figure 8. Typical Operating Circuit and Capacitor Values**

### 9.2.1 Design Requirements

- Recommended $V_{CC}$ is 3.3 V or 5 V. 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 1000 kbps
- Use capacitors as shown in Figure 8

.

### 9.2.2 Detailed Design Procedure

- All DIN, $\overline{\text{FORCEOFF}}$, and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on $V_{CC}$ level for best performance.

### 9.2.3 Application Curve

Driver input as top waveform and driver output as bottom waveform.

- 3.3-V $V_{CC}$
- 1000-kbit/s data rate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## Typical Application (continued)

- 200-pF and 3-kΩ Load

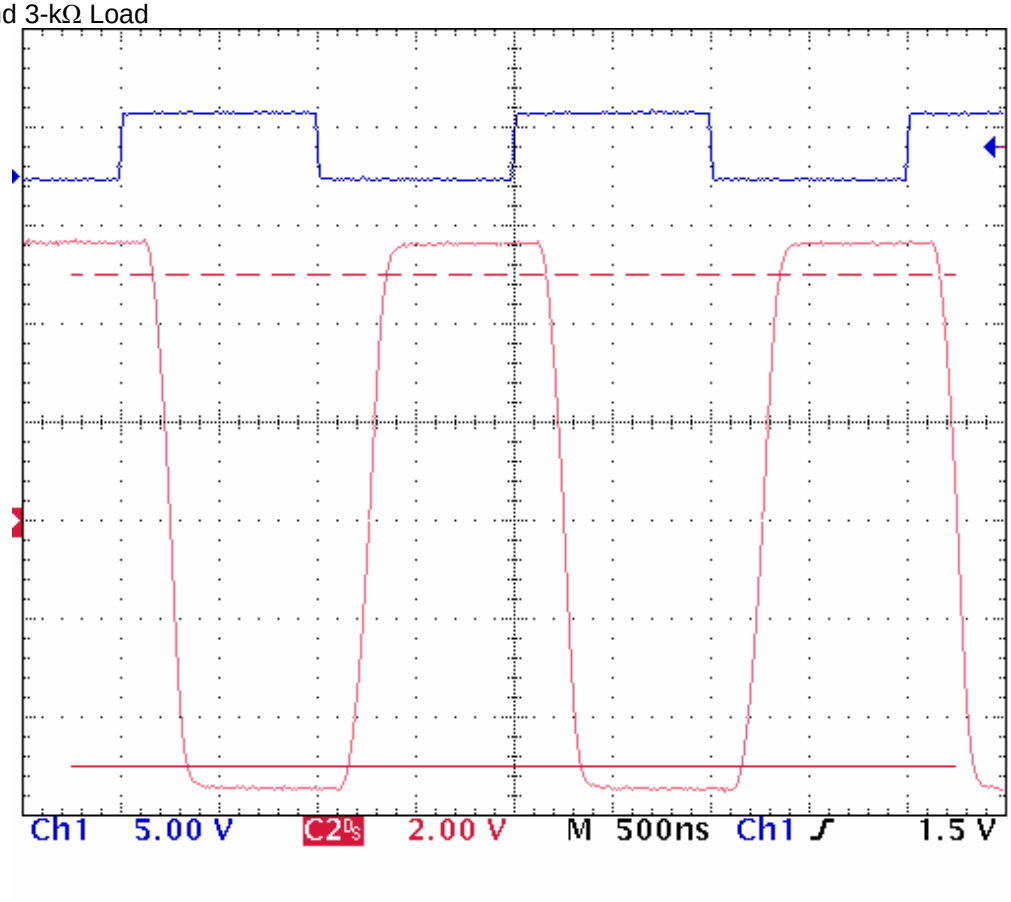


**Figure 9. 1000-kbps Driver Timing Waveform**

## 10 Power Supply Recommendations

$V_{CC}$ must be between 3.3 and 5 V. Capacitors must be selected according to the table in Figure 8.

## 11 Layout

### 11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

### 11.2 Layout Example

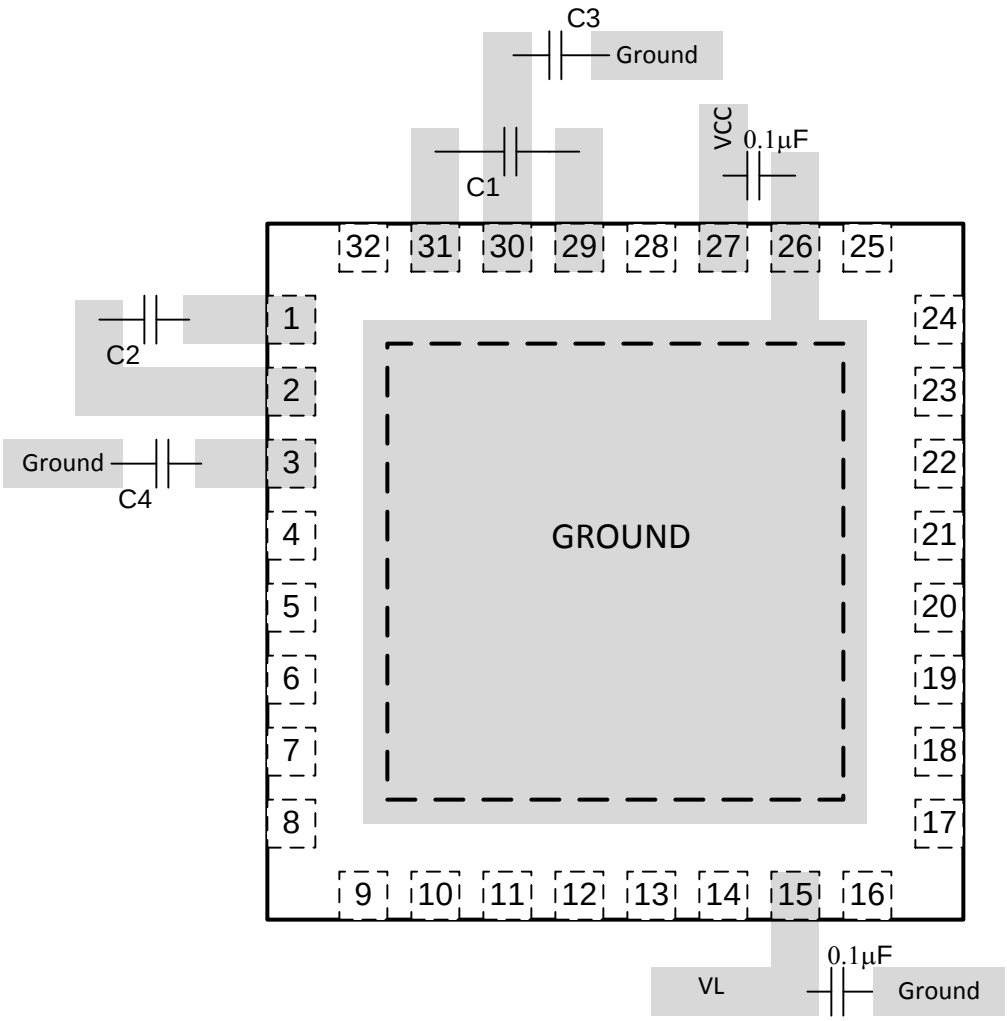


**Figure 10. Layout Diagram**


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# 12 Device and Documentation Support

## 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TRS3253EIRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | RS53EI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TRS3253E :**

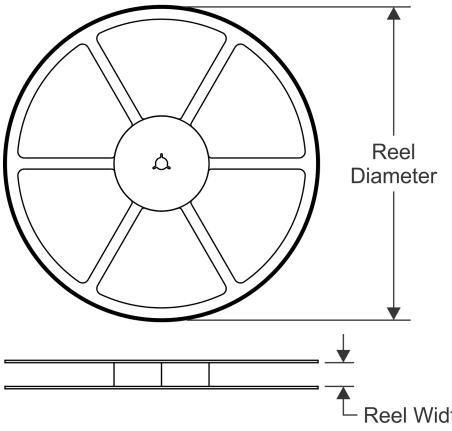
- Enhanced Product: TRS3253E-EP

NOTE: Qualified Version Definitions:

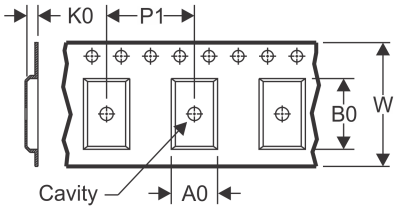
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

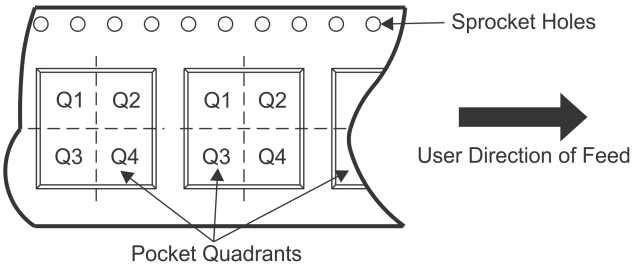



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

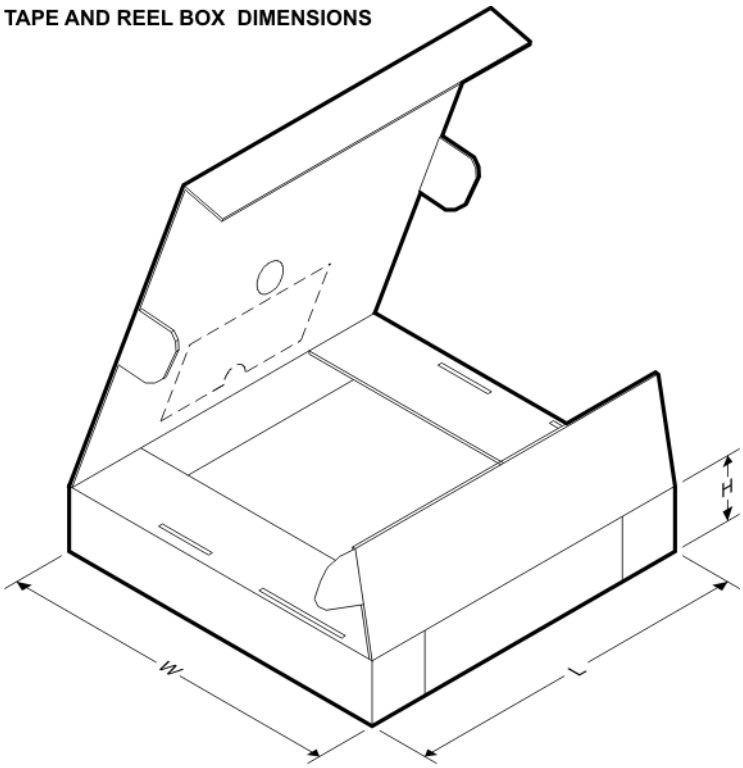
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRS3253EIRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TRS3253EIRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |

# GENERIC PACKAGE VIEW

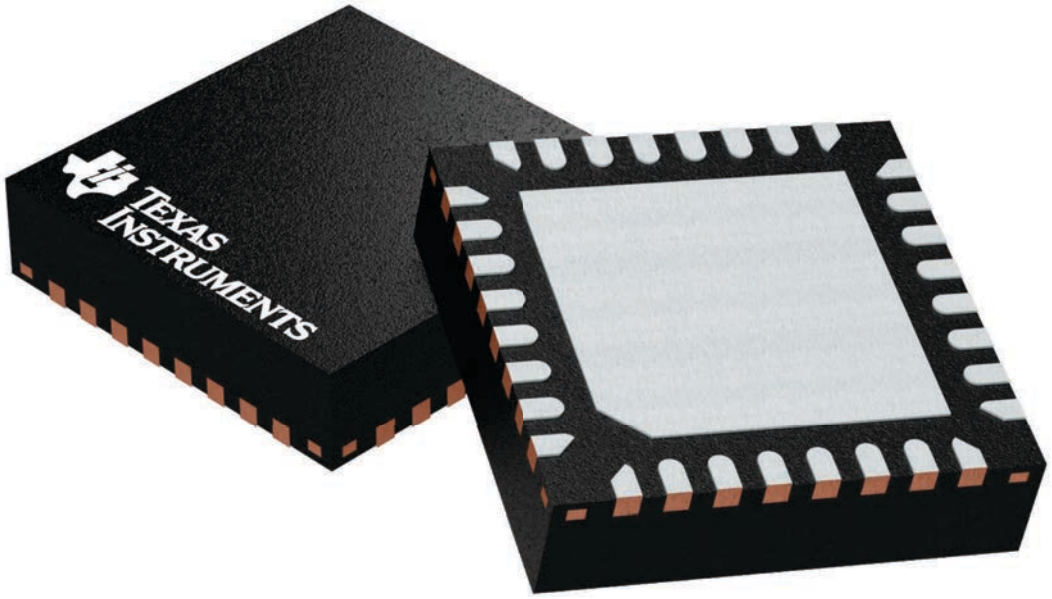
## RSM 32

## VQFN - 1 mm max height

**4 x 4, 0.4 mm pitch**

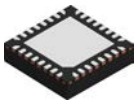
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224982/A

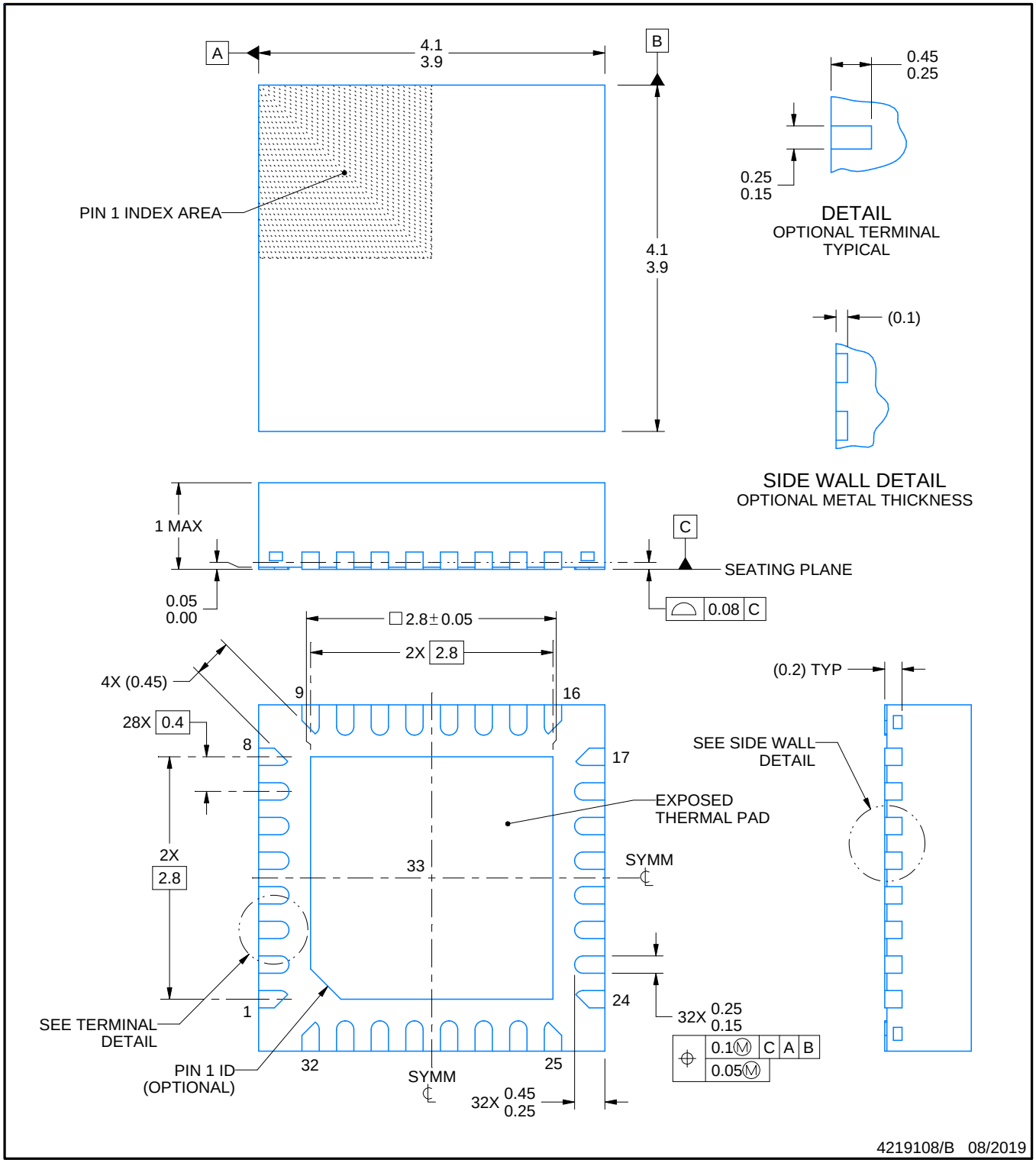
# RSM0032B



# PACKAGE OUTLINE

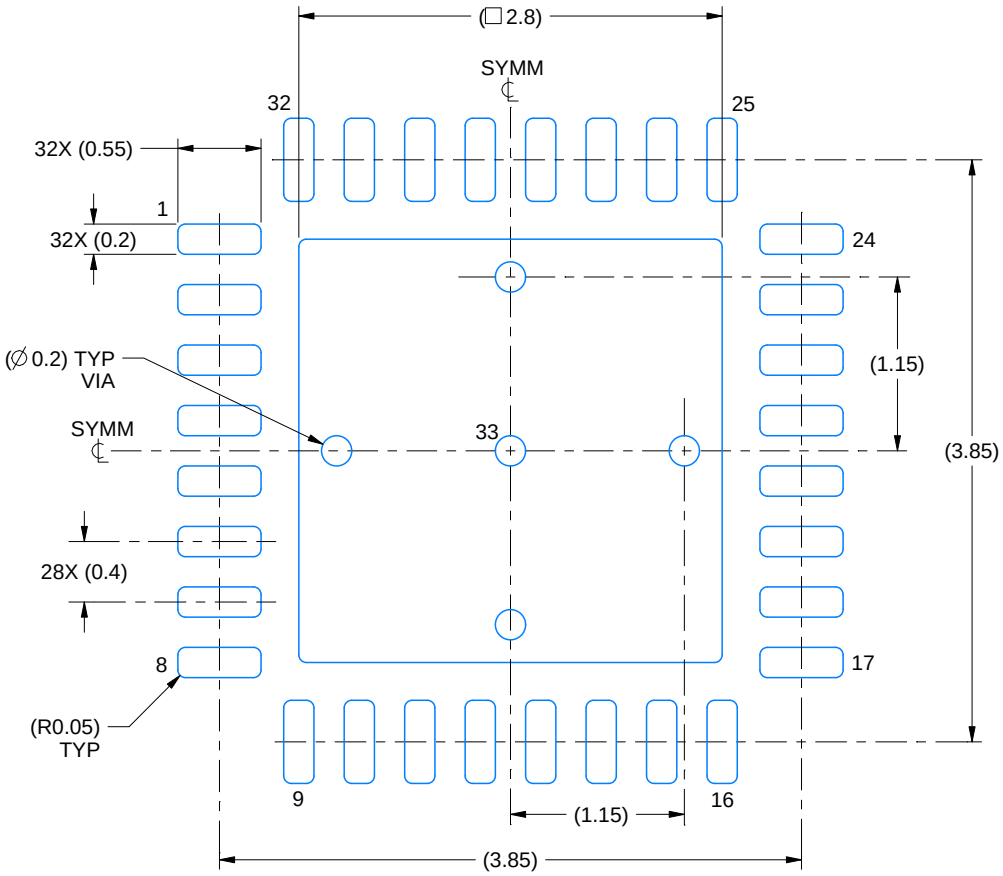
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

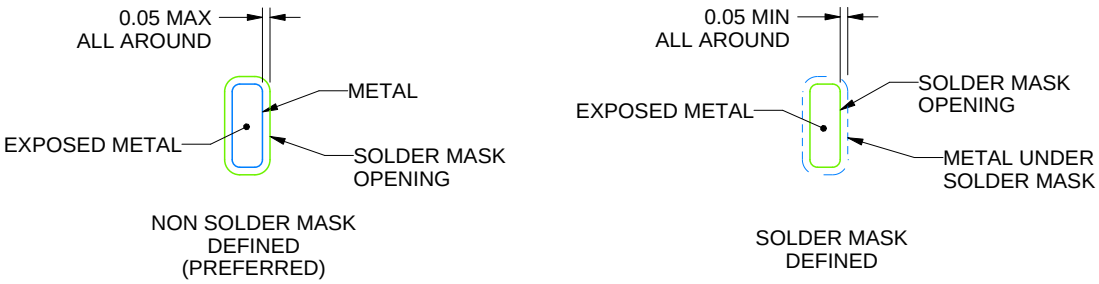



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

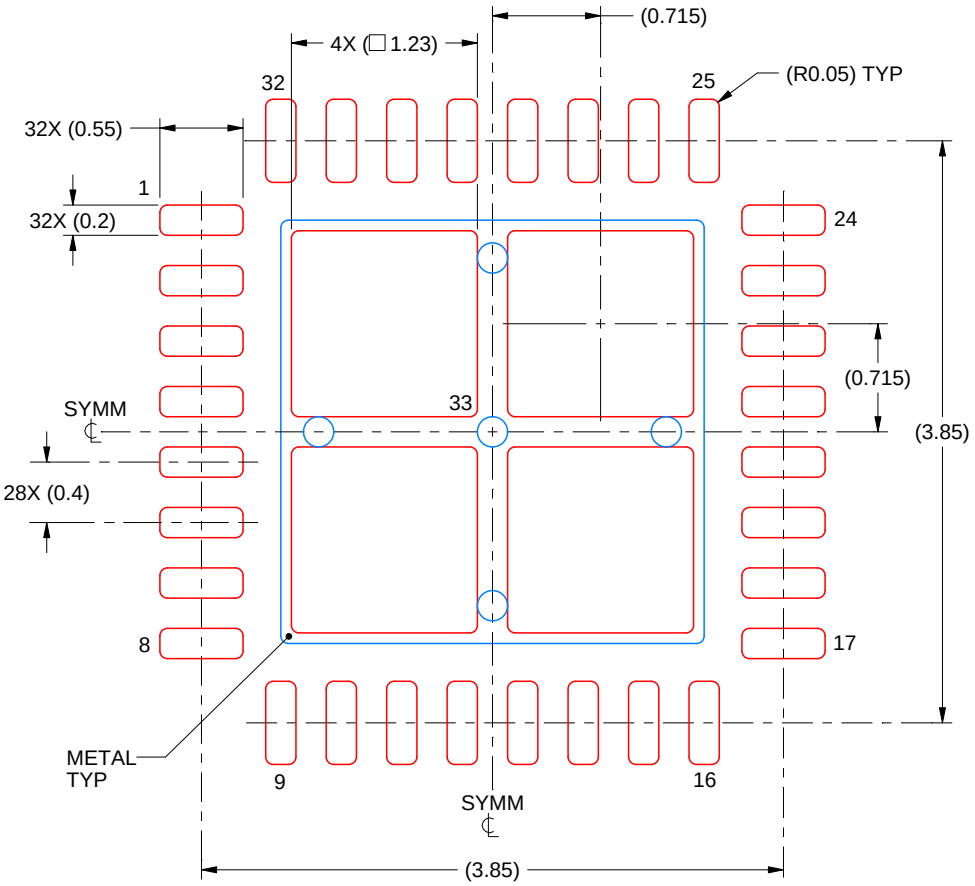



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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