2-bit Bidirectional Level Shifter for Open-Drain and Push-Pull

Features

- 2-bit Bidirectional Level Shifter
- Open-Drain and Push-Pull Output
- Max Data Rate (V_{CCA} = 3.3 V V_{CCB} = 5 V):
  - 100 Mbps (Push-Pull), 1.2 Mbps (Open-drain)
- Voltage-Level Translation between:
  - V_{CCA} Range: 1.4 V to 3.6 V
  - V_{CCB} Range: 1.65 V to 5.5 V
- 5 V Tolerant OE Enable Pin
- High-Impedance A1~2 and B1~2 Pins for OE = LOW
- VCC Isolation Feature: Either VCC Input = GND, All Outputs in High-Impedance State
- I_{OFF} Supports Partial Power-down Mode
- No Power-up Sequency Required for V_{CCA}, V_{CCB}
- ESD Protection:
  - A Port ±4000-V Human-Body Model
  - B Port ±8000-V Human-Body Model
  - B Port ±4000-V IEC 61000-4-2 Contact Discharge
  - 1500-V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/ Consumer handsets
- Industrial Automation

Description

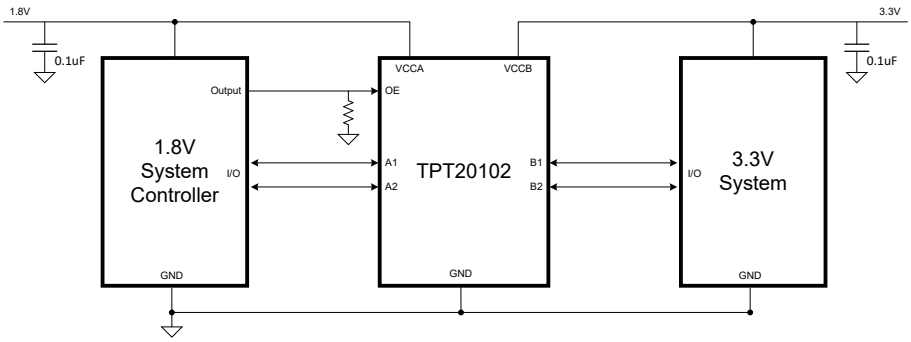
The TPT20102 device is a 2-bit level shifter with an enable (OE) input and can work from 1.4 V to 3.6 V V_{CCA} and 1.65 V to 5.5 V V_{CCB}. V_{CCA} must be less than or equal to V_{CCB}. The TPT20102 supports bidirectional voltage translation among 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V.

The A1~2 I/Os are connected to the B1~2 I/Os, which allows bidirectional data flow between ports. If OE is low, the translator switch is off, and a high-impedance state exists between A ports and B ports to isolate both sides. OE input circuit is internally connected to V_{CCA}.

The 2-bit bidirectional buffer isolates capacitance and allows 15 pF on either side of the device to support 100 Mbps speeds in Push-Pull mode in 3.3 V V_{CCA} and 5 V V_{CCB} supply, and support 1.2 Mbps speeds in Open-Drain mode.

The TPT20102 is available in a VSSOP8 package and is characterized from −40°C to +125°C.

Typical Application



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Revision History

Date	Revision	Notes
2025-09-15	Rev.Pre.0	Initial version
2026-01-01	Rev.A.0	Released version

Pin Configuration and Functions

TPT20102-VS3R
VSSOP8 Package
Top View

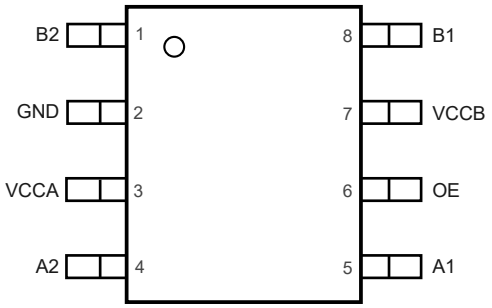


Table 1. Pin Functions: TPT20102

Pin		I/O	Description
No.	Name		
1	B2	I/O	Input/output B2. Referenced to V_{CCB}
2	GND	P	Supply ground
3	VCCA	P	Side-A supply voltage
4	A2	I/O	Input/output A2. Referenced to V_{CCA}
5	A1	I/O	Input/output A1. Referenced to V_{CCA}
6	OE	I	Active-high enable input. Referenced to V_{CCA}. Not allowed to be floating
7	VCCB	P	Side-B supply voltage
8	B1	I/O	Input/output B1. Referenced to V_{CCB}

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CCA}	DC Reference Voltage Range (side-A)	−0.5	4.6	V
V_{CCB}	DC Reference Bias Voltage Range (side-B)	−0.5	6.5	V
V_I	Input Voltage Range, side-A	−0.5	4.6	V
	Input Voltage Range, side-B	−0.5	6.5	V
V_O	Voltage Range Applied to Any Output in the High-impedance or Power-off State, V_O, side-A	−0.5	4.6	V
	Voltage Range Applied to Any Output in the High-impedance or Power-off State, V_O, side-B	−0.5	6.5	V
	Voltage Range Applied to Any Output in the High or Low State, V_O, side-A	−0.5	V_{CCA} + 0.5	V
	Voltage Range Applied to any Output in the High or Low State, V_O, side-A	−0.5	V_{CCB} + 0.5	V
I_{IK}	Input Clamp Current, V_I < 0		−50	mA
I_{OK}	Output Clamp Current, $V_{I/O}$ < 0		−50	mA
I_O	Continuous Output Current	−50	50	mA
I_C	Continuous Current through Each V_{CCA}, V_{CCB}, or GND	−100	100	mA
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The values of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Value	Unit
HBM	Human Body Model ESD, side-A ports	ANSI/ESDA/JEDEC JS-001 (1)	±4	kV
	Human Body Model ESD, side-B ports	ANSI/ESDA/JEDEC JS-001 (1)	±8	kV
IEC ESD	IEC Contact Discharge	IEC-61000-4-2, Bus Pin: B ports	±4	kV
	IEC Air-Gap Discharge	IEC-61000-4-2, Bus Pin: B ports	±8	kV
CDM	Charged Device Model ESD, side-A and side-B ports	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV
LU	Latch up	LU, per JESD78, All Pins	±500	mA

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA}	Reference Voltage, side-A			1.4	3.6	V
V_{CCB}	Reference Voltage, side-B			1.65	5.5	V
V_{IH}	Side-A Ports High-level Input Voltage	1.4 V to 1.95 V	1.65 V to 5.5 V	V_{CCI} - 0.2	V_{CCI}	V
	Side-A Ports High-level Input Voltage	2.3 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} - 0.4	V_{CCI}	V
	Side-B Ports High-level Input Voltage	1.4 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} - 0.4	V_{CCI}	V
	OE Inputs High-level Input Voltage	1.4 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} x 0.65	5.5	V
V_{IL}	Side-A Ports Low-level Input Voltage	1.4 V to 3.6 V	1.65 V to 5.5 V	0	0.15	V
	Side-B Ports Low-level Input Voltage	1.4 V to 3.6 V	1.65 V to 5.5 V	0	0.15	V
	OE Inputs Low-level Input Voltage	1.4 V to 3.6 V	1.65 V to 5.5 V	0	V_{CCA} x 0.35	V
Δt/Δv	Side-A Ports Input Transition Rise or Fall Rate	1.4 V to 3.6 V	1.65 V to 5.5 V		10	ns/V
	Side-B Ports Input Transition Rise or Fall Rate	1.4 V to 3.6 V	1.65 V to 5.5 V		10	
	OE Input Transition Rise or Fall Rate	1.4 V to 3.6 V	1.65 V to 5.5 V		10	
T_A	Operating Ambient Temperature			−40	125	°C

(1) V_{CCI} is the supply voltage of the input side-A or side-B port.
(2) V_{CCA} should be less than or equal to V_{CCB}, and V_{CCA} must not be higher than 3.6 V.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
VSSOP8	113	49	°C/W

Electrical Characteristics

All test conditions: V_{CCA} = 1.4 V to 3.6 V, V_{CCB} = 1.65 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Parameter		Conditions	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
Supply Voltage and Current								
V_{OHA}	Port A High-level Output voltage	I_{OH} = –20 μA, V_{IB} ≥ V_{CCB} - 0.4 V	1.4 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} x 0.67			V
V_{OLA}	Port A Low-level Output Voltage	I_{OL} = 220 μA, V_{IB} ≤ 0.15 V	1.65 V	1.65 V to 5.5 V			0.4	V
		I_{OL} = 300 μA, V_{IB} ≤ 0.15 V	2.3 V	1.65 V to 5.5 V			0.4	
		I_{OL} = 400 μA, V_{IB} ≤ 0.15 V	3.0 V	3.0 V to 5.5 V			0.55	
		I_{OL} = 1000 μA, V_{IB} ≤ 0.15 V	1.65 V to 3.6 V	3.0 V to 5.5 V			0.6	
V_{OHB}	Port B High-level Output voltage	I_{OH} = −20 μA, V_{IA} ≥ V_{CCA} - 0.2 V	1.4 V to 3.6 V	1.65 V to 5.5 V	V_{CCB} x 0.67			V
V_{OLB}	Port B Low-level Output voltage	I_{OL} = 220 μA, V_{IA} ≤ 0.15 V	1.4 V to 3.6 V	1.65 V			0.4	V
		I_{OL} = 300 μA, V_{IA} ≤ 0.15 V	1.4 V to 3.6 V	2.3 V			0.4	
		I_{OL} = 400 μA, V_{IA} ≤ 0.15 V	1.4 V to 3.6 V	3.0 V			0.55	
		I_{OL} = 620 μA, V_{IA} ≤ 0.15 V	1.4 V to 3.6 V	4.5 V			0.55	
		I_{OL} = 1000 μA, V_{IA} ≤ 0.15 V	1.4 V to 3.6 V	4.5 V			0.6	
I_I	Input Leakage Current	OE: V_I = V_{CCI} or GND	1.4 V	1.65 V to 5.5 V	−2		2	μA
I_{OZ}	High-impedance State Output Current	Port A or B, OE = GND	1.4 V	1.65 V to 5.5 V	−2		2	μA
I_{CCA}	Quiescent Supply Current for V_{CCA}	V_I = V_O = Open, I_O = 0, OE = V_{CCA}	1.4 V to 3.6 V	1.65 V to 5.5 V			5	μA
			3.6 V	0			5	
			0	5.5 V	−1		1	
I_{CCB}	Quiescent Supply Current for V_{CCB}	V_I = V_O = Open, I_O = 0, OE = V_{CCA}	1.4 V to 3.6 V	1.65 V to 5.5 V			15	μA
			3.6 V	0	−1		1	
			0	5.5 V			10	

Parameter		Conditions	V_{CCA}	V_{CCB}	Min	Typ	Max	Unit
I_{CCA}+ I_{CCB}	Combined Supply Current	V_I = V_{CCI}, I_O = 0, OE = V_{CCA}	1.4 V to 3.6 V	1.65 V to 5.5 V			15	μA
I_{OFF}	OFF Current	A port: VI or Vo =0 to 3.6	0	0 V to 5.5 V	−5		5	μA
		B port: VI or Vo =0 to 3.6	0 V to 3.6 V	0	−5		5	μA
I_{CCZA}	High Impedance State V_{CCA} Supply Current	V_I= V_O = Open, I_O = 0, OE = GND	1.4 V to 3.6 V	1.65 V to 5.5 V			5	μA
I_{CCZB}	High Impedance State V_{CCB} Supply Current	V_I = V_O = Open, I_O = 0, OE = GND	1.4 V to 3.6 V	1.65 V to 5.5 V			15	μA
C_I	Input Capacitance (1)	OE	3.3 V	3.3 V		5	10	pF
C_{IO}	Input/output Capacitance (1)	Port A	3.3 V	3.3 V		7	10	pF
		Port B	3.3 V	3.3 V		10	15	pF

(1) Test data based on bench tests and design simulation.

AC Timing Requirements -- VCCA = 1.8 V

All test conditions: V_{CCA} = 1.65 V to 1.95 V, T_A = −40°C to +125°C, unless otherwise noted. The data is based on bench test and design simulation.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
f_D	Data rate	Push-pull mode	1.65 V to 1.95 V			40	Mbps
			2.3 V to 2.7 V			45	Mbps
			3.0 V to 3.6 V			40	Mbps
			4.5 V to 5.5 V			40	Mbps
		Open-drain mode	1.65 V to 1.95 V			0.8	Mbps
			2.3 V to 2.7 V			0.8	Mbps
			3.0 V to 3.6 V			0.8	Mbps
			4.5 V to 5.5 V			1	Mbps
t_W	Pulse duration	Push-pull mode	1.65 V to 1.95 V	25			ns
			2.3 V to 2.7 V	22.22			ns
			3.0 V to 3.6 V	25			ns
			4.5 V to 5.5 V	25			ns
		Open-drain mode	1.65 V to 1.95 V	1250			ns
			2.3 V to 2.7 V	1250			ns
			3.0 V to 3.6 V	1250			ns
			4.5 V to 5.5 V	1000			ns
t_{PHL}	Propagation Delay (High-to-Low)	A-to-B, push-pull driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V			20	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		A-to-B, open-drain driving	1.65 V to 1.95 V	1.7		20	ns
			2.3 V to 2.7 V	1.7		20	ns
			3.0 V to 3.6 V	1.6		15	ns
			4.5 V to 5.5 V	1.5		15	ns
t_{PLH}	Propagation Delay (Low-to-High)	A-to-B, push-pull driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V			20	ns
			3.0 V to 3.6 V			15	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			4.5 V to 5.5 V			15	ns
		A-to-B, open-drain driving	1.65 V to 1.95 V			800	ns
			2.3 V to 2.7 V			700	ns
			3.0 V to 3.6 V			600	ns
			4.5 V to 5.5 V			500	ns
t_{PHL}	Propagation Delay (High-to-Low)	B-to-A, push-pull driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V			17	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		B-to-A, open-drain driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V	2		20	ns
			3.0 V to 3.6 V	1.9		15	ns
			4.5 V to 5.5 V	1.8		15	ns
t_{PLH}	Propagation Delay (Low-to-High)	B-to-A, push-pull driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		B-to-A, open-drain driving	1.65 V to 1.95 V			900	ns
			2.3 V to 2.7 V			700	ns
			3.0 V to 3.6 V			600	ns
			4.5 V to 5.5 V			500	ns
t_{en}	Enable time	OE-to-A or B, push-pull driving	1.65 V to 5.5 V			100	ns
t_{dis}	Disable time	OE-to-A or B, push-pull driving	1.65 V to 5.5 V			410	ns
tr_A	Input rise time	A-port rise time, push-pull driving	1.65 V to 1.95 V			20	ns
			2.3 V to 2.7 V	1.6		20	ns
			3.0 V to 3.6 V	1.4		15	ns
			4.5 V to 5.5 V	1.4		15	ns
		A-port rise time, open-drain driving	1.65 V to 1.95 V	1.7		1200	ns
			2.3 V to 2.7 V	1.7		800	ns
			3.0 V to 3.6 V	1.4		600	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
			4.5 V to 5.5 V	1.2		500	ns
tr_B	Input rise time	B-port rise time, push-pull driving	1.65 V to 1.95 V	1.3		22	ns
			2.3 V to 2.7 V	1.3		20	ns
			3.0 V to 3.6 V	0.9		15	ns
			4.5 V to 5.5 V	0.7		15	ns
		B-port rise time, open-drain driving	1.65 V to 1.95 V	1		1200	ns
			2.3 V to 2.7 V	1		800	ns
			3.0 V to 3.6 V	1		700	ns
			4.5 V to 5.5 V	0.6		500	ns
tf_A	Input fall time	A-port fall time, push-pull driving	1.65 V to 1.95 V	1		20	ns
			2.3 V to 2.7 V	1.6		20	ns
			3.0 V to 3.6 V	1.4		15	ns
			4.5 V to 5.5 V	1.4		15	ns
		A-port fall time, open-drain driving	1.65 V to 1.95 V	1.7		20	ns
			2.3 V to 2.7 V	1.7		15	ns
			3.0 V to 3.6 V	1.4		15	ns
			4.5 V to 5.5 V	1.2		15	ns
tf_B	Input fall time	B-port fall time, push-pull driving	1.65 V to 1.95 V	1.3		20	ns
			2.3 V to 2.7 V	1.3		15	ns
			3.0 V to 3.6 V	0.9		10	ns
			4.5 V to 5.5 V	0.7		10	ns
		B-port fall time, open-drain driving	1.65 V to 1.95 V	1		20	ns
			2.3 V to 2.7 V	1		20	ns
			3.0 V to 3.6 V	1		15	ns
			4.5 V to 5.5 V	0.7		15	ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew, push-pull driving	1.65 V to 5.5 V			1	ns

AC Timing Requirements -- VCCA = 2.5 V

All test conditions: V_{CCA} = 2.3 V to 2.7 V, T_A = −40°C to +125°C, unless otherwise noted. The data is based on bench test and design simulation.

Parameter		Condition	VCCB	Min	Typ	Max	Unit
f_D	Data rate	Push-pull mode	2.3 V to 2.7 V			60	Mbps
			3.0 V to 3.6 V			75	Mbps
			4.5 V to 5.5 V			75	Mbps
		Open-drain mode	2.3 V to 2.7 V			0.8	Mbps
			3.0 V to 3.6 V			0.8	Mbps
			4.5 V to 5.5 V			1	Mbps
t_W	Pulse duration	Push-pull mode	2.3 V to 2.7 V	16.66			ns
			3.0 V to 3.6 V	13.33			ns
			4.5 V to 5.5 V	13.33			ns
		Open-drain mode	2.3 V to 2.7 V	1250			ns
			3.0 V to 3.6 V	1250			ns
			4.5 V to 5.5 V	1000			ns
t_{PHL}	Propagation Delay (High-to-Low)	A-to-B, push-pull driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		A-to-B, open-drain driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
t_{PLH}	Propagation Delay (Low-to-High)	A-to-B, push-pull driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		A-to-B, open-drain driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			30	ns
			4.5 V to 5.5 V			20	ns
t_{PHL}	Propagation Delay (High-to-Low)	B-to-A, push-pull driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		B-to-A, open-drain driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
t_{PLH}	Propagation Delay (Low-to-High)	B-to-A, push-pull driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns

Parameter		Condition	VCCB	Min	Typ	Max	Unit
		B-to-A, open-drain driving	2.3 V to 2.7 V			15	ns
			3.0 V to 3.6 V			10	ns
			4.5 V to 5.5 V			10	ns
t_{en}	Enable time	OE-to-A or B, push-pull driving	2.3 V to 5.5 V			100	ns
t_{dis}	Disable time	OE-to-A or B, push-pull driving	2.3 V to 5.5 V			400	ns
tr_A	Input rise time	A-port rise time, push-pull driving	2.3 V to 2.7 V	1.89		15	ns
			3.0 V to 3.6 V	1.6		15	ns
			4.5 V to 5.5 V	1.5		15	ns
		A-port rise time, open-drain driving	2.3 V to 2.7 V	110		800	ns
			3.0 V to 3.6 V	157		700	ns
			4.5 V to 5.5 V	116		500	ns
tr_B	Input rise time	B-port rise time, push-pull driving	2.3 V to 2.7 V	1.7		15	ns
			3.0 V to 3.6 V	1.3		10	ns
			4.5 V to 5.5 V	0.9		10	ns
		B-port rise time, open-drain driving	2.3 V to 2.7 V	107		800	ns
			3.0 V to 3.6 V	140		600	ns
			4.5 V to 5.5 V	77		500	ns
tf_A	Input fall time	A-port fall time, push-pull driving	2.3 V to 2.7 V	1.5		10	ns
			3.0 V to 3.6 V	1.2		10	ns
			4.5 V to 5.5 V	1.3		10	ns
		A-port fall time, open-drain driving	2.3 V to 2.7 V	1.5		10	ns
			3.0 V to 3.6 V	1.2		10	ns
			4.5 V to 5.5 V	1.1		10	ns
tf_B	Input fall time	B-port fall time, push-pull driving	2.3 V to 2.7 V	1.4		10	ns
			3.0 V to 3.6 V	0.9		10	ns
			4.5 V to 5.5 V	0.7		10	ns
		B-port fall time, open-drain driving	2.3 V to 2.7 V	0.4		20	ns
			3.0 V to 3.6 V	0.5		10	ns
			4.5 V to 5.5 V	0.4		10	ns
$t_{SK(O)}$	Skew (time), output	Channel-to channel skew, push-pull driving	2.3 V to 5.5 V			1	ns

AC Timing Requirements -- VCCA = 3.3 V

All test conditions: V_{CCA} = 3.0 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise noted. The data is based on bench test and design simulation.

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
f_D	Data rate	Push-pull mode	3.0 V to 3.6 V			80	Mbps
		Push-pull mode	4.5 V to 5.5 V			100	Mbps
		Open-drain mode	3.0 V to 3.6 V			0.8	Mbps
		Open-drain mode	4.5 V to 5.5 V			1.2	Mbps
t_W	Pulse duration	Push-pull mode	3.0 V to 3.6 V	12.5			ns
		Push-pull mode	4.5 V to 5.5 V	10			ns
		Open-drain mode	3.0 V to 3.6 V	1250			ns
		Open-drain mode	4.5 V to 5.5 V	833			ns
t_{PHL}	Propagation Delay (High-to-Low)	A-to-B, push-pull driving	3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			10	ns
		A-to-B, open-drain driving	3.0 V to 3.6 V	2.1		20	ns
			4.5 V to 5.5 V	1.5		15	ns
t_{PLH}	Propagation Delay (Low-to-High)	A-to-B, push-pull driving	3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		A-to-B, open-drain driving	3.0 V to 3.6 V	0.15		900	ns
			4.5 V to 5.5 V	0.3		500	ns
t_{PHL}	Propagation Delay (High-to-Low)	B-to-A, push-pull driving	3.0 V to 3.6 V			15	ns
			4.5 V to 5.5 V			15	ns
		B-to-A, open-drain driving	3.0 V to 3.6 V	3.19		20	ns
			4.5 V to 5.5 V	1.8		15	ns
t_{PLH}	Propagation Delay (Low-to-High)	B-to-A, push-pull driving	3.0 V to 3.6 V			20	ns
			4.5 V to 5.5 V			10	ns
		B-to-A, open-drain driving	3.0 V to 3.6 V			900	ns
			4.5 V to 5.5 V			500	ns
t_{en}	Enable time	OE-to-A or B, push-pull driving	3.0 V to 5.5 V			100	ns
t_{dis}	Disable time	OE-to-A or B, push-pull driving	3.0 V to 3.6 V			410	ns
tr_A	Input rise time	A-port rise time, push-pull driving	3.0 V to 3.6 V	2.1		15	ns
			4.5 V to 5.5 V	1.4		15	ns
		A-port rise time, open-drain driving	3.0 V to 3.6 V	2.2		446	ns
			4.5 V to 5.5 V	1.2		337	ns
tr_B	Input rise time	B-port rise time, push-pull driving	3.0 V to 3.6 V	2		15	ns
			4.5 V to 5.5 V	0.7		10	ns

Parameter		Condition	V_{CCB}	Min	Typ	Max	Unit
		B-port rise time, open-drain driving	3.0 V to 3.6 V	2		427	ns
			4.5 V to 5.5 V	0.6		290	ns
tf_A	Input fall time	A-port fall time, push-pull driving	3.0 V to 3.6 V	1.4		10	ns
			4.5 V to 5.5 V	1.2		10	ns
		A-port fall time, open-drain driving	3.0 V to 3.6 V	1.4		10	ns
			4.5 V to 5.5 V	1.2		10	ns
tf_B	Input fall time	B-port fall time, push-pull driving	3.0 V to 3.6 V	1.3		10	ns
			4.5 V to 5.5 V	1.1		10	ns
		B-port fall time, open-drain driving	3.0 V to 3.6 V	1.3		10	ns
			4.5 V to 5.5 V	1.1		10	ns
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew, push-pull driving	3.0 V to 5.5 V			1	ns

Typical Performance Characteristics

All test conditions: V_{CCA} = 1.65 V to 3.6 V_{CCB} = 1.65 V to 5.5 V, unless otherwise noted.

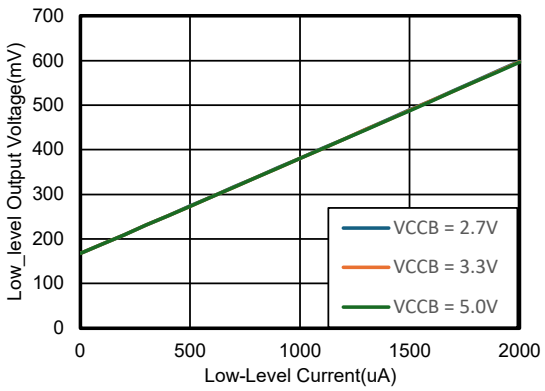


Figure 1. $V_{OL(Bx)}$ vs $I_{OL(Bx)}$, V_{CCA} = 1.8 V, $V_{IL(A)}$ = 0.15 V

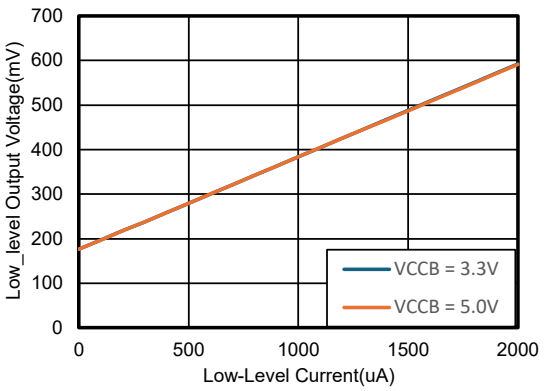


Figure 2. $V_{OL(Bx)}$ vs $I_{OL(Bx)}$, V_{CCA} = 2.5 V, $V_{IL(A)}$ = 0.15 V

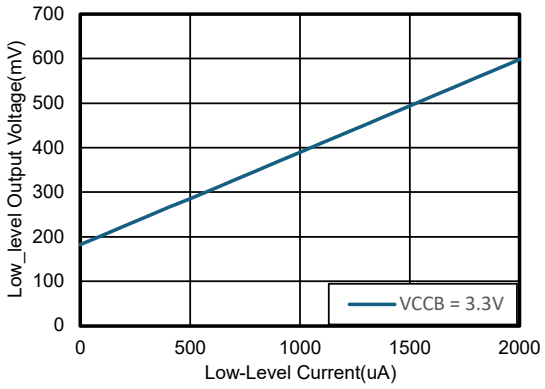


Figure 3. $V_{OL(Bx)}$ vs $I_{OL(Bx)}$, V_{CCA} = 3.3 V, $V_{IL(A)}$ = 0.15 V

Parameter Measurement Waveforms

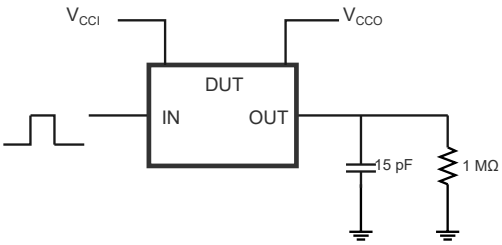


Figure 4. Timing Measurement Load Circuit of Push-Pull Driver

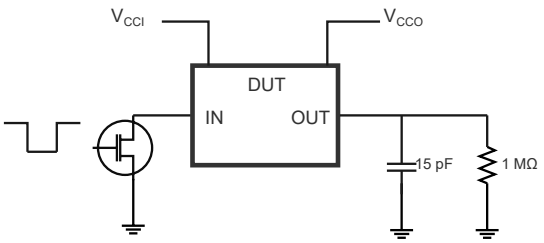


Figure 5. Timing Measurement Load Circuit of Push-Pull Driver

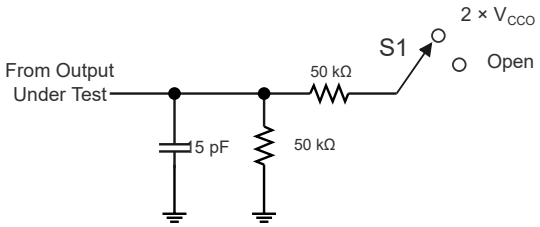


Figure 6. Load Circuit for Enable and Disable Time Measurement

Test	S1
t_{PZL}/t_{PLZ}	2 x V_{CCO}
t_{PHZ}/t_{PZH}	Open

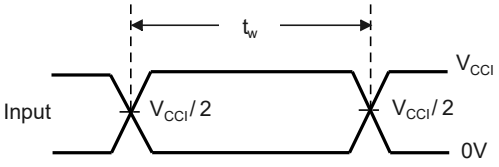


Figure 7. Pulse Duration

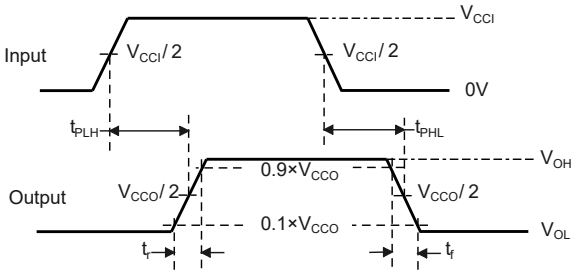


Figure 8. Propagation Delay Times

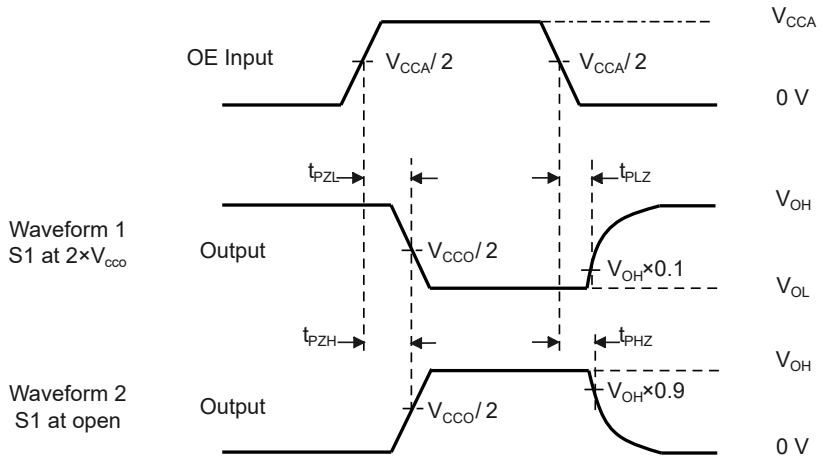


Figure 9. Enable and Disable Times

Detailed Description

Overview

The TPT20102 device is a 2-bit level shifter with an enable (OE) input, and can work from 1.4 V to 3.6 V V_{CCA} and 1.65 V to 5.5 V V_{CCB}. V_{CCA} must be less than or equal to V_{CCB}. The TPT20102 supports bidirectional voltage translation between 1.5V, 1.8 V, 2.5 V, 3.3 V, and 5 V. The A1~2 I/Os are connected to the B1~2 I/O, which allows bidirectional data flow between ports. If OE is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides. 2-bit bidirectional buffer isolates capacitance and allows 15 pF on either side of the device to support 100 Mbps speeds in Push-Pull mode in 3.3 V V_{CCA} and 5 V V_{CCB}, and support 1.2 Mbps speed in Open-Drain mode.

Functional Block Diagram

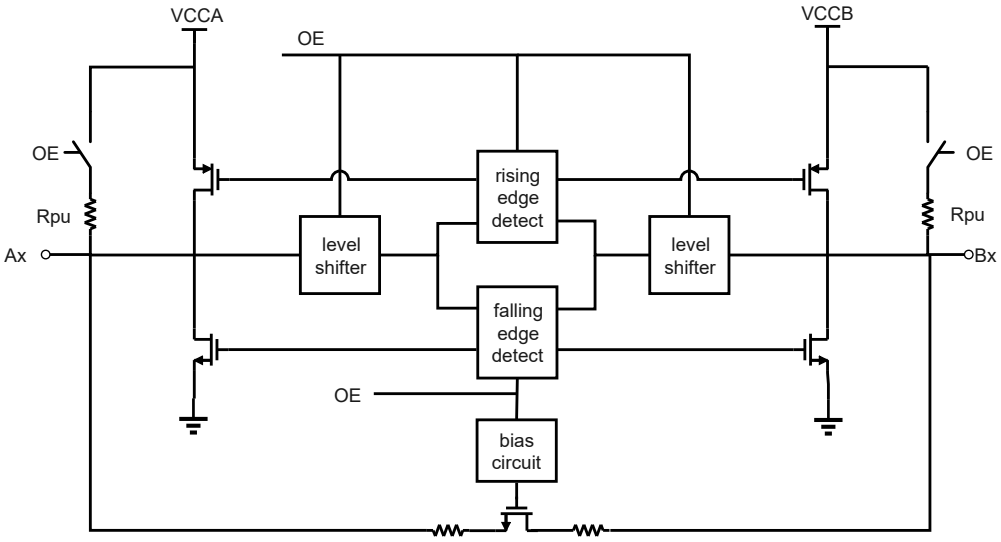


Figure 10. Functional Block Diagram

Feature Description

Power Up

During operation, make sure that $V_{CCA} \leq V_{CCB}$ at all times. During the power-up period, even if $V_{CCA} \geq V_{CCB}$, it does not damage the device, so there is no power-on sequence requirement; any power supply can be ramped up first.

Enable (OE)

The OE pin is active-HIGH, with switching thresholds referenced to V_{CCA}. When driven LOW, OE disables the TPT20102 and places all I/Os in a high-impedance state. The t_{dis} parameter indicates the delay time between the OE pin going low and I/Os outputs entering the high-impedance state. Then Enable time t_{en} indicates the period of time that the user operates the one-shot circuit after the OE pin goes high.

To ensure the high-impedance state during power-up or power-down, the OE pin should be connected to GND through a pull-down resistor, the minimum value of this resistor is determined by the current-sourcing capability of the driver.

Table 2. Device Function

Input OE	Translator Function
H	Ax = Bx
L	Ax is disconnected to Bx, high-impedance

(1) The OE pin should be pulled up to V_{CCA} or pulled down to GND, not allowed to be floating.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPT20102 device is a 2-bit level shifter, with an enable (OE) input, and can work from 1.4 V to 3.6 V V_{CCA} and 1.65 V to 5.5 V V_{CCB}. V_{CCA} must be less than or equal to V_{CCB}. TPT20102 supports bidirectional voltage translation between 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V. The A1~2 I/Os are connected to the B1~2 I/O, which allows bidirectional data flow between ports. If OE is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides.

- Servers/ Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/ Consumer handsets
- Industrial Automation

Typical Application

A typical application is shown in Figure 11. The TPT20102 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TPT20102 device is ideal for use in applications where an open-drain driver is connected to the data I/Os, and also can be used in applications where a push-pull driver is connected to the data I/Os.

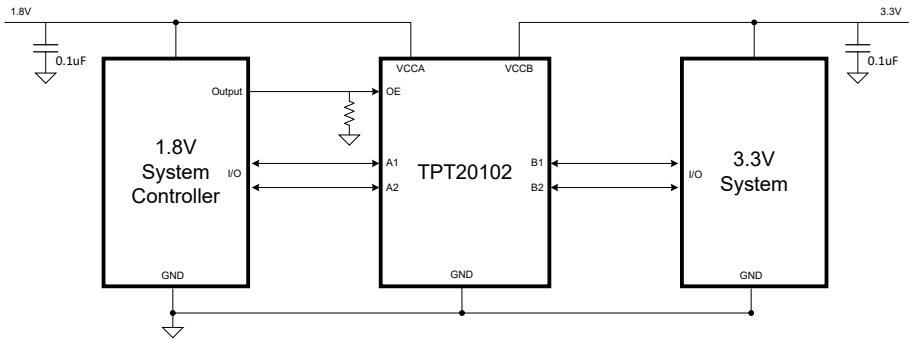


Figure 11. Typical Application Circuit

Layout

Layout Example

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they have to turn corners. The following shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

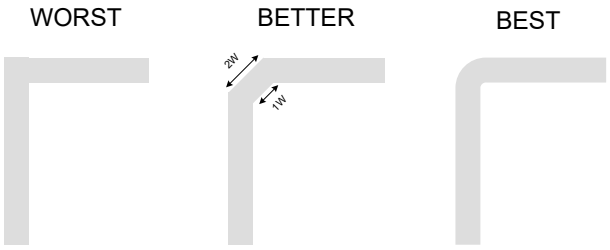


Figure 12. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

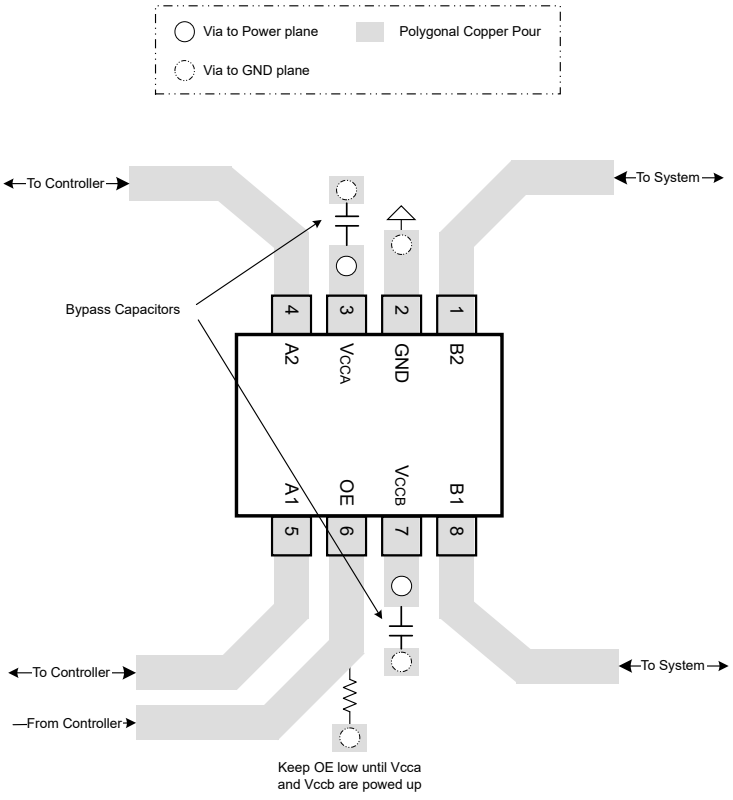
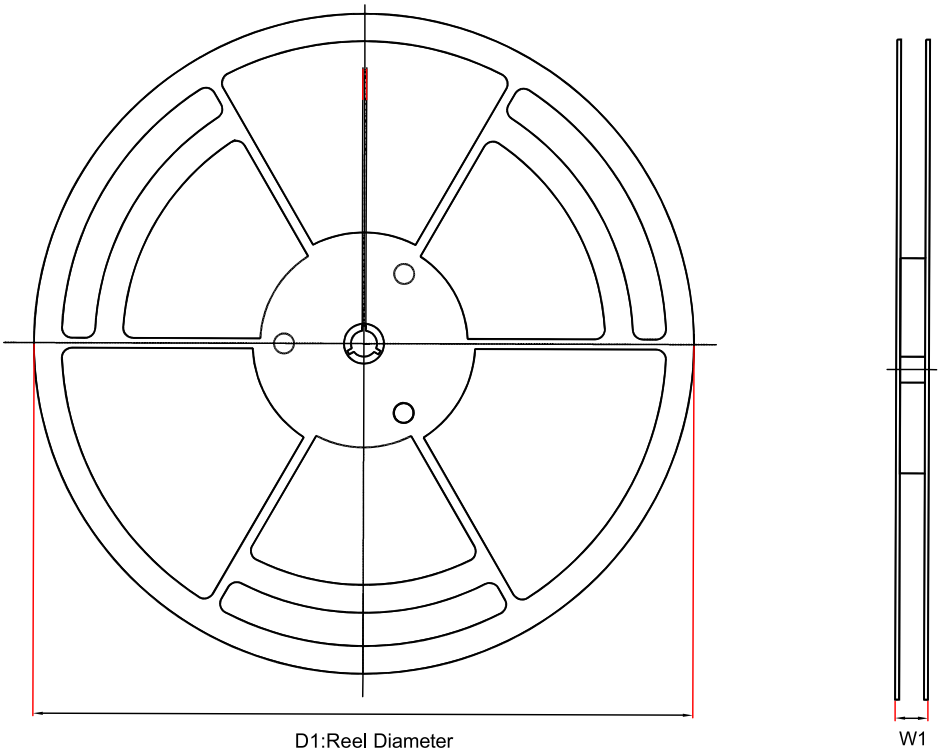
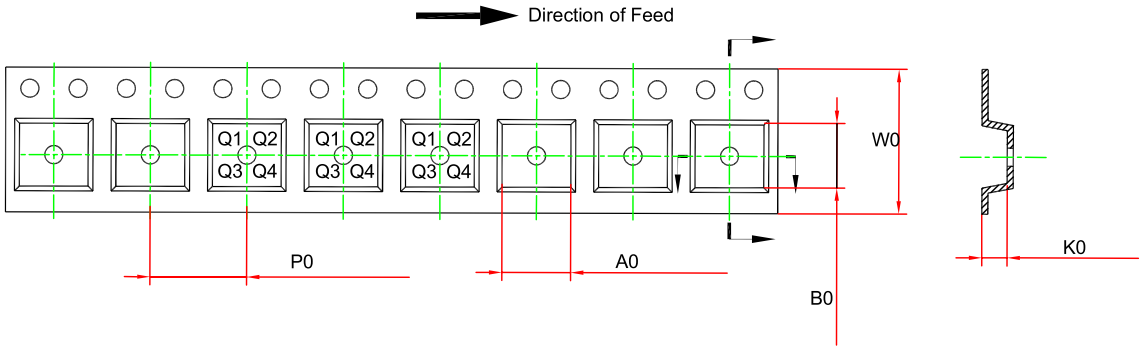


Figure 13. Layout Example

Tape and Reel Information



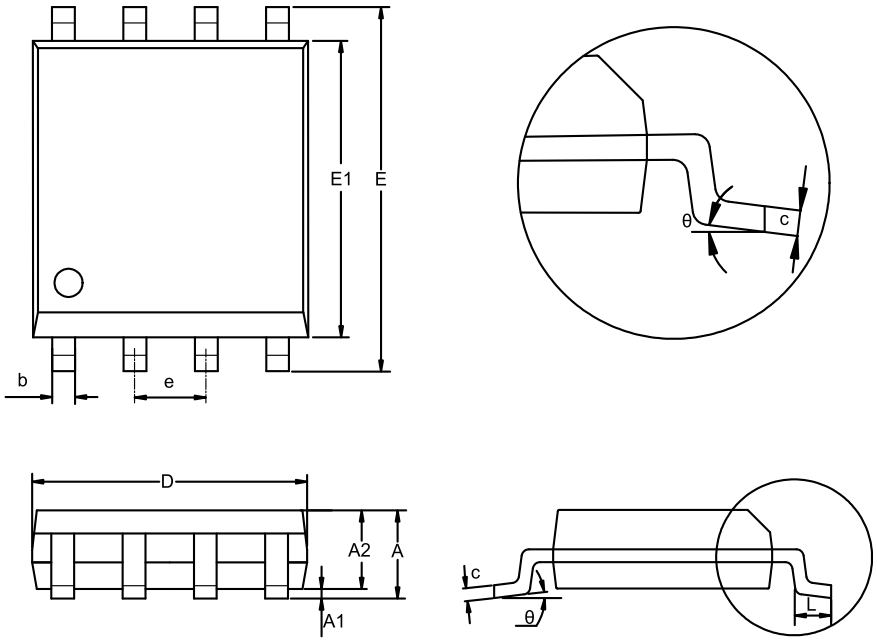


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT20102-VS3R	VSSOP8	178.0	2.25	1.05	8.0	11.4	3.35	4.0	Q3

Package Outline Dimensions

VSSOP8

Package Outline Dimensions VS3(VSSOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	1.000	0.028	0.039
A1	0.000	0.150	0.000	0.006
A2	0.600	0.850	0.024	0.033
b	0.170	0.270	0.007	0.011
c	0.080	0.230	0.003	0.009
D	1.900	2.100	0.075	0.083
E	3.000	3.200	0.118	0.126
E1	2.200	2.400	0.087	0.094
e	0.500 BSC		0.020 BSC	
L	0.150	0.400	0.006	0.016
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT20102-VS3R	−40 to 125°C	VSSOP8	T12	MSL1	Tape and Reel,3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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