TEXAS INSTRUMENTS

TLV320DAC23

Stereo Audio D/A Converter, 8- to 96-kHz With Integrated Headphone Amplifier

Data Manual

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Digital Audio Products

SLES001C

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1 Introduction

The TLV320DAC23 is a high performance stereo DAC with highly integrated analog functionality. The DACs within the TLV320DAC23 are comprised of multibit sigma-delta technology with integrated over-sampling digital interpolation filters. Supported data transfer word lengths are 16, 20, 24, and 32 bits with sample rates from 8 kHz to 96 kHz. The DAC sigma-delta modulator features a second order multibit architecture with up to 100 dBA SNR at audio sample rates up to 96 kHz. This enables high quality digital audio playback capability while consuming less than 19 mW during playback only. The TLV320DAC23 is the ideal choice for portable digital audio player applications such as MP3 digital audio players.

Integrated analog features consist of stereo line inputs with an analog bypass path and a stereo headphone amplifier with analog volume control and mute. The headphone amplifier is capable of delivering 30 mW per channel into 32 Ω. The analog bypass path allows use of the stereo line inputs and the headphone amplifier with analog volume control while completely bypassing the DAC, thus enabling further design flexibility such as integrated FM tuners.

While the TLV320DAC23 supports the industry standard over-sample rates of 256 f_S and 384 f_S, unique over-sample rates of 250 f_S and 272 f_S are provided which optimize interface considerations in designs using TI C54x DSPs and USB data interfaces. A single 12-MHz crystal can be used to supply clocking to the DSP, USB, and DAC. The TLV320DAC23 features an internal oscillator which, when connected to a 12-MHz external crystal, will provide a system clock to the DSP and other peripherals at either 12 MHz or 6 MHz using an internal clock buffer and selectable divider. Audio sample rates of 48 kHz and CD standard rates of 44.1 kHz are directly supported from a 12-MHz master clock with 250 f_S and 272 f_S over-sample rates.

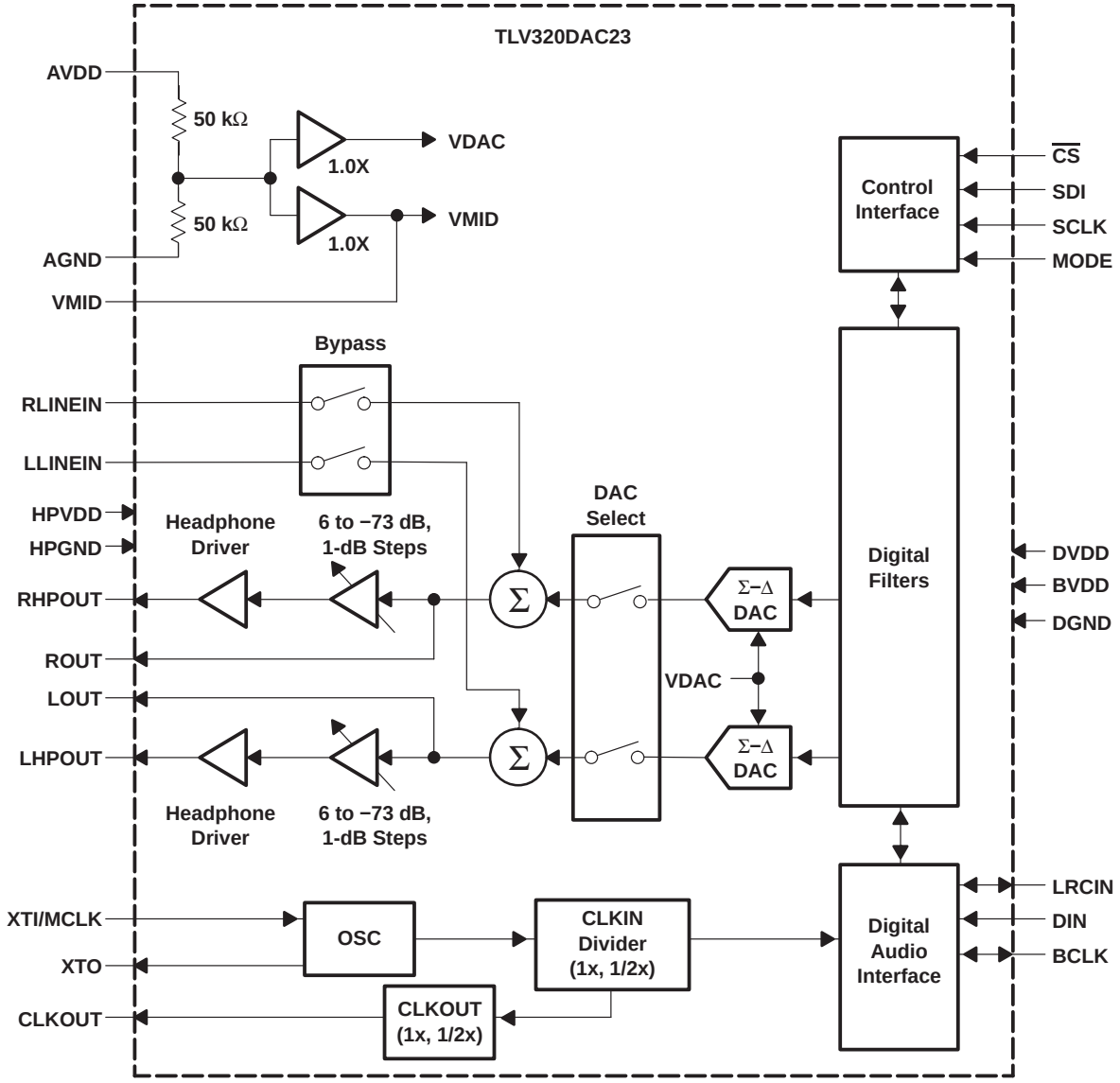
Low power consumption and flexible power management allow selective shutdown of DAC functions, thus extending battery life in portable applications. Couple this design solution with the industry's smallest package, the TI proprietary MicroStar Junior™ using only 25 mm^2 of board area, powerful portable stereo audio designs are easily realizable in a cost effective, space saving total analog solution.

MicroStar Junior is a trademark of Texas Instruments.

1.1 Features

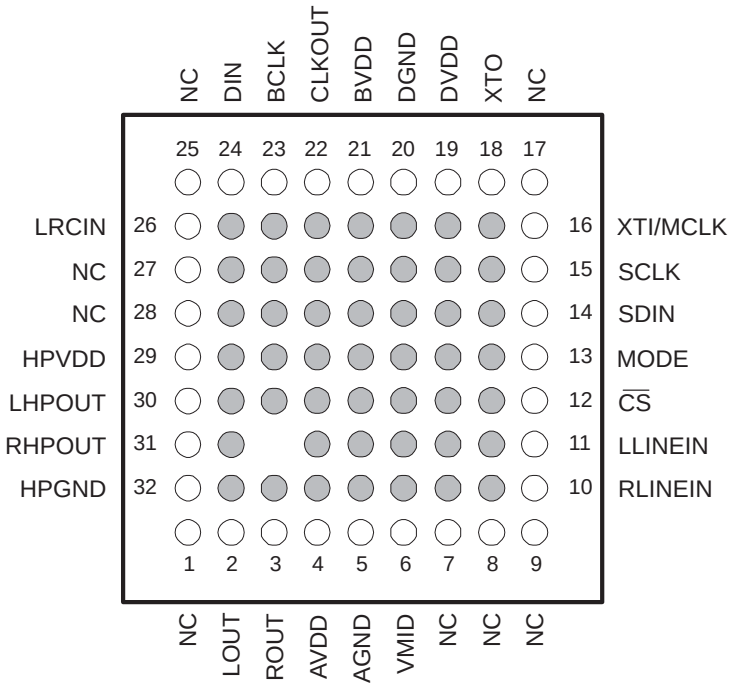
- High-Performance Stereo DAC
  - 100-dB SNR multibit sigma-delta ADC (A-weighted at 48 kHz)
  - 1.42 V – 3.6 V digital supply: compatible with TI C54x DSP core voltages
  - 2.7 V – 3.6 V analog supply: compatible TI C54x DSP buffer voltages
  - 8-kHz – 96-kHz sampling-frequency support
- Software control via TI McBSP-compatible multiprotocol serial port
  - 2-wire-compatible and SPI-compatible serial port protocols
  - Glueless interface to TI McBSPs
- Audio data input/output via TI McBSP compatible programmable audio interface
  - I^2S-compatible interface
  - Standard I^2S, MSB, or LSB justified data transfers
  - 16/20/24/32-bit word lengths
  - Audio master/slave timing capability optimized for TI DSPs (250/272 f_S)
  - Industry-standard master/slave support also provided (256/384 f_S)
  - Glueless interface to TI McBSPs
- Stereo line inputs
- Stereo line outputs
  - Analog stereo mixer for DAC and analog bypass path
- Analog volume control with mute
- Highly efficient linear headphone amplifier
  - 30 mW into 32 Ω from a 3.3-V analog supply voltage
- Flexible power management under total software control
  - 18-mW power consumption during playback mode
  - Standby power consumption <150 μW
  - Power-down power consumption <15 μW
- Industry's smallest package: 32-Pin TI proprietary MicroStar Junior
  - 25 mm^2 total board area
  - 28-Pin TSSOP available (62 mm^2 total board area)
  - 28-Pin QFN available (25 mm^2 total board area)
- Ideally suitable for portable solid-state audio players and recorders

1.2 Functional Block Diagram

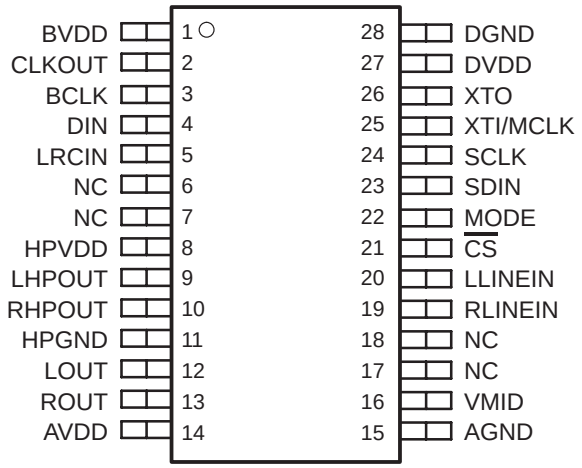


1.3 Terminal Assignments

GQE PACKAGE
(TOP VIEW)

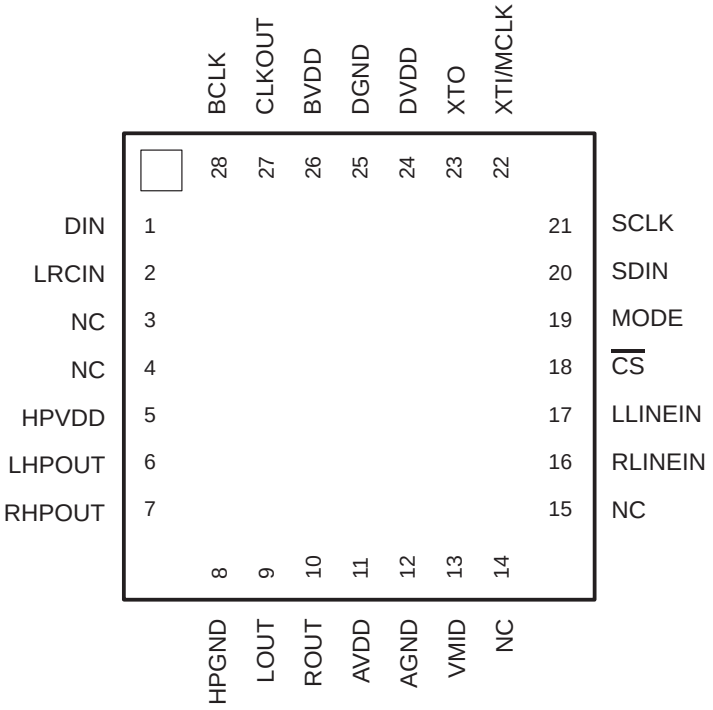


PW PACKAGE
(TOP VIEW)



NC − No internal connection

RHD PACKAGE
(TOP VIEW)



NC − No internal connection

1.4 Ordering Information

T_A	PACKAGE		
	32-Pin MicroStar Junior GQE	**28-Pin TSSOP PW**	**28-Pin QFN RHD**
−10°C to 70°C	TLV320DAC23GQE	TLV320DAC23PW	TLV320DAC23RHD
−40°C to 85°C	TLV320DAC23IGQE	TLV320DAC23IPW	TLV320DAC23IRHD

1.5 Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	NUMBER				
	GQE	PW	RHD		
AGND	5	15	12	−	Analog supply return
AVDD	4	14	11	−	Analog supply input. Voltage level is 3.3 V nominal.
BCLK	23	3	28	I/O	I^2S serial-bit clock. In audio master mode, the DAC23 generates this signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
BVDD	21	1	26	−	Buffer supply input. Voltage range is from 2.7 V to 3.6 V.
CLKOUT	22	2	27	O	Clock output. This is a buffered version of the XTI input and is available in 1X or 1/2X frequencies of XTI. Frequency selection is controlled by bit X in control register XX.
$\overline{CS}$	12	21	18	I	Control port input latch/address select. For SPI control mode this input acts as the data latch control. For 2-wire control mode this input defines the seventh bit in the device address field. See Section 3.1 for details.
DIN	24	4	1	I	I^2S format serial data input to the sigma-delta stereo DAC
DGND	20	28	25	−	Digital supply return
DVDD	19	27	24	−	Digital supply input. Voltage range is 1.4 V to 3.6 V.
HPGND	32	11	8	−	Analog headphone amplifier supply return
HPVDD	29	8	5	−	Analog headphone amplifier supply input. Voltage level is 3.3 V nominal.
LHPOUT	30	9	6	O	Left stereo mixer-channel amplified headphone output. Nominal 0-dB output level is 1.0 V_{RMS}. Gain of –73 dB to 6 dB is provided in 1-dB steps.
LLINEIN	11	20	17	I	Left stereo-line input channel
LOUT	2	12	9	O	Left stereo mixer-channel line output. Nominal output level is 1.0 V_{RMS}.
LRCIN	26	5	2	I/O	I^2S DAC-word clock signal. In audio master mode, the DAC23 generates this framing signal and sends it to the DSP. In audio slave mode, the signal is generated by the DSP.
MODE	13	22	19	I	Serial interface mode input. See Section 3.1 for details.
NC	1, 7, 8, 9, 17, 25, 27, 28	6, 7, 17,18	3, 4, 14, 15	−	Not Used—No internal connection
RHPOUT	31	10	7	O	Right stereo mixer-channel amplified headphone output. Nominal 0-dB output level is 1.0 V_{RMS}. Gain of −73 dB to 6 dB is provided in 1-dB steps.
RLINEIN	10	19	16	I	Right stereo-line input channel
ROUT	3	13	10	O	Right stereo mixer-channel line output. Nominal output level is 1.0 V_{RMS}.
SCLK	15	24	21	I	Control port serial data clock. For both SPI and 2-wire control modes this is the serial clock input. See Section 3.1 for details.
SDIN	14	23	20	I	Control port serial data input. For both SPI and 2-wire control modes this is the serial data input and also is used to select the control protocol after reset. See Section 3.1 for details.
VMID	6	16	13	I	Midrail voltage decoupling input. 10-µF and 0.1-µF capacitors should be connected in parallel to this terminal for noise filtering. Voltage level is 1/2 AVDD nominal.
XTI/MCLK	16	25	22	I	Crystal or external clock input. Used for derivation of all internal clocks on the DAC23.
XTO	18	26	23	O	Crystal output. Connect to external crystal for applications where the DAC23 is the audio timing master. Not used in applications where external clock source is used.

2 Specifications

2.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range, AV_{DD} to AGND, DV_{DD} to DGND, BV_{DD} to DGND, HPV_{DD} to HPGND (see Note 1) . . . . . −0.3 V to + 3.63 V
Analog supply return to digital supply return, AGND to DGND . . . . . −0.3 V to + 0 .3 V
Input voltage range, all input signals: Digital . . . . . −0.3 V to DV_{DD} + 0.3 V
Analog . . . . . −0.3 V to AV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . −10°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: DV_{DD} may not exceed BV_{DD} + 0.3V; BV_{DD} may not exceed AV_{DD} + 0.3V or HPV_{DD} + 0.3.

2.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD}, HPV_{DD} (see Note 2)	2.7	3.3	3.6	V
Digital buffer supply voltage, BV_{DD} (see Note 2)	2.7	3.3	3.6	V
Digital core supply voltage, DV_{DD} (see Note 2)	1.42	1.5	3.6	V
Analog input voltage, (AV_{DD} = 3.3 V)		1		V_{RMS}
Stereo line output load resistance	10			kΩ
Headphone amplifier output load resistance	0			Ω
CLKOUT digital output load capacitance		20		pF
All other digital output load capacitance		10		pF
Stereo-line output load capacitance		50		pF
XTI master clock Input			18.43	MHz
DAC conversion rate			96	kHz
Operating free-air temperature, T_A	−10		70	°C

NOTE 2: Digital voltage values are with respect to DGND; analog voltage values are with respect to AGND.

2.3 Electrical Characteristics Over Recommended Operating Conditions, AV_{DD}, HPV_{DD}, BV_{DD} = 3.3 V, DV_{DD} = 1.5 V, Master Mode, XTI = 12 MHz, (unless otherwise stated)

2.3.1 DAC

2.3.1.1 Load = 10 kΩ, 50 pF

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0-dB full-scale output voltage				1.0		V_{RMS}
Signal-to-noise ratio, A-weighted, 0-dB gain (see Notes 3, 4, and 5)	AV_{DD} = 3.3 V	f_S = 44.1kHz	90	100		dB
		f_S = 96 kHz		98		
	AV_{DD} = 2.7 V	f_S = 44.1 kHz		93		
Dynamic range, A-weighted (see Note 5)	AV_{DD} = 3.3 V		85	90		dB
Total harmonic distortion (THD)	AV_{DD} = 3.3 V	1 kHz, 0 dB		–88	–80	dB
		1 kHz, −3 dB		−92		
	AV_{DD} = 2.7 V	1 kHz, 0 dB		−88	−80	dB
		1 kHz, −3 dB		−92		
Power supply rejection ratio	1 kHz, 100 mV_{pp}			50		dB
DAC channel separation				100		dB
THD+N	AV_{DD}=3.3 V, 1 kHz, 0dB			−84	−79	dB

2.3.2 Analog Line Input to Line Output

2.3.2.1 Load = 10 kΩ, 50 pF, no gain on input

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0-dB full-scale output voltage				1.0		V_{RMS}
Signal-to-noise ratio, (SNR) A-weighted, 0-dB gain (see Notes 3, 5)	AV_{DD} = 3.3 V		90	95		dB
Total harmonic distortion (THD)	AV_{DD} = 3.3 V	1 kHz, 0 dB		–86	–80	dB
		1 kHz, −3 dB		−92	−86	
	AV_{DD} = 2.7 V	1 kHz, 0 dB		−86		dB
		1 kHz, −3 dB		−92		
Power supply rejection ratio	1 kHz, 100 mV_{pp}			50		dB
Mute attenuation	1 kHz, 0 dB			80		dB
Input resistance			10 k	24 k		Ω

2.3.3 Stereo Headphone Output

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
0-dB full-scale output voltage				1.0		V_{RMS}
Maximum output power, P_O	R_L = 32 Ω			30		mW
	R_L = 16 Ω			40		mW
Signal-to-noise ratio, A-weighted (see Note 4)	AV_{DD} = 3.3 V		90	97		dB
Total harmonic distortion	AV_{DD} = 3.3 V, 1 kHz output, into 32Ω	P_O = 10 mW			−60	dB
		P_O = 20 mW			−40	dB
Power supply rejection ratio	1 kHz, 100 mV_{pp}			50		dB
Programmable gain	1 kHz output		−73		6	dB
Programmable-gain step size				1		dB
Mute attenuation	1 kHz output			80		dB

NOTES:
3. Ratio of output level with 1-kHz full-scale input, to the output level with the input short circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
4. All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter results in higher THD + N and lower SNR and dynamic range readings than shown in the electrical characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
5. Ratio of output level with 1-kHz full-scale input, to the output level with all zeros into the digital input, measured A-weighted over a 20-Hz to 20-kHz bandwidth.

2.3.4 Analog Reference Levels

PARAMETER	MIN	TYP	MAX	UNIT
Reference voltage, V_{MID}	AVDD/2 − 50 mV		AVDD/2 + 50 mV	V
Divider resistance, R_{VMID}	40	50	60	kΩ

2.3.5 Digital I/O

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Input low level			$0.3 \times BV_{DD}$	V
V_{IH}	Input high level	$0.7 \times BV_{DD}$			V
V_{OL}	Output low level			$0.1 \times BV_{DD}$	V
V_{OH}	Output high level	$0.9 \times BV_{DD}$			V

2.3.6 Supply Current

PARAMETER			MIN	TYP	MAX	UNIT
I_{TOT}	Total supply current, no input signal (3.3 V supply)	Line playback only (Clk power off, 50 Ω)		6	8	mA
		Line playback only (Clk power on, 50 Ω)		15		mA
		Analog bypass (line in to line out)		3		mA
		Power down: Oscillator enabled		1.5		mA
		Power down: Oscillator disabled		0.01	0.025	mA

2.4 Digital-Interface Timing

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(1)}$	System-clock pulse duration, MCLK/XTI	High	18			ns
$t_{w(2)}$		Low	18			
$t_{c(1)}$	System-clock period, MCLK/XTI		54			ns
	Duty cycle, MCLK/XTI		40/60%		60/40%	
$t_{pd(1)}$	Propagation delay, CLKOUT		0		10	ns

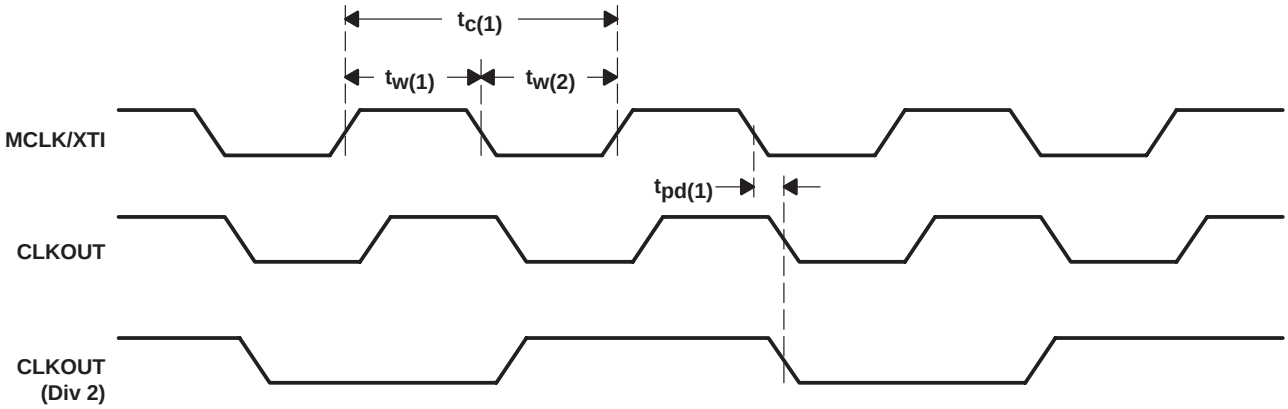


Figure 2−1. System-Clock Timing Requirements

2.4.1 Audio Interface (Master Mode)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{pd(2)}$	Propagation delay, LRCIN	0		10	ns
$t_{su(1)}$	Setup time, DIN	10			ns
$t_{h(1)}$	Hold time, DIN	10			ns

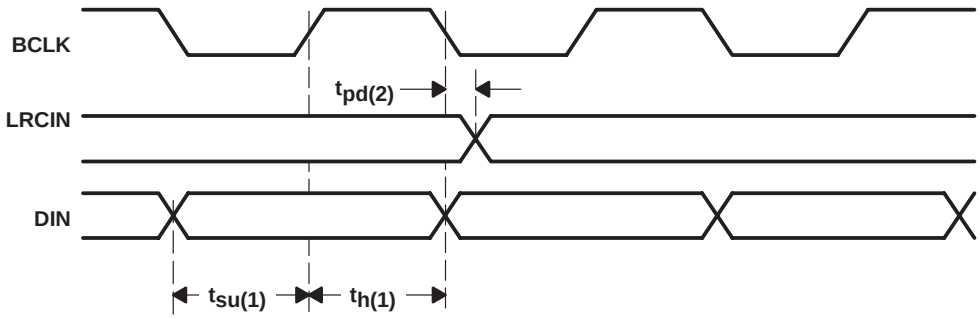


Figure 2−2. Master-Mode Timing Requirements

2.4.2 Audio Interface (Slave-Mode)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(3)}$	Pulse duration, BCLK	High	20			ns
$t_{w(4)}$		Low	20			
$t_{c(2)}$	Clock period, BCLK		50			ns
$t_{su(2)}$	Setup time, DIN		10			ns
$t_{h(2)}$	Hold time, DIN		10			ns
$t_{su(3)}$	Setup time, LRCIN		10			ns
$t_{h(3)}$	Hold time, LRCIN		10			ns

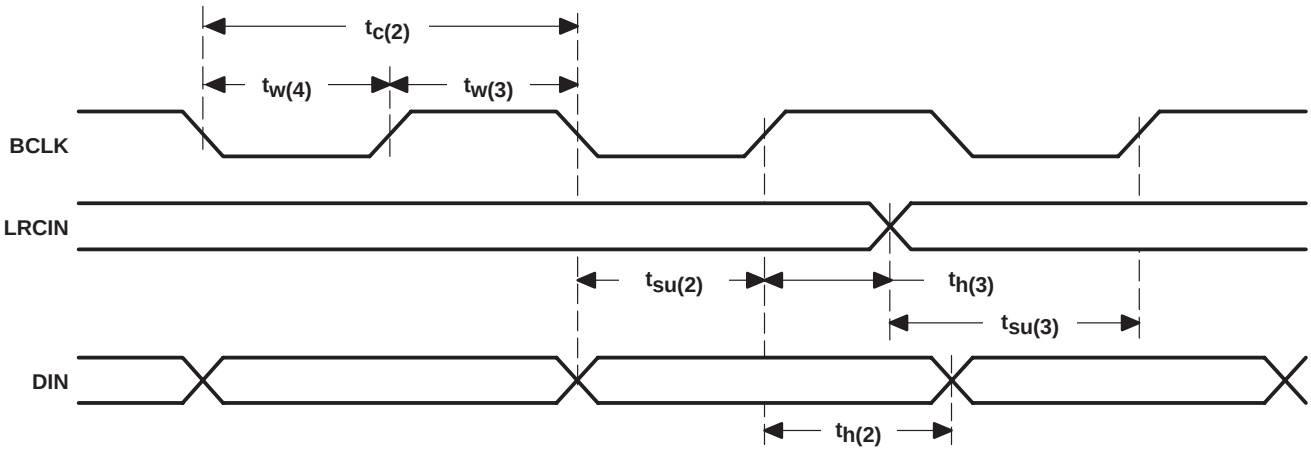


Figure 2−3. Slave-Mode Timing Requirements

2.4.3 Three-Wire Control Interface (SDI)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(5)}$	Clock pulse duration, SCLK	High	20			ns
$t_{w(6)}$		Low	20			
$t_{c(3)}$	Clock period, SCLK		80			ns
$t_{su(4)}$	Clock rising edge to $\overline{CS}$ rising edge, SCLK		60			ns
$t_{su(5)}$	Setup time, SDIN to SCLK		20			ns
$t_{h(4)}$	Hold time, SCLK to SDIN		20			ns
$t_{w(7)}$	Pulse duration, $\overline{CS}$	High	20			ns
$t_{w(8)}$		Low	20			

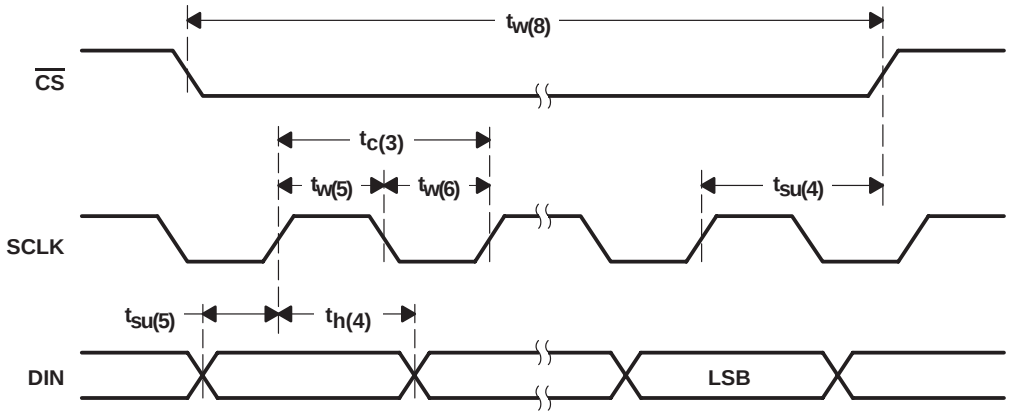


Figure 2−4. Three-Wire Control Interface Timing Requirements

2.4.4 Two-Wire Control Interface

PARAMETER			MIN	TYP	MAX	UNIT
$t_{w(9)}$	Clock pulse duration, SCLK	High	1.3			µs
$t_{w(10)}$		Low	600			ns
f(sf)	Clock frequency, SCLK		0		400	kHz
$t_{h(5)}$	Hold time (start condition)		600			ns
$t_{su(6)}$	Setup time (start condition)		600			ns
$t_{h(6)}$	Data hold time				900	ns
$t_{su(7)}$	Data setup time		100			ns
t_r	Rise time, SDIN, SCLK				300	ns
t_f	Fall time, SDIN, SCLK				300	ns
$t_{su(8)}$	Setup time (stop condition)		600			ns

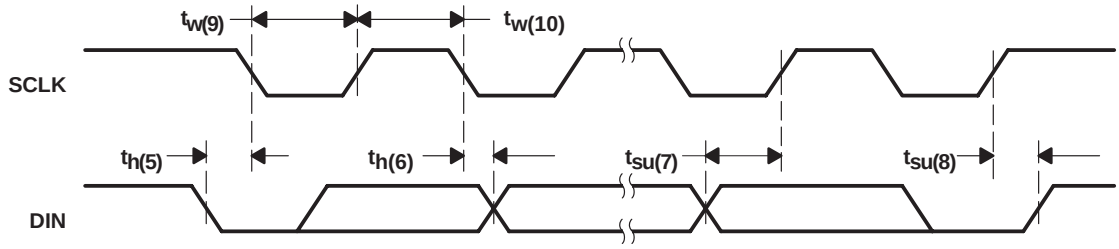


Figure 2−5. Two-Wire Control Interface Timing Requirements

3 How to Use the DAC23

3.1 Control Interfaces

The TLV320DAC23 has many programmable features. The control interface is used to program the registers of the device. The control interface complies with SPI (three-wire operation) and two-wire operation specifications. The state of the MODE terminal selects the control interface type. The MODE pin must be hardwired to the required level.

MODE	INTERFACE
0	2-wire
1	SPI

3.1.1 SPI

In SPI mode, SDI carries the serial data, SCLK is the serial clock and $\overline{CS}$ latches the data word into the TLV320DAC23. The interface is compatible with microcontrollers and DSPs with an SPI interface.

A control word consists of 16 bits, starting with the MSB. The data bits are latched on the rising edge of SCLK. A rising edge on $\overline{CS}$ after the sixteenth rising clock edge latches the data word into the DAC (see Figure 3-1).

The control word is divided into two parts. The first part is the address block, the second part is the data block:

B[15:9] Control address bits
B[8:0] Control data bits

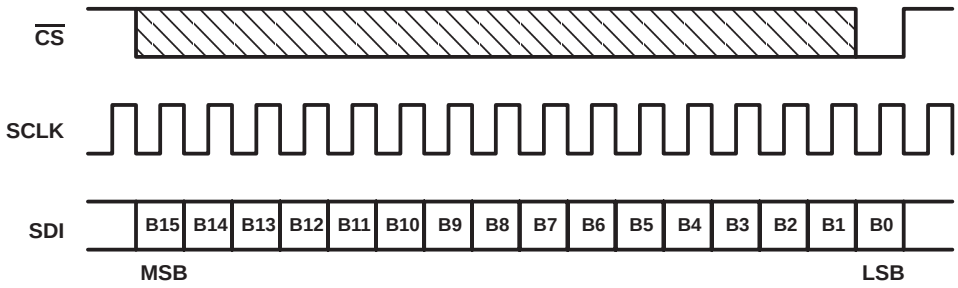


Figure 3−1. SPI Timing

3.1.2 2-Wire

In 2-wire mode, the data transfer uses SDI for the serial data and SCLK for the serial clock. The start condition is a falling edge on SDIN while SCLK is high. The seven bits following the start condition determine the device on the 2-wire bus that receives the data. R/W determines the direction of the data transfer. The TLV320DAC23 is a write only device and responds only if R/W is 0. The device operates only as a slave device whose address is selected by setting the state of the CS pin as follows.

$\overline{CS}$ STATE (Default = 0)	ADDRESS
0	0011010
1	0011011

The device that recognizes the address responds by pulling SDI low during the ninth clock cycle, acknowledging the data transfer. The control follows in the next two eight-bit blocks. The stop condition after the data transfer is a rising edge on SDI when SCLK is high (see Figure 3-2).

The 16-bit control word is divided into two parts. The first part is the address block, the second part is the data block:

B[15:9] Control address bits
B[8:0] Control data bits

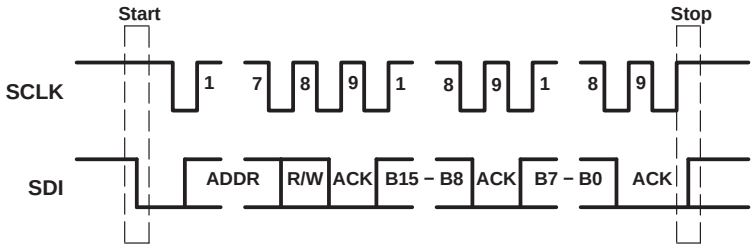


Figure 3−2. 2-Wire Compatible Timing

3.1.3 Register Map

The TLV320DAC23 has the following set of registers, which are used to program the modes of operation.

ADDRESS	REGISTER
0000000	Left line input channel control
0000001	Right line input channel control
0000010	Left channel headphone volume control
0000011	Right channel headphone volume control
0000100	Analog audio path control
0000101	Digital audio path control
0000110	Power down control
0000111	Digital audio interface format
0001000	Sample rate control
0001001	Digital interface activation
0001111	Reset register

Left Line Input Channel Control (Address: 0000000)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	LRS	LIM	X	X	X	X	X	X	X
Default	0	1	0	0	0	0	0	0	0

LRS Left/right line simultaneous volume/mute update
Simultaneous update 0 = Disabled 1 = Enabled
LIM Left line input mute 0 = Normal 1 = Muted
X Reserved

Right Line Input Channel Control (Address: 0000001)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	RLS	RIM	X	X	X	X	X	X	X
Default	0	1	0	0	0	0	0	0	0

RLS Right/left line simultaneous volume/mute update
Simultaneous update 0 = Disabled 1 = Enabled
RIM Right line input mute 0 = Normal 1 = Muted
X Reserved

Left Channel Headphone Volume Control (Address: 0000010)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	LRS	LZC	LHV6	LHV5	LHV4	LHV3	LHV2	LHV1	LHV0
Default	0	1	1	1	1	1	0	0	1

LRS — Left/right headphone channel simultaneous volume/mute update
Simultaneous update 0 = Disabled 1 = Enabled

LZC — Left-channel zero-cross detect
Zero-cross detect 0 = Off 1 = On

LHV[6:0] — Left Headphone volume control (1111001 = 0 dB default)
1111111 = +6 dB, 79 steps between +6 dB and −73 dB (mute), 0110000 = −73 dB (mute), any thing below 0110000 does nothing − you are still muted

Right Channel Headphone Volume Control (Address: 0000011)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	RLS	RZC	RHV6	RHV5	RHV4	RHV3	RHV2	RHV1	RHV0
Default	0	1	1	1	1	1	0	0	1

RLS — Right/left headphone channel simultaneous volume/mute Update
Simultaneous update 0 = Disabled 1 = Enabled

RZC — Right-channel zero-cross detect
Zero-cross detect 0 = Off 1 = On

RHV[6:0] — Right headphone volume control (1111001 = 0 dB default)
1111111 = +6 dB, 79 steps between +6 dB and −73 dB (mute), 0110000 = −73 dB (mute), any thing below 0110000 does nothing − you are still muted

Analog Audio Path Control (Address: 0000100)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	DAC	BYP	X	X	X
Default	0	0	0	0	0	1	0	1	0

DAC — DAC select 0 = DAC off 1 = DAC selected
BYP — Bypass 0 = Disabled 1 = Enabled
X — Reserved

Digital Audio Path Control (Address: 0000101)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	DACM	DEEMP1	DEEMP0	X
Default	0	0	0	0	0	1	0	0	0

DACM — DAC soft mute 0 = Disabled 1 = Enabled
DEEMP[1:0] — De-emphasis control 00 = Disabled 01 = 32 kHz 10 = 44.1 kHz 11 = 48 kHz
X — Reserved

Power Down Control (Address: 0000110)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	OFF	CLK	OSC	OUT	DAC	X	X	LINE
Default	0	0	0	1	1	1	1	1	1

OFF — Power 0 = On 1 = Off
CLK — Clock 0 = On 1 = Off
OSC — Oscillator 0 = On 1 = Off
OUT — Outputs 0 = On 1 = Off
DAC — DAC 0 = On 1 = Off
LINE — Line input 0 = On 1 = Off
X — Reserved

Digital Audio Interface Format (Address: 0000111)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	MS	LRSWAP	LRP	IWL1	IWL0	FOR1	FOR0
Default	0	0	0	0	0	0	0	0	1

MS	Master/slave mode	0 = Slave	1 = Master		
LRSWAP	DAC left/right swap	0 = Disabled	1 = Enabled		
LRP	DAC left/right phase	0 = Right channel on, LRCIN high			
		1 = Right channel on, LRCIN low			
IWL[1:0]	Input bit length	00 = 16 bit	01 = 20 bit	10 = 24 bit	11 = 32 bit
FOR[1:0]	Data format	11 = DSP format, frame sync followed by two data words			
		10 = I^2S format, MSB first, left – 1 aligned			
		01 = MSB first, left aligned			
		00 = MSB first, right aligned			
X	Reserved				

NOTES: 1. In Master mode, the TLV320AIC23 supplies the BCLK and LRCIN. In Slave mode, BCLK and LRCIN are supplied to the TLV320AIC23.
2. In normal mode, BCLK = MCLK/4 for all sample rates except for 88.2 kHz and 96 kHz. For 88.2 kHz and 96 kHz sample rate, BCLK = MCLK.
3. In USB mode, bit BCLK = MCLK

Sample Rate Control (Address: 0001000)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	CLKOUT	CLKIN	SR3	SR2	SR1	SR0	BOSR	USB/Normal
Default	0	0	0	0	0	0	0	0	0

CLKOUT	Clock output divider	0 = MCLK	1 = MCLK/2
CLKIN	Clock input divider	0 = MCLK	1 = MCLK/2
SR[3:0]	Sampling rate control (see Sections 3.3.2.1 AND 3.3.2.2)		
BOSR	Base oversampling rate		
	USB mode:	0 = 250 f_S	1 = 272 f_S
	Normal mode:	0 = 256 f_S	1 = 384 f_S
USB/Normal	Clock mode select:	0 =Normal	1 = USB
X	Reserved		

Digital Interface Activation (Address: 0001001)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	X	X	X	X	ACT
Default	0	0	0	0	0	0	0	0	0

ACT	Activate interface	0 = Inactive	1 = Active
X	Reserved		

Reset Register (Address: 0001111)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0	0	0

RES	Write to this register triggers reset

3.2 Analog Interface

3.2.1 Line Inputs

The TLV320DAC23 has line inputs for the left and the right audio channels (RLINEIN and LLINEIN). Both line inputs have independently programmable mutes. Active and passive filters for the two channels prevent high frequencies from folding back into the audio band.

The line inputs are biased internally to VMID. When the line inputs are muted or the device is set to standby mode, the line inputs are kept biased to VMID using special antithump circuitry. This reduces audible clicks that otherwise might be heard when reactivating the inputs.

For interfacing to a CD system, the line input should be scaled to 1 V_{RMS} to avoid clipping, using the circuit shown in Figure 3-3.

Where:

R1 = 5 kΩ
R2 = 5 kΩ
C1 = 47 pF
C2 = 470 nF

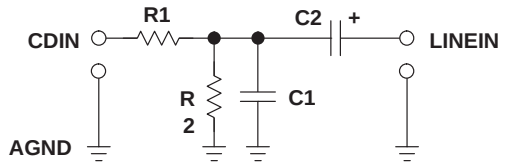


Figure 3−3. Analog Line Input Circuit

R1 and R2 divide the input signal by two, reducing the 2 V_{RMS} from the CD player to the nominal 1 V_{RMS} of the DAC23 inputs. C1 filters high-frequency noise, and C2 removes any dc component from the signal.

3.2.2 Line Outputs

The TLV320DAC23 has two low-impedance line outputs (LLINEOUT and RLINEOUT) capable of driving line loads with 10-kΩ and 50-pF impedances.

The DAC full-scale output voltage is 1.0 V_{RMS} at AV_{DD} = 3.3 V. The full-scale range tracks linearly with the analog supply voltage $AV_{DD.}$ The DAC is connected to the line outputs via a low-pass filter that removes out-of-band components. No further external filtering is required in most applications.

The DAC outputs and the line inputs are summed into the line outputs. The line outputs are muted by either muting the DAC (analog) or soft muting (digital) and disabling the bypass path (see Section 3.1.3).

3.2.3 Headphone Output

The TLV320DAC23 has stereo headphone outputs (LHPOUT and RHPOUT), and is designed to drive 16-Ω or 32-Ω headphones. The headphone output includes a high-quality volume control and mute function.

The headphone volume is logarithmically adjustable from 6 dB to –73 dB in 1-dB steps. Writing 000000 to the volume-control registers (see Section 3.1.3) mutes the headphone output. When the headphone output is muted or the device is placed in standby mode, the dc voltage is maintained at the outputs to prevent audible clicks.

A zero-cross detection circuit is provided under the control of the LZC and RZC bits. If this circuit is enabled, the volume-control values are updated only when the input signal to the gain stage is close to the analog ground level. This minimizes audible clicks as the volume is changed or the device is muted. This circuit has no time-out, so if only dc levels are being applied to the gain stage input of more than 20 mV, the gain is not updated.

The gain is independently programmable on the left and right channels. Both channels can be locked to the same value by setting the RLS and LRS bits (see Section 3.1.3).

3.3 Digital Audio Interface

3.3.1 Digital Audio-Interface Modes

The TLV320DAC23 supports four audio-interface modes.

- Right justified
- Left justified
- I^2S mode
- DSP mode

The four modes are MSB first and operate with a variable word width between 16 to 32 bits (except right-justified mode, which does not support 32 bits).

The digital audio interface consists of clock signal BCLK, data signals DIN and and the synchronization signal LRCIN. BCLK is an output in master mode and an input in slave mode.

3.3.1.1 Right-Justified Mode

In right-justified mode, the LSB is available on the rising edge of BCLK, preceding a falling edge on LRCIN (see Figure 3-4).

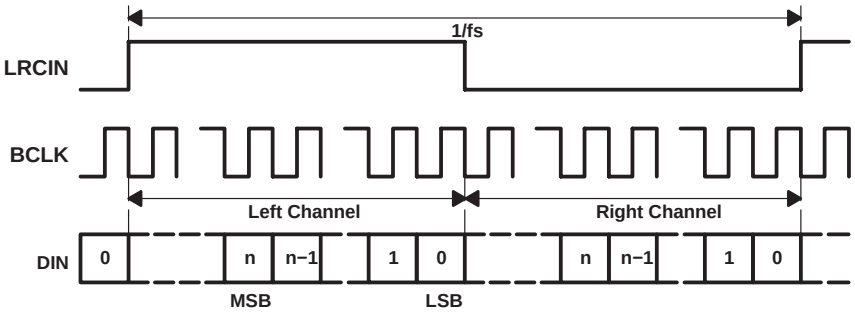


Figure 3−4. Right Justified Mode Timing

3.3.1.2 Left-Justified Mode

In left-justified mode, the MSB is available on the rising edge of BCLK, following a rising edge on LRCIN (see Figure 3-5)

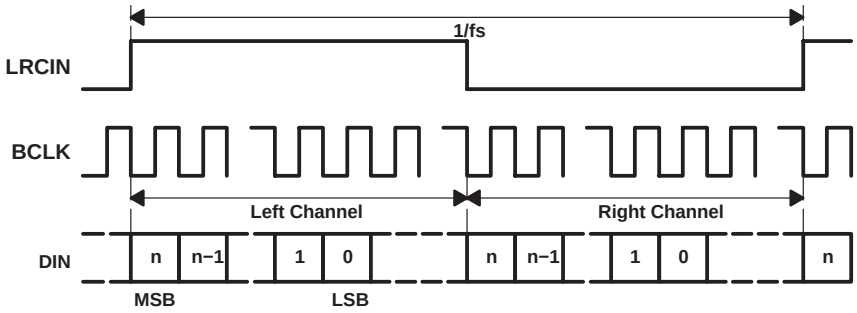


Figure 3−5. Left Justified Mode Timing

3.3.1.3 I^{2}S Mode

In I^{2}S mode, the MSB is available on the second rising edge of BCLK, after the falling edge on LRCIN (see Figure 3-6).

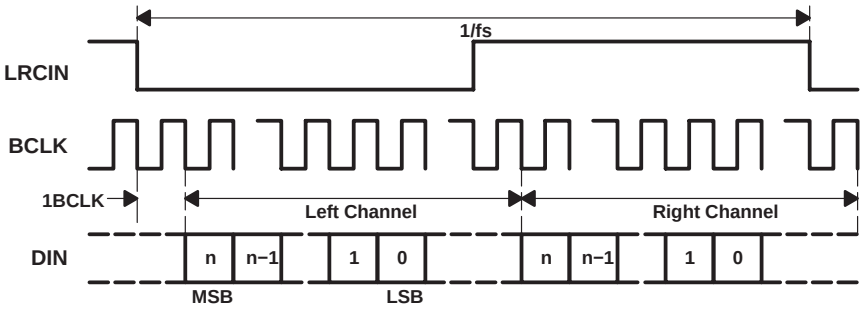


Figure 3−6. I^{2}S Mode Timing

3.3.1.4 DSP Mode

The DSP mode is compatible with the McBSP ports of TI DSPs. LRCIN must be connected to the Frame Sync signal of the McBSP. A falling edge on LRCIN starts the data transfer. The left-channel data consists of the first data word, which is immediately followed by the right channel data word (see Figure 3-7).

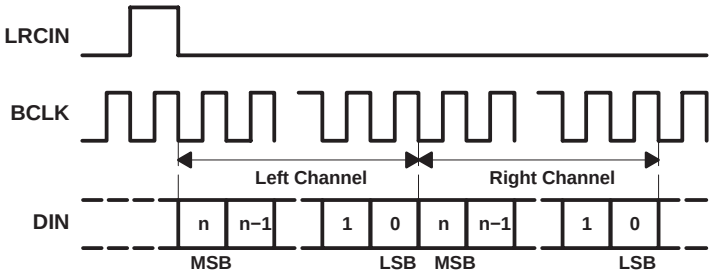


Figure 3−7. DSP Mode Timing

3.3.2 Audio Sampling Rates

The TLV320DAC23 can operate in master or slave clock mode. In the master mode, the TLV320DAC23 clock and sampling rates are derived from a 12-MHz MCLK signal. This 12-MHz clock signal is compatible with the USB specification. The TLV320DAC23 can be used directly in a USB system.

In the slave mode, the TLV320DAC23 clock and sample rates are controlled by using an appropriate MCLK or crystal frequency and the sample rate control register settings.

The settings in the sample rate control register control the clock mode and sampling rates.

Sample Rate Control (Address: 0001000)

BIT	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function	X	CLKOUT	CLKIN	SR3	SR2	SR1	SR0	BOSR	USB/Normal
Default	0	0	0	0	0	0	0	0	0

CLKOUT	Clock output divider	0 = MCLK	1 = MCLK/2
CLKIN	Clock input divider	0 = MCLK	1 = MCLK/2
SR[3:0]	Sample rate control (see Sections 3.3.2.1 and 3.3.2.2)		
BOSR	Base oversampling rate		
	USB mode:	0 = 250 f_S	1 = 272 f_S
	Normal mode:	0 = 256 f_S	1 = 384 f_S
USB/Normal	Clock mode select:	0 =Normal	1 =USB
X	Reserved		

The clock circuit of the DAC23 has two internal dividers. The first, controlled by CLKIN, applies to the sampling-rate generator of the DAC. The second, controlled by CLKOUT, applies only to the CLKOUT terminal. By setting CLKIN to 1, the entire DAC is clocked with half the frequency, effectively dividing the resulting sampling rates by two.

3.3.2.1 USB-Mode Sampling Rates

In the USB mode, the following DAC sampling rates are available:
(MCLK = 12 MHz)

SAMPLING RATE kHz	FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS					
		SR3	SR2	SR1	SR0	BOSR	CLKIN
96	3	0	1	1	1	0	0
88.235	2	1	1	1	1	1	0
48	0	0	0	0	0	0	0
44.118	1	1	0	0	0	1	0
32	0	0	1	1	0	0	0
8.021	1	1	0	1	1	1	0
8	0	0	0	1	1	0	0
48	3	0	1	1	1	0	1
44.118	2	1	1	1	1	1	1
24	0	0	0	0	0	0	1
22.059	1	1	0	0	0	1	1
16	0	0	1	1	0	0	1
4.0105	1	1	0	1	1	1	1
4	0	0	0	1	1	0	1

(MCLK = 6 MHz)

SAMPLING RATE kHz	FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS					
		SR3	SR2	SR1	SR0	BOSR	CLKIN
48	3	0	1	1	1	0	0
44.118	2	1	1	1	1	1	0
24	0	0	0	0	0	0	0
22.059	1	1	0	0	0	1	0
16	0	0	1	1	0	0	0
4.0105	1	1	0	1	1	1	0
4	0	0	0	1	1	0	0
24	3	0	1	1	1	0	1
22.059	2	1	1	1	1	1	1
12	0	0	0	0	0	0	1
11.029	1	1	0	0	0	1	1
8	0	0	1	1	0	0	1
2.005	1	1	0	1	1	1	1
2	0	0	0	1	1	0	1

3.3.2.2 Normal-Mode Sampling Rates

In Normal mode, the following DAC sampling rates, depending on the MCLK frequency, are available:

MCLK = 12.288 MHz

SAMPLING RATE kHz	FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS					
		SR3	SR2	SR1	SR0	BOSR	CLKIN
96	2	0	1	1	1	0	0
48	1	0	0	0	0	0	0
32	1	0	1	1	0	0	0
8	1	0	0	1	1	0	0
48	2	0	1	1	1	0	1
24	1	0	0	0	0	0	1
16	1	0	1	1	0	0	1
4	1	0	0	1	1	0	1

MCLK = 11.2896 MHz

SAMPLING RATE kHz	FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS					
		SR3	SR2	SR1	SR0	BOSR	CLKIN
88.2	2	1	1	1	1	0	0
44.1	1	1	0	0	0	0	0
8.021	1	1	0	1	1	0	0
44.1	2	1	1	1	1	0	1
22.05	1	1	0	0	0	0	1
4.0105	1	1	0	1	0	0	1

MCLK = 18.432 MHz

SAMPLING RATE kHz	FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS					
		SR3	SR2	SR1	SR0	BOSR	CLKIN
96	2	0	1	1	1	1	0
48	1	0	0	0	0	1	0
32	1	0	1	1	0	1	0
8	1	0	0	1	1	1	0
48	2	0	1	1	1	1	1
24	1	0	0	0	0	1	1
16	1	0	1	1	0	1	1
4	1	0	0	1	1	1	1

MCLK = 16.9344 MHz

SAMPLING RATE kHz	FILTER TYPE	SAMPLING-RATE CONTROL SETTINGS					
		SR3	SR2	SR1	SR0	BOSR	CLKIN
88.2	2	1	1	1	1	1	0
44.1	1	1	0	0	0	1	0
8.021	1	1	0	1	1	1	0
44.1	2	1	1	1	1	1	1
22.05	1	1	0	0	0	1	1
4.0105	1	1	0	1	1	1	1

3.3.3 Digital Filter Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Filter Characteristics (48-kHz Sampling Rate)					
Passband	±0.03 dB	0.416 f_S			Hz
Stopband	−6 dB		0.5 f_S		Hz
Passband ripple				±0.03	dB
Stopband attenuation	f > 0.584 f_S		−50		dB
DAC Filter Characteristics (44.1-kHz Sampling Rate)					
Passband	±0.03 dB	0.4535 f_S			Hz
Stopband	−6 dB		0.5 fs		Hz
Passband ripple				±0.03	dB
Stopband attenuation	f > 0.5465 f_S		−50		dB

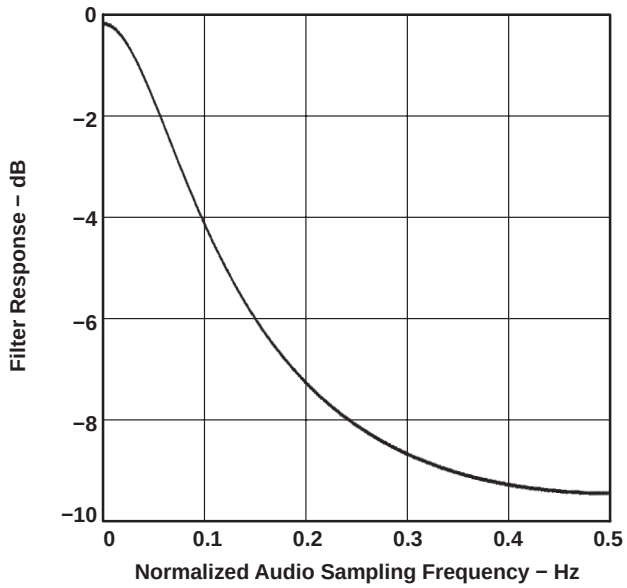


Figure 3−8. Digital De-Emphasis Filter Response − 44.1 kHz Sampling

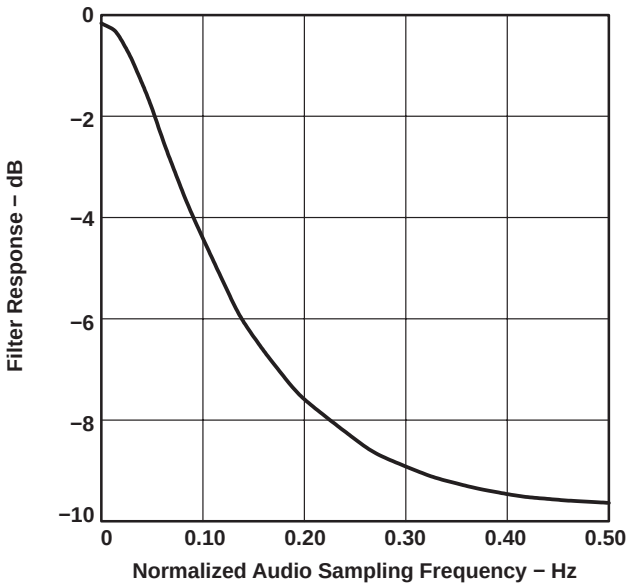


Figure 3−9. Digital De-Emphasis Filter Response − 48 kHz Sampling

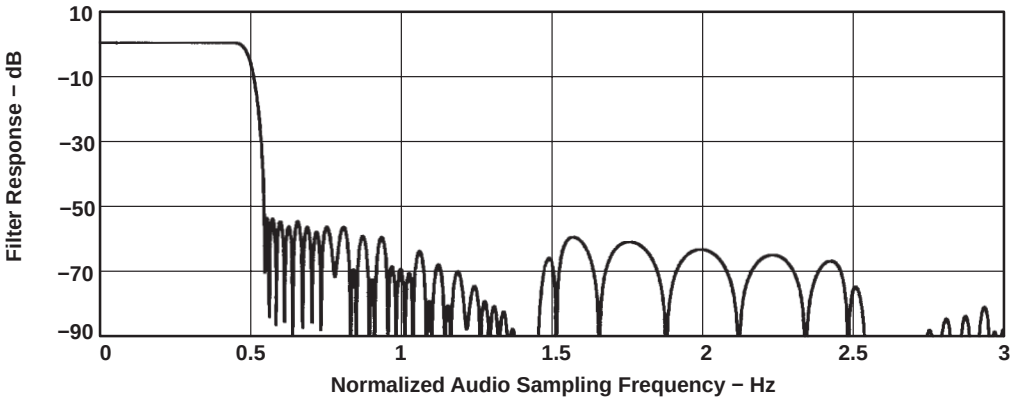


Figure 3−10. DAC Digital Filter Response 0: USB Mode

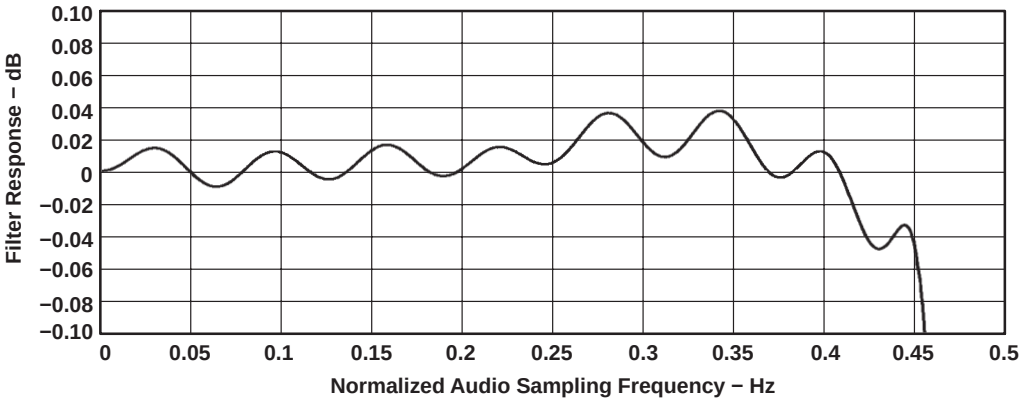


Figure 3−11. DAC Digital Filter Ripple 0: USB Mode

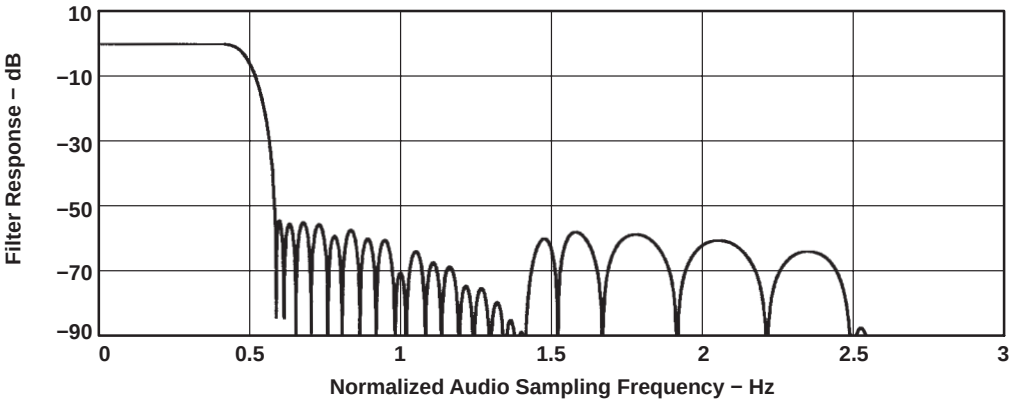


Figure 3−12. DAC Digital Filter Response 1: USB Mode Only

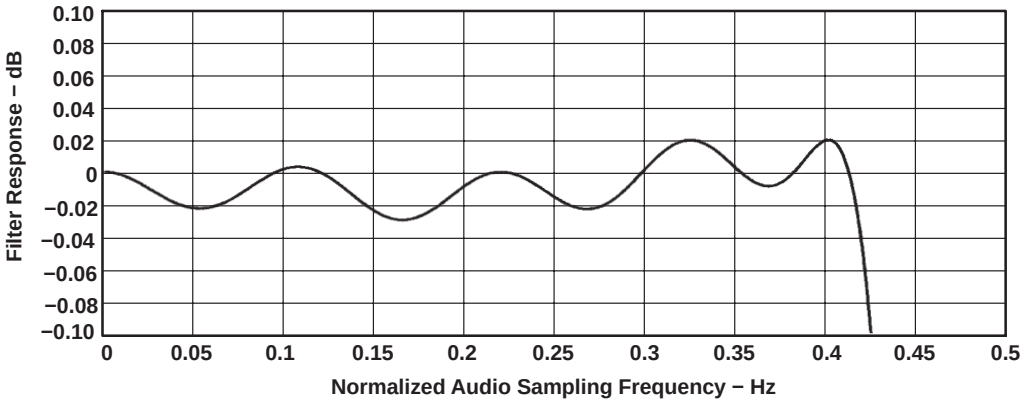


Figure 3−13. DAC Digital Filter Ripple 1: USB Mode Only

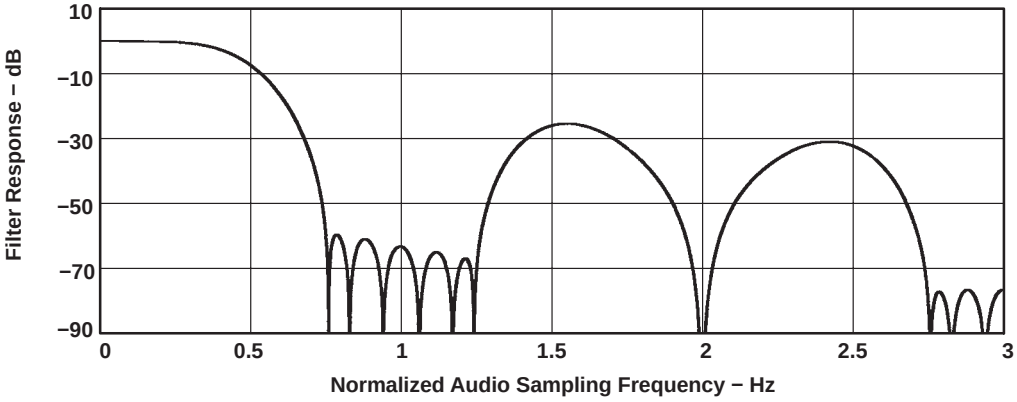


Figure 3−14. DAC Digital Filter Response 2: USB Mode and Normal Modes

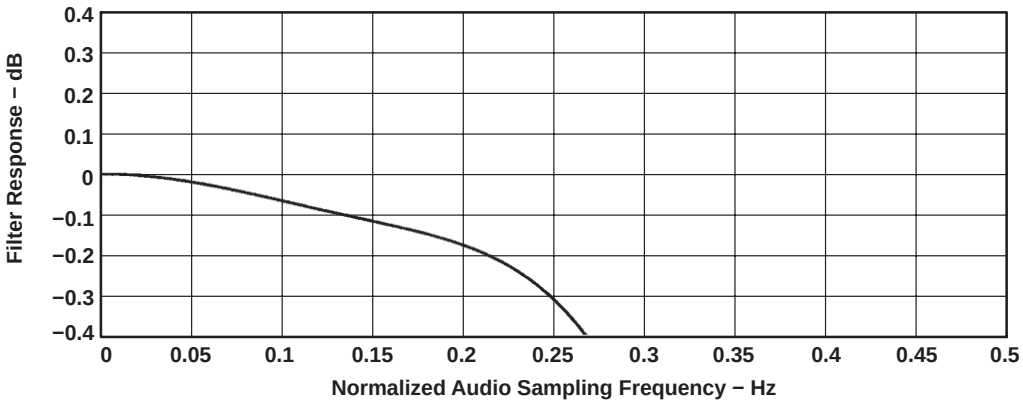


Figure 3−15. DAC Digital Filter Ripple 2: USB Mode and Normal Modes

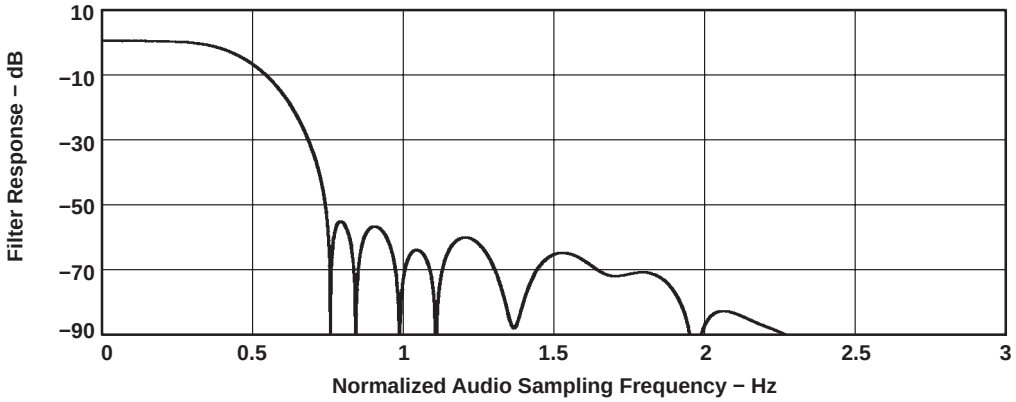


Figure 3−16. DAC Digital Filter Response 3: USB Mode Only

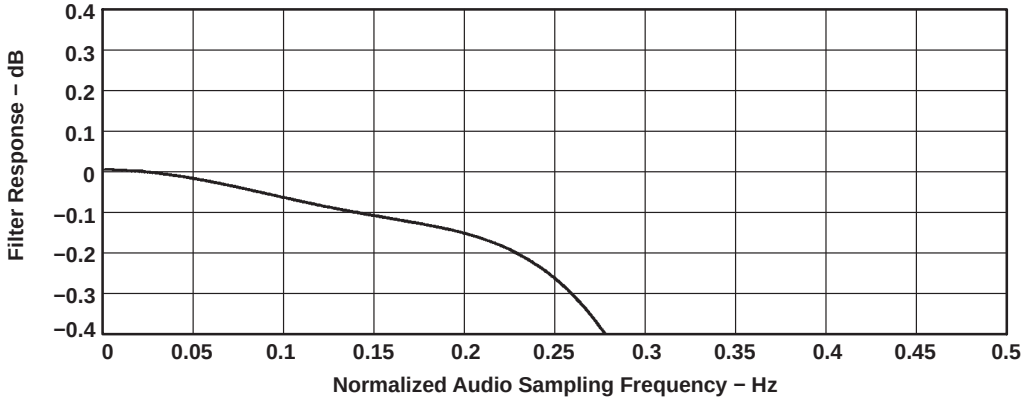


Figure 3−17. DAC Digital Filter Ripple 3: USB Mode Only

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320DAC23GQE	LIFEBUY	BGA MICROSTAR JUNIOR	GQE	80	360	TBD	SNPB	Level-2A-235C-4 WKS	0 to 0	320DAC23	
TLV320DAC23IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	320DAC23I	Samples
TLV320DAC23IPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	320DAC23I	Samples
TLV320DAC23IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	320DAC23I	Samples
TLV320DAC23IRHD	ACTIVE	VQFN	RHD	28	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC23I	Samples
TLV320DAC23PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-10 to 70	320DAC23	Samples
TLV320DAC23PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-10 to 70	320DAC23	Samples
TLV320DAC23RHD	ACTIVE	VQFN	RHD	28	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	DAC23	Samples
TLV320DAC23RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	DAC23	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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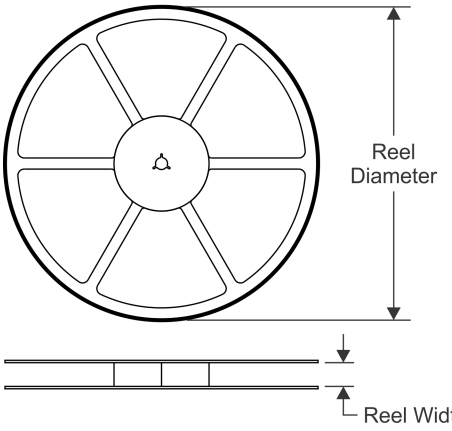
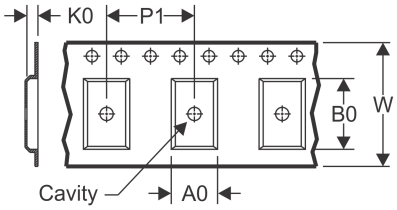
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

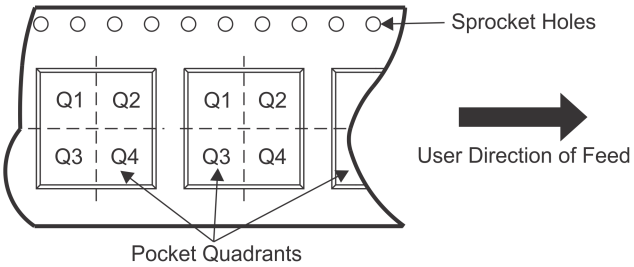


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

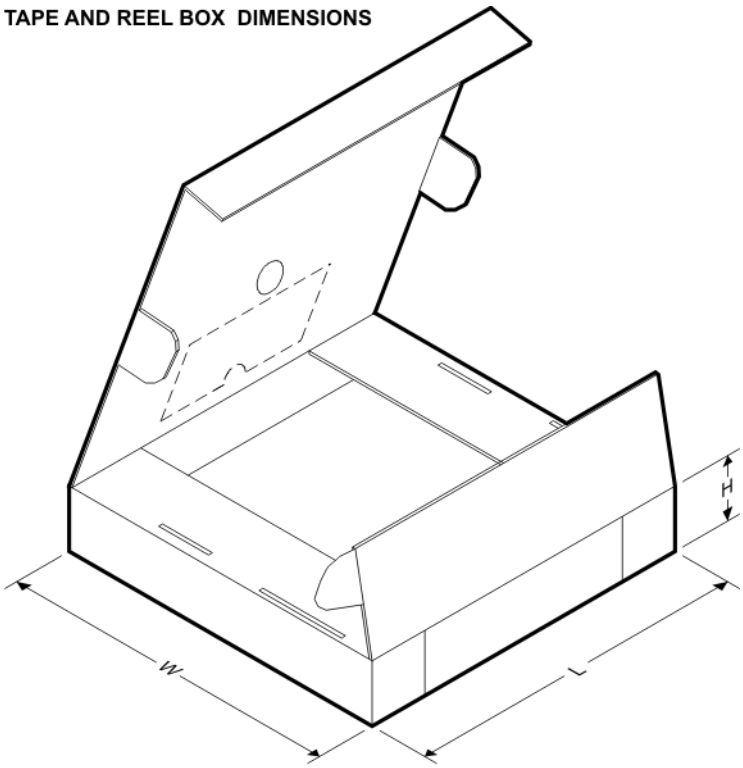
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320DAC23IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLV320DAC23PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TLV320DAC23RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320DAC23IPWR	TSSOP	PW	28	2000	350.0	350.0	43.0
TLV320DAC23PWR	TSSOP	PW	28	2000	350.0	350.0	43.0
TLV320DAC23RHDR	VQFN	RHD	28	3000	350.0	350.0	43.0

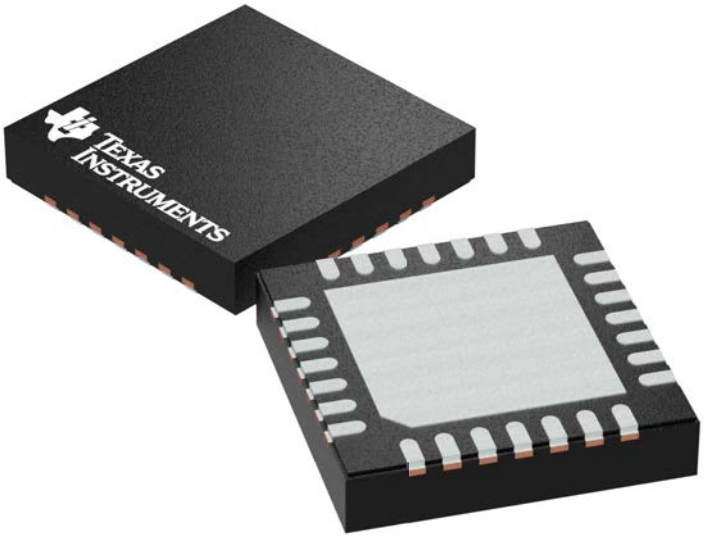
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

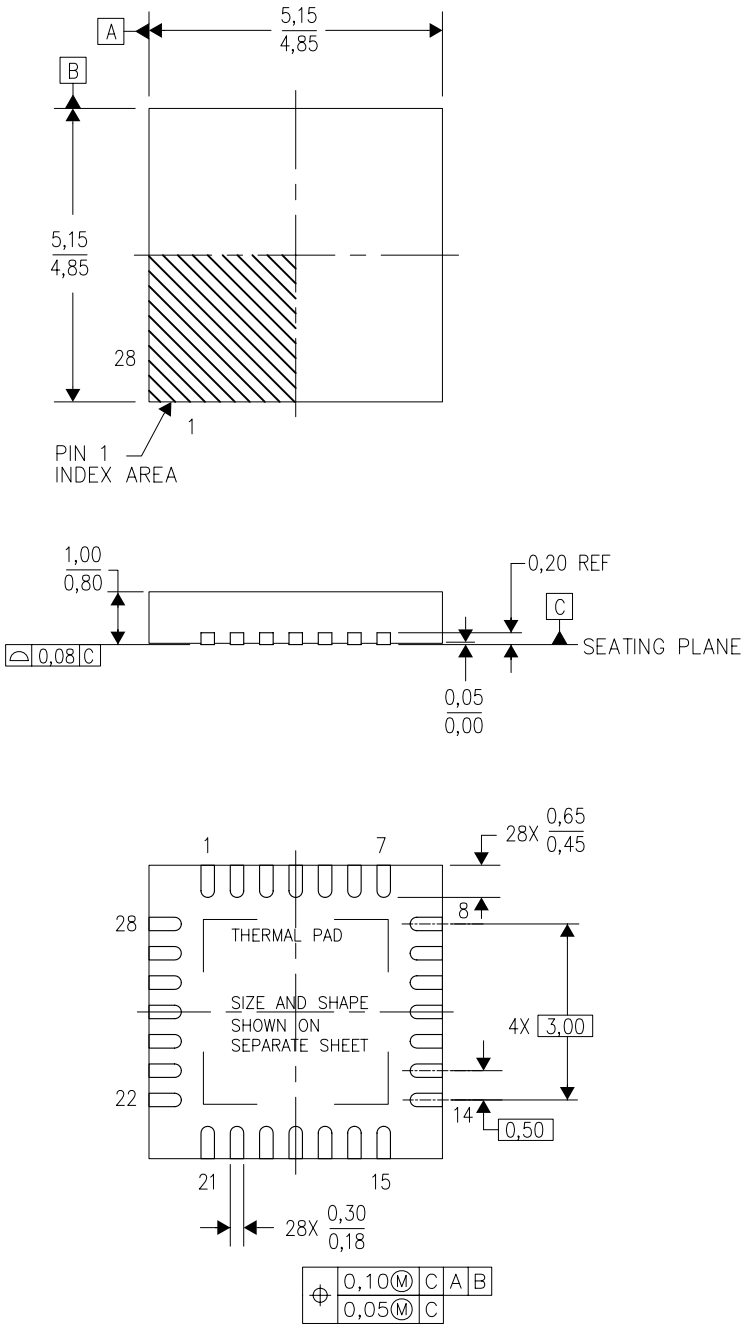
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204400/G

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

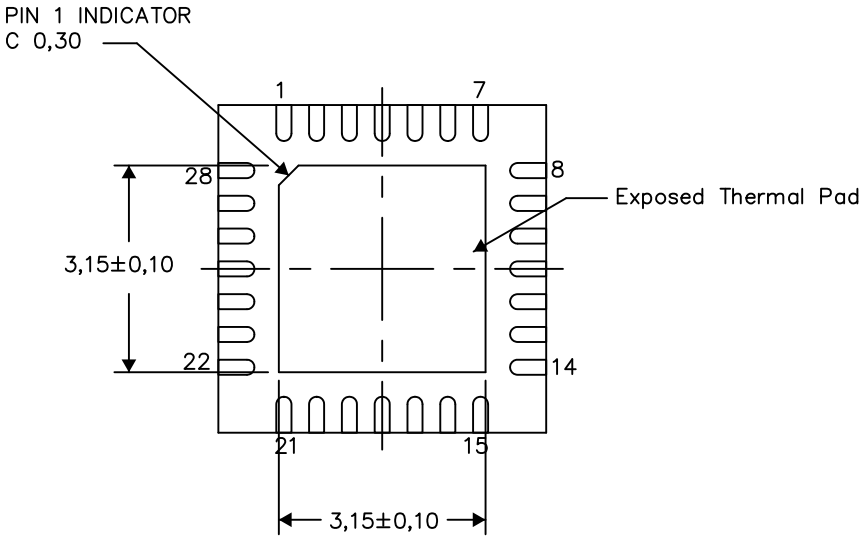
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



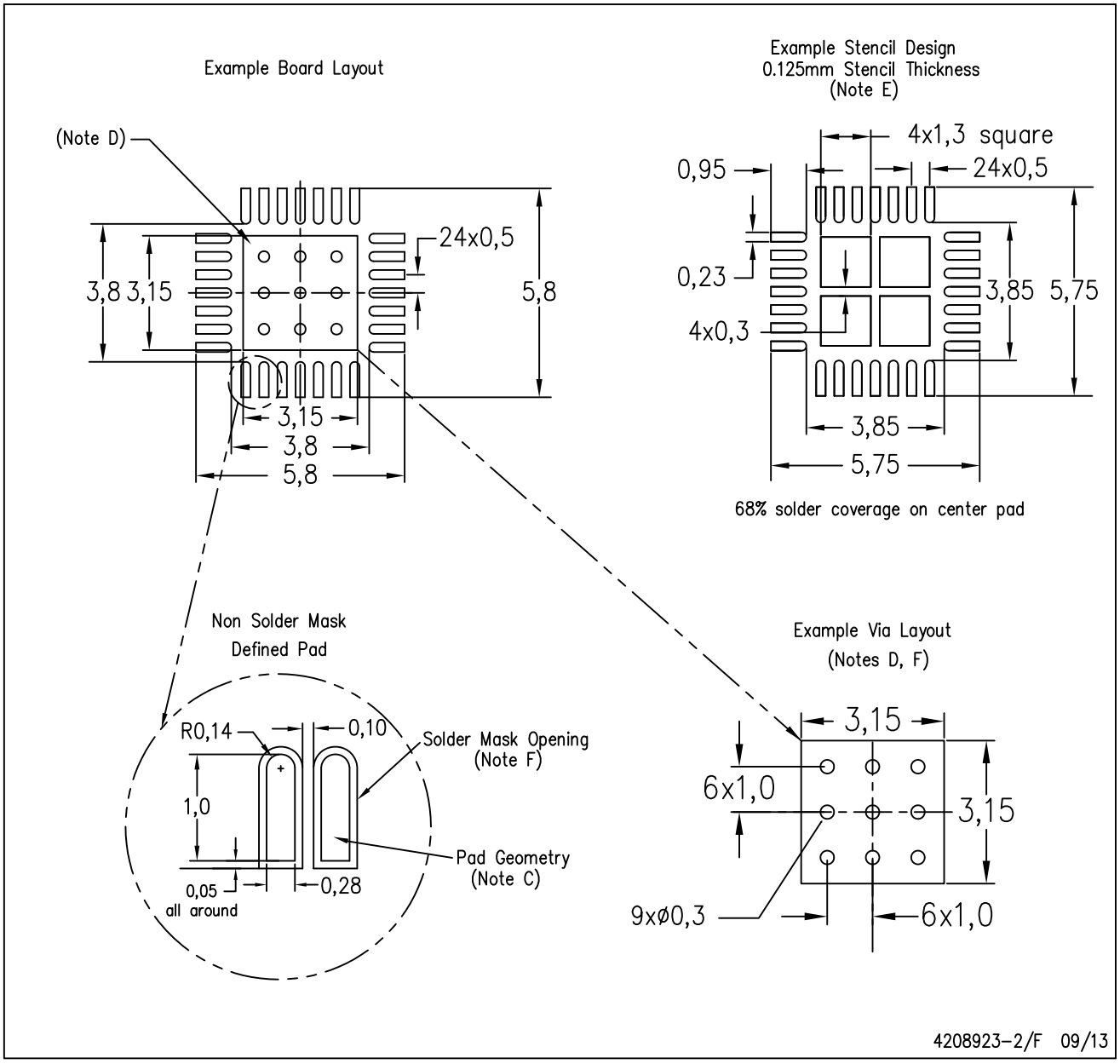
Bottom View

Exposed Thermal Pad Dimensions

4206358–2/L 05/15

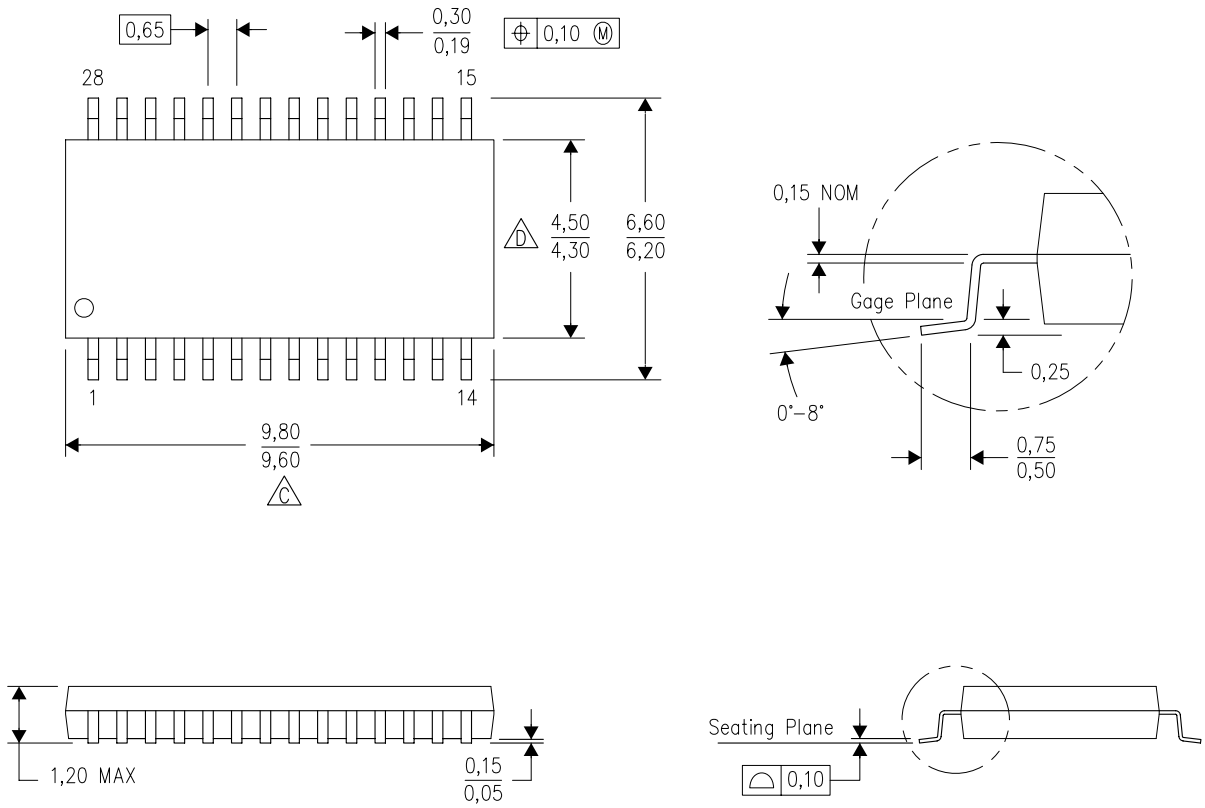
NOTE: All linear dimensions are in millimeters

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



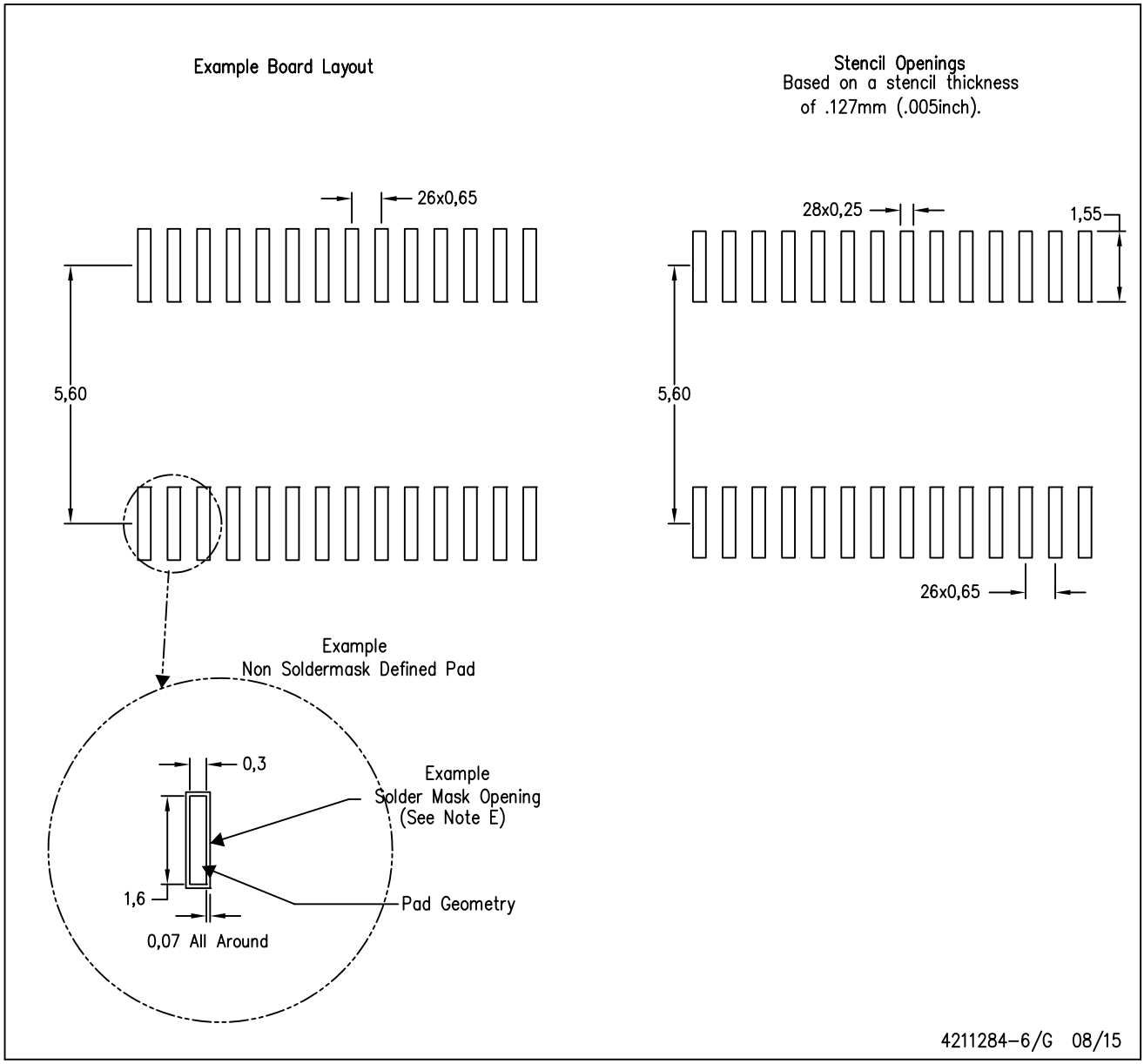
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



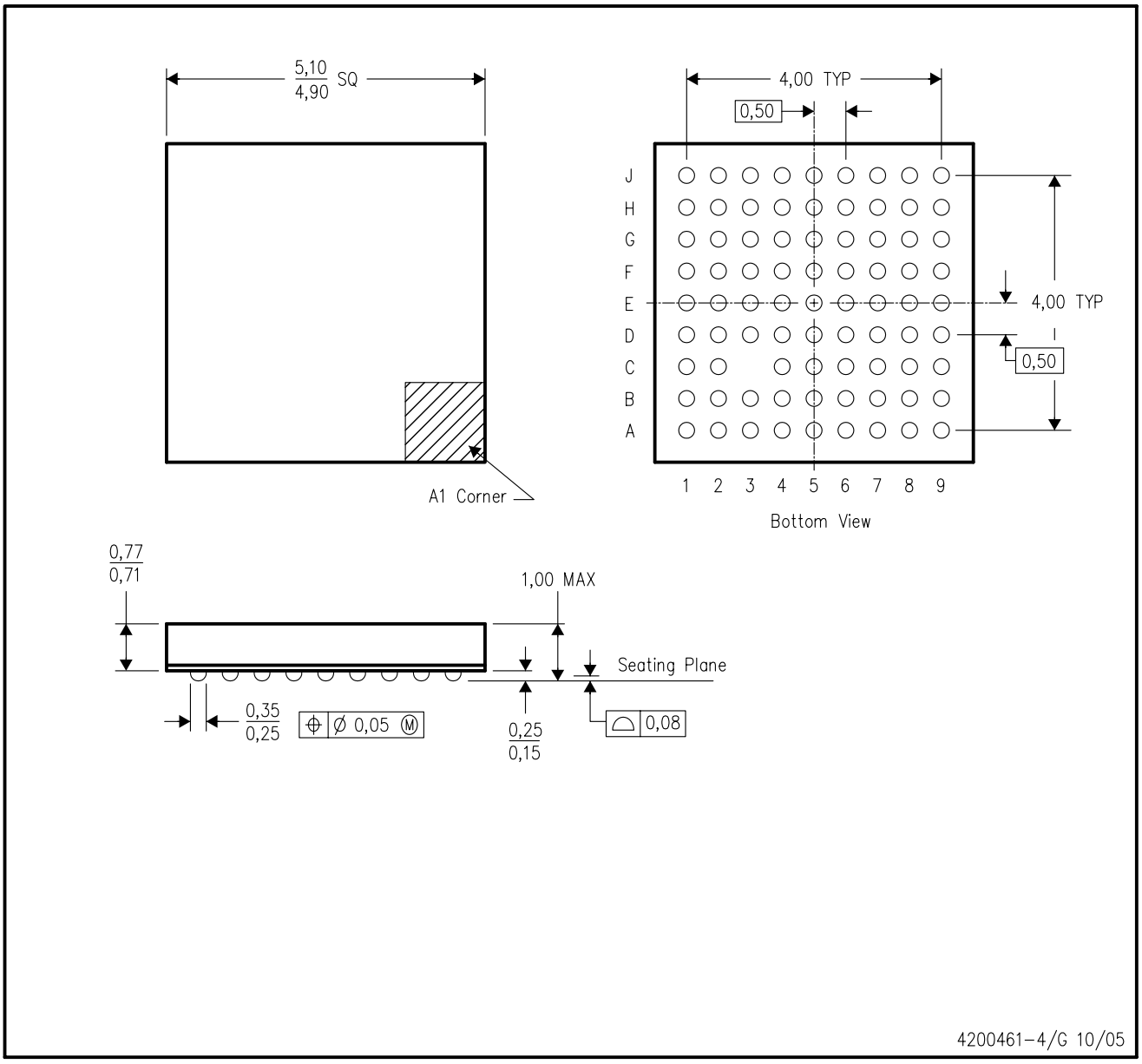
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225

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