Titanium FPGA Selector Guide

Titanium FPGAs are fabricated on a 16 nm process, delivering high performance with the lowest possible power and a small physical size. They feature the innovative Quantum® compute fabric that, with its enhanced compute capability, makes Titanium FPGAs ideal for embedded hardware acceleration applications. With a wide range of logic element (LE) densities from 35K to 1M, and compatibility with the Efinix RISC-V SoCs, they can help you turn a tiny chip into an accelerated embedded compute system.

Titanium Ordering Codes

You can use HSIO pairs for a various differential standards such as LVDS (1.5 Gbps), differential HSTL/SSTL, or MIPI RX and TX data/clock lanes (1.5 Gbps).

FPGA	LEs	RAM (Mbits)	RAM Blocks (10 Kb)	DSP Blocks	Package	Pins	HVIO	HSIO	PLLs	2.5G MIPI D-PHY	Hardened RISC-V Block	LPDDR 4/4x	Xcvr [2] Banks	PCIe®	25.8G Xcvr	Temp.	Speed Grade	Ordering Code
Ti35	36,176	1.53	153	93	FBGA	100[1]	–	61	3	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti35F100C3/3L/4/4L
																		Ti35F100S3F2 C3/3L/4/4L
																I	3, 3L	Ti35F100I3/3L
																		Ti35F100S3F2I3/3L
						225	23	140	4	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti35F225C3/3L/4/4L
																I	3, 3L	Ti35F225I3/3L
						256	27	142	4	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti35F256C3/3L/4/4L
																I	3, 3L	Ti35F256I3/3L
Ti60	62,016	2.6	256	160	WLCSP	64	–	34	2	–	–	–	–	–	–	C	3	Ti60W64C3
																I	3	Ti60W64I3
					FBGA	100[1]	–	61	3	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti60F100C3/3L/4/4L
																		Ti60F100S3F2 C3/3L/4/4L
																I	3, 3L	Ti60F100I3/3L
																		Ti60F100S3F2I3/3L
						225	23	140	4	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti60F225C3/3L/4/4L
																I	3, 3L	Ti60F225I3/3L
																Q	3	Ti60F225Q3
						256	27	142	4	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti60F256C3/3L/4/4L
																I	3, 3L	Ti60F256I3/3L
Ti85	83,232	6.18	604	300	FBGA	484	21	85	8	1 TX 1 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti85N484C3/3L/4/4L
																I		Ti85N484I3/3L/4/4L
						676	84	139	9	2 TX 2 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti85N676C3/3L/4/4L
																I		Ti85N676I3/3L/4/4L

FPGA	LEs	RAM (Mbits)	RAM Blocks (10 Kb)	DSP Blocks	Package	Pins	HVIO	HSIO	PLLs	2.5G MIPI D-PHY	Hardened RISC-V Block	LPDDR 4/4x	Xcvr [2] Banks	PCIe®	25.8G Xcvr	Temp.	Speed Grade	Ordering Code
Ti90	92,534	6.88	688	336	FBGA	361	20	110	8	2 TX 2 RX	–	x16	–	–	–	C	3, 3L, 4, 4L	Ti90J361C3/3L/4/4L
																I		Ti90J361I3/3L/4/4L
						400	74	200	8	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti90G400C3/3L/4/4L
																I		Ti90G400I3/3L/4/4L
						484	27	116	8	4 TX 4 RX	–	x32	–	–	–	C	3, 3L, 4, 4L	Ti90J484C3/3L/4/4L
																I		Ti90J484I3/3L/4/4L
																Q	3	Ti90J484Q3
						529	48	210	8	–	–	x32	–	–	–	C	3, 3L, 4, 4L	Ti90G529C3/3L/4/4L
																I		Ti90G529I3/3L/4/4L
Ti120	123,379	9.18	918	448	FBGA	361	20	110	8	2 TX 2 RX	–	x16	–	–	–	C	3, 3L, 4, 4L	Ti120J361C3/3L/4/4L
																I		Ti120J361I3/3L/4/4L
						400	74	200	8	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti120G400C3/3L/4/4L
																I		Ti120G400I3/3L/4/4L
						484	27	116	8	4 TX 4 RX	–	x32	–	–	–	C	3, 3L, 4, 4L	Ti120J484C3/3L/4/4L
																I		Ti120J484I3/3L/4/4L
																Q	3	Ti120J484Q3
						529	48	210	8	–	–	x32	–	–	–	C	3, 3L, 4, 4L	Ti120G529C3/3L/4/4L
																I		Ti120G529I3/3L/4/4L
Ti135	132,192	9.83	960	480	FBGA	484	21	85	8	1 TX 1 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti135N484C3/3L/4/4L
																I		Ti135N484I3/3L/4/4L
						676	84	139	9	2 TX 2 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti135N676C3/3L/4/4L
																I		Ti135N676I3/3L/4/4L
Ti165	162,800	12.1	1,182	590	FBGA	484	20	85	9	1 TX 1 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti165N484C3/3L/4/4L
																I		Ti165N484I3/3L/4/4L
						529	51	176	12	–	Quad Core	x32	–	–	–	C	3, 3L, 4, 4L	Ti165C529C3/3L/4/4L
																I		Ti165C529I3/3L/4/4L
						1,156	103	234	12	3 TX 3 RX	Quad Core	2 x32	up to 4	2x Gen4	–	C	3, 3L, 4, 4L	Ti165N1156C3/3L/4/4L
																I		Ti165N1156I3/3L/4/4L
Ti180	176,256	13.11	1,280	640	FBGA	361	20	110	8	2 TX 2 RX	–	x16	–	–	–	C	3, 3L, 4, 4L	Ti180J361C3/3L/4/4L
																I		Ti180J361I3/3L/4/4L
						400	74	200	8	–	–	–	–	–	–	C	3, 3L, 4, 4L	Ti180G400C3/3L/4/4L
																I		Ti180G400I3/3L/4/4L
						484[3]	54	190	8	2 TX 2 RX	–	x16	–	–	–	C	4	Ti180J484D1C4
																I	3	Ti180J484D1I3
							27	116	8	4 TX 4 RX	–	x32	–	–	–	C	3, 3L, 4, 4L	Ti180J484C3/3L/4/4L
																I		Ti180J484I3/3L/4/4L
																Q	3	Ti180J484Q3
						529	48	210	8	–	–	x32	–	–	–	C	3, 3L, 4, 4L	Ti180G529C3/3L/4/4L
																I		Ti180G529I3/3L/4/4L

FPGA	LEs	RAM (Mbits)	RAM Blocks (10 Kb)	DSP Blocks	Package	Pins	HVIO	HSIO	PLLs	2.5G MIPI D-PHY	Hardened RISC-V Block	LPDDR 4/4x	Xcvr [2] Banks	PCIe®	25.8G Xcvr	Temp.	Speed Grade	Ordering Code
Ti240	236,888	17.62	1,721	860	FBGA	484	20	85	9	1 TX 1 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti240N484C3/3L/4/4L
																I		Ti240N484I3/3L/4/4L
						529	51	176	12	–	Quad Core	x32	–	–	–	C	3, 3L, 4, 4L	Ti240C529C3/3L/4/4L
																I		Ti240C529I3/3L/4/4L
						1,156	103	234	12	3 TX 3 RX	Quad Core	2 x32	up to 4	2x Gen4	–	C	3, 3L, 4, 4L	Ti240N1156C3/3L/4/4L
																I		Ti240N1156I3/3L/4/4L
Ti375	370,137	27.53	2,688	1,344	FBGA	484	20	85	9	1 TX 1 RX	Quad Core	x32	up to 2	1x Gen4	–	C	3, 3L, 4, 4L	Ti375N484C3/3L/4/4L
																I		Ti375N484I3/3L/4/4L
						529	51	176	12	–	Quad Core	x32	–	–	–	C	3, 3L, 4, 4L	Ti375C529C3/3L/4/4L
																I		Ti375C529I3/3L/4/4L
						900	50	168	12	0 TX 2 RX	Quad Core	2 x32	up to 4	2x Gen4	–	C	3, 3L, 4, 4L	Ti375N900C3/3L/4/4L
																I		Ti375N900I3/3L/4/4L
						1,156	103	234	12	3 TX 3 RX	Quad Core	2 x32	up to 4	2x Gen4	–	C	3, 3L, 4, 4L	Ti375N1156C3/3L/4/4L
																I		Ti375N1156I3/3L/4/4L

1. The F100 pin package is available as a regular package as well as a SIP that incorporates SPI flash and HyperRAM in addition to the FPGA.
2. Each transceiver bank has 4 lanes. All banks support SGMII, 10GBase-KR, and PMA Direct. 1 bank supports PCIe.
3. The 484 pin package is a SIP that incorporates LPDDR DRAM in addition to the FPGA.

Package Dimensions

Package	Pitch (mm)	Dimensions (mm)
64-ball FBGA	0.4	3.5x3.4
100-ball FBGA	0.5	5.5x5.5
225-ball FBGA	0.65	10x10
256-ball FBGA	0.8	13x13
361-ball FBGA	0.65	13x13
400-ball FBGA	0.8	16x16
484-ball FBGA	0.8	18x18
529-ball FBGA	0.8	19x19
676-ball FBGA	0.8	22x22
900-ball FBGA	0.8	25x25
1156-ball FBGA	1.0	35x35

Example Ordering Code

Titanium FPGA — **Ti60 F 225 C 3**

Package Code
C, F, G, J, N: FBGA Package
W: Wafer-Level Chip-Scale Package

Number of Pins

System-In-Package
S3F2: HyperRAM and flash (Ti60F100)
D1: LPDDR4x SDRAM (Ti180J484)
Some ordering codes include extra characters to designate additional components in the package.

Speed Grade
3, 3L, 4, 4L (L is low power)
Higher numbers are faster

Operating Temperature
C: Commercial (T_j = 0° C to 85° C)
I: Industrial (T_j = -40° C to 100° C)
Q: Automotive (T_j = -40° C to 125° C)

Product Longevity

At Efinix we are committed to supplying our customers with a stable supply of supported products throughout their product life cycle. We are committed to supporting our Titanium family of FPGAs in customer designs until at least 2045. Contact your local sales representative for more information on product life cycles.

EFINIX®
www.efinixinc.com