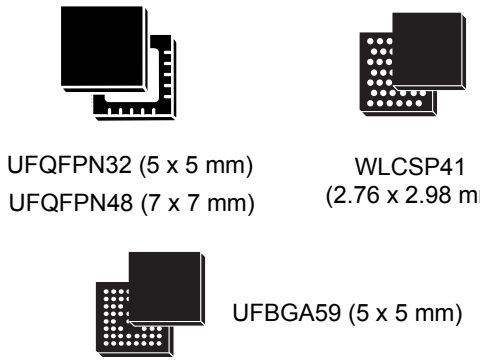
STM32WBA5xxx

Multiprotocol wireless 32-bit MCU Arm®-based Cortex®-M33 with TrustZone®, FPU, Bluetooth® LE and IEEE 802.15.4 radio solution

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Ultra-low power radio
  - 2.4 GHz radio
  - RF transceiver supporting Bluetooth® LE, IEEE 802.15.4-2015 PHY and MAC, supporting Thread, Matter and Zigbee®
  - RX sensitivity: -96 dBm (Bluetooth® LE at 1 Mbps), -97.5 dBm (IEEE 802.15.4 at 250 kbps)
  - Programmable output power, +10 dBm with 1 dB steps
  - Support for external PA
  - Isochronous channel (Auracast/Unicast), AOA/AOD, long range
  - Packet traffic arbitration
  - Integrated balun to reduce BOM
  - Single crystal operation
  - Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T66
- Bluetooth® LE
  - LE 2M
  - LE coded
  - Direction finding
  - LE power control
  - Isochronous channels
  - Extended and periodic advertising
  - LE secure connections
  - LE audio
  - Mesh networking
  - Core Specification 6.0
- Operating conditions:
  - 1.71 to 3.6 V power supply
  - -40 to 85/105°C temperature range



- Ultra-low power platform with FlexPowerControl
  - Autonomous peripherals with DMA, functional down to Stop 1 mode
  - 160 nA Standby mode (16 wake-up pins)
  - 0.9 µA Standby mode with 64-Kbyte SRAM
  - 6.5 µA Stop mode with 64-Kbyte SRAM
  - 23 µA/MHz Run mode at 3.3 V
  - Radio: Rx 4.4 mA / Tx at 0 dBm 5.2 mA
  - Embedded regulator LDO and SMPS step-down converter supporting switch on-the-fly and voltage scaling
- Core: Arm® 32-bit Cortex®-M33 CPU with TrustZone®, MPU, DSP, and FPU running at up to 100 MHz
- ART Accelerator: 8-Kbyte instruction cache allowing 0-wait-state execution from flash memory (frequency up to 100 MHz)
- Benchmarks
  - 410 CoreMark® (4.10 CoreMark/MHz)
- Real time clock (RTC) with hardware calendar, alarms, and calibration
- Clock sources
  - 32 MHz crystal oscillator
  - 32 kHz crystal oscillator (LSE)
  - Internal low-power 32 kHz (±5%) RC

  - Internal low frequency 32 kHz RC (500 ppm/°C)
  - Internal 16 MHz factory trimmed RC (±1%)
  - PLL for system clock, audio, and ADC
- Memories
  - 1 Mbyte flash memory with ECC, including 256 Kbytes with 100k cycles
  - 128-Kbyte SRAM, including 64 KB with parity check
  - 512-byte (32 rows) OTP
- Rich analog peripherals (independent supply)
  - 12-bit ADC 2.5 Msps, up to 16-bit with hardware oversampling
  - Two ultra-low power comparators
- Communication peripherals
  - One SAI (serial audio interface)
  - Three UARTs (ISO 7816, IrDA, modem)
  - Two SPIs
  - Two I2C Fm+ (1 Mbit/s), SMBus/PMBus®
- System peripherals
  - Touch sensing controller, up to 20 sensors, supporting touch key, linear, and rotary touch sensors
  - One 16-bit, advanced motor control timer
  - Three 16-bit timers
  - One 32-bit timer
  - Two low-power 16-bit timers (available in Stop mode)
  - Two Systick timers
  - Two watchdogs
  - 8-channel DMA controller, functional in Stop mode
- Security and cryptography
  - Arm® TrustZone® and securable I/Os, memories, and peripherals
  - Flexible life cycle scheme with RDP and password protected debug
  - Root of trust thanks to unique boot entry and secure hide protection area (HDP)
  - SFI (secure firmware installation) thanks to embedded RSS (root secure services)
  - Secure data storage with root hardware unique key (RHUK)
  - Secure firmware upgrade support with TF-M
  - Two AES co-processors, including one with DPA resistance
  - Public key accelerator, DPA resistant
  - HASH hardware accelerator
  - True random number generator, NIST SP800-90B compliant
  - 96-bit unique ID
  - Active tampers
  - CRC calculation unit
- General purpose input/output:
  - Up to 35 I/Os (most of them 5 V-tolerant) with interrupt capability
- Development support
  - Serial wire debug (SWD), JTAG
- ECOPACK2 compliant packages

Table 1. Device summary

Reference	Part numbers
STM32WBA52xx	STM32WBA52CE, STM32WBA52CG, STM32WBA52KE, STM32WBA52KG
STM32WBA54xx	STM32WBA54KG, STM32WBA54CG, STM32WBA54KE, STM32WBA54CE
STM32WBA55xx	STM32WBA55CG, STM32WBA55CE, STM32WBA55HG, STM32WBA55UG, STM32WBA55UE

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1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32WBA5xxx microcontrollers, based on Arm® [a]cores[b]. It must be read in conjunction with the reference manual (RM0493), available from the STMicroelectronics website *www.st.com*.

For information on the device errata with respect to the datasheet and reference manual refer to the STM32WBA5xxx errata sheet (ES0592), available from the STMicroelectronics website *www.st.com*.

For information on the Arm® Cortex®[c]-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available on the www.arm.com website.

For information on Bluetooth®, refer to www.bluetooth.com.

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2 Description

The STM32WBA5xxx multiprotocol wireless and ultra-low power devices embed a powerful and ultra-low power radio compliant with Bluetooth® LE (Low Energy). They operate at a frequency of up to 100 MHz.

The devices integrate a 2.4 GHz RADIO supporting Bluetooth LE.

The STM32WBA5xxx are based on a high-performance Arm Cortex-M33 32-bit RISC core, featuring a single-precision floating-point unit (FPU), supporting all the Arm single-precision data-processing instructions and all the data types. This core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (up to 1 Mbyte of flash memory and up to 128 Kbytes of SRAM), an extensive range of enhanced I/Os and peripherals connected to AHB and APB buses on the 32-bit multi-AHB bus matrix.

The devices offer security foundation compliant with the TBSA (trusted-based security architecture) requirements from Arm. It embeds the necessary security features to implement a secure boot, secure data storage, and secure firmware update. Besides these capabilities, the devices incorporate a secure firmware installation feature that allows the customer to secure the provisioning of the code during its production. A flexible life cycle is managed thanks to multiple levels readout protection and debug unlock with password.

Firmware hardware isolation is supported thanks to securable peripherals, memories and I/Os, and privilege configuration of peripherals and memories.

Several protection mechanisms are available for embedded flash memory and SRAM, namely readout and write protection, secure, and hide protection areas.

The devices embed several peripherals reinforcing security: a fast AES coprocessor, a secure AES coprocessor with DPA resistance and hardware unique key that can be shared by hardware with fast AES,a PKA (public key accelerator) with DPA resistance, a HASH hardware accelerator, and a true random number generator.

Active tamper detection and protection against transient perturbation attacks, is achieved thanks to several internal monitoring generating secret data erase in case of attack. This helps to fit the PCI requirements for point of sales applications.

Hardware semaphores enable the synchronization between software processes.

The devices offer one 12-bit ADC (2.5 Msps), two comparators, a low-power RTC, one 32-bit general-purpose timer, one 16-bit PWM timer for motor control, three 16-bit general-purpose timers, and two 16-bit low-power timers. They also feature standard and advanced communication interfaces, namely two I2Cs, two SPIs, one SAI, two USARTs, and one low-power UART. The feature set is product-dependent.

The STM32WBA5xxx operate in the -40 to 105°C (120°C junction) temperature range from a 1.71 to 3.6 V power supply.

The design of low-power applications is enabled by a comprehensive set of power-saving modes.

Many peripherals (including radio, communication, analog, and timer peripherals) can be functional and autonomous in Stop mode with direct memory access thanks to BAM (background autonomous mode) support.

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Some independent power supplies are supported, like an analog independent supply input for ADC and comparators, and radio dedicated supply inputs for the 2.4 GHz RADIO.

The STM32WBA5xxx devices offer three packages, up to 59 pins, with or without SMPS.

Table 2. STM32WBA52xx device features and peripheral counts

Feature		STM32 WBA52CG	STM32 WBA52KG	STM32 WBA52CE	STM32 WBA52KE
Flash memory density		1024 KB		512 KB	
SRAM density	SRAM1	64 KB		32 KB	
	SRAM2	64 KB			
Bluetooth LE		Yes			
802.15.4		No			
SMPS		No			
PTA		No			
External PA support		No			
BLE AoA, AoD support		No			
Real time clock (RTC)		Yes			
Backup registers		32 x 32 bits			
Timers	Advanced control	1 (16-bit)			
	General purpose	1 (32-bit) + 3 (16-bit)			
	Low power	2 (16-bit)			
	SysTick	2			
	Watchdog (independent, window)	2			
Communication interfaces	SPI	2			
	I2C	2			
	SAI	No			
	USART	2			
	LPUART	1			
Tamper pins (active tampers)(1)		5 (4)	3 (2)	5 (4)	3 (2)
Wake-up pins		15	8	15	8
GPIOs		35	20	35	20
Capacitive sensing (channels)		20	12	20	12
12-bit ADC		1 (9 channels)	1 (8 channels)	1 (9 channels)	1 (8 channels)
True random number generator		Yes			
Analog comparators		No			
SAES, AES		Yes			
Public key accelerator (PKA)		Yes			
HASH		Yes			

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Table 2. STM32WBA52xx device features and peripheral counts (continued)

Feature	STM32 WBA52CG	STM32 WBA52KG	STM32 WBA52CE	STM32 WBA52KE
Maximum CPU frequency	100 MHz			
Operating temperature	Ambient: -40 to 85°C and -40 to 105°C Junction: -40 to 105°C and -40 to 120°C			
Operating voltage	1.71 to 3.6 V			
Package	UFQFPN48	UFQFPN32	UFQFPN48	UFQFPN32

1. Active tampers in output sharing mode (one output shared by all inputs).

Table 3. STM32WBA54/55xx device features and peripheral counts

Feature		STM32WBA54KG	STM32WBA54KE	STM32WBA54CG	STM32WBA54CE	STM32WBA55CG	STM32WBA55CE	STM32WBA55UG	STM32WBA55UE	STM32WBA55HG
Flash memory density (Kbytes)		1024	512	1024	512	1024	512	1024	512	1024
SRAM density	SRAM1 (Kbytes)	64	32	64	32	64	32	64	32	64
	SRAM2 (Kbytes)	64								
Bluetooth LE		Yes								
802.15.4		Yes								
SMPS		No				Yes				
PTA		Yes								
External PA support		Yes								
BLE AoA, AoD support		Yes								
Real time clock (RTC)		Yes								
Backup registers		32 x 32-bit								
Timers	Advanced control	1 (16-bit)								
	General purpose	1 (32-bit) + 3 (16-bit)								
	Low power	2 (16-bit)								
	SysTick	2								
	Watchdog (independent, window)	2								
Communication interfaces	SPI	2								
	I2C	2								
	SAI	1								
	USART	2								
	LPUART	1								

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Table 3. STM32WBA54/55xx device features and peripheral counts (continued)

Feature	STM32WBA54KG	STM32WBA54KE	STM32WBA54CG	STM32WBA54CE	STM32WBA55CG	STM32WBA55CE	STM32WBA55UG	STM32WBA55UE	STM32WBA55HG
Tamper pins (active tampers)[1]	3 (2)		5 (4)		5 (4)		6 (5)		3 (2)
Wake-up pins	8		15		14		16		8
GPIOs	20		35		31		35		20
Capacitive sensing (channels)	12		21		16		21		12
12-bit ADC	1 (8 channels)		1 (9 channels)		1 (8 channels)		1 (10 channels)		1 (8 channels)
Analog comparator	2								
True random number generator	Yes								
SAES, AES	Yes								
Public key accelerator (PKA)	Yes								
HASH	Yes								
Maximum CPU frequency	100 MHz								
Operating temperature	Ambient:-40 to 85°C and -40 to 105°C Junction: -40 to 105°C and -40 to 120°C								
Operating voltage	1.71 to 3.6 V								
Package	UFQFPN32		UFQFPN48				UFBGA59		WLCSP41

1. Active tampers in output sharing mode (one output shared by all inputs).

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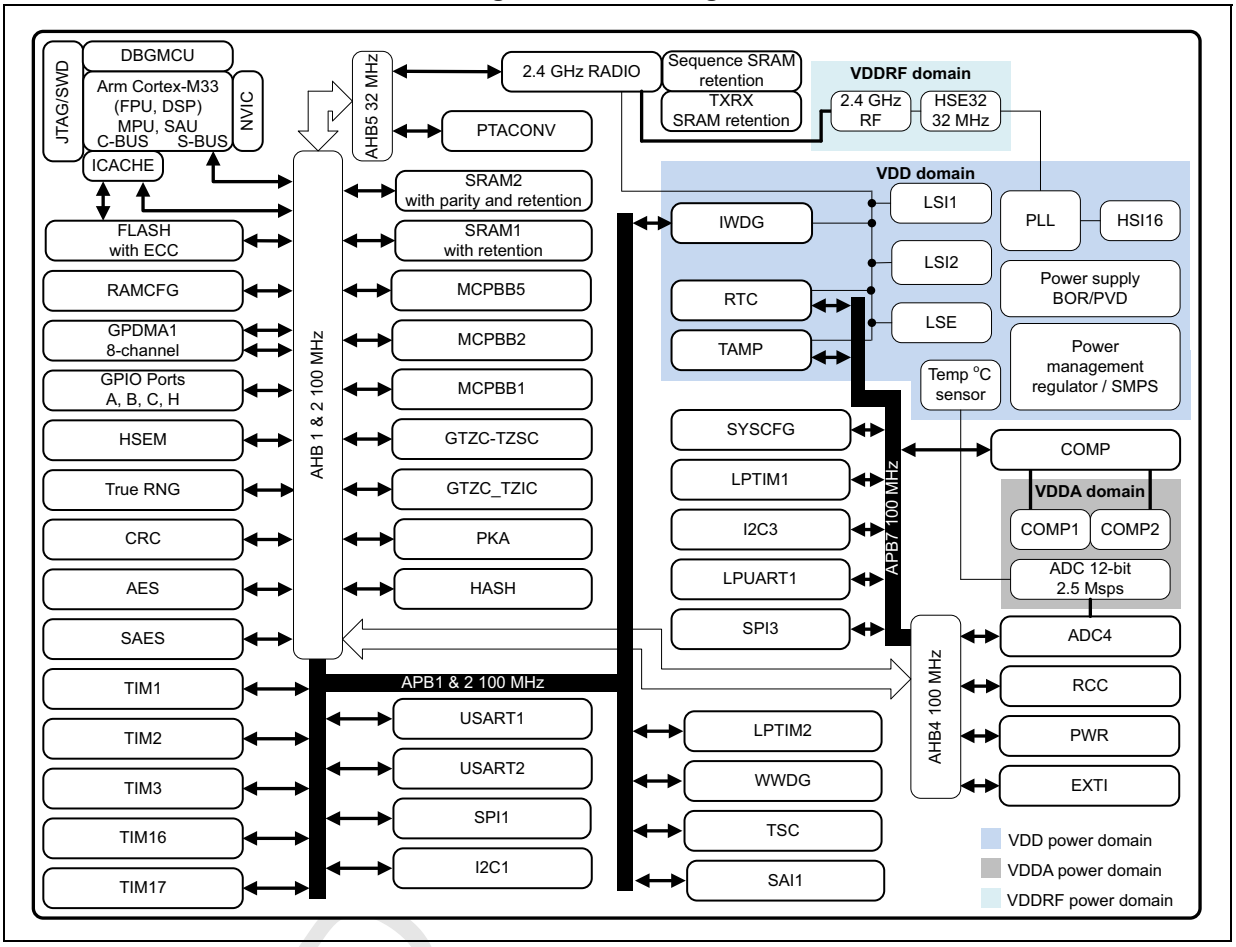
Figure 1 shows the general block diagram of the devices (some blocks are not available on some versions).

Figure 1. Block diagram



3 Functional overview

3.1 Arm Cortex-M33 core with TrustZone, MPU, DSP, and FPU

The Cortex-M33 with TrustZone, MPU, DSP and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and nonsecure states
- MPUs (memory protection units), supporting up to 16 regions for secure and nonsecure applications
- Configurable SAU (secure attribute unit) supporting up to eight memory regions as secure or nonsecure
- Floating-point arithmetic functionality, with support for single precision arithmetic

The processor supports a set of DSP instructions for efficient signal processing and complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB (S-AHB) bus: used for instruction fetch and data access to the memory-mapped SRAM, peripheral, and Vendor_SYS regions of the Armv8-M memory map.
- Code AHB (C-AHB) bus: used for instruction fetch and data access to the code region of the Armv8-M memory map.

3.2 ART Accelerator (ICACHE)

The ICACHE (instruction cache) is introduced on C-AHB code bus of Cortex-M33 processor to improve performance when fetching instruction (or data) from internal memories.

ICACHE offers the following features:

- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal flash memory
  - Master2 port performing refill requests to internal SRAMs
  - Second slave port dedicated to ICACHE registers access
- Close to 0 wait-states instructions/data access performance:
  - 0 wait-state on cache hit
  - Hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance

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  - Dual master ports to decouple internal flash memory and SRAM traffic, on fast and slow buses, respectively; also minimizing impact on interrupt latency
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of cacheable region beyond the code memory space, by means of address remapping logic enabling the definition of four regions
- Power consumption intrinsically reduced (more accesses to cache memory rather than to bigger main memories), even improved by configuring ICACHE as direct mapped (rather than the default two-ways set-associative mode)
- TrustZone security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The MPU is used to manage the CPU accesses to the memory and to prevent tasks to accidentally corrupt the memory or the resources used by other active tasks. This memory area is organized into up to 16 protected areas. The MPU regions and registers are banked across secure and nonsecure states.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to execute.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all the masters (CPU, GPDMA1) and the slaves (flash memory, SRAMs, AHB, and APB) peripherals. It also ensures a seamless and efficient operation even when several peripherals work simultaneously.

3.5 Embedded flash memory

The devices feature up to 1 Mbyte of embedded flash memory, available to store programs and data. This memory supports 10000 cycles, and up to 100000 cycles on 32 pages (256 Kbytes).

A 128-bit instruction prefetch is implemented and can optionally be enabled.

The flash memory contains up to 128 pages of 8 Kbytes, and embeds a 512-byte OTP (one time programmable) for user data.

The configuration of flexible protections is possible thanks to the option bytes:

- RDP (readout protection) to protect the whole memory, has four levels of protection available (see *Table 4* and *Table 5*):
  - Level 0: no readout protection

– Level 0.5: available only when TrustZone is enabled

All read/write operations (if no write protection is set) from/to the nonsecure flash memory are possible. The debug access to secure area is prohibited, that to nonsecure area remains possible.

– Level 1: memory readout protection

The flash memory cannot be read from or written to if either the debug features are connected or the boot in SRAM or bootloader are selected. If TrustZone is enabled, the nonsecure debug is possible and the boot in SRAM is not possible. Regressions from Level 1 to lower levels can be protected by password authentication.

– Level 2: chip readout protection

The debug features, the boot in RAM and the bootloader selection are disabled. A secure secret key can be configured in the secure options to allow the regression capability from Level 2 to Level 1. By default (key not configured), this Level 2 selection is irreversible and JTAG/SWD interfaces are disabled. If the secret key was previously configured in lower RDP levels, the device enables the RDP regression from Level 2 to Level 1 after password authentication through JTAG/SWD interface.

- Write protection (WRP) to protect areas against erasing and programming. Two areas can be selected with 8-Kbyte granularity.

Table 4. Access status versus protection level and execution modes when TZEN = 0

Area	RDP level	User execution (boot from flash memory)			Debug/boot from RAM/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	1	Yes	Yes	Yes	No	No	No(4)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory (2)	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(3)	1	Yes	Yes(4)	N/A	Yes	Yes(4)	N/A
	2	Yes	No	N/A	N/A	N/A	N/A
OTP	1	Yes	Yes(5)	N/A	Yes	Yes(5)	N/A
	2	Yes	Yes(5)	N/A	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A	No	No	N/A(6)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port, the boot from RAM, and the boot from system memory are disabled.
2. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
3. Option bytes are accessible only through the flash memory interface registers and OPSTRT bit.
4. The flash main memory is erased when the RDP option byte changes from level 1 to level 0.
5. OTP can be written only once.
6. The backup registers are erased when RDP changes from level 1 to level 0.
7. All SRAMs are erased when RDP changes from level 1 to level 0.

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Table 5. Access status versus protection level and execution modes when TZEN = 1

Area	RDP level	User execution (boot from flash memory)			Debug/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	0.5	Yes	Yes	Yes	Yes(2)	Yes(2)	Yes(2)
	1	Yes	Yes	Yes	No	No	No(5)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory (3)	0.5	Yes	No	No	Yes	No	No
	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(4)	0.5	Yes	Yes(5)	N/A	Yes	Yes (5)	N/A
	1	Yes	Yes(5)	N/A	Yes	Yes(5)	N/A
	2	Yes	No	N/A	N/A	N/A	N/A
OTP	0.5	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	1	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	2	Yes	Yes(6)	N/A	N/A	N/A	N/A
Backup registers	0.5	Yes	Yes	N/A	Yes(2)	Yes(2)	N/A(7)
	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	0.5	Yes	Yes	N/A	Yes(2)	Yes(2)	N/A(8)
	1	Yes	Yes	N/A	No	No	N/A(8)
	2	Yes	Yes	N/A	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port and the bootloader mode are disabled.
2. Depends upon TrustZone security access rights.
3. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
4. Option bytes are accessible only through the flash registers interface and OPSTRT bit.
5. The flash main memory is erased when the RDP option byte regresses from level 1 to level 0.
6. OTP can be written only once.
7. The backup registers are erased when RDP changes from level 1 to level 0.5 or level 0.
8. All SRAMs are erased when RDP changes from level 1 to level 0.5 or level 0.

The whole nonvolatile memory embeds the ECC (error correction code) feature supporting:

- single-error detection and correction
- double-error detection
- ECC fail address report

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3.5.1 Flash memory protections when TrustZone is activated

When the TrustZone security is enabled through option bytes, the whole flash memory is secure after reset and the following protections are available:

- Non volatile watermark-based secure flash memory area

  The secure area can be accessed only in Secure mode. One area can be selected with a page granularity.
- Secure hide protection area (HDP)

  It is part of the flash memory secure area and can be protected to deny access to any data read, write, and instruction fetch. For example, a software code in the secure flash memory hide protection area can be executed only once, and deny any further access to this area until the next system reset. One area can be selected at the beginning of the secure area.
- Volatile block-based secure flash memory area

  Each page can be programmed on-the-fly as secure or nonsecure.

3.5.2 Flash memory privilege protection

Each flash memory page can be programmed on-the-fly as privileged or unprivileged.

3.6 Embedded SRAMs

SRAM1 and SRAM2 are the main SRAMs embedded in the devices, each with specific features. Both can be used for peripherals background autonomous mode (BAM).

These SRAMs can be powered down in Stop mode to reduce consumption:

- SRAM1: one up to 64-Kbyte block, can be retained in Standby mode
- SRAM2: one 64-Kbyte block with parity, can be retained in Standby mode.

3.6.1 SRAMs TrustZone security

When TrustZone security is enabled, SRAMs are secure after reset. SRAM1 and SRAM2 can be programmed as secure or nonsecure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes.

3.6.2 SRAMs privilege protection

The SRAM1 and SRAM2 can be programmed as privileged or non-privileged by blocks, using the MPCBB. The granularity of SRAM block-based privilege is a page of 512 bytes.

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3.7 Boot modes

At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx[24:0] (x = 0, 1), and SECBOOTADD0[24:0] option bytes are used to select the boot memory address. This includes:

- Boot from any address in user flash memory
- Boot from system memory bootloader
- Boot from any address in embedded SRAM
- Boot from RSS (root security services)

The BOOT0 value comes from the PH3-BOOT0 pin or from an option bit, depending upon the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory, programmed by ST during production. It is used to program the flash memory by using USART, I^2C or SPI in device mode.

The bootloader is available on all devices. Refer to AN2606 *STM32 microcontroller system memory boot mode*, available on *www.st.com*, for more details.

The RSS are embedded in the flash memory area named secure information block, programmed during ST production. For example, the RSS enables the SFI (secure firmware installation), thanks to the RSSe (RSS extension firmware).

This feature allows the customers to produce the confidentiality of the firmware to be provisioned into the STM32, when production is subcontracted to untrusted third party.

The RSS is available on all devices, after enabling the TrustZone through the TZEN option bit. Refer to AN4992 *STM32 MCUs secure firmware install (SFI) overview*, available on *www.st.com*, for more details.

Refer to *Table 6* and *Table 7*, respectively, for boot modes with TrustZone disabled and enabled.

Table 6. Boot modes when TrustZone is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x08000 000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF8 8000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF8 8000

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in the secure area. The SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit, allowing to boot always at the address selected by SECBOOTADD0[24:0] option bytes. All other boot options are ignored.

Table 7. Boot modes when TrustZone is enabled (TZEN = 1)

BOOT_LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	-	1	1	0	N/A	RSS	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	0	-	0	0	N/A	RSS	RSS: 0x0FF8 0000
	-	-	-	≠0	N/A	RSS	RSS: 0x0FF8 0000
1	-	-	-	-	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000

The boot address option bytes allow any boot memory address to be programmed. The allowed address space depends on the flash memory RDP level.

If the programmed boot memory address is out of the allowed memory mapped area when RDP level is 0.5 or higher, the default boot address is forced either in secure or nonsecure flash memory, depending on TrustZone security option, as detailed in *Table 8*.

Table 8. Boot space versus RDP protection

RDP	TZEN = 1	TZEN = 0
0	Any boot address	Any boot address
0.5	Boot address only in RSS or secure flash memory: 0x0C00 0000 - 0x0C0F FFFF. Otherwise, forced boot address is 0x0FF8 0000	N/A
1		Any boot address
2		Boot address only in flash memory: 0x0800 0000 - 0x080F FFFF. Otherwise, forced boot address is 0x0800 0000

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3.8 Global TrustZone controller (GTZC)

GTZC is used to configure TrustZone and privileged attributes within the full system.

The GTZC includes different sub-blocks:

- **TZSC**: TrustZone security controller

  This sub-block defines the secure/privilege state of slave/master peripherals. The TZSC block informs some peripherals (such as RCC or GPIO) about the secure status of each securable peripheral.
- **TZIC**: TrustZone illegal access controller

  This sub-block gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- **MPCBB**: block-based memory protection controller

  This sub-block controls secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral configures the internal RAM in a TrustZone system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Independent 32-bit AHB interfaces for TZSC, TZIC and MPCBB
- Secure and nonsecure access supported for privileged/unprivileged part of TZSC
- Set of registers to define product security settings:
  - Secure/privilege access mode for securable peripherals
  - Secure/privilege access mode for securable memories
  - Illegal access interrupt notification

3.9 TrustZone security architecture

The security architecture is based on Arm TrustZone with the Armv8-M main extension.

The TZEN option bit in the FLASH_OPTR register activates the TrustZone security.

When TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) define the access permissions based on secure and nonsecure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: provides a first memory partition as nonsecure or nonsecure callable attributes. It is then combined with the results from the SAU security attribution, and the higher security state is selected.

Based on IDAU security attribution, the flash memory, system SRAM and peripheral memory space is aliased twice for secure and nonsecure states.

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Table 9 shows an example of typical SAU regions configuration based on IDAU regions.

Table 9. Example of memory map security attribution versus SAU configuration regions

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
Reserved	0x0000 0000 0x07FF FFFF	Nonsecure	Secure or Nonsecure or Nonsecure callable	
Code flash memory and SRAM	0x0800 0000 0x0BFF FFFF	Nonsecure		
	0x0C00 0000 0x0FFF FFFF	Nonsecure callable	Secure or NSC	
Reserved	0x1000 0000 0x17FF FFFF	Nonsecure	Nonsecure	
	0x1800 0000 0x1FFF FFFF			
SRAM	0x2000 0000 0x2FFF FFFF	Nonsecure		
	0x3000_0000 0x3FFF FFFF	Nonsecure callable	Secure or Nonsecure callable	
Peripherals	0x4000 0000 0x4FFF FFFF	Nonsecure		
	0x5000 0000 0x5FFF FFFF	Nonsecure callable	Secure or Nonsecure callable	
Reserved	0x6000 0000 0xDFFF FFFF	Nonsecure	Secure or Nonsecure or Nonsecure callable	

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3.9.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be securable or TrustZone-aware:

- Securable: peripheral protected by an AHB/APB firewall gate controlled from TZSC to define security properties.
- TrustZone-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone behavior, such as a subset of registers being secure.

3.9.2 Default TrustZone security state

The default system security state is detailed below:

- CPU: Cortex-M33 is in secure state after reset. The boot address must be in secure area.
- Memory map: SAU is fully secure after reset. Consequently, all memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - Flash memory security area is defined by watermark user options.
  - Flash memory block based area is nonsecure after reset.

- SRAMs: all are secure after reset, MPCBB is secure.
- Peripherals
  - Securable peripherals are nonsecure after reset.
  - TrustZone-aware peripherals are nonsecure after reset.
- All GPIOs are secure after reset.
- Interrupts (NVIC): all interrupts are secure after reset. NVIC is banked for secure and nonsecure state.
- TZIC: all illegal access interrupts are disabled after reset.

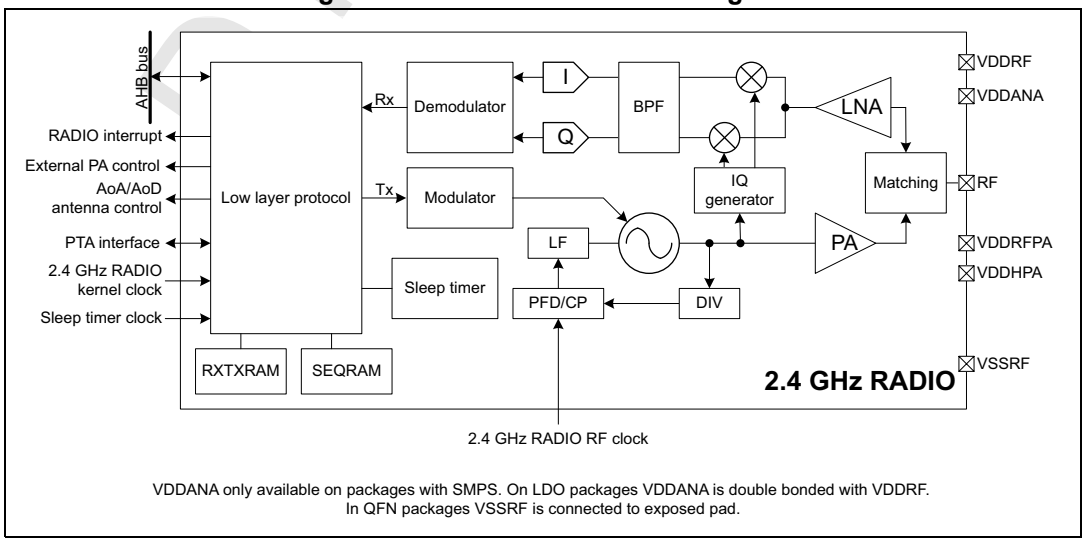
3.10 2.4 GHz RADIO

The 2.4 GHz RADIO is ultra-low power, operating in the 2.4 GHz ISM band. It provides Bluetooth LE 1 Mbps coded, 1 Mbps and 2 Mbps non-coded GFSK, and IEEE802.15.4 125 kbps and 250 kbps modulation. It is compliant with the Bluetooth® LE, Zigbee, Thread, specifications and radio regulations including ETSI EN 300 328, EN 300 440, EN 301 489-17, ARIB STD-T66, FCC CFR47 part 15 section 15.205, 15.209, 15.247 and 15.249, IC RSS-139 and RSS-210.

The 2.4 GHz RADIO supports the following features:

- Radio protocol:
  - Bluetooth LE
  - IEEE802.15.4
  - Concurrent mode
- Bluetooth AoA/AoD
- External PA support
- Packet traffic arbitration

Figure 2. 2.4 GHz RADIO block diagram



3.11 PTA interface

The PTA interface enables packet traffic arbitration with other connectivity devices, such as WiFi®. Its main features are:

- based on IEEE802.15.2 standard
- supports both grant and deny signaling
- supports from 1- up to 4-wire protocols
- programmable transmit receive PTA_STATUS polarity
- programmable priority polarity
- programmable grant polarity
- programmable active polarity
- programmable PTA_ACTIVE timing
- programmable PTA_STATUS time multiplexed priority timing.
- programmable transmit packet abort

3.12 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE})
  - V_{DD} and backup domain
  - Analog domain (V_{DDA})
  - SMPS power stage (V_{DDSMPS}, available only on SMPS packages)
  - V_{DDRF} for 2.4 GHz RADIO
- System supply voltage regulation
  - SMPS step-down converter
  - Voltage regulator (LDO)
- Power supply supervision
  - BOR monitor
  - PVD monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- TrustZone security and privilege protection

3.12.1 Power supply schemes

The devices require a 1.71 to 3.6 V V_{DD} operating voltage supply. Independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 to 3.6 V (functionality guaranteed down to V_{BORx} minimum value)

  External power supply for the I/Os, the internal regulator, the system analog such as reset, power management, and internal clocks and the backup domain. It is provided externally through the VDD pins. VDDRF must be connected to the same supply used

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for VDD.

- V_{DDA} = 1.62 to 3.6 V
  External analog power supply for ADC. The voltage level is independent from the V_{DD} voltage and must be connected to VDD (preferably) or to VSS pin when this peripheral is not used.
- V_{DDSMPS} = 1.71 to 3.6 V
  External power supply for the SMPS step down converter. It is provided externally through VDDSMPS supply pin and must be connected to the same supply as V_{DD}.
- V_{LXSMPS} is the switched SMPS step down converter output.

Note: The SMPS power supply pins are available only on packages with SMPS step-down converter option.

- V_{DDRF} = 1.71 to 3.6 V
  External power supply for the 2.4 GHz RADIO, it must be connected to the same supply used for VDD.
- V_{DDANA} = 0 to 3.6 V (must be ≥ 1.2 V for 2.4 GHz RADIO operation)
  External power supply for the 2.4 GHz RADIO, it can be connected to V_{DD11}. This supply must be equal or lower than V_{DDRF}.

Note: VDDANA pin is available only on packages with SMPS step-down converter option.

- V_{DDRFPA} = 0 to 3.6 V (must be ≥ 1.2 V for 2.4 GHz RADIO operation)
  External power supply for the 2.4 GHz RADIO and power amplifier regulator. The maximum reachable transmit output power is determined by V_{DDRFPA} supply level. This supply must be equal or lower than V_{DDRF}.

The devices embed two regulators: one LDO and one SMPS in parallel to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, 2.4 GHz RADIO, and embedded flash memory. The LDO generates this voltage on VCAP pin connected to an external capacitor of 4.7 µF (typical). The SMPS generates this voltage on VDD11 pin, with a total external capacitor of 4.7 µF (typical).

Both regulators can provide two different voltages (voltage scaling), and can operate in Stop modes.

It is possible to switch from SMPS to LDO and vice-versa on-the-fly.

The VDDHPA pin is provided to connect to an external capacitor (typical value 470 nF).

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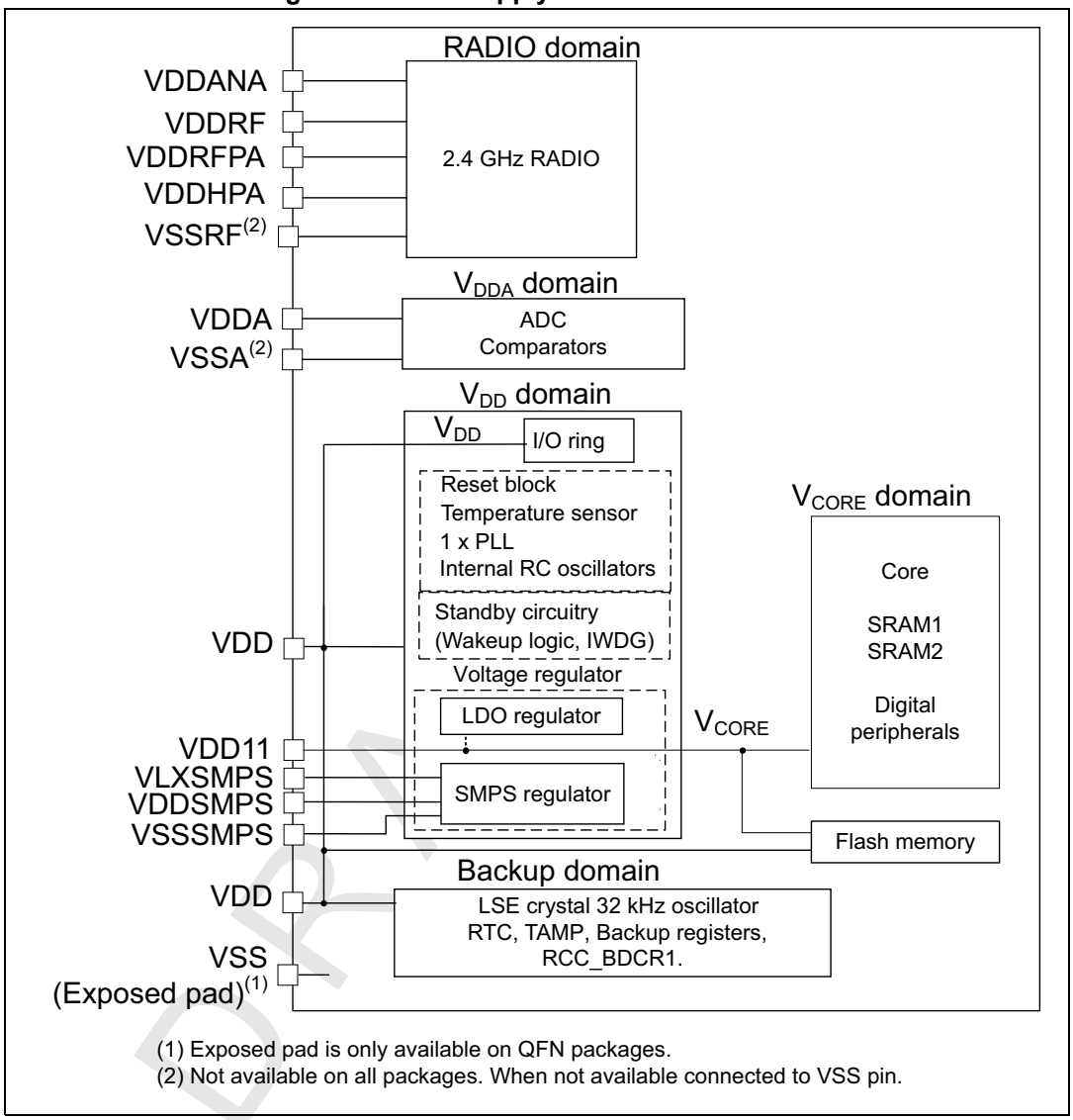
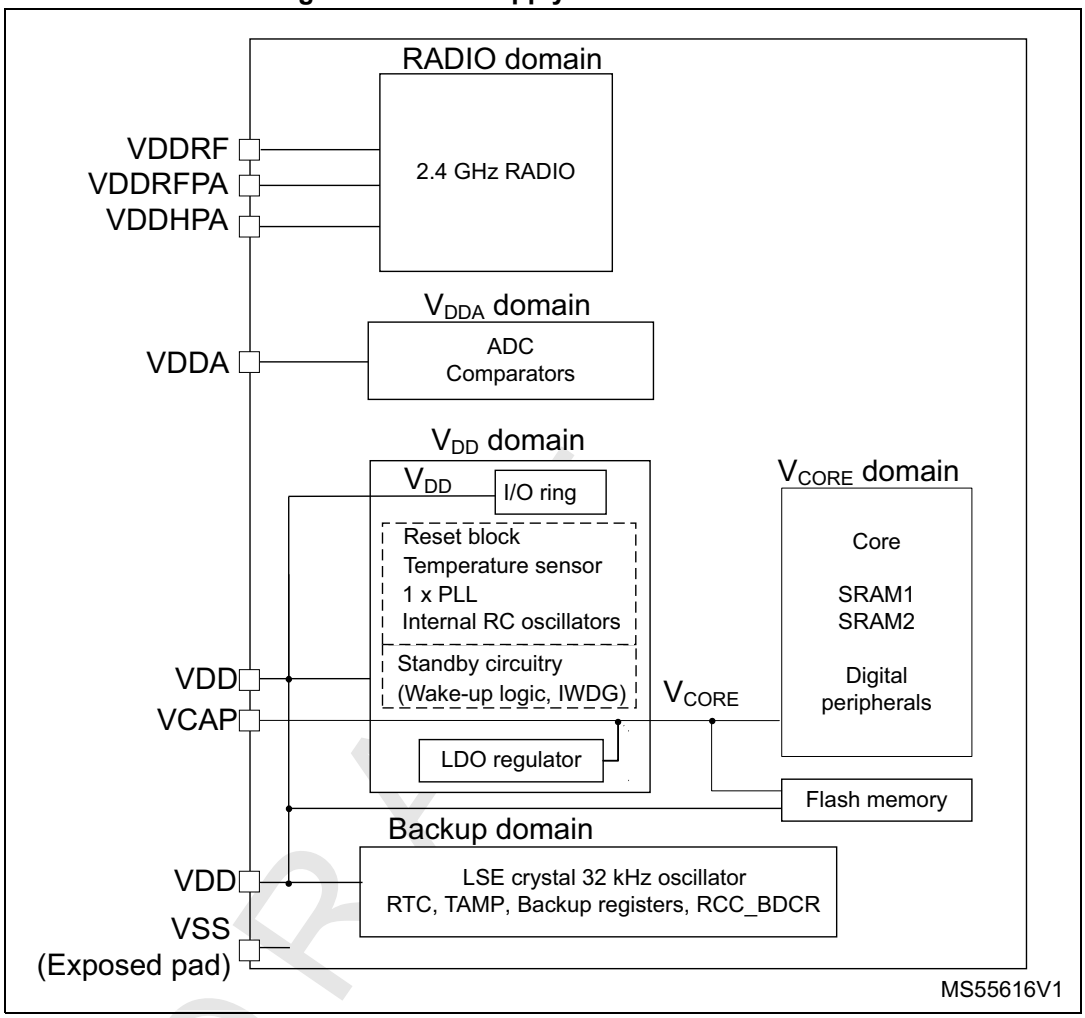
Figure 3. Power supply overview with SMPS



Caution: When SMPS devices are used in an LDO application, without inductor between VLXSMPS and VDD11, VDDSMPS and VLXSMPS must be connected to ground.

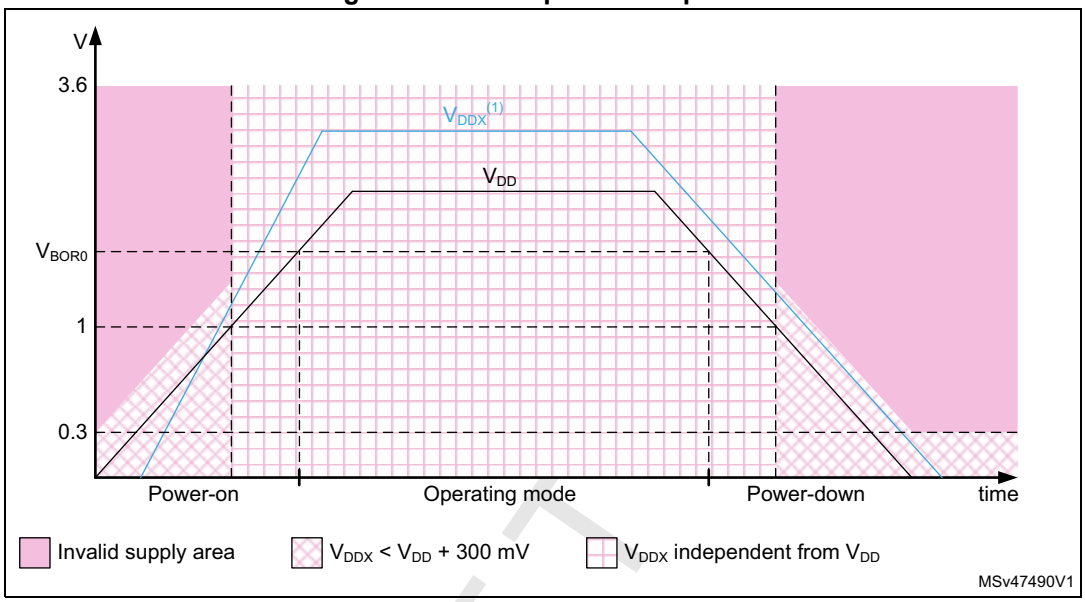
Figure 4. Power supply overview with LDO



During power-up and power-down phases, respect the following requirements:

- When V_{DD} is below 1 V, other power supplies (namely V_{DDA}) must remain below V_{DD} + 300 mV.
- When V_{DD} is equal to or above 1 V, other power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up/down sequence



1. V_{DDX} refers to power supply V_{DDA}.

3.12.2 Power supply supervisor

The devices have an integrated ultra-low power BOR (brownout reset) active in all modes. The BOR ensures proper operation after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded PVD (programmable voltage detector) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below and/or rises above the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 1 (V_{CORE} = 1.2 V) with CPU and peripherals running at up to 100 MHz
- Range 2 (V_{CORE} = 0.9 V) with CPU and peripherals running at up to 16 MHz

Low-power modes

The devices support different low-power modes to achieve the best compromise between low-power consumption, startup time, available peripherals, and available wake-up sources.

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Table 10. Operating modes overview

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	Range 2					All except 2.4 GHz RADIO	
Sleep	Range 1	No	ON	ON[4]	Any	All	Any interrupt or event
	Range 2					All except 2.4 GHz RADIO	
Stop 0	Range 1	No	OFF	ON[5]	LSE LSI [6]	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4[7] (temperature sensor), USARTx (x = 1, 2)[8], LPUART1, SPIx (x = 1, 2)[9], I2Cx (x = 1, 2)[10], LPTIMx (x = 1, 2)[11], GPIO, GPDMA1[12], 2.4 GHz RADIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 (temperature sensor), USARTx (x = 1, 2), LPUART1, SPIx (x = 1, 2), I2Cx (x = 1, 2), LPTIMx (x = 1, 2), GPDMA1, 2.4 GHz RADIO
	Range 2					All from Stop 0 range 1 except 2.4 GHz RADIO	
Stop 1[13]	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 and temperature sensor), USARTx (x = 1, 2), LPUART1, SPIx (x = 1, 2), I2Cx (x = 1, 2), LPTIMx (x = 1, 2), GPIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 and temperature sensor, USARTx (x = 1, 2), LPUART1, SPIx (x = 1, 2), I2Cx (x = 1, 2), LPTIMx (x = 1, 2)

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Table 10. Operating modes overview (continued)

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Standby retention	LPR	Powered off	OFF	ON[5]	LSE LSI	BOR, RTC, TAMP, IWDG, SLEEP_TIMER All other peripherals are powered off. I/O configuration can be retained, floating, pull-up or pull-down.	Reset pin, WKUPx (x = 1...8), BOR, RTC, TAMP, IWDG, SLEEP_TIMER
Standby	OFF			Powered off		All from mode Standby retention, except SLEEP_TIMER	

1. LPR means that the main regulator is OFF and the low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1 and SRAM2 clocks can be gated on or off independently.
5. The SRAM can be individually powered off to save power consumption.
6. HSI16 can be temporary enabled upon peripheral request, for autonomous functions with DMA or wake-up from Stop event detections.
7. The ADC conversion is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on conversion events.
8. U(S)ART and LPUART transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
9. SPI transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
10. I2C transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
11. LPTIM is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on all events.
12. GPDMA is functional and autonomous in Stop 0 mode, and can generate a wake-up interrupt on events.
13. Active peripherals ADC, U(S)ART, LPUART, SPI, I2C, and LPTIM, can generate bus clock request and/or a wake-up interrupt on event.

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By default, the microcontroller is in Run mode after a system or a power on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt or event occurs.

- **Stop 0 and Stop 1**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the V_{CORE} domain are stopped, the PLL, the HSI16, and the HSE32 crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC, TAMP, IWDG and SLEEP_TIMER can remain active.

  Some peripherals are autonomous and can operate in Stop mode by requesting their kernel clock and their bus clock when needed, in order to transfer data with DMA Stop 0 modes will be entered. Refer to *PWR background autonomous mode (BAM)* for more details. In Stop modes the bus clocks when requested use HSI16.

  Stop 0 offer the largest number of active peripherals, with or without DMA, and wake-up sources, a smaller wake-up time but a higher consumption than Stop 1.

  In Stop 0 mode, the main regulator remains ON, allowing a very fast wake-up time, but with much higher power consumption.

  Stop 1 is the lowest power mode with full retention, but the functional peripherals and sources of wake-up are reduced.

  The BOR can be configured in ultra-low power mode to further reduce power consumption during Stop 1 mode.

  The system clock when exiting from Stop 0 or Stop 1 modes is HSI16.

- **Standby retention and Standby**

  The Standby mode is used to achieve the lowest power consumption. The internal regulator is switched off so that the V_{CORE} domain is powered off. The PLL, the HSI16 and the HSE32 crystal oscillators are also switched off. The LSE or LSI is still running.

  The RTC and IWDG can remain active.

  The BOR always remains active in Standby mode.

  The BOR can be configured in ultra-low power mode to further reduce power consumption during Standby mode.

  The state of each I/O during Standby mode can be retained with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAMs and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the full SRAM1 and/or SRAM2 can be retained in Standby mode, supplied by the low-power regulator (Standby with RAM retention mode). Also optionally the 2.4 GHz RADIO can be retained in Standby mode, supplied by the low-power regulator (Standby with 2.4 GHz RADIO retention mode).

  The device exits Standby modes when an external reset (NRST pin), an IWDG event or reset, WKUP pin event (configurable rising or falling edge), an RTC event occurs (alarm, periodic wake-up, timestamp), or a tamper detection. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  When in Standby with 2.4 GHz RADIO retention mode also the SLEEP_TIMER can exit the device from Standby mode.

  The system clock after wake-up is HSI16.

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PWR background autonomous mode (BAM)

The devices support BAM (background autonomous mode), that allows peripherals to be functional and autonomous in Stop mode (Stop 0 and Stop 1 modes), so without any software running.

In Stop 0 modes, the autonomous peripherals are the following: ADC4, LPTIMx (x = 1, 2), U(S)ARTx (x = 1, 2), LPUART1, SPIx (x = 1, 2), I2Cx (x = 1, 2), 2.4 GHz RADIO, and GPDMA1. In this mode the GPDMA1 can be used to transfer data or control peripherals and access SRAM1 and SRAM2. The ADC4 can also be used to measure temperature. The 2.4 GHz RADIO is autonomous only in Stop 0 range 1.

In Stop 1 mode, the autonomous peripherals are the following: ADC4, LPTIMx (x = 1, 2), U(S)ARTx (x = 1, 2), LPUART1, SPIx (x = 1, 2), I2Cx (x = 1, 2). These peripherals can request a transition to Stop 0 mode allowing then data transfers with GPDMA1.

Those peripherals support the features detailed below:

- Functionality in Stop mode thanks to its own independent clock (named kernel clock) request capability: the peripheral kernel clock is automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it.
- DMA transfers supported in Stop 0 mode thanks to system clock request capability: the system clock (HSI16) automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it. When the system clock is requested by an autonomous peripheral, Stop 0 mode is automatically entered and the system clock is woken up and distributed to all peripherals enabled in the RCC. This allows the DMA to access the enabled SRAM, and any enabled peripheral register (for instance GPIO registers). When no peripheral requests its bus clock Stop 1 mode is automatically re-entered when Stop 1 mode selected as low-power mode.
- Automatic start of the peripheral thanks to hardware synchronous or asynchronous triggers (such as I/Os edge detection and low-power timer event).
- Wake-up from Stop mode with peripheral interrupt.

The GPDMA is fully functional and the linked-list is updated in Stop 0 mode, allowing the different DMA transfers to be linked without any CPU wake-up. This can be used to chain different peripherals transfers, or to write peripherals registers, to change their configuration while remaining in Stop 0 mode.

The DMA transfers from memory to memory can be started by hardware synchronous or asynchronous triggers, and the DMA transfers between peripherals and memories can also be gated by those triggers.

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Here below some use-cases that can be done while remaining in Stop mode:

- A/D conversion triggered by a low-power timer (or any other trigger)
  - wake-up from Stop mode on analog watchdog if the A/D conversion result is out of programmed thresholds
  - wake-up from Stop mode on DMA buffer event
- I^2C slave reception or transmission, SPI reception, UART/LPUART reception
  - wake-up at the end of peripheral transfer or on DMA buffer event
- I^2C master transfer, SPI transmission, UART/LPUART transmission, triggered by a low-power timer (or any other trigger):
  - example: sensor periodic read
  - wake-up at the end of peripheral transfer or on DMA buffer event
- Bridges between peripherals
  - example: ADC converted data transferred by communication peripherals
- Data transfer from/to GPIO to/from SRAM for:
  - controlling external components
  - implementing data transmission and reception protocols

Table 11. Functionalities depending on the working mode(1)

Peripheral	Run		Sleep		Stop 0			Stop 1		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
CPU	Y		R		R		-	R	-	-	-	-	-
Flash memory	O(2)		O(2)		R		-	R	-	R	-	R	-
SRAM1	O		O		O(3)		-	O(3)	-	O(3)	-	O(3)	-
SRAM2	O		O		O(3)		O(4)	O(3)		O(3)	-	O(3)	-
Backup registers	O		O		O		-	R	-	R	-	R	-
ICACHE	O		R		R		-	R	-	-	-	-	-
2.4 GHz RADIO	O	R	O	R	O	R	O	R	-	-	-	-	-
2.4 GHz RADIO SRAM	O	R	O	R	O	R	-	R	-	R	-	-	-
SLEEP_TIMER	O		O		O		O	O	O	O	O	-	-
BOR	Y		Y		Y		Y	Y	Y	Y	Y	Y	Y
PVD	O		O		O		O	O	O	-	-	-	-
HSI16	O		O		O(5)		-	O(5)	-	-	-	-	-
HSE32	O		O		O(6)	-	-	-	-	-	-	-	-
LSI	O		O		O		-	O	-	O	-	O	-
LSE	O		O		O		-	O	-	O	-	O	-
HSECSS	O		O		O	-	O	-	-	-	-	-	-

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Table 11. Functionalities depending on the working mode[1] (continued)

Peripheral	Run		Sleep		Stop 0			Stop 1		Standby retention		Standby	
	Range 1	Range 2	Range 1	Range 2	Range 1	Range 2	Wake-up capability	-	Wake-up capability	-	Wake-up capability	-	Wake-up capability
LSECSS	O		O		O		O	O	O	O	O	O	O
IWDG	O		O		O		O	O	O	O	O	O	O
RTC	O		O		O		O	O	O	O	O	O	O
TAMP tamper pins	Up to 6		Up to 6		Up to 6		O	Up to 6	O	Up to 6	O	Up to 6	O
GPIO pins	O		O		O		O	O	O	O/R[7]	O[8]	O/R[7]	O[8]
U(S)ARTx (x = 1, 2)	O		O		O		O[9]	O	O[9]	-	-	-	-
LPUART1	O		O		O		O[9]	O	O[9]	-	-	-	-
I2Cx (x = 1, 2)	O		O		O		O[10]	O	O[10]	-	-	-	-
SPIx (x = 1, 2)	O		O		O		O[11]	O	O[11]	-	-	-	-
ADC4	O		O		O		O[12]	O	O[12]	-	-	-	-
COMPx (x = 1, 2)	O		O		O		O	O	O	-	-	-	-
LPTIMx (x = 1, 2)	O		O		O		O[13]	O	O[13]	-	-	-	-
GPDMA1	O		O		O		O[14]	R	-	-	-	-	-
PTACONV	O		O		O	R	-	R	-	-	-	-	-
TIMx (x = 1, 2, 3, 16, 17)	O		O		R		-	R	-	-	-	-	-
SAI1	O		O		R		-	R	-	-	-	-	-
TSC	O		O		R		-	R	-	-	-	-	-
RNG	O		O		R		-	R	-	-	-	-	-
AES and SAES	O		O		R		-	R	-	-	-	-	-
PKA	O		O		R		-	R	-	-	-	-	-
HASH	O		O		R		-	R	-	-	-	-	-
CRC	O		O		R		-	R	-	-	-	-	-
WWDG	O		O		R		-	R	-	-	-	-	-
SysTick timer	O		O		R		-	R	-	-	-	-	-
HSEM	O		R		R		-	R	-	-	-	-	-
DBGMCU	O		O		O[15]		-	O[15]	-	O[16]	-	O[16]	-

1. Legend: Y = yes (enabled). O = optional (disabled by default, can be enabled by software).R = retained, - = not available. Gray cells highlight the wake-up capability in each mode.
2. The flash memory can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAMs can be powered on or off independently.
4. Parity error interrupt or NMI wake-up from Stop mode.

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5. Some peripherals with autonomous mode and wake-up from Stop capability can request HSI16 to be enabled. In this case, the oscillator is woken up by the peripheral, and is automatically put off when no peripheral needs it.
6. The 2.4 GHz RADIO peripheral in autonomous mode request HSE32 to be enabled. In this case, the oscillator is kept active by the peripheral, and is automatically put off when it no longer needs it.
7. I/O levels can be retained with pull-up, pull-down, or floating.
8. There are 16 wake-up pins available.
9. U(S)ART and LPUART reception and transmission are functional and autonomous in Stop mode in asynchronous and in SPI master modes, and generate a wake-up interrupt on transfer events.
10. I2C reception and transmission is functional and autonomous in Stop mode and generates a wake-up interrupt on transfer events.
11. SPI reception and transmission is functional and autonomous in Stop mode and generates a wake-up interrupt on transfer events.
12. A/D conversion is functional and autonomous in Stop mode, and generates a wake-up interrupt on conversion events.
13. LPTIM is functional and autonomous in Stop mode, and generates a wake-up interrupt on events.
14. GPDMA transfers are functional and autonomous in Stop 0 mode, and generates a wake-up interrupt on transfer events.
15. DBGMCU remains accessible trough AP0.
16. DBGMCU remains accessible through AP0 when CDBGPWRUPREQ is set.

3.12.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.12.4 PWR TrustZone security

When TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security secures the following configuration:

- Low-power mode
- WKUP (wake-up) pins
- Voltage detection
- Backup domain control

Some of the PWR configuration bits security is defined by the security of other peripherals:

- The VOS (voltage scaling) configuration is secure when the system clock selection is secure in RCC.
- The I/O Standby mode retention configuration is secure when the corresponding GPIO is secure.

3.13 Reset and clock controller (RCC)

The RCC (reset and clock controller) manages device and peripheral reset and distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

- Device reset source monitoring.
- Individual peripheral reset control.

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- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- Clock selection system: clock sources can be changed safely on-the-fly in Run mode through a configuration register.
- Clock management: to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- System clock source: different clock sources can be used to drive the system clock SYSCLK:
  - HSE32 (32 MHz high-speed external crystal oscillator), trimmable by software. The HSE32 can also be used with an external clock.
  - HSI16 (16 MHz high-speed internal RC oscillator), trimmable by software.
  - System PLL that can be fed by HSE32 or HSI16 with a maximum output frequency at 100 MHz.
- Auxiliary clock source: three ultra-low power clock sources that can be used to drive, for instance, the real-time clock:
  - LSE (32.000 kHz or 32.768 kHz low-speed external crystal oscillator), supporting programmable drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - LSI1 (32 kHz low-speed internal RC oscillators), also used to drive the independent watchdog. The LSI1 clock absolute accuracy is ±5%, it can be divided by 128 to output a 250 Hz as source clock.
  - LSI2 (32 kHz high stability, ±500 ppm), can be used to drive the 2.4 GHz RADIO sleep timer.
- Peripheral clock sources: several peripherals have their own independent kernel clock whatever the system clock. The PLL has three independent outputs allowing the highest flexibility and can generate clocks for the ADC and the RNG.
- Startup clock: after reset, the microcontroller restarts by default with the HSI16. The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- CSS (Clock security systems): these features can be enabled by software.
  - If a HSE32 clock failure occurs, the system clock automatically switches to HSI16 and a software interrupt is generated if enabled.
  - LSE failure can also be detected and generates an interrupt, in this case the clock switches to LSI.
- Clock-out capability:
  - MCO (microcontroller clock output): outputs one of the internal clocks for external use by the application. (only available in Run, Sleep and Stop mode)
  - LSCO (low-speed clock output): outputs LSI or LSE in all operating modes.

Several prescalers allow AHB and APB frequencies configuration. The maximum frequency of the AHB and the APB clock domains is 100 MHz, except for AHB5 domain, limited to 32 MHz.

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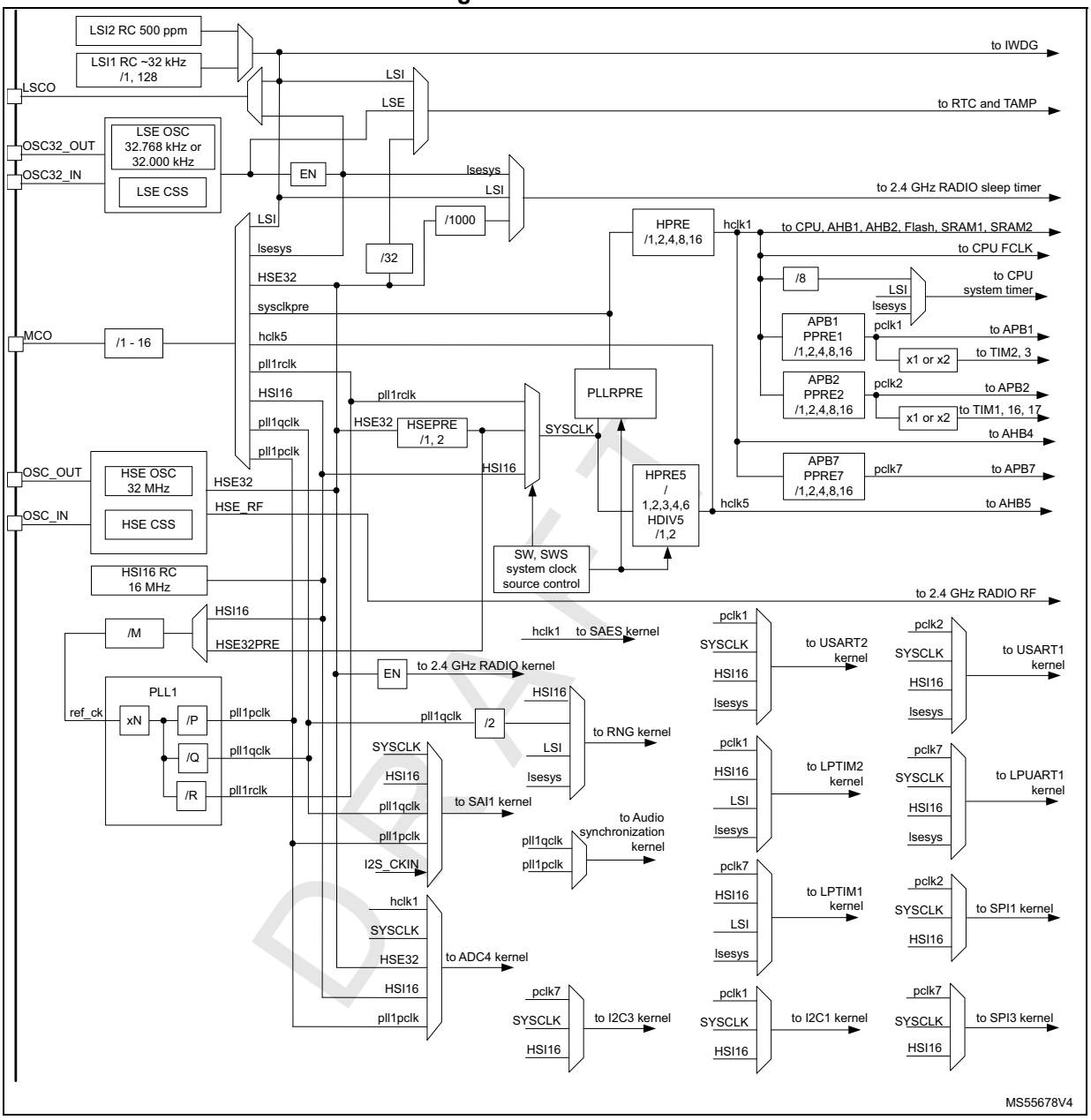
Figure 6. Clock tree



3.13.1 RCC TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security secures some RCC system configuration and peripheral configurations from being read or modified by nonsecure accesses: when a peripheral is secure, the related peripheral clock, reset, clock source selection, and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- For securable peripherals, when the corresponding SEC security bit is set in the TZSC (TrustZone security controller).
- For TrustZone-aware peripherals, when a security feature of the peripheral is enabled through dedicated peripheral bits.

3.14 General-purpose input/output (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

The GPIO allows dynamic I/O control in Stop 0 mode thanks to GPDMA1. All I/Os can be configured and controlled as input or output (open-drain or push-pull depending on GPIO configuration).

When enabled in the PWR, latest I/Os output level can be retained by pulling the I/Os high or low before entering Standby mode. I/O levels are retained after exit from Standby mode, until they are reconfigured by software.

3.14.1 GPIO TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a nonsecure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.15 System configuration controller (SYSCFG)

The main purpose of the SYSCFG (system configuration controller) are the following:

- Managing robustness features
- Configuring FPU interrupts
- Enabling/disabling the I^2C fast-mode plus high-drive mode of some I/Os and booster for I/Os analog switches
- Managing the I/O compensation
- Provides memory erase status
- Communication channel with the RSS

3.15.1 SYSCFG TrustZone security

When TrustZone security is activated by the TZEN option bit, the SYSCFG is switched in TrustZone security mode.

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The SYSCFG TrustZone security secures the following configuration:

- FPU interrupt configuration
- Robustness features
- I/O compensation and memory erase status

Some of the SYSCFG configuration bits security is defined by the security of other peripherals:

- The FMP high-drive mode of some I/Os configuration is secure when the corresponding GPIO is secure.
- The booster for I/Os analog switches configuration is secure when the ADC4 is secure.

3.16 Peripheral interconnect matrix

Several peripherals have direct connections between them, to have autonomous communication between them and to support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep and Stop modes.

3.17 General purpose direct memory access controller (GPDMA)

This controller is a bus master and system peripheral.

The GPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The GPDMA main features are:

- Dual bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Run, Sleep and Stop 0 modes
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension
- Per channel interrupt generation, with separately programmed interrupt enable per event
- Eight concurrent DMA channels:
  - Per channel FIFO for queuing source and destination transfers

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  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers
  - Programmable data handling between source and destination: byte-based reordering, packing or unpacking, padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Programmable DMA request and trigger selection
  - Programmable DMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the DMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting including FIFO level and event flags
- TrustZone support:
  - Support for secure and nonsecure DMA transfers, independently at a first channel level, and independently at a source/destination and link sub-levels
  - Secure and nonsecure interrupts reporting, resulting from any of the respectively secure and nonsecure channels
  - TrustZone-aware AHB slave port, protecting any DMA secure resource (register, register field) from a nonsecure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port.

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Table 12. GPDMA1 channels implementation and usage

Channel x	Hardware parameters		Features
	dma_fifo_ size[x]	dma_ addressing[x]	
x = 0 to 5	2	0	Channel x is implemented with: – a FIFO of 8 bytes, 2 words – fixed/contiguously incremented addressing These channels may be also used for GPDMA transfers, between an APB or AHB peripheral and SRAM.
x = 6 to 7	4	0	Channel x is implemented with: – a FIFO of 32 bytes, 8 words – fixed/contiguously incremented addressing These channels may be also used for GPDMA transfers, between a demanding AHB or APB peripheral and SRAM.

Table 13. GPDMA1 autonomous mode and wake-up in low-power modes

Feature	Low-power modes
Autonomous mode and wake-up	Sleep, Stop 0 modes

3.18 Interrupts and events

3.18.1 Nested vectored interrupt controller (NVIC)

The devices embed a NVIC (nested vectored interrupt controller) that is able to manage 16 priority levels and to handle up to 72 maskable interrupt vectors plus the 16 interrupt vectors of the Cortex-M33.

The NVIC benefits are the following:

- closely coupled NVIC giving low-latency interrupt processing
- interrupt entry vector table address passed directly to the core
- early processing of interrupts
- processing of late arriving higher priority interrupts
- support for tail chaining
- processor state automatically saved
- interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support: NVIC registers banked across secure and nonsecure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.18.2 Extended interrupt/event controller (EXTI)

The EXTI (extended interrupts and event controller) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the

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power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run and Sleep modes. The EXTI also includes the peripheral interconnect EXTI multiplexer I/O port selection.

The EXTI main features are the following:

- All event inputs allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- TrustZone secure events
  - The access to control and configuration bits of secure input events can be made secure
- EXTI I/O port selection for peripheral interconnect use.

3.19 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, that can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

3.20 Analog-to-digital converter (ADC4)

The devices embed one successive approximation analog-to-digital converter.

Table 14. ADC features

ADC modes/features(1)	ADC4
Resolution	12 bits
Maximum sampling speed for 12-bit resolution	2.5 Msps
Hardware offset calibration	X
Hardware linearity calibration	-
Single-ended inputs	X
Differential inputs	-

Table 14. ADC features (continued)

ADC modes/features[1]	ADC4
Injected channel conversion	-
Oversampling	Up to x256
Data register	16 bits
DMA support	X
Autonomous mode	X
Offset compensation	-
Gain compensation	-
Number of analog watchdogs	3
Wake-up from Stop mode	X

1. X = supported.

3.20.1 Analog-to-digital converter (ADC4)

The 12-bit ADC4 is a successive approximation analog-to-digital converter. It has up to 19 multiplexed channels allowing it to measure signals from 9 external and 3 internal sources (the other channels are reserved). ADC conversion of the various channels can be performed in Single, Continuous, Scan or Discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency. The ADC4 is autonomous in low-power modes down to Stop modes.

A built-in hardware oversampler allows analog performances to be improved while off-loading the related computational burden from the CPU.

The ADC4 main features are:

- High performance
  - 12-, 10-, 8- or 6-bit configurable resolution
  - ADC conversion time: 0.4 µs for 12-bit resolution (2.5 MHz), faster conversion times obtained by lowering resolution
  - Self-calibration
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support
- Low-power
  - PCLK frequency reduced for low-power operation while still keeping optimum ADC performance
  - Wait mode: ADC overrun prevented in applications with low frequency PCLK
  - Auto-off mode: ADC automatically powered off except during the active conversion phase, dramatically reducing the ADC power consumption

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  - Autonomous mode: In low-power modes down to Stop 1 mode, the ADC4 is automatically switched on when a trigger occurs to start conversion, and it is automatically switched off after conversion. Data are transfered to SRAM with DMA.
  - ADC4 interrupts wake up the device from Stop modes.
- Analog input channels
  - Nine external analog inputs
  - One channel for the internal temperature sensor (V_{SENSE})
  - One channel for the internal reference voltage (V_{REFINT})
  - One channel for the internal digital core voltage (V_{CORE})
- Start-of-conversion can be initiated:
  - By software
  - By hardware triggers with configurable polarity (timer events or GPIO input events)
- Conversion modes
  - Conversion of a single channel or scan of a sequence of channels
  - Selected inputs converted once per trigger in Single mode
  - Selected inputs converted continuously in Continuous mode
  - Discontinuous mode
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events, with wake-up from Stop capability
- Three analog watchdogs
- ADC supply requirements: 1.62 to 3.6 V
- ADC input range: $V_{SSA} < V_{IN} < V_{DDA}$

Note: The ADC4 analog block clock frequency after the ADC4 prescaler must be between 140 kHz and 55 MHz.

Note: V_{SSA} is connected to package pin VSS.

3.20.2 Temperature sensor (V_{SENSE})

The temperature sensor generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to ADC4 input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

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Table 15. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	Temperature sensor ADC4 12-bit raw data acquired at (30 ± 5)°C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 0710 - 0x0BF9 0711
TS_CAL2	Temperature sensor ADC4 12-bit raw data acquired at (130 ± 5)°C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 0742 - 0x0BF9 0743

3.20.3 Internal voltage reference (V_{REFINT})

The internal voltage reference voltage V_{REFINT} provides a stable (bandgap) voltage for the ADC. The V_{REFINT} is internally connected to ADC4 input channel that is used to convert the voltage into a digital value.

The precise voltage of VREFINT is individually measured for each part by STMicroelectronics during production test and stored in the system memory area. It is accessible in read-only mode.

Table 16. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Internal voltage reference ADC4 12-bit raw data acquired at (30 ± 5)°C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 07A5 - 0x0BF9 07A6

3.21 Comparators (COMP)

The devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low-speed for low-power) and with selectable output polarity.

The reference voltage can be an internal reference voltage or sub-multiple (1/4, 1/2, 3/4).

The voltage on an external I/O can be compared to the reference voltage.

All comparators can wake up from Stop 0 and Stop 1 modes, generate interrupts and breaks for the timers and can also be combined into a window comparator.

3.22 Touch sensing controller (TSC)

The TSC (touch sensing controller) provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The TSC is fully supported by the STMTouch touch sensing firmware library that is free to use and allows touch sensing functionality to be implemented reliably in the end application.

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The TSC main features are the following:

- Proven and robust surface charge transfer acquisition principle
- Support of up to 20 capacitive sensing channels
- Up to six capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to three capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the packages and subject to I/O availability.

3.23 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- Delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)
- Produces four 32-bit random samples every 412 AHB clock cycles if f_{AHB} < 77 MHz (256 RNG clock cycles otherwise)
- Embeds start-up and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management
- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- Has an AHB slave peripheral, accessible through 32-bit word single accesses only (else an AHB bus error is generated, and the write accesses are ignored)

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3.24 Secure advanced encryption standard hardware accelerator (SAES) and encryption standard hardware accelerator (AES)

The devices embed two AES accelerators (SAES and AES). The SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks. The SAES can share its current key register information with the faster AES using a dedicated hardware bus.

The SAES and the AES can be used to encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits. ECB, CBC, CTR, CCM, GCM and GMAC chaining are supported by both SAES and AES.

The SAES and AES support DMA single transfers for incoming and outgoing data (two DMA channels required).

The SAES supports the selection of all the following key sources, while the AES support only the first:

- 256-bit software key, written by the application in the key registers (write only)
- 256-bit DHUK (derived hardware unique key), computed inside the SAES engine from a non-volatile OTP based RHUK (root hardware unique key)
- 256-bit BHK (boot hardware key), stored in tamper-resistant secure backup registers, written by a secure code during boot. Once written, this key cannot be read or write by any application until the next product reset.
- XOR of DHUK (provisioned chip secret) and BHK (software secret)

DHUK, BHK and their XOR are not visible by any software (even secure).

Note: 128-bit key size can also be selected.

BHK key is cleared in case of tamper or RDP regression.

When the SAES is secure (respectively nonsecure), DHUK secure (respectively nonsecure) is used.

The SAES peripheral is connected by hardware to the true random number generator RNG (for side-channel resistance).

The peripherals support:

- Compliant implementation of standard NIST *Special Publication 197, Advanced Encryption Standard (AES)* and *Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation*
- 128-bit data block processing
- Support for cipher keys length of 128-bit and 256-bit
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode

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- 528 or 743 clock cycle latency in ECB encryption mode for SAES processing one 128-bit block of data with, respectively, 128- or 256-bit key
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128- or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (four 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit input buffer and one 32-bit output buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)
- Data swapping logic to support 1-, 8-, 16- or 32-bit data
- Possibility for software to suspend a message if the SAES/AES needs to process another message with a higher priority (suspend/resume operation)
- SAES additional features:
  - Security context enforcement for keys
  - Hardware secret key encryption/ decryption (wrapped key mode) and sharing with faster AES peripheral (Shared key mode)
  - Protection against DPA (differential power analysis) and related side-channel attacks
  - Optional hardware loading of two hardware secret keys (BHK, DHUK) that can be XOR-ed together

On top of standard AES encryption and decryption with a key loaded by software, SAES peripheral makes possible the following advanced use cases:

- Allow or deny the sharing of a key between a secure and a nonsecure application, enforced by hardware
- Encrypt once a key using side-channel resistant AES, then share it to a faster AES engine by decrypting it (Shared key mode)
- On-chip encrypted storage using secret DHUK
- Transport key generation by encrypting the device public unique ID with the application secret BHK
- Binding of device secure storage keys, using the secret derived hardware unique key (DHUK) XORed with the secret boot hardware key (BHK). If BHK is lost, the whole device secure storage is lost.

Note: Encrypted storage or derived keys that are using DHUK or BHK, cannot be used anymore when a security breach is detected.

Table 17. AES/SAES features

AES/SAES modes/features(1)	AES	SAES
ECB, CBC chaining	X	X
CTR, CCM, GCM chaining	X	X
AES 128-bit ECB encryption in cycles	51	528
DHUK and BHK key selection	-	X

Table 17. AES/SAES features (continued)

AES/SAES modes/features[1]	AES	SAES
Side-channel attacks resistance	-	X
Shared key between SAES and AES	X	

1. X = supported.

3.25 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA2-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the keyed-hash message authentication code (HMAC) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes Federal information processing standards (FIPS) approved digests of length of 160, 224, 256 bits, for messages of up to (2^{64} – 1) bits. It also computes 128 bits digests for the MD5 algorithm.

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, *Digital* Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 1321, *MD5* Message-Digest Algorithm
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message* Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, SHA-256, and MD5
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
  - 66 clock cycles for processing one 512-bit block of data using MD5 algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest

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- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of 4 supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.26 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, DU (Diffie-Hellmann) or (ECC) elliptic curve cryptography over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications. More specifically:
  - RSA modular exponentiation, RSA CRT (Chinese remainder theorem) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations
- Protection against DPA (differential power analysis) and related side-channel attacks.

3.27 Timers and watchdogs

The devices include one advanced control timer, four general-purpose timers, two low-power timers, two watchdog timers, and two SysTick timers.

Table 18 compares the features of the advanced control and general-purpose timers.

Table 18. Timers comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2	32 bits	Up, down, up/down			4	No
	TIM3	16 bits					
	TIM16, TIM17	16 bits	Up			1	1

3.27.1 Advanced-control timers (TIM1)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes) with full modulation capability (0 - 100%)
- One-pulse mode output

In Debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in the next section) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the *Timer Link* feature for synchronization or event chaining.

3.27.2 General-purpose timers (TIM2, TIM3, TIM16, TIM17)

There are up to four synchronizable general-purpose timers embedded in the device (see *Table 18* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3
  - Full-featured general-purpose timers with 32-bit auto-reload up/downcounter (TIM2), 16-bit auto-reload up/downcounter (TIM3), both with 16-bit prescaler.
  - Feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.
  - The counters can be frozen in Debug mode.
  - Independent DMA request generation, support of quadrature encoders.
- TIM16, TIM17
  - General-purpose timers with mid-range features.
  - 16-bit auto-reload upcounters and 16-bit prescalers. and one channel and one complementary channel.
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
  - The timers can work together via the *Timer Link* feature for synchronization or event chaining. The timers have independent DMA request generation.
  - The counters can be frozen in Debug mode.
  - Independent DMA request generation.

3.27.3 Low-power timers (LPTIM1, LPTIM2)

The devices embed two low-power timers, with an independent clock, running in Stop mode if clocked by HSI16, LSE, LSI, or an external clock. They are able to wake up the system from Stop mode.

LPTIM1, LPTIM2 are active in Stop modes.

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The low-power timers support the following features:

- 16-bit up counter with 16-bit autoreload register
- 3-bit prescaler with following possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity
- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.27.4 Infrared interface (IRTIM)

An infrared interface (IRTIM) for remote control is available on the device. It can be used with an infrared LED to perform remote control functions. It uses internal connections with TIM16 and TIM17.

3.27.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and a 10-bit prescaler. It is clocked from the independent LSI and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software enabled through the option bytes. The counter can be frozen in low-power and Debug mode.

3.27.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

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3.27.7 SysTick timer

The Cortex-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, secure instance
- SysTick, nonsecure instance

When TrustZone is disabled, only one SysTick timer is available.

This timer (secure or nonsecure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.28 Real-time clock (RTC)

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

As long as the V_{DD} supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under reset).

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in binary-coded decimal (BCD) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a reference clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or nonsecure configuration
  - Alarm A, alarm B, wake-up timer and timestamp individual privileged protection

The RTC is supplied from the V_{DD} supply.

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The RTC clock sources can be one of the following:

- LSE, used as 32.768 kHz external crystal oscillator
- LSE, with external resonator or oscillator
- LSI, internal low-power RC oscillator (with typical frequency of 32 kHz)
- HSE32, high-speed external clock divided by a prescaler in the RCC.

The RTC is functional in all low-power modes when it is clocked by the LSE or LSI.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes.

3.29 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. The 32-bit backup registers are retained in all low-power modes. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with up to five tamper pins and nine internal tampers. The external tamper pins can be configured for level detection with or without filtering, or active tamper, which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- A tamper detection can erase the backup registers, SRAM2, ICACHE and cryptographic peripherals.
- 32 backup registers (32-bit):
  - These registers (TAMP_BKPxR) are implemented in the Backup domain, which remains powered-on by V_{DD} power.
- Up to six tamper pins for external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from two (each input associated to its own exclusive output) to four meshes (single output shared for up to four tamper inputs)
  - Passive tampers: ultra-low power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- Nine internal tamper events to protect against transient or environmental perturbation attacks:
  - LSE monitoring
  - RTC calendar overflow
  - JTAG/SWD access if RDP different from 0
  - Monotonic counter overflow
  - Cryptographic peripherals fault (RNG, SAES, AES, PKA)
  - Independent watchdog reset when tamper flag is already set
  - Three ADC4 watchdogs
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase

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  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- TrustZone support:
  - Tamper secure or nonsecure configuration.
  - Backup registers configuration in three configurable-size areas:
    - a read/write secure area
    - a write secure/read nonsecure area
    - a read/write nonsecure area
  - Secret boot hardware key (BHK) only usable by secure SAES peripheral, stored in backup registers, protected against read and write access
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.30 Inter-integrated circuit interface (I2C)

The device embeds two I2C, refer to *Table 19* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Target and Controller modes, multi-controller capability
  - Standard-mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast-mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit target addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware packet error checking (PEC) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Autonomous functionality in Stop modes with wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

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Table 19. I2C implementation

I2C features[1]	I2C1	I2C3
Standard-mode (up to 100 Kbit/s)	X	X
Fast-mode (up to 400 Kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X
Independent clock	X	X
Autonomous in Stop modes with wake-up capability	X	X

1. X: supported

3.31 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have two embedded universal synchronous receiver transmitters (USART1, USART2) and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 20. U(S)ART and LPUART features

USART modes/features[1]	USART1	USART2	LPUART1
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode (master/slave)	X	X	-
Smartcard mode	X	X	-
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	-
LIN mode	X	X	-
Dual-clock domain and wake-up from Stop modes	X	X	X
Receiver timeout interrupt	X	X	-
Modbus communication	X	X	-
Auto-baud rate detection	X	X	-
Driver enable	X	X	X
USART data length	7, 8, and 9 bits		
Tx/Rx FIFO	X	X	X
Tx/Rx FIFO size	8 bytes		
Autonomous mode	X	X	X

1. X = supported.

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3.31.1 USART/UART

The U(S)ART offers a flexible means to perform full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The U(S)ART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbauds are possible by using the direct memory access (DMA) for multibuffer configuration.

The U(S)ART main features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmit and receive data, each of them can be enabled/disabled by software and come with a status flag
- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Auto baud rate detection
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous Master/Slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability

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  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.31.2 LPUART

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed for LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data, each of them can be enabled/disabled by software and come with status flags for FIFOs states
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags

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- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from Mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from Stop capability

3.32 Serial peripheral interface (SPI)

The devices embed two SPIs (serial peripheral interfaces) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally just to setup communication with concrete slave and to assure it handles the data flow properly. The Motorola data format is used by default, but some other specific modes are supported as well.

The SPI main features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4-bit to 32-bit data size selection or fixed to 8-bit and 16-bit only
- Multi master or multi slave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in Master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO and MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:

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  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 16 x or 8 x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from stop capability
- Optional status pin RDY signalizing the slave device ready to handle the data flow.

Table 21. SPI features

SPI feature(1)	SPI1 (full feature set instances)	SPI3 (limited feature set instance)
Data size	Configurable from 4- to 32-bit	8- and 16-bit
CRC computation	CRC polynomial length, configurable from 5- to 33-bit	CRC polynomial length, configurable from 9- to 17-bit
Size of FIFOs	16 x 8-bit	8 x 8-bit
Number of transfered data	Unlimited, expandable	Up to 1024, no data counter
Autonomous in Stop modes with wake-up capability	X	X

1. X: supported

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3.33 Serial audio interfaces (SAI)

The devices embed one SAI, refer to *Table 22* for its features. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

Depending upon the device, the SAI peripheral can support:

- Two independent audio sub-blocks that can be transmitters or receivers with their respective FIFOs
- 8-word integrated FIFOs for each audio sub-block
- Synchronous or Asynchronous mode between the audio sub-blocks
- Master or slave configuration independent for both audio sub-blocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24- and 32-bit
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/mono audio frame capability
- Communication clock strobing edge configurable (SCK)
- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in Slave mode
  - Late frame synchronization signal detection in Slave mode
  - Codec not ready for the AC'97 mode in reception
- Interruption sources when enabled:
  - Errors
  - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block

Table 22. SAI implementation(1)

Features	SAI1
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/mono audio frame capability	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24- and 32-bit	X

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Table 22. SAI implementation[1] (continued)

Features	SAI1
FIFO size	X (8 words)
SPDIF	X
PDM	X

1. X: supported.

3.34 Development support

3.34.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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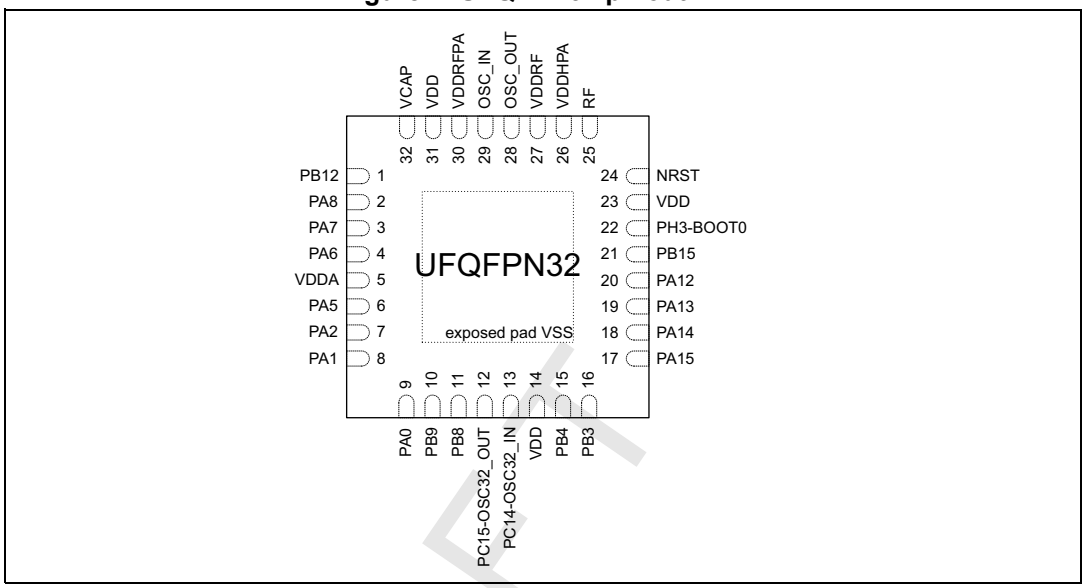
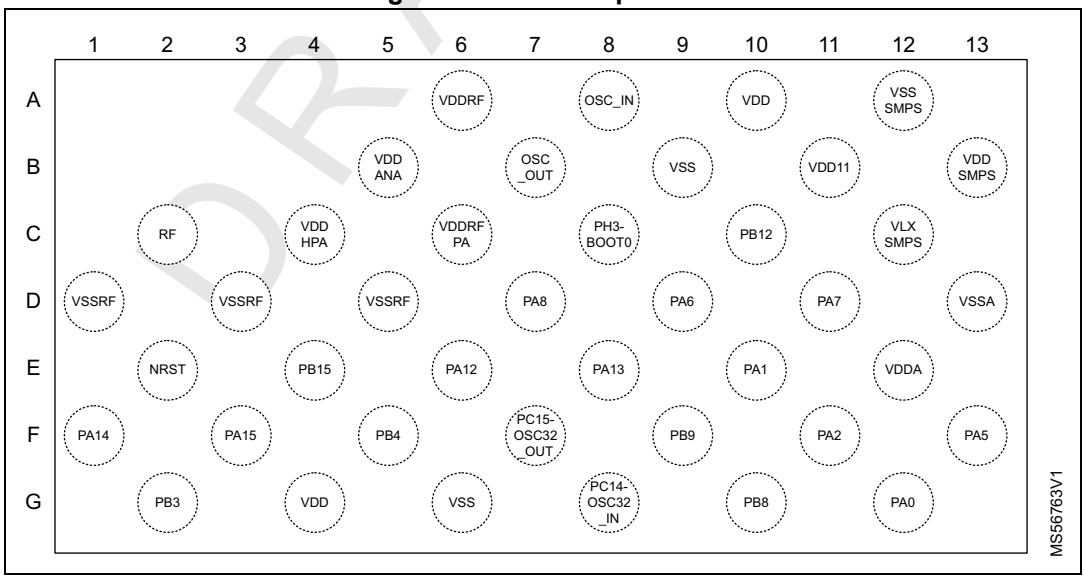
4 Pinouts and pin description

Figure 7. UFQFPN32 pinout(1) (2)



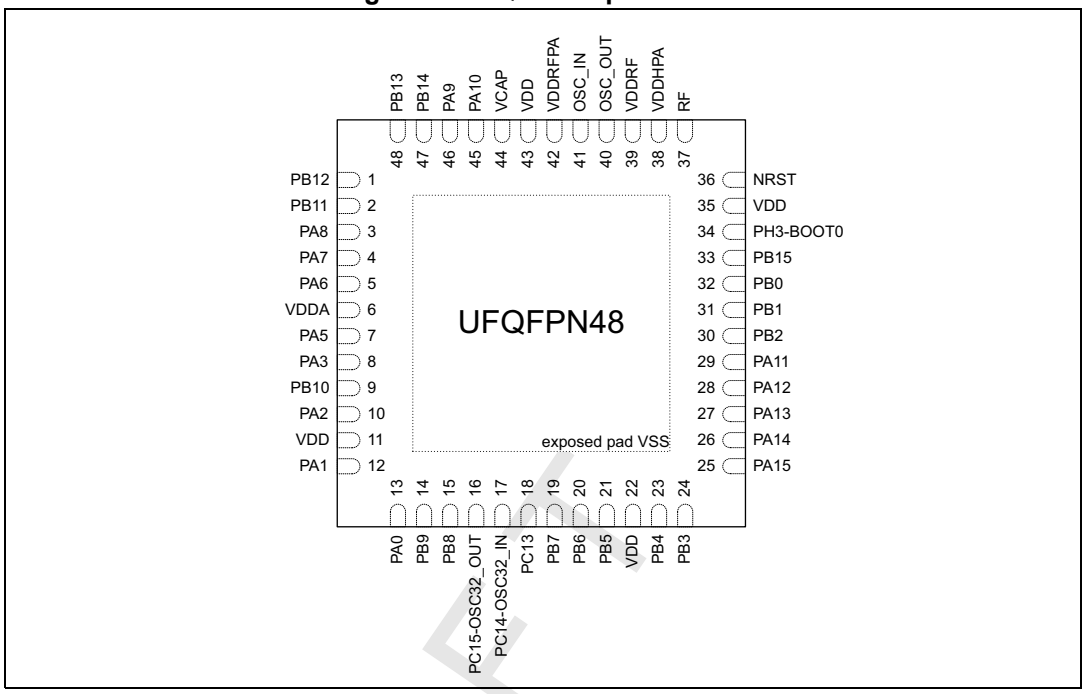
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 8. WLCSP41 pinout(1)



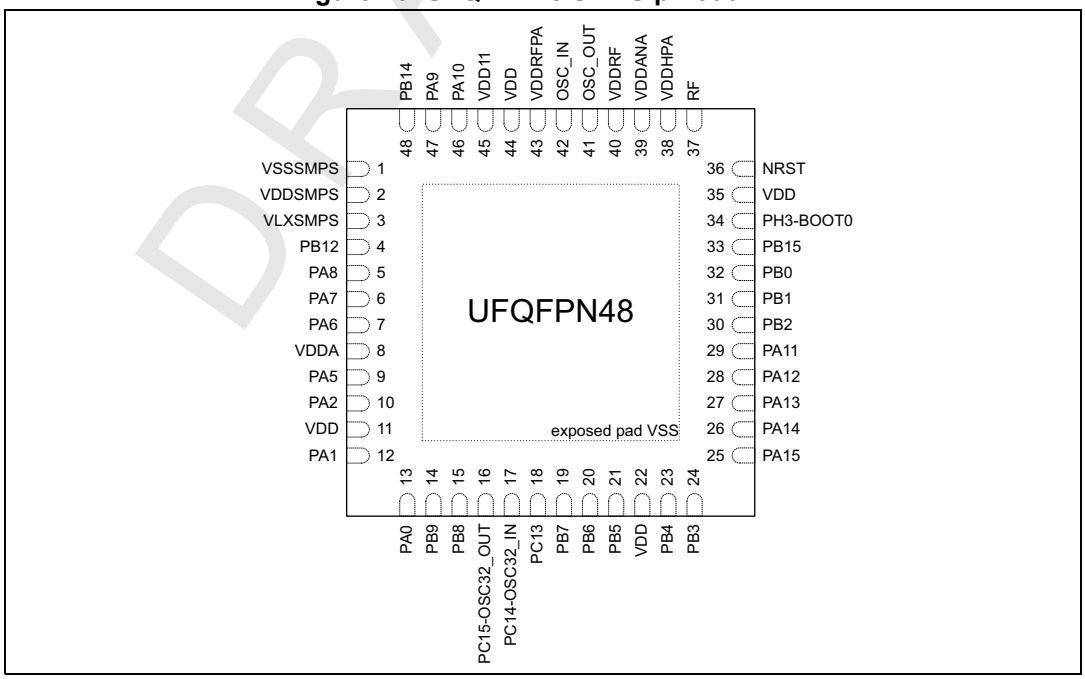
1. The above figure shows the package top view.

Figure 9. UFQFPN48 pinout(1) (2)



1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 10. UFQFPN48 SMPS pinout(1) (2)



1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

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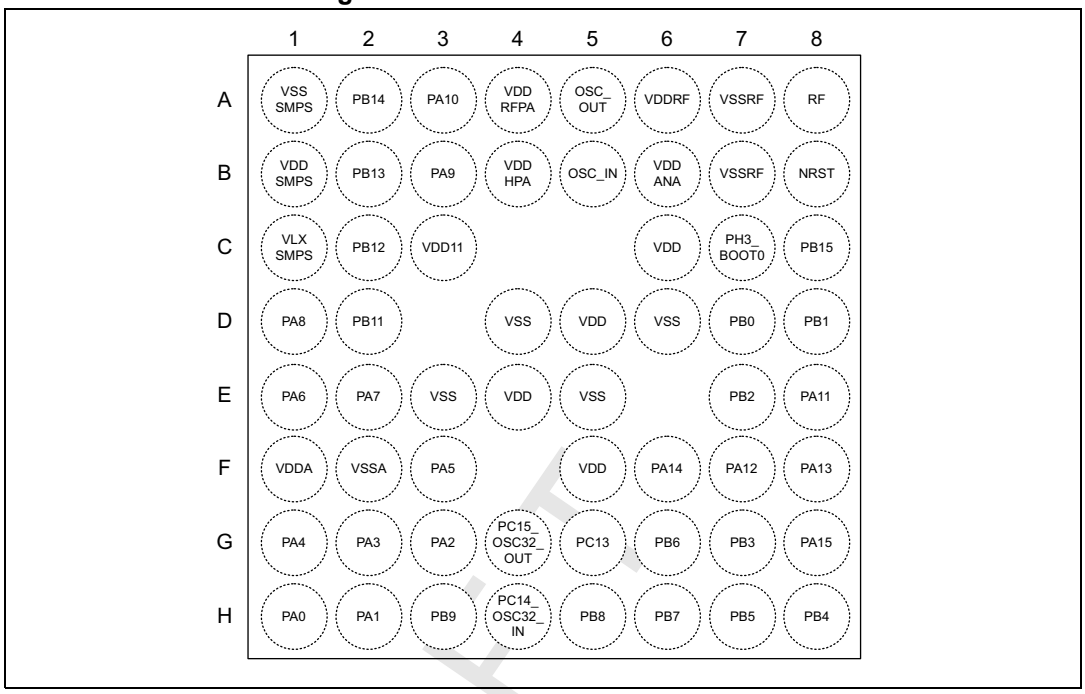
Figure 11. UFBGA59 SMPS ballout(1)



1. The above figure shows the package top view.

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Table 23. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function supplied by V_{DDA}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 24* are a concatenation of various options. Examples: FT_a, FT_fa, FT_f.

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Table 24. Device pin definitions

Pin							I/O structure	Notes	Alternate functions	Additional functions
Number					Name (function after reset)	Type				
UFQFPN32	WLCSP41	UFQFPN48	UFQFPN48 SMPS	UFBGA59 SMPS						
-	A12	-	1	A1	VSSSMPS	S	-	-	-	-
-	B13	-	2	B1	VDDSMPS	S	-	-	-	-
-	C12	-	3	C1	VLXSMPS	S	-	-	-	-
-	B9	-	-	D4	VSS	S	-	-	-	-
1	C10	1	4	C2	PB12	I/O	FT_	-	TIM2_CH1, TIM2_ETR, SPI1_RDY, USART1_TX, TSC_SYNC, SAI1_SD_A, TIM3_ETR, EVENTOUT	-
-	-	2	-	D2	PB11	I/O	FT_	-	LPTIM1_CH1, LPTIM1_ETR, LPUART1_TX, EVENTOUT	-
2	D7	3	5	D1	PA8	I/O	FT_a	-	MCO, TIM2_CH2, LPTIM1_CH2, SPI3_RDY, USART1_RX, TSC_G1_IO1, SAI1_FS_A, EVENTOUT	ADC4_IN1
3	D11	4	6	E2	PA7	I/O	FT_fa	-	TIM2_CH3, I2C3_SDA, USART1_CTS, TSC_G1_IO2, COMP1_OUT, SAI1_SCK_A, EVENTOUT	ADC4_IN2, WKUP8, TAMP_IN1/TAMP_OUT2
4	D9	5	7	E1	PA6	I/O	FT_fa	-	CSTOP, TIM2_CH4, SAI1_CK2, I2C3_SCL, SPI3_RDY, USART1_RTS_DE, TSC_G1_IO3, SAI1_MCLK_A, EVENTOUT	ADC4_IN3, WKUP7
-	D13	-	-	F2	VSSA	S	-	-	-	-
5	E12	6	8	F1	VDDA	S	-	-	-	-

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Table 24. Device pin definitions (continued)

Pin							I/O structure	Notes	Alternate functions	Additional functions
Number					Name (function after reset)	Type				
UFQFPN32	WLCSP41	UFQFPN48	UFQFPN48 SMPS	UFBGA59 SMPS						
6	F13	7	9	F3	PA5	I/O	FT_a	-	CSLEEP, TIM2_CH1, TIM2_ETR, SAI1_D2, SPI3_NSS, USART1_CK, TSC_G1_IO4, AUDIOCLK, LPTIM2_ETR, EVENTOUT	ADC4_IN4, WKUP6
-	-	-	-	G1	PA4	I/O	FT_a	-	USART1_CTS, TSC_G4_IO1, AUDIOCLK, TIM16_CH1, EVENTOUT	ADC4_IN5, WKUP2, TAMP_IN6/TAMP_OUT3
-	-	8	-	G2	PA3	I/O	FT_a	-	USART1_RTS_DE, TSC_G4_IO2, TIM16_CH1N, EVENTOUT	ADC4_IN6, WKUP5
-	-	9	-	-	PB10	I/O	FT_a	-	USART1_CK, TSC_G4_IO3, TIM16_BKIN, EVENTOUT	-
7	F11	10	10	G3	PA2	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, SAI1_D1, USART1_RTS_DE, LPUART1_TX, TSC_G4_IO4, TIM16_CH1, EVENTOUT	COMP1_INP1, ADC4_IN7, WKUP4, LSCO
-	-	11	11	-	VDD	S	-	-	-	-
8	E10	12	12	H2	PA1	I/O	FT_a	-	TIM1_CH1N, TIM3_CH2, SAI1_CK1, SPI1_RDY, USART1_CK, LPUART1_RX, TSC_G2_IO1, LPTIM2_CH2, TIM17_CH1, EVENTOUT	COMP1_INM1, ADC4_IN8, WKUP3
9	G12	13	13	H1	PA0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH2N, TIM3_CH3, SPI3_SCK, LPUART1_CTS, TSC_G2_IO2, TIM3_ETR, EVENTOUT	COMP2_INP1, ADC4_IN9, WKUP1

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Table 24. Device pin definitions (continued)

Pin							I/O structure	Notes	Alternate functions	Additional functions
Number					Name (function after reset)	Type				
UFQFPN32	WLCSP41	UFQFPN48	UFQFPN48 SMPS	UFBGA59 SMPS						
10	F9	14	14	H3	PB9	I/O	FT_a	-	IR_OUT, TIM1_CH3N, TIM3_CH4, SPI3_MISO, LPUART1_RTS_DE, TSC_G2_IO3, LPTIM2_IN1, TIM16_CH1, EVENTOUT	COMP2_INM1, ADC4_IN10, WKUP8
11	G10	15	15	H5	PB8	I/O	FT_a	-	LPTIM1_ETR, TIM1_CH1, USART2_RX, SPI3_MOSI, TSC_G2_IO4, COMP1_OUT, TIM3_ETR, TIM16_CH1N, EVENTOUT	PVD_IN
12	F7	16	16	G4	PC15-OSC32_OUT	I/O	FT_	-	EVENTOUT	OSC32_OUT
13	G8	17	17	H4	PC14-OSC32_IN	I/O	FT_	-	EVENTOUT	OSC32_IN
-	G6	-	-	E3	VSS	S	-	-	-	-
-	G4	-	-	-	VDD	S	-	-	-	-
-	-	18	18	G5	PC13	I/O	FT_a	-	TIM1_BKIN2, TSC_G5_IO1, EVENTOUT	WKUP2, RTC_TS/RTC_OUT1, TAMP_IN4/TAMP_OUT5
-	-	19	19	H6	PB7	I/O	FT_a	-	TIM1_CH4N, TSC_G5_IO2, SAI1_SD_B, EVENTOUT	WKUP5, TAMP_IN5/TAMP_OUT4
14	-	-	-	F5	VDD	S	-	-	-	-
-	-	-	-	E5	VSS	S	-	-	-	-
-	-	20	20	G6	PB6	I/O	FT_a	-	TIM2_CH1, TIM2_ETR, TSC_G5_IO3, SAI1_SCK_B, EVENTOUT	WKUP3

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Table 24. Device pin definitions (continued)

Pin Number					Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	WLCSP41	UFQFPN48	UFQFPN48 SMPS	UFBGA59 SMPS						
-	-	21	21	H7	PB5	I/O	FT_a	-	TIM3_CH1, SAI1_D2, LPUART1_TX, TSC_G5_IO4, SAI1_FS_B, EVENTOUT	-
-	-	22	22	-	VDD	S	-	-	-	-
15	F5	23	23	H8	PB4	I/O	FT_a	-	NJTRST, TIM1_CH3, LPTIM2_IN2, USART2_RX, SPI1_SCK, TSC_G3_IO1, SAI1_MCLK_B, TIM17_CH1, PTA_ACTIVE, PTA_PRIORITY, EVENTOUT	-
16	G2	24	24	G7	PB3	I/O	FT_fa	-	JTDO/TRACESWO, TIM1_CH4, LPTIM1_IN2, USART2_CK, I2C1_SDA, SPI1_MISO, TSC_G3_IO2, TIM17_CH1N, PTA_ACTIVE, EVENTOUT	-
17	F3	25	25	G8	PA15	I/O	FT_fa	-	JTDI, TIM1_ETR, LPTIM1_CH2, USART2_RTS_DE, I2C1_SCL, SPI1_MOSI, TSC_G3_IO3, TIM17_BKIN, PTA_STATUS, EVENTOUT	-
18	F1	26	26	F6	PA14	I/O	FT_	-	JTCK/SWCLK, USART2_TX, COMP2_OUT, PTA_STATUS, EVENTOUT	TAMP_IN3/TAMP_OUT6
19	E8	27	27	F8	PA13	I/O	FT_	-	JTMS/SWDIO, IR_OUT, PTA_PROIORITY, EVENTOUT	-
20	E6	28	28	F7	PA12	I/O	FT_a	-	TIM1_CH2, USART2_TX, SPI1_NSS, TSC_G3_IO4, RF_ANTSW0, COMP2_OUT, PTA_STATUS, EVENTOUT	WKUP6

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Table 24. Device pin definitions (continued)

Pin					Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
Number										
UFQFPN32	WLCSP41	UFQFPN48	UFQFPN48 SMPS	UFBGA59 SMPS						
-	-	29	29	E8	PA11	I/O	FT_	-	TIM1_CH1, USART2_RX, RF_ANTSW1, LPTIM2_CH1, EVENTOUT	-
-	-	30	30	E7	PB2	I/O	FT_f	-	TIM1_CH1N, USART2_CTS, I2C1_SCL, I2C3_SCL, RF_ANTSW2, EVENTOUT	WKUP1, RTC_OUT2
-	-	31	31	D8	PB1	I/O	FT_f	-	TIM1_CH2N, USART2_RTS_DE, I2C1_SDA, I2C3_SDA, EVENTOUT	WKUP4
-	-	32	32	D7	PB0	I/O	FT_	-	TIM1_CH3N, LPTIM2_IN2, USART2_TX, EVENTOUT	-
21	E4	33	33	C8	PB15	I/O	TT_	-	TIM1_BKIN2, USART2_CTS, I2C1_SMBA, I2C3_SMBA, LPUART1_CTS, RF_EXTPABYP, TIM16_BKIN, PTA_GRANT, EVENTOUT	-
22	C8	34	34	C7	PH3-BOOT0	I/O	TT_	-	RF_EXTPABYP, PTA_GRANT, EVENTOUT	TAMP_IN2/TAMP_OUT1
23	-	35	35	C6	VDD	S	-	-	-	-
-	-	-	-	D6	VSS	S	-	-	-	-
24	E2	36	36	B8	NRST	I/O	RST	-	-	-
25	C2	37	37	A8	RF	I/O	RF	-	-	-
-	D1	-	-	A7	VSSRF	S	-	-	-	-
26	C4	38	38	B4	VDDHPA	S	-	-	-	-
-	D3	-	-	B7	VSSRF	S	-	-	-	-

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Table 24. Device pin definitions (continued)

Pin					Name (function after reset)	Type	I/O structure	Notes	Alternate functions	Additional functions
Number										
UFQFPN32	WLCSP41	UFQFPN48	UFQFPN48 SMPS	UFBGA59 SMPS						
-	B5	-	39	B6	VDDANA	S	-	-	-	-
27	A6	39	40	A6	VDDRF	S	-	-	-	-
-	D5	-	-	-	VSSRF	S	-	-	-	-
28	B7	40	41	A5	OSC_OUT	O	RF	-	-	-
29	A8	41	42	B5	OSC_IN	I	RF	-	-	-
30	C6	42	43	A4	VDDRFPA	S	-	-	-	-
-	-	-	-	E4	VDD	S	-	-	-	-
31	A10	43	44	D5	VDD	S	-	-	-	-
32	-	44	-	-	VCAP	S	-	-	-	-
-	B11	-	45	C3	VDD11	S	-	-	-	-
-	-	45	46	A3	PA10	I/O	FT_	-	TIM3_CH1, SAI1_D1, LPUART1_RX, EVENTOUT	-
-	-	46	47	B3	PA9	I/O	FT_	-	TIM3_CH2, SAI1_CK1, LPUART1_RTS_DE, EVENTOUT	-
-	-	47	48	A2	PB14	I/O	FT_a	-	RTC_REFIN, TIM3_CH3, USART1_TX, TSC_G6_IO1, SAI1_SD_A, EVENTOUT	WKUP7
-	-	48	-	B2	PB13	I/O	FT_a	-	TIM3_CH4, TSC_G6_IO2, EVENTOUT	-
33	-	49	49	-	VSS (exposed pad)	S	-	-	-	-

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4.1 Alternate functions

Table 25. Alternate function AF0 to AF7[1]

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS_AF	TIM1/2	LPTIM1/2/TIM1/2/3	SAI1/USART2	I2C1/3	SPI1	I2C3/SPI3	USART1
Port A	PA0	LPTIM1_IN1	TIM1_CH2N	TIM3_CH3	-	-	-	SPI3_SCK	-
	PA1	-	TIM1_CH1N	TIM3_CH2	SAI1_CK1	-	SPI1_RDY	-	USART1_CK
	PA2	-	TIM1_BKIN	TIM3_CH1	SAI1_D1	-	-	-	USART1_RTS_DE
	PA3	-	-	-	-	-	-	-	USART1_RTS_DE
	PA4	-	-	-	-	-	-	-	USART1_CTS
	PA5	CSLEEP	TIM2_CH1	TIM2_ETR	SAI1_D2	-	-	SPI3_NSS	USART1_CK
	PA6	CSTOP	TIM2_CH4	-	SAI1_CK2	I2C3_SCL	-	SPI3_RDY	USART1_RTS_DE
	PA7	-	TIM2_CH3	-	-	I2C3_SDA	-	-	USART1_CTS
	PA8	MCO	TIM2_CH2	LPTIM1_CH2	-	-	-	SPI3_RDY	USART1_RX
Port A	PA9	-	-	TIM3_CH2	SAI1_CK1	-	-	-	-
	PA10	-	-	TIM3_CH1	SAI1_D1	-	-	-	-
	PA11	-	TIM1_CH1	-	USART2_RX	-	-	-	-
	PA12	-	TIM1_CH2	-	USART2_TX	-	SPI1_NSS	-	-
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	-	-	USART2_TX	-	-	-	-
	PA15	JTDI	TIM1_ETR	LPTIM1_CH2	USART2_RTS_DE	I2C1_SCL	SPI1_MOSI	-	-

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Table 25. Alternate function AF0 to AF7[(1)] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS_AF	TIM1/2	LPTIM1/2/TIM1/2/3	SAI1/USART2	I2C1/3	SPI1	I2C3/SPI3	USART1
Port B	PB0	-	TIM1_CH3N	LPTIM2_IN2	USART2_TX	-	-	-	-
	PB1	-	TIM1_CH2N	-	USART2_RTS_DE	I2C1_SDA	-	I2C3_SDA	-
	PB2	-	TIM1_CH1N	-	USART2_CTS	I2C1_SCL	-	I2C3_SCL	-
Port B	PB3	JTDO/TRACESWO	TIM1_CH4	LPTIM1_IN2	USART2_CK	I2C1_SDA	SPI1_MISO	-	-
	PB4	NJTRST	TIM1_CH3	LPTIM2_IN2	USART2_RX	-	SPI1_SCK	-	-
	PB5	-	-	TIM3_CH1	SAI1_D2	-	-	-	-
	PB6	-	TIM2_CH1	TIM2_ETR	-	-	-	-	-
	PB7	-	TIM1_CH4N	-	-	-	-	-	-
	PB8	LPTIM1_ETR	TIM1_CH1	TIM3_ETR	USART2_RX	-	-	SPI3_MOSI	-
	PB9	-	TIM1_CH3N	TIM3_CH4	IR_OUT	-	-	SPI3_MISO	-
	PB10	-	-	-	-	-	-	-	USART1_CK
	PB11	LPTIM1_CH1	-	LPTIM1_ETR	-	-	-	-	-
	PB12	-	TIM2_CH1	TIM2_ETR	-	-	SPI1_RDY	-	USART1_TX
Port B	PB13	-	-	TIM3_CH4	-	-	-	-	-
	PB14	RTC_REFIN	-	TIM3_CH3	-	-	-	-	USART1_TX
	PB15	-	TIM1_BKIN2	-	USART2_CTS	I2C1_SMBA	-	I2C3_SMBA	-
Port C	PC13	-	-	TIM1_BKIN2	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
Port H	PH3	-	-	-	-	-	-	-	-

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1. For AF8 to AF15, refer to *Table 26*.

Table 26. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	TSC	PTA	RF	COMP1/2/PTA	LPTIM2/SAI1	LPTIM2/TIM3/16/17	EVENOUT
Port A	PA0	LPUART1_CTS	TSC_G2_IO2	-	-	-	-	TIM3_ETR	EVENTOUT
-	PA1	LPUART1_RX	TSC_G2_IO1	-	-	-	LPTIM2_CH2	TIM17_CH1	EVENTOUT
-	PA2	LPUART1_TX	TSC_G4_IO4	-	-	-	-	TIM16_CH1	EVENTOUT
-	PA3	-	TSC_G4_IO2	-	-	-	-	TIM16_CH1N	EVENTOUT
-	PA4	-	TSC_G4_IO1	-	-	-	AUDIOCLK	TIM16_CH1	EVENTOUT
-	PA5	-	TSC_G1_IO4	-	-	-	AUDIOCLK	LPTIM2_ETR	EVENTOUT
-	PA6	-	TSC_G1_IO3	-	-	-	SAI1_MCLK_A	-	EVENTOUT
-	PA7	-	TSC_G1_IO2	-	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
-	PA8	-	TSC_G1_IO1	-	-	-	SAI1_FS_A	-	EVENTOUT
-	PA9	LPUART1_RTS_DE	-	-	-	-	-	-	EVENTOUT
-	PA10	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
-	PA11	-	-	-	RF_ANTSW1	-	-	LPTIM2_CH1	EVENTOUT
-	PA12	-	TSC_G3_IO4	PTA_STATUS	RF_ANTSW0	COMP2_OUT	-	-	EVENTOUT
-	PA13	-	-	PTA_PRIORITY	-	-	-	-	EVENTOUT
-	PA14	-	-	PTA_STATUS	-	COMP2_OUT	-	-	EVENTOUT
-	PA15	-	TSC_G3_IO3	PTA_STATUS	-	-	-	TIM17_BKIN	EVENTOUT
Port B	PB0	-	-	-	-	-	-	-	EVENTOUT

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Table 26. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	TSC	PTA	RF	COMP1/2/PTA	LPTIM2/SAI1	LPTIM2/TIM3/16/17	EVENOUT
-	PB1	-	-	-	-	-	-	-	EVENTOUT
-	PB2	-	-	-	RF_ANTSW2	-	-	-	EVENTOUT
-	PB3	-	TSC_G3_IO2	PTA_ACTIVE	-	-	-	TIM17_CH1N	EVENTOUT
-	PB4	-	TSC_G3_IO1	PTA_PRIORITY	-	PTA_ACTIVE	SAI1_MCLK_B	TIM17_CH1	EVENTOUT
-	PB5	LPUART1_TX	TSC_G5_IO4	-	-	-	SAI1_FS_B	-	EVENTOUT
-	PB6	-	TSC_G5_IO3	-	-	-	SAI1_SCK_B	-	EVENTOUT
-	PB7	-	TSC_G5_IO2	-	-	-	SAI1_SD_B	-	EVENTOUT
-	PB8	-	TSC_G2_IO4	-	-	COMP1_OUT	-	TIM16_CH1N	EVENTOUT
-	PB9	LPUART1_RTS_DE	TSC_G2_IO3	-	-	-	LPTIM2_IN1	TIM16_CH1	EVENTOUT
-	PB10	-	TSC_G4_IO3	-	-	-	-	TIM16_BKIN	EVENTOUT
-	PB11	LPUART1_TX	-	-	-	-	-	-	EVENTOUT
-	PB12	-	TSC_SYNC	-	-	-	SAI1_SD_A	TIM3_ETR	EVENTOUT
-	PB13	-	TSC_G6_IO2	-	-	-	-	-	EVENTOUT
-	PB14	-	TSC_G6_IO1	-	-	-	SAI1_SD_A	-	EVENTOUT
-	PB15	LPUART1_CTS	-	PTA_GRANT	RF_EXTPABYP	-	-	TIM16_BKIN	EVENTOUT
Port C	PC13	-	TSC_G5_IO1	-	-	-	-	-	EVENTOUT
-	PC14	-	-	-	-	-	-	-	EVENTOUT
-	PC15	-	-	-	-	-	-	-	EVENTOUT
Port H	PH3	-	-	PTA_GRANT	RF_EXTPABYP	-	-	-	EVENTOUT

1. For AF0 to AF7, refer to *Table 25*.

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5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C and supply voltage V_{DD} = V_{DDA} = V_{DDRF} = 3 V. They are only given as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error lower than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines, and are not tested.

5.1.4 Loading capacitor

Unless otherwise specified, the loading conditions used for pin parameter measurement are shown in *Figure 12*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

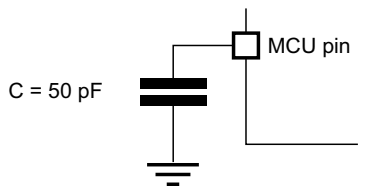
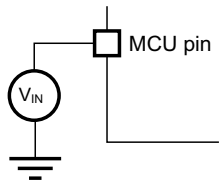


Figure 13. Pin input voltage



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5.1.6 Power supply scheme

Figure 14. Power supply scheme with LDO

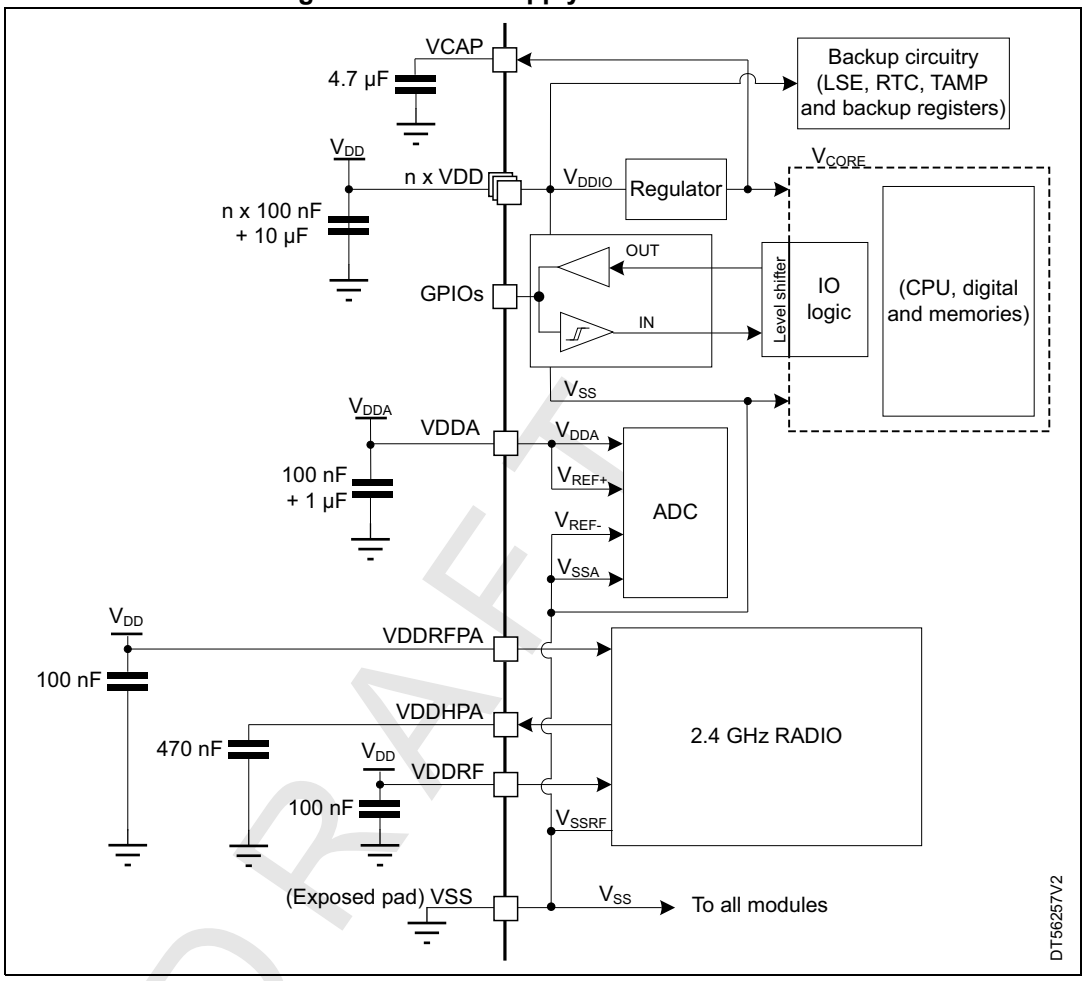

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Figure 15. Power supply scheme with SMPS

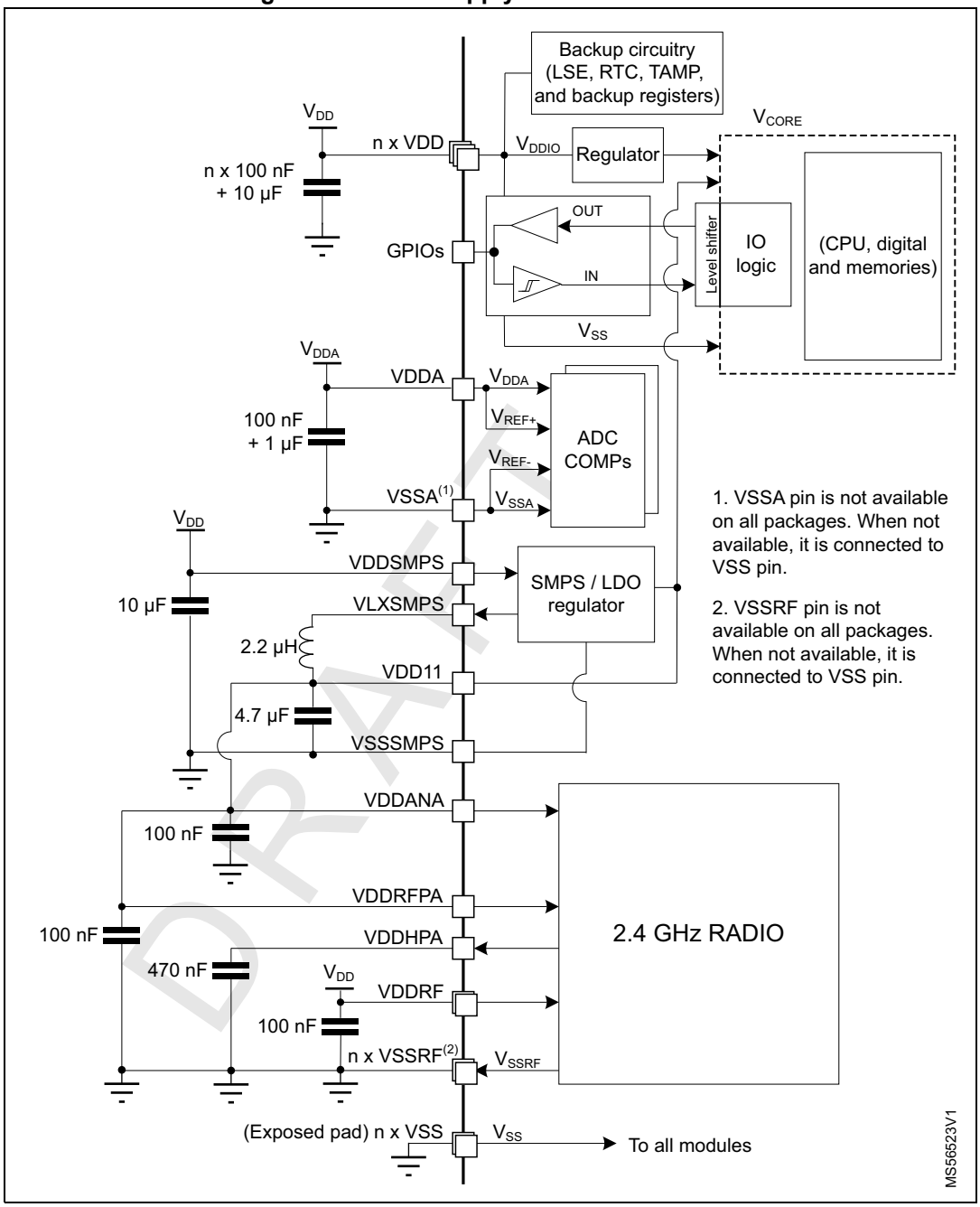

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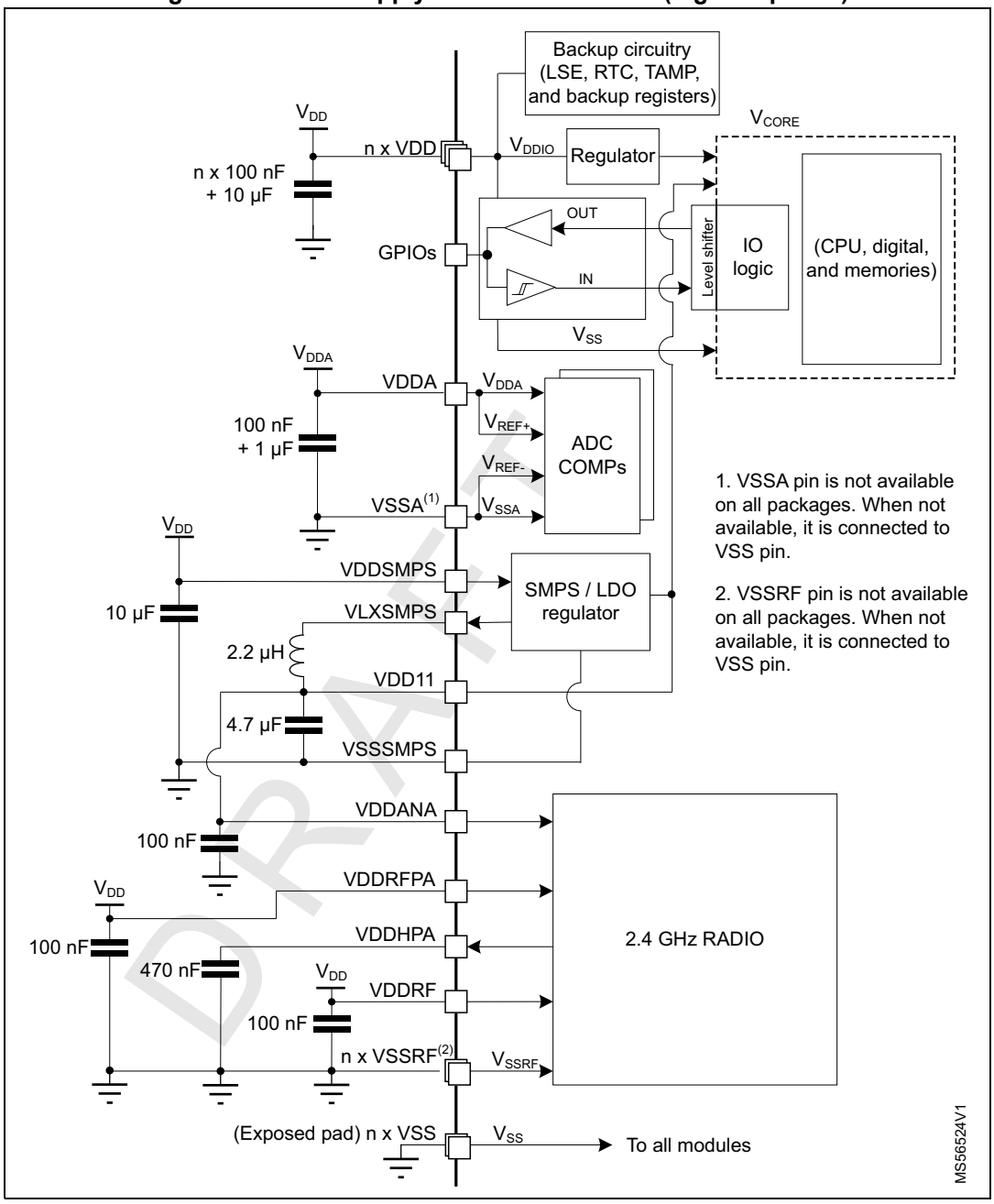
Figure 16. Power supply scheme with SMPS (high RF power)



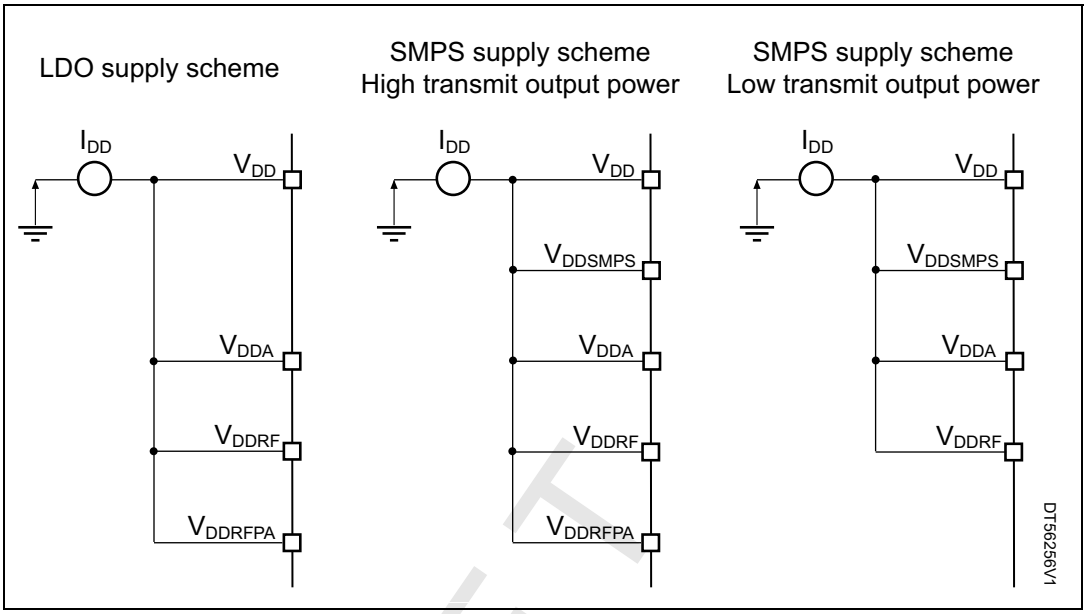
Caution: Each power supply pair (V_{DD} / V_{SS}, V_{DDA} / V_{SS}, V_{DDRFPA} / V_{SS}, V_{DDRF} / V_{SS}) must be decoupled with filtering ceramic capacitors as shown. These capacitors must be placed as close as possible to (or below) the appropriate pins to ensure correct device functionality.

Caution: V_{DD} and V_{DDRF} must be connected to the same supply.

5.1.7 Current consumption measurement

The I_{DD} parameters in the tables in the next sections represent the total MCU consumption, including the current supplying V_{DD}, V_{DDA}, V_{DDRF}, V_{DDRFPA}, and V_{DDSMPS} (if the device embeds the SMPS), or the total 2.4 GHz RADIO current supplying V_{DDRF} and V_{DDRFPA}.

Figure 17. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 27*, *Table 28*, and *Table 29* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 27. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DDX} - V_{SS}$	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDRF}, V_{DDRFPA}, V_{DDANA}, V_{DDSMPS})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_ (any option) pins	V_{SS} - 0.3	min (min (V_{DD}, V_{DDA}) + 4.0, 6.0)(3)(4)	
	Input voltage on any other pin		4.0	
$\|\Delta V_{DDx}\|$	Variations between different VDDX power pins of the same domain	-	50.0	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50.0	

1. All main power (VDD, VDDA, VDDRF, VDDRFPA, VDDANA, VDDSMPS) and ground (VSS, VSSA, VSSRF, VSSSMPS) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 28* for the maximum allowed injected current values.
3. To sustain a voltage higher than 4 V, the internal pull-up/pull-down resistors must be disabled.
4. This formula applies only to power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}) + 4.0 V, and 6.0 V.

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Table 28. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	200	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	200	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\sum I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	120	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST pins	–5/+0	
$\sum \lvert I_{INJ(PIN)} \rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (VDD, VDDA, VDDRF, VDDRFPA, VDDANA, VDDSMPS) and ground (VSS, VSSA, VSSRF, VSSSMPS) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 27* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum \lvert I_{INJ(PIN)} \rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 29. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_{JMAX}	Maximum junction temperature	140	

5.3 Operating conditions

5.3.1 Summary of main performance

Table 30. Main performance at V_{DD} = 3.3 V

Parameter		Test conditions	Typ	Unit
I_{DD}	Core current consumption	Standby (64 Kbytes RAM retention)	0.93	µA
		Stop 1	6.5	
		Sleep (V_{DD} = 3.0 V, 16 MHz)	0.22	mA
		Run (100 MHz)	3.35	
		Radio BLE Rx 1 Mbps(1)	4.41	
		Radio BLE Tx 0 dBm output power(1)	5.24	

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Table 30. Main performance at V_{DD} = 3.3 V (continued)

Parameter			Test conditions	Typ	Unit
I_{DD}	Peripheral current consumption	BLE	Advertising using Standby mode(2) (Tx = 0 dBm; Period 1.28 s; 31 bytes, 3 channels)	10.7	µA
			Advertising using Standby mode(2) (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	2.6	

1. Power consumption including RF subsystem and digital processing.
2. Power consumption integrated over 100 s, including Cortex-M33, 2.4 GHz RADIO subsystem and digital processing.

5.3.2 General operating conditions

Table 31. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.71(1)	-	3.6	V
V_{DDSMPS}	Supply voltage for internal SMPS step-down converter	-	V_{DD}			V
V_{DDA}	Analog supply voltage	ADC used	1.62	-	3.6	V
		COMP used	1.58	-		
		ADC, COMP not used	0	-		
V_{DDRF}	RF operating voltage	-	1.71	-	3.6	V
V_{DDRFPA}	RF power amplifier operating voltage	V_{DDRFPA} must be equal or lower than V_{DDRF}	1.15(2)	-	3.6	V
V_{DDANA}	RF analog supply	V_{DDANA} must be equal or lower than V_{DDRF}	1.15	-	3.6	
V_{IN}	I/O input voltage	All I/Os FT_ (any option) pins	–0.3	-	Min (min (V_{DD}, V_{DDA}) + 3.6 , 5.5)(3)(4)	V
V_{CORE}	Internal regulator ON	Range 1	1.15	1.21	1.27	V
		Range 2	0.81	0.90	0.99	
f_{HCLK}	Internal AHB1, AHB2, and AHB4 clock frequency	Range 1	-	-	100	MHz
		Range 2	-	-	16	
f_{PCLK}	Internal APB1, APB2, and APB7 clock frequency	Range 1	-	-	100	
		Range 2	-	-	16	
f_{HCLK5}	Internal AHB5 clock frequency	Range 1	-	-	32	
		Range 2	-	-	12	
Δf_{HCLK1}	Internal AHB1, AHB2 and AHB4 clock incremental frequency step(5)	-	-	-	84	MHz
P_D	Power dissipation at T_A = 85°C (suffix 6 version) or T_A = 105°C (suffix 7 version)	See *Section 6.6* for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T_A), maximum junction temperature (T_J), and selected thermal resistance.				mW

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Table 31. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature	Suffix 6 version	–40	-	85	°C
	Ambient temperature	Suffix 7 version	–40	-	105	
T_J	Junction temperature range	Suffix 6 version	–40	-	105	°C
		Suffix 7 version(6)		-	120	

1. When RESET is released functionality is guaranteed down to V_{BORx} min.
2. When the 2.4 GHz RADIO is active, when inactive supply can go down to 0 V.
3. This formula applies only to power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}) + 3.6 V and 5.5 V.
4. For operation with voltages higher than min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Without system clock frequency step limiting.
6. Junction temperature above 105°C must be limited to 30% of 10 years life time.

5.3.3 RF characteristics

Table 32. Generic RF transmitter characteristics(1)

Symbol	Parameter		Test conditions	Standard	Min	Typ	Max	Unit
P_{txmax}	Maximum output power		V_{DDRFPA} ≥ 2.50 V	-	-	9.5	-	dBm
			V_{DDRFPA} ≥ 1.71 V	-	-	7.5	-	
P_{txmin}	Minimum output power		-	-	-	-20	-	
ΔP_{tx}	Output power step		-	-	-	1	-	dB
$P_{freqband}$	Output power ± variation over the frequency band		P_{txmax} max setting	-	-	0.4	-	
P_{temp}	Output power ± variation over the temperature		P_{txmax} max setting -40°C ≤ T_J ≤ +105°C	-	-	2.9	-	
$P_{2ndHARM}$	Second harmonic		P_{txmax} max setting	-	-	-69.5	-	dBm
$P_{3rdHARM}$	Third harmonic		P_{txmax} max setting	-	-	-70.5	-	
$OBSE_{1Mbps}$	Out of band spurious emission 1 Mbps	< 1 GHz	P_{txmax} max setting	(2)	-	-51	-	
		≥ 1 GHz	P_{txmax} max setting		-	-43	-	
$OBSE_{2Mbps}$	Out of band spurious emission 2 Mbps	< 1 GHz	P_{txmax} max setting	(2)	-	-54	-	
		≥ 1 GHz	P_{txmax} max setting		-	-45	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

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Table 33. Generic RF receiver characteristics(1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$Rssi_{max}$	RSSI maximum value	-	-	-	-32	-	dBm
$Rssi_{min}$	RSSI minimum value	-	-	-	-75	-	
$Rssi_{accu}$	RSSI accuracy	-	-	-	±6	-	dB

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 34. RF Bluetooth LE characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency channel operating band	-	2402	-	2480	MHz
ΔF	Delta frequency	-	-	250	-	kHz
Rgfsk	On air data rate	-	0.125	-	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

Table 35. RF transmitter Bluetooth LE characteristics(1)

Symbol	Parameter		Test conditions	Standard	Min	Typ	Max	Unit
$BW6dB_{1Mbps}$	6 dB signal bandwidth		P_{txmax} max setting	-	-	665	-	kHz
$BW6dB_{2Mbps}$	6 dB signal bandwidth		P_{txmax} max setting	-	-	1142	-	
$IBSE_{1Mbps}$	In band spurious emission	2 MHz	-	-20	-	-41	-20	dBm
		≥ 3 MHz	-	-30	-	-47.5	-30	
$IBSE_{2Mbps}$	In band spurious emission	4 MHz	-	-20	-	-42.5	-20	dBm
		5 MHz	-	-20	-	-44	-20	
		≥ 6 MHz	-	-30		-45	-30	
f_d	Frequency drift		-	±50	-50	-	+50	kHz
dr_{max}	Maximum drift rate	Uncoded	-	±20	-20	-	+20	kHz/ 50 µs
		Coded	-	±19.2	-19.2	-	+19.2	
fo	Frequency offset		-	±150	-150	-	+150	kHz
$Δf1_{1Mbps}$	Frequency deviation average 1 Mbps		-	225 - 275	225	-	275	
$Δf1_{2Mbps}$	Frequency deviation average 2 Mbps		-	450 - 550	450	-	550	
$Δf1_{CodedS8}$	Frequency deviation average Coded S = 8		-	225 - 275	225	-	275	
$Δf2_{1Mbps}$	Frequency deviation 99.9% 1 Mbps		-	185	185	-	-	
$Δf2_{2Mbps}$	Frequency deviation 99.9% 2 Mbps		-	370	370	-	-	

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1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 36. RF receiver Bluetooth LE characteristics (1)(2)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
P_{rxmax}	Maximum input signal	PER ≤ 30.8%	-10	-	6	-	dBm
$P_{sens2Mbps}$(3)	Sensitivity 2 Mbps	SMPS bypass	-70	-	-93	-	dBm
		SMPS on(2)		-		-	
$P_{sens1Mbps}$(3)	Sensitivity 1 Mbps	SMPS bypass(2)	-70	-	-96	-	
		SMPS on(2)		-		-	
$P_{sens500kbps}$(3)	Sensitivity 500 kbps	SMPS bypass(2)	-75	-	-99	-	
		SMPS on(2)		-		-	
$P_{sens125kbps}$(3)	Sensitivity 125 kbps	SMPS bypass(2)	-82	-	-102	-	
		SMPS on(2)		-		-	
$P_{IMD1Mbps}$	Intermodulation 1Mbps	|f2 - f1| = 3 MHz	-50	-50	-37	-	dBm
		|f2 - f1| = 4 MHz		-50	-27	-	
		|f2 - f1| = 5 MHz		-50	-28	-	
$P_{OBB1Mbps}$	Out of band blocking (for desired signal at -67 dBm and 1 Mbps)	30 to 2000 MHz	-30	-30	-10	-	
		2000 to 2399 MHz	-35	-35	-22	-	
		2484 to 2999 MHz	-35	-35	-15	-	
		3 to 12.75 GHz	-30	-30	-10	-	
$P_{IMD2Mbps}$	Intermodulation 2 Mbps	|f2 - f1| = 3 MHz	-50	-50	-37	-	dBm
		|f2 - f1| = 4 MHz		-50	-30	-	
		|f2 - f1| = 5 MHz		-50	-30	-	
$P_{OBB2Mbps}$	Out of band blocking (for desired signal at -67 dBm and 2 Mbps)	30 to 2000 MHz	-30	-30	-10	-	
		2000 to 2399 MHz	-35	-35	-33	-	
		2484 to 2999 MHz	-35	-35	-19	-	
		3 to 12.75 GHz	-30	-30	-10	-	
$C/Ico_{125kbps}$	Co-channel rejection 125 kbps	-	12	-	3	-	dB
$C/I_{125kbps}$	Adjacent channel interference 125 kbps	Adj = ±1 MHz	6	-	-2	6	
		Adj = 2 MHz	-26	-	-38	-26	
		Adj-Image = -2 MHz	-18	-	-27	-18	
		Adj ≥ 3 MHz	-36	-	-43	-36	
		Adj = -3 MHz	-24	-	-28	-24	
		Adj ≤ -4 MHz	-36	-	-43	-36	
$C/Ico_{250kbps}$	Co-channel rejection 250 kbps	-	17	-	5	17	dB

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Table 36. RF receiver Bluetooth LE characteristics (1)(2) (continued)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$C/I_{500kbps}$	Adjacent channel interference 500 kbps	Adj = ±1 MHz	11	-	-2	11	dB
		Adj = 2 MHz	-21	-	-34	-21	
		Adj-Image = -2 MHz	-13	-	-26	-13	
		Adj ≥ 3 MHz	-31	-	-39	-31	
		Adj = -3 MHz	-19	-	-27	-19	
		Adj ≤ -4 MHz	-31	-	-37	-31	
C/Ico_{1Mbps}	Co-channel rejection 1 Mbps	-	21	-	8	21	dB
C/I_{1Mbps}	Adjacent channel interference 1 Mbps	Adj = ±1 MHz	15	-	0	15	
		Adj = 2 MHz	-17	-	-38	-17	
		Adj-Image = -2 MHz	-9	-	-23	-9	
		Adj ≥ 3 MHz	-27	-	-36	-27	
		Adj = -3 MHz	-15	-	-27	-15	
		Adj ≤ -4 MHz	-27	-	-38	-27	
C/Ico_{2Mbps}	Co-channel rejection 2 Mbps	-	21	-	8	21	dB
C/I_{2Mbps}	Adjacent channel interference 2 Mbps	Adj = ±2 MHz	15	-	0	15	
		Adj = 4 MHz	-17	-	-35	-17	
		Adj-Image = -4 MHz	-9	-	-23	-9	
		Adj ≥ 6 MHz	-27	-	-33	-27	
		Adj = -6 MHz	-15	-	-26	-15	
		Adj ≤ -8 MHz	-27	-	-34	-27	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. The payload length used in all receiver tests is 37 bytes, which means that the limit for each parameter is reached for a BER of 0.1% (PER of 30.8%), as defined in the Bluetooth LE core specification.
3. With ideal transmitter.

Table 37. RF Bluetooth LE power consumption for V_{DD} = 3.3 V(1)(2)

Symbol	Parameter	Typ	Unit
I_{tx}	Tx 0 dBm output power consumption (LDO)	10.51	mA
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	5.54	
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD11)	5.24	
	Tx +10 dBm output power consumption (LDO)	21.15	
	Tx +10 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	19.40	

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Table 37. RF Bluetooth LE power consumption for V_{DD} = 3.3 V(1)(2) (continued)

Symbol	Parameter	Typ	Unit
I_{rx}	Rx consumption 1 Mbps (LDO)	7.91	mA
	Rx consumption 1 Mbps (SMPS ON, VDDRFPA connected to VDD)	5.22	
	Rx consumption 1 Mbps (SMPS ON, VDDRFPA connected to VDD11)	4.41	
	Rx consumption 2 Mbps (LDO)	8.53	
	Rx consumption 2 Mbps (SMPS ON, VDDRFPA connected to VDD)	8.00	
	Rx consumption 2 Mbps (SMPS ON, VDDRFPA connected to VDD11)	5.00	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Power consumption including 2.4 GHz RADIO subsystem and digital processing.

5.3.4 RF IEEE802.15.4 characteristics

Table 38. RF IEEE802.15.4 characteristics(1)

Symbol	Parameter	Conditions	Standard	Min	Typ	Max	Unit
F_{op}	Frequency channel operating band	-	-	2405	-	2480	MHz
ΔF	Delta frequency	-	-	-	5	-	
Roqpsk	On air data rate	-	-	-	250	-	kbps
PLLres	RF channel spacing	-	-	-	5	-	MHz

1. Guaranteed by characterization results, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 39. RF transmitter IEEE802.15.4 characteristics(1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
P_{txmax}	Maximum output power	V_{DDRFPA} ≥ 2.50 V	-	-	9.5	-	dBm
		V_{DDRFPA} ≥ 1.71 V	-	-	7.5	-	
P_{txmin}	Minimum output power	-	-	-	-15	-	
$ΔP_{tx}$	Output power step	-	-	0.5	1	2	dB
$P_{freqband}$	Output power ± variation over the frequency band	P_{txmax} max setting	-	-	0.5	-	
P_{temp}	Output power ± variation over the temperature	P_{txmax} max setting -40°C ≤ T_J ≤ +130°C	-	-	2.5	-	
$P_{2ndHARM}$	Second harmonic	P_{txmax} max setting	-	-	-69.5	-	dBm
$P_{3rdHARM}$	Third harmonic	P_{txmax} max setting	-	-	-70.5	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

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Table 40. RF receiver IEEE802.15.4 characteristics(1)

Symbol	Parameter	Conditions	Standard	Min	Typ	Max	Unit
P_{rxmax}	Maximum input signal	PER ≤ 1%	-20	-	-20	-	dBm
$P_{sens250kbps}$	Sensitivity 250 kbps (LDO)	PER ≤ 1%	-85	-	-97.5	-	
	Sensitivity 250 kbps (SMPS ON)		-85	-	-97.5	-	
C/I_{adj}	Adjacent channel rejection	-	0	-	10	-	dB
C/I_{alt}	Alternate channel rejection	-	30	-	30	-	

1. Guaranteed by characterization results, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5948), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 41. RF IEEE802.15.4 power consumption for V_{DD} = 3.3 V(1)(2)

Symbol	Parameter	Typ	Unit
I_{tx}	Tx 0 dBm output power consumption (LDO)	13.6	mA
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	7.2	
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD11)	6.85	
	Tx +10 dBm output power consumption (LDO)	25.3	
	Tx +10 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	22.7	
I_{rx}	Rx consumption (LDO)	10.2	
	Rx consumption (SMPS ON, VDDRFPA connected to VDD)	6.25	
	Rx consumption (SMPS ON, VDDRFPA connected to VDD11)	5.52	

1. Guaranteed by characterization results, unless otherwise specified.
2. Power consumption including 2.4 GHz RADIO subsystem and digital processing.

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5.3.5 Operating conditions at power-up/power-down

The parameters in *Table 42* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 31*.

Table 42. Operating conditions at power-up / power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate	ULPMEN = 0	20	∞	µs/V
		Standby mode with ULPMEN = 1	250	∞	ms/V

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.6 Embedded reset and power control block characteristics

The parameters in *Table 43* are derived under ambient temperature and supply voltage conditions summarized in *Table 31*.

Table 43. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after V_{BOR0} threshold detection	V_{DD} rising	-	-	900	µs
V_{BOR0}(2)	Brown-out reset threshold 0	V_{DD} rising	1.60	1.66	1.71	V
		V_{DD} falling	1.58	1.64	1.69	
V_{BOR1}(2)	Brown-out reset threshold 1	V_{DD} rising	1.98	2.08	2.17	
		V_{DD} falling	1.90	2.00	2.10	
V_{BOR2}(2)	Brown-out reset threshold 2	V_{DD} rising	2.18	2.29	2.39	
		V_{DD} falling	2.08	2.18	2.25	
V_{BOR3}(2)	Brown-out reset threshold 3	V_{DD} rising	2.48	2.59	2.70	
		V_{DD} falling	2.39	2.50	2.61	
V_{BOR4}(2)	Brown-out reset threshold 4	V_{DD} rising	2.76	2.88	3.00	
		V_{DD} falling	2.67	2.79	2.90	
V_{PVD0}(2)	Programmable voltage detector threshold 0	V_{DD} rising	2.03	2.13	2.23	V
		V_{DD} falling	1.93	2.03	2.12	
V_{PVD1}(2)	PVD threshold 1	V_{DD} rising	2.18	2.29	2.39	
		V_{DD} falling	2.08	2.18	2.28	
V_{PVD2}(2)	PVD threshold 2	V_{DD} rising	2.33	2.44	2.55	
		V_{DD} falling	2.23	2.34	2.44	
V_{PVD3}(2)	PVD threshold 3	V_{DD} rising	2.47	2.59	2.70	
		V_{DD} falling	2.39	2.50	2.61	
V_{PVD4}(2)	PVD threshold 4	V_{DD} rising	2.60	2.72	2.83	
		V_{DD} falling	2.50	2.62	2.73	
V_{PVD5}(2)	PVD threshold 5	V_{DD} rising	2.76	2.88	3.00	
		V_{DD} falling	2.66	2.78	2.90	
V_{PVD6}(2)	PVD threshold 6	V_{DD} rising	2.83	2.96	3.08	
		V_{DD} falling	2.76	2.88	3.00	
V_{hyst_BOR0}(2)	BOR0 hysteresis voltage	-	-	20	-	mV
$V_{hyst_BOR_PVD}$(2)	BOR1, 2, 3, 4 and PVD hysteresis voltage	-	-	80	-	
$t_{sampling_BOR0}$(2)	BOR0 ultra-low power sampling monitoring period	ULPMEN = 1	-	12	30	ms
$I_{DD_BOR_PVD}$(1)	BOR1, 2, 3, 4 and PVD consumption from V_{DD}, and additional BOR0 consumption for ULPMEN = 0 vs. ULPMEN = 1 (3)	-	-	1.7	2.5	µA

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production.
3. BOR0 is enabled in all modes, its consumption is therefore included in the supply current characteristics tables.

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5.3.7 Embedded voltage reference

The parameters in *Table 44* are derived under ambient temperature and supply voltage conditions summarized in *Table 31*.

Table 44. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	Range 1	1.175	1.209	1.243	V
		Range 2 and low power modes	1.170	1.206	1.248	
$t_{S_vrefint}$(2)	ADC sampling time when reading the internal reference voltage(3)	-	11.25	-	-	µs
$t_{start_vrefint}$(2)	Start time of reference voltage buffer when ADC is enabled	-	-	4	6	
$I_{DD(VREFINTBUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	1.5	2.1	µA
ΔV_{REFINT}(4)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V -40°C ≤ T_J ≤ +130°C	-	6.0	19.0	mV
T_{Coeff}	Temperature coefficient		-	84	155	ppm/°C
A_{Coeff}(2)	Long term stability	1000 hours, T = 25°C	-	400	-	ppm
$V_{DDCoeff1}$(2)	Voltage coefficient	3.0 V ≤ V_{DD} ≤ 3.6 V -40°C ≤ T_J ≤ +130°C	-	600	2300	ppm/V
$V_{DDCoeff2}$(2)	Voltage coefficient	1.8 V ≤ V_{DD} ≤ 3.6 V -40°C ≤ T_J ≤ +130°C	-	270	1350	
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% of V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. V_{REFINT} does not take into account package and soldering effects.
2. Specified by design, not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.
4. Evaluated by characterization, not tested in production.

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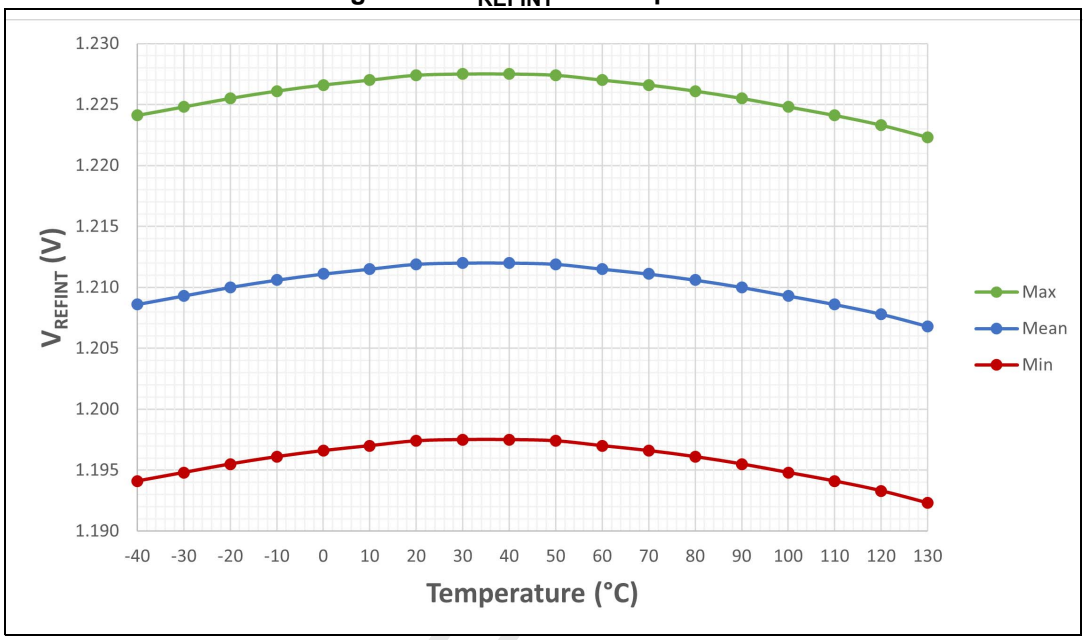
Figure 18. V_{REFINT} vs. temperature



5.3.8 Supply current characteristics

The current consumption is measured as described in *Section 5.1.7*. It depends upon several parameters, such as operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and executed binary code.

Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled, except when otherwise mentioned
- The flash memory and SRAM access time is adjusted with the minimum wait states number, depending upon the f_{HCLK} frequency (refer to tables in the reference manual).
- When the peripherals are enabled $f_{PCLKx} = f_{HCLK1}$
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Voltage range 1 for 16 MHz < f_{HCLK1} ≤ 100 MHz and 12 MHz < f_{HCLK5} ≤ 32 MHz
  - Voltage range 2 for f_{HCLK1} ≤ 16 MHz and f_{HCLK5} ≤ 12 MHz

The parameters given in *Table 45* and *Table 46* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 31*.

Table 45. Current consumption in Run modes on LDO, code with data processing running from flash memory, Cache ON (1-way), prefetch OFF, V_{DD} = 3.3 V(1)(2)(3)

Symbol	Parameter	Conditions			Typ			Unit
		-	Voltage scaling	f_{HCLK1}	25°C	55°C	85°C	
$I_{DD(Run)}$	Supply current in Run mode	f_{HCLK1} = f_{HSI16} = 16 MHz	Range 2	16 MHz	0.91	0.95	1.10	mA
		f_{HCLK1} = f_{HSE32} = 32 MHz	Range 1	32 MHz	2.29	2.41	2.73	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		100 MHz	6.16	6.30	6.63	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Reduced code used for characterization.
3. All peripherals disabled, SRAM1 and SRAM2 enabled.

Table 46. Current consumption in Run modes on SMPS, code with data processing running from flash memory, Cache ON (1-way), prefetch OFF, V_{DD} = 3.3 V(1)(2)(3)

Symbol	Parameter	Conditions			Typ			Unit
		-	Voltage scaling	f_{HCLK1}	25°C	55°C	85°C	
$I_{DD(Run)}$	Supply current in Run mode	f_{HCLK1} = f_{HSI16} = 16 MHz	Range 2	16 MHz	0.45	0.46	0.53	mA
		f_{HCLK1} = f_{HSE32} = 32 MHz	Range 1	32 MHz	1.47	1.55	1.73	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		100 MHz	3.35	3.48	3.66	

1. Guaranteed by characterization results, unless otherwise specified.
2. Reduced code used for characterization results
3. All peripherals disabled, SRAM1 and SRAM2 enabled.

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Table 47. Current consumption in Run mode on LDO, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF[1]

Symbol	Parameter	Conditions			Typ 25°C			Unit	Typ 25°C			Unit
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enabled	Range 2, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	0.96	0.96	0.96	mA	59.7	59.7	59.8	µA/MHz
				Coremark®	0.96	0.96	0.96		60.2	60.2	60.2	
				SecureMark	1.00	1.00	1.01		62.8	62.8	62.8	
				Fibonacci	0.86	0.86	0.86		53.7	53.7	53.7	
				While(1)	0.67	0.67	0.67		41.8	41.8	41.8	
			Range 1, $f_{HCLK1} = f_{HSE32}$ = 32 MHz	Reduced code	2.25	2.37	2.41		70.3	74.2	75.2	
				Coremark®	2.26	2.39	2.42		70.6	74.6	75.6	
				SecureMark	2.40	2.52	2.56		74.9	78.8	79.8	
				Fibonacci	2.06	2.18	2.22		64.3	68.2	69.2	
				While(1)	1.64	1.77	1.80		51.3	55.3	56.3	
			Range 1, f_{HCLK1} = HSE32 + PLL at 100 MHz	Reduced code	6.37	6.49	6.52		63.7	64.9	65.2	
				Coremark®	6.41	6.53	6.56		64.1	65.3	65.6	
				SecureMark	6.73	6.86	6.89		67.3	68.6	68.9	
				Fibonacci	5.85	5.97	6.01		58.5	59.7	60.1	
				While(1)	4.45	4.58	4.61		44.5	45.8	46.1	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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Table 48. Current consumption in Run mode on SMPS, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF[1]

Symbol	Parameter	Conditions			Typ 25°C			Unit	Typ 25°C			Unit
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enabled	Range 2, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	0.64	0.48	0.46	mA	40.2	30.3	29.0	µA/MHz
				Coremark®	0.65	0.49	0.47		40.7	30.5	29.1	
				SecureMark	0.68	0.50	0.48		42.3	31.5	30.0	
				Fibonacci	0.56	0.45	0.43		34.7	28.0	26.8	
				While(1)	0.47	0.37	0.36		29.3	23.4	22.6	
			Range 1, $f_{HCLK1} = f_{HSE32}$ = 32 MHz	Reduced code	1.91	1.55	1.52		59.7	48.6	47.5	
				Coremark®	1.92	1.56	1.52		60.0	48.8	47.6	
				SecureMark	2.02	1.63	1.59		63.3	50.9	49.7	
				Fibonacci	1.76	1.46	1.43		55.1	45.6	44.7	
				While(1)	1.44	1.25	1.24		45.0	39.1	38.7	
			Range 1, f_{HCLK1} = HSE32 + PLL at 100 MHz	Reduced code	5.15	3.71	3.52		51.5	37.1	35.2	
				Coremark®	5.18	3.73	3.54		51.8	37.3	35.4	
				SecureMark	5.44	3.90	3.70		54.4	39.0	37.0	
				Fibonacci	4.73	3.44	3.28		47.3	34.4	32.8	
				While(1)	3.65	2.74	2.63		36.5	27.4	26.3	

1. Guaranteed by characterization results, unless otherwise specified.

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Table 49. Current consumption in Sleep modes, flash memory in power-down(1)(2)

Symbol	Parameter	Conditions				Typ			Unit
		-	-	Voltage scaling	f_{HCLK}	25°C	55°C	85°C	
I_{DD} (Sleep)	Supply current in Sleep mode	$f_{HCLK1} = f_{HSI16}$ = 16 MHz	LDO	Range 2	16 MHz	0.34	0.38	0.52	mA
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz		Range 1	32 MHz	0.95	1.06	1.36	
		f_{HCLK1} = HSE32 + PLL > 32 MHz			100 MHz	2.14	2.25	2.56	
		$f_{HCLK1} = f_{HSI16}$ = 16 MHz	SMPS	Range 2	16 MHz	0.22	0.24	0.29	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz		Range 1	32 MHz	0.82	0.89	1.07	
		f_{HCLK1} = HSE32 + PLL > 32 MHz			100 MHz	1.50	1.59	1.77	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. All peripherals disabled.

Table 50. Flash memory static power consumption(1)

Symbol	Parameter	Conditions	Typ			Unit
			25°C	55°C	85°C	
I_{DD} (Flash)	Static consumption in normal mode	PD = 1 versus PD = 0	44.6	48.5	59.0	µA
I_{DD} (Flash_LPM)	Additional static consumption in normal versus low-power mode	LPM = 1 versus LPM = 0	25.2	26.2	28.7	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 51. Current consumption in Stop 0 mode(1)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	V_{DD}	25°C	55°C	85°C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode, SRAM2 + CACHE retained	LDO	Range 2	1.8 V	48	79	181	µA
				2.4 V	48	79	180	
				3.0 V	49	80	182	
				3.3 V	49	82	186	
				3.6 V	50	82	197	
	Supply current in Stop 0 mode, all RAMs + CACHE retained			1.8 V	49	81	186	
				2.4 V	49	81	186	
				3.0 V	49	82	188	
				3.3 V	50	83	190	
				3.6 V	51	84	203	

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Table 51. Current consumption in Stop 0 mode(1) (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	V_{DD}	25°C	55°C	85°C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode, SRAM2 + CACHE retained	SMPS	Range 2	1.8 V	15	32	94	µA
				2.4 V	12	26	74	
				3.0 V	11	23	63	
				3.3 V	11	22	60	
				3.6 V	11	22	70	
	Supply current in Stop 0 mode, all RAMs + CACHE retained			1.8 V	15	33	98	
				2.4 V	13	27	77	
				3.0 V	12	24	66	
				3.3 V	12	23	62	
				3.6 V	12	23	72	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 52. Current consumption in Stop 1 mode(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25°C	55°C	85°C	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode, SRAM1 retained, ULPMEN = 1	LDO	1.8 V	20.2	49.0	134.5	µA
			2.4 V	22.1	50.3	133.9	
			3.0 V	20.5	51.3	135.7	
			3.3 V	22.6	53.7	136.0	
			3.6 V	20.9	56.0	152.5	
		SMPS	1.8 V	10.5	26.8	85.0	
			2.4 V	8.2	20.9	66.1	
			3.0 V	6.8	17.6	55.6	
			3.3 V	6.5	16.7	52.2	
			3.6 V	6.4	18.7	62.8	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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Table 53. Current consumption in Standby retention mode(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25°C	55°C	85°C	
$I_{DD(Standby)}$	Supply current in Standby mode, SRAM1 retained, ULPMEN = 1	LDO standby retention mode	1.8 V	2.25	4.85	14.8	µA
			2.4 V	2.40	5.41	15.1	
			3.0 V	2.39	5.66	15.5	
			3.3 V	2.58	5.51	16.2	
			3.6 V	2.76	8.52	17.6	
		SMPS standby retention mode	1.8 V	1.07	2.85	9.83	
			2.4 V	0.87	2.35	8.35	
			3.0 V	0.81	2.20	7.80	
			3.3 V	0.93	2.35	7.99	
			3.6 V	1.23	2.88	8.83	
	Supply current in Standby mode, all SRAMs + BLE retained, ULPMEN = 1	LDO standby retention mode	1.8 V	3.71	8.46	25.9	
			2.4 V	4.06	9.06	26.2	
			3.0 V	3.74	9.33	26.8	
			3.3 V	4.23	10.1	27.4	
			3.6 V	4.89	13.1	29.0	
		SMPS standby retention mode	1.8 V	1.87	4.90	16.7	
			2.4 V	1.49	3.94	13.6	
			3.0 V	1.31	3.50	12.1	
			3.3 V	1.37	3.57	12.0	
			3.6 V	1.67	4.51	12.6	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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Table 54. Current consumption in Standby mode(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25°C	55°C	85°C	
$I_{DD(Standby)}$	Supply current in Standby mode, all peripherals disabled	ULPMEN = 1	1.8 V	0.16	0.58	3.02	µA
			2.4 V	0.18	0.64	3.29	
			3.0 V	0.24	0.79	3.81	
			3.3 V	0.37	1.06	4.50	
			3.6 V	0.71	1.69	5.93	
		ULPMEN = 0	1.8 V	1.26	1.71	4.05	
			2.4 V	1.61	2.07	4.57	
			3.0 V	2.00	2.54	5.34	
			3.3 V	2.29	2.96	6.18	
			3.6 V	2.81	3.77	7.71	
	Supply current in Standby mode, IWDG enabled	Clocked by LSI1, ULPMEN = 0	1.8 V	1.44	1.82	3.74	
			2.4 V	1.81	2.22	4.25	
			3.0 V	2.24	2.71	4.99	
			3.3 V	2.55	3.14	5.78	
			3.6 V	3.07	3.91	7.18	
		Clocked by LSI1 / 128, ULPMEN = 0	1.8 V	1.37	1.74	3.67	
			2.4 V	1.71	2.12	4.13	
			3.0 V	2.10	2.58	4.85	
			3.3 V	2.40	2.98	5.61	
			3.6 V	2.89	3.73	7.01	

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Table 54. Current consumption in Standby mode[1] (continued)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25°C	55°C	85°C	
$I_{DD(Standby\ with\ RTC)}$	Supply current in Standby mode, no IWDG, RTC enabled	Clocked by LSI1, ULPMEN = 0	1.8 V	1.48	1.85	3.78	µA
			2.4 V	1.87	2.27	4.30	
			3.0 V	2.31	2.78	5.06	
			3.3 V	2.64	3.22	5.86	
			3.6 V	3.17	4.02	7.27	
		Clocked by LSI1 / 128, ULPMEN = 0	1.8 V	1.36	1.74	3.67	
			2.4 V	1.71	2.12	4.15	
			3.0 V	2.11	2.58	4.85	
			3.3 V	2.40	2.98	5.61	
			3.6 V	2.90	3.75	7.02	
		Clocked by LSE bypass 32.768 kHz, ULPMEN = 0	1.8 V	1.51	1.89	4.03	
			2.4 V	1.91	2.32	4.55	
			3.0 V	2.36	2.84	5.36	
			3.3 V	2.70	3.28	6.16	
			3.6 V	3.24	4.06	7.61	
		Clocked by LSE crystal 32.768 kHz in medium low-drive, ULPMEN = 0	1.8 V	1.66	1.98	3.43	
			2.4 V	2.03	2.37	3.90	
			3.0 V	2.45	2.89	4.77	
			3.3 V	2.76	3.32	5.54	
			3.6 V	3.29	4.06	6.84	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

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I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Section 5.3.17*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

An additional current consumption is due to I/Os configured as inputs when an intermediate voltage level is applied externally. This is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is the case of ADC input pins, which must be configured as analog inputs.

Caution: Any floating input pin can settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

I/O dynamic current consumption

The I/Os used in application increase the consumption measured previously (see *Table 55*). When an I/O pin switches, it uses the current from the I/O supply voltage to supply the pin circuitry, and to charge/discharge the capacitive load (internal and external) connected to it:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
  - C_{INT} is the I/O pin capacitance
  - C_{EXT} is any connected external device pin capacitance
  - C_S is the PCB board capacitance

The pin is configured in push-pull output mode, and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The power consumption of the digital part of the peripherals is given in *Table 55*, while that of the analog part (when applicable) is indicated in the related sections.

The MCU is put under the following conditions:

- All I/O pins are in analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- The ambient operating temperature and supply voltage conditions summarized in *Table 31*

Table 55. Peripheral typical dynamic current consumption(1)

Bus	Peripheral	Range 1 LDO	Range 2 LDO	Range 1 SMPS	Range 2 SMPS	Unit
AHB1	AHB1 bus	0.27	0.19	0.13	0.07	µA/MHz
	SRAM1	0.29	0.22	0.15	0.08	
	TSC	1.25	0.92	0.62	0.35	
	CRC	0.30	0.22	0.15	0.08	
	RAMCFG	0.22	0.17	0.11	0.06	
	GPDMA1	1.48	1.10	0.73	0.42	
	ICACHE	0.46	0.34	0.23	0.13	
	FLASH interface	1.70	1.26	0.85	0.48	
	GTZC1	0.48	0.36	0.24	0.14	

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Table 55. Peripheral typical dynamic current consumption(1) (continued)

Bus	Peripheral	Range 1 LDO	Range 2 LDO	Range 1 SMPS	Range 2 SMPS	Unit
AHB2	AHB2 bus(2)	0.27	0.18	0.13	0.08	µA/MHz
	SRAM2	0.34	0.26	0.17	0.09	
	PKA	4.91	3.63	2.43	1.38	
	HSEM	0.08	0.07	0.04	0.02	
	SAES	65.22	48.52	32.36	18.44	
	RNG	0.88	0.69	0.44	0.25	
	HASH	1.47	1.11	0.74	0.41	
	AES	1.77	1.34	0.89	0.50	
	GPIOA	0.05	0.06	0.04	0.02	
	GPIOB	0.06	0.06	0.04	0.02	
	GPIOC	0.03	0.05	0.02	0.01	
	GPIOH	0.02	0.05	0.02	0.01	
AHB4	AHB4 bus	0.00	0.03	0.00	0.01	µA/MHz
	ADC4 kernel clock domain	1.60	1.17	0.79	0.46	
	ADC4 bus clock domain	2.76	2.03	1.37	0.77	
	PWR	0.04	0.02	0.03	0.01	
AHB5	AHB5 bus + peripherals(3)	0.07	0.05	0.03	0.02	µA/MHz
APB1	AHB to APB1(4)	0.00	0.00	0.00	0.00	µA/MHz
	TIM2	3.00	2.22	1.49	0.85	
	TIM3	2.65	1.96	1.31	0.74	
	WWDG	0.21	0.16	0.11	0.06	
	USART2 kernel clock domain	2.81	2.07	1.38	0.77	
	USART2 bus clock domain	1.35	1.00	0.66	0.38	
	I2C1 kernel clock domain	1.79	1.34	0.90	0.51	
	I2C1 bus clock domain	2.52	1.85	1.24	0.70	
	LPTIM2 kernel clock domain	2.87	2.13	1.42	0.81	
	LPTIM2 bus clock domain	3.83	2.82	1.89	1.07	

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Table 55. Peripheral typical dynamic current consumption(1) (continued)

Bus	Peripheral	Range 1 LDO	Range 2 LDO	Range 1 SMPS	Range 2 SMPS	Unit
APB2	AHB to APB2(4)	0.62	0.46	0.31	0.18	µA/MHz
	TIM1	4.67	3.45	2.33	1.31	
	SPI1 kernel clock domain	0.91	0.68	0.45	0.25	
	SPI1 bus clock domain	2.45	1.82	1.20	0.69	
	TIM17	1.65	1.22	0.81	0.47	
	TIM16	1.63	1.22	0.81	0.46	
	USART1 kernel clock domain	3.21	2.39	1.60	0.91	
	USART1 bus clock domain	4.66	3.45	2.31	1.31	
	SAI1 kernel clock domain	0.95	0.70	0.47	0.27	
	SAI1 bus clock domain	1.37	1.03	0.67	0.39	
APB7	AHB to APB7(4)	0.27	0.22	0.13	0.09	µA/MHz
	SYSCFG	0.32	0.24	0.16	0.09	
	SPI3 kernel clock domain	1.01	0.74	0.50	0.28	
	SPI3 bus clock domain	2.32	1.71	1.16	0.65	
	LPUART1 kernel clock domain	2.79	2.05	1.37	0.78	
	LPUART1 bus clock domain	3.97	2.94	1.98	1.12	
	I2C3 kernel clock domain	1.78	1.32	0.88	0.50	
	I2C3 bus clock domain	2.52	1.86	1.25	0.71	
	LPTIM1 kernel clock domain	4.40	3.26	2.19	1.25	
	LPTIM1 bus clock domain	5.33	3.96	2.65	1.51	
	COMP	0.19	0.14	0.09	0.05	
	RTC/TAMP	1.81	1.34	0.90	0.51	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. The AHB bus is automatically active when at least one peripheral is ON on the AHB or associated APB.
3. RADIO inactive.
4. The AHB to APB bridge is automatically active when at least one peripheral is ON on the APB.

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5.3.9 Wake-up time from low-power modes and voltage scaling transition times

The times given in *Table 56* are the latency between the event and the execution of the first user instruction (FSTEN = 1 in PWR_CR3 if not mentioned differently).

The device goes in Low-power mode after the WFE (Wait For Event) instruction.

Table 56. Low-power mode wake-up timings - LDO(1)

Symbol	Parameter	Conditions	Typ	Unit
$t_{WU(Sleep)}$	Wake-up time from Sleep to Run mode	SLEEP_PD = 0	14	CPU clock cycles
$t_{WU(Stop\ 0)}$	Wake-up time from Stop 0 to Run mode in flash memory, SRAMs retained	FLASHFWU = 0	9.98	µs
	Wake-up time from Stop 0 to Run mode in SRAM2	FLASHFWU = 0	10.4	
$t_{WU(Stop\ 1)}$	Wake-up time from Stop 1 to Run mode in flash memory, SRAMs retained	FLASHFWU = 0	24.1	µs
	Wake-up time from Stop 1 to Run mode in SRAM2	FLASHFWU = 0	24.7	
$t_{WU(Standby\ with\ Retention)}$	Wake-up time from Standby retention to Run mode in flash memory	FSTEN = 1	48.5	µs
		FSTEN = 0	48.5	
$t_{WU(Standby)}$	Wake-up time from Standby to Run mode in flash memory	FSTEN = 1	101.6	µs
		FSTEN = 0	553.4	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 57. Low-power mode wake-up timings - SMPS(1)

Symbol	Parameter	Conditions	Typ	Unit
$t_{WU(Sleep)}$	Wake-up time from Sleep to Run mode	SLEEP_PD = 0	14	CPU clock cycles
$t_{WU(Stop\ 0)}$	Wake-up time from Stop 0 to Run mode in flash memory, SRAMs retained	FLASHFWU = 0	9.92	µs
	Wake-up time from Stop 0 to Run mode in SRAM2	FLASHFWU = 0	10.4	
$t_{WU(Stop\ 1)}$	Wake-up time from Stop 1 to Run mode in flash memory, SRAMs retained	FLASHFWU = 0	17.9	µs
	Wake-up time from Stop 1 to Run mode in SRAM2	FLASHFWU = 0	18.2	
$t_{WU(Standby\ with\ Retention)}$	Wake-up time from Standby retention to Run mode in flash memory	FSTEN = 1	42.2	µs
		FSTEN = 0	43.2	
$t_{WU(Standby)}$	Wake-up time from Standby to Run mode in flash memory	FSTEN = 1	101.6	µs
		FSTEN = 0	553.4	

1. Guaranteed by characterization results, unless otherwise specified.

Table 58. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Unit
t_{LDO}	SMPS to LDO transition time	Range 2	21.5	µs
		Range 1	17.2	
t_{SMPS}	LDO to SMPS transition time	Range 2	21.1	
		Range 1	20.2	

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Table 58. Regulator modes transition times(1) (continued)

Symbol	Parameter	Conditions	Typ	Unit
t_{VOST}(2)	Range 2 to range 1	LDO	47.3	µs
		SMPS	53.9	
	Range 1 to range 2(3)	LDO	39.0	
		SMPS	39.8	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Time for ACTVOSRDY in PWR_SVMSR to indicate the selected new VOS range.
3. VOSRDY remains at 1 on a transition from range 1 to range 2.

Table 59. Wake-up time using USART/LPUART(1)

Symbol	Parameter	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baudrate needed to wake up from Stop mode when USART/LPUART kernel clock source is HSI16	-	$t_{su(HSI16)}$ max	µs

1. Specified by design, not tested in production.

5.3.10 External clock source characteristics

High-speed external clock

The high-speed external (HSE32) clock can be supplied with a 32 MHz crystal or a clock source. The devices include internal programmable capacitances that can be used to trim the crystal frequency, to compensate the PCB parasitic one.

Table 60. HSE32 crystal requirements(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSE}	Oscillator frequency(2)	-		-	32	-	MHz
f_{TOL}	Frequency tolerance(3)	Includes initial accuracy, stability over temperature, aging, and frequency pulling due to incorrect load capacitance	Bluetooth LE	-50	-	50	ppm
C_L	Load capacitance	-		8	-	18	pF
C_O	Shunt capacitance	-		-	-	4	
ESR	Equivalent series resistance	-		60	-	150	Ω
C_{bank}	Capacitor bank range	-		6.6	-	23.6	pF
$C_{bank\text{-}step}$	Capacitor bank step size	-		215	270	325	fF
t_{STAB}	Oscillator stabilization time	-		-	100	160	µs
$I_{DDRF(HSE32)}$	Current consumption	-		-	205	-	µA

1. Specified by design, not tested in production.
2. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.
3. After capacitor bank trimming.

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Table 61. HSE32 clock source requirements(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSE32}	External clock source frequency(2)	-		-	32	-	MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, and aging	Bluetooth LE	-50	-	50	ppm
			IEEE802.15.4	-40	-	40	
V_{HSE32}	Clock input voltage limits	Input level		0	-	0.9	V
		Amplitude(3)		200	-	900	mV_{PP}
$DuCy_{HSE32}$	Duty cycle	-		45	-	55	%
$\varphi_{n(HSE32)}$	Phase noise for 32 MHz	Offset = 10 kHz		-	-	-127	dBc/Hz
		Offset = 100 kHz		-	-	-135	
		Offset = 1 MHz		-	-	-138	

1. Specified by design, not tested in production.
2. $f_{HSE} = 1 / t_{HSE}$.
3. AC coupling is supported (470 pF to 100 nF capacitor).

Note: For information about oscillator trimming, refer to AN5042 "Precise HSE frequency and startup time tuning for STM32 wireless MCUs", available on www.st.com.

Low-speed external clock

The low-speed external (LSE) clock can be supplied with a crystal or a clock source. The information provided in this section is based on design simulation results, obtained with the typical external components specified in *Table 62*. In the application, the crystal and the load capacitors must be placed as close as possible to the oscillator pins, to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 62. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{LSE}	Oscillator frequency(2)	-		-	32.000 or 32.768	-	kHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance	Bluetooth LE	-500	-	500	ppm
$I_{DD(LSE)}$	LSE current consumption	LSEDRV = medium-low drive capability		-	450	-	nA
		LSEDRV = medium-high drive capability		-	590	-	
		LSEDRV = high drive capability		-	700	-	
$Gm_{critmax}$	Maximum critical crystal Gm	LSEDRV = medium-low drive capability		-	-	0.75	µA/V
		LSEDRV = medium-high drive capability		-	-	1.70	
		LSEDRV = high drive capability		-	-	2.70	

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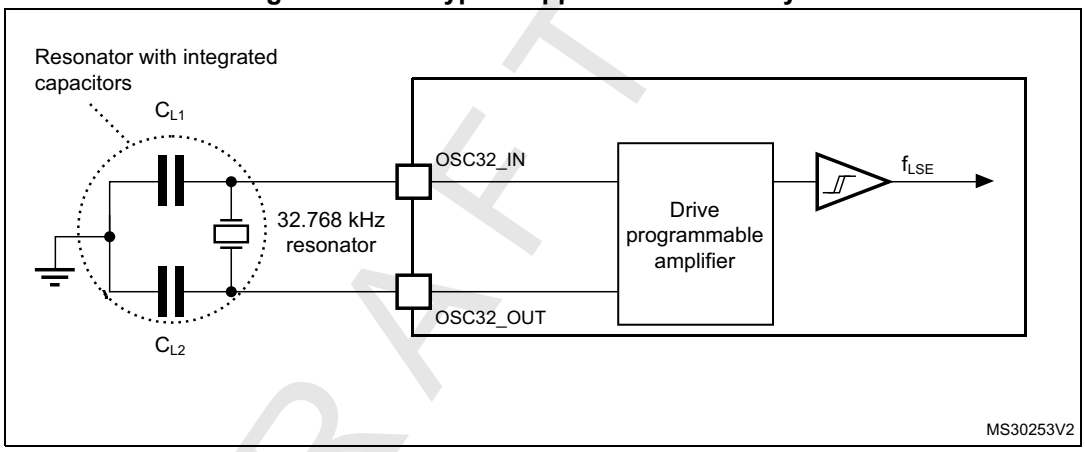
Table 62. LSE oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{S_PARA}	Internal stray parasitic capacitance(3)	-	-	3	-	pF
$t_{SU(LSE)}$	Startup time(4)	V_{DD} is stabilized	-	2	-	s

1. Specified by design, not tested in production.
2. For information on selecting the crystal, refer to AN2867 '*Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs*".
3. CS_PARA is the equivalent capacitance seen by the crystal due to OSC32_IN and OSC32_OUT internal parasitic capacitances.
4. Time measured from when the LSE is enabled by software, until a stable LSE oscillation is reached. This value is measured for a standard crystal, and can vary significantly with the crystal used.

Figure 19. LSE typical application with a crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

Table 63. LSE clock source requirements(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{LSE}	External clock source frequency(2)	-		32.000	32.768	-	kHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, and aging	Bluetooth LE	-500	-	500	ppm
			Thread CSL	-255	-	255	
V_{LSE_ext}	Clock input voltage range	-		0	-	V_{DD}	V
$V_{LSE_ext_PP}$	Clock input peak-to-peak amplitude(3)	-		0.3	-	V_{DD}	V
$DuCy_{LSE}$	Duty cycle	-		40	-	60	%

1. Specified by design, not tested in production.
2. $f_{LSE} = 1/t_{LSE}$.
3. AC coupled is supported (10 pF capacitor).

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The clock input waveforms are shown in *Figure 20* and *Figure 21*.

Figure 20. LSE external square clock source AC timing diagram

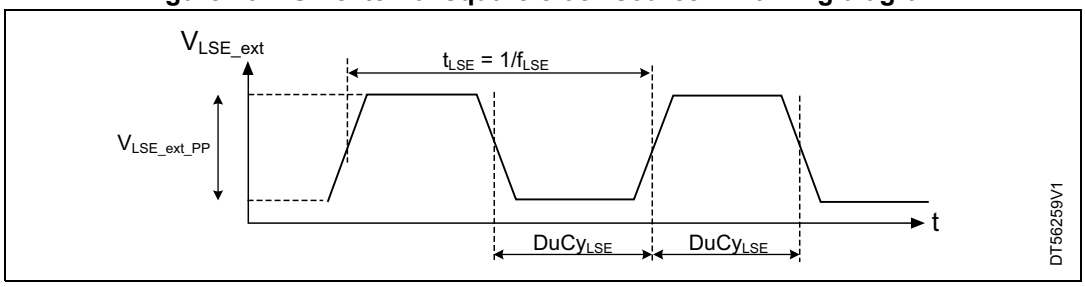
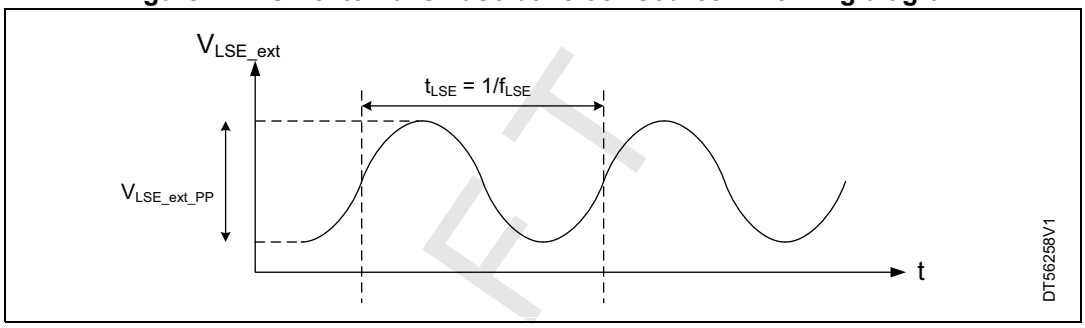


Figure 21. LSE external sinusoidal clock source AC timing diagram



In bypass mode the LSE oscillator is switched off, and the input pin OSC32_IN is a standard GPIO.

Table 64. LSE external clock bypass mode characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(2)	-	32.000	32.768	-	kHz
f_{TOL}	Frequency tolerance (Bluetooth LE)	Includes initial accuracy and stability over temperature	-500	-	500	ppm
V_{IL}	OSC32_IN input low level voltage	-	-	-	0.3 x V_{DD}	V
V_{IH}	OSC32_IN input high level voltage	-	0.7 x V_{DD}	-	-	V
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN input high or low time for square signal	-	10	-	-	µs

1. Specified by design, not tested in production.
2. $f_{LSE} = 1/t_{LSE}$.

5.3.11 Internal clock source characteristics

The parameters given in the following tables are derived under ambient operating temperature and supply voltage conditions summarized in *Table 31*.

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High-speed internal (HSI16) RC oscillator

Table 65. HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency after factory calibration	V_{DD} = 3.0 V, T_J = 30°C calibrated during production	15.92	16	16.08	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -10 to 100°C(1)	15.84	16	16.16	
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -40 to 130°C (1)	15.65	16	16.35	
TRIM(2)	User trimming step	-	18	29	40	kHz
$DuCy_{HSI16}$(2)	Duty cycle	-	45	-	55	%
$t_{su(HSI16)}$(2)	Startup time	-	-	2.5	3.6	µs
$t_{stab(HSI16)}$(2)	Stabilization time	-	-	4	6	
$I_{DD(HSI16)}$(2)	Power consumption	-	-	150	210	µA

1. Evaluated by characterization, not tested in production, unless otherwise specified. It does not take into account package and soldering effects.
2. Specified by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 66. LSI1 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI1}	Frequency	V_{DD} = 3.0 V, T_J = 30°C, LSI1PREDIV = 1	0.245	0.25	0.255	kHz
		V_{DD} = 3.0 V, T_J = 30°C, LSI1PREDIV = 0	31.4	32.0	32.6	
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -40 to 85°C, LSI1PREDIV = 0 (1)	30.4	32.0	33.6	
$DuCy_{LSI1}$	Duty cycle	LSI1PREDIV = 1	-	50	-	%
$t_{SU(LSI1)}$(2)	Startup time	-	-	230	260	µs
$t_{STAB(LSI1)}$(2)	Stabilization time	5% of final frequency	-	230	260	
$I_{DD(LSI1)}$(2)	Power consumption	LSI1PREDIV = 0	-	140	255	nA
		LSI1PREDIV = 1	-	130	240	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Specified by design, not tested in production.

Table 67. LSI2 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI2}	Frequency	-	24	32	48	kHz
$t_{SU(LSI2)}$(1)	Startup time	-	550	-	750	µs
$t_{STAB(LSI2)}$(1)	Stabilization time	5% of final frequency	-	650	1100	

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Table 67. LSI2 oscillator characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Δ_{TEMP}(2)	Stability over temperature	-	-200	-	200	ppm/°C
$I_{DD(LSI2)}$(2)	Power consumption	-	-	1	2	µA

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.12 PLL characteristics

The parameters given in *Table 68* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 31*.

Table 68. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(1)	PLL input clock	-	4	-	16	MHz
$DuCy_{PLL_IN}$(1)	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}(1)	PLL output clock P, Q, and R	-	1	-	100	MHz
$DuCy_{PLL_OUT}$(1)	PLL output clock duty cycle	Division 1	40	-	60	%
f_{VCO_OUT}(1)	PLL VCO output	-	128	-	544	MHz
t_{LOCK}(2)	PLL lock time(3)	Integer mode	-	25	54	µs
		Fractional mode	-	40	65	
Jitter(1)	RMS cycle-to-cycle jitter	Integer mode, VCO = 544 MHz	-	±20	-	ps
		Fractional mode, VCO = 544 MHz	-	±70	-	
	RMS period jitter	Integer mode, VCO = 544 MHz	-	±35	-	
		Fractional mode, VCO = 544 MHz	-	±45	-	
	Long-term jitter(4) f_{PLL_IN} = 8 MHz	Integer mode, VCO = 544 MHz	-	±160	-	
		Fractional mode, VCO = 544 MHz	-	±170	-	
$I_{DD(PLL)}$(1)	PLL power consumption on V_{DD} with LDO	VCO freq = 100 MHz	-	370	-	µA
		VCO freq = 200 MHz	-	460	-	
		VCO freq = 336 MHz	-	710	-	
		VCO freq = 544 MHz	-	1100	-	
	PLL power consumption on V_{DD} with SMPS	VCO freq = 100 MHz, 1 clock output	-	260	-	µA
		VCO freq = 100 MHz, 3 clock outputs	-	270	-	
		VCO freq = 200 MHz, 1 clock output	-	320	-	
		VCO freq = 336 MHz, 1 clock output	-	470	-	
		VCO freq = 544 MHz, 1 clock output	-	730	-	

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production, unless otherwise specified.
3. Lock time is the duration until PLL1RDY flag (2% of final frequency).

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4. Measured on 5000 cycles.

5.3.13 Flash memory characteristics

Table 69. Flash memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}(2)	128-bit programming time	Normal mode	118	118	µs
		Burst mode	48	48	
t_{prog_page}(2)	One 8-Kbyte page programming time	f_{AHB} = 100 MHz, normal mode	62	-	ms
		f_{AHB} = 100 MHz, burst mode	24.9	-	
t_{prog_flash}(2)	1-Mbyte programming time	f_{AHB} = 100 MHz, normal mode	7930	-	
		f_{AHB} = 100 MHz, burst mode	3180	-	
t_{ERASE}(2)	One 8-Kbyte page erase time	10 k endurance cycles	1.5	2.4	
		100 k endurance cycles(3)	1.7	3.4	
t_{ME}(2)	Mass erase time	10 k endurance cycles	195	308	
I_{DD}(4)	Average consumption from V_{DD}	Write mode	2.1	-	mA
		Erase mode	1.3	-	
	Maximum current (peak) from V_{DD}	Write mode	2.6	-	
		Erase mode	3.0	-	

1. Evaluated by characterization after cycling, not tested in production.
2. Specified by design, not tested in production, unless otherwise specified.
3. Erase time applies to all pages in user area in flash main memory (only 32 pages can be cycled more than 10 k times)
4. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 70. Flash memory endurance and data retention(1)

Symbol	Parameter	Conditions		Min	Unit
N_{END}	Endurance	Whole user flash	T_A = –40 to +85°C	10	kcycles
		Limited to 32 pages in user area		100	
t_{RET}	Data retention(2)	Whole user flash	T_A = 85°C after 1 kcycles	30	Years
			T_A = 55°C after 10 kcycles	30	
			T_A = 85°C after 10 kcycles	15	
		Limited to 32 pages in user area	T_A = 55°C after 100 kcycles	30	
			T_A = 85°C after 100 kcycles	15	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Cycling performed over the whole temperature range.

5.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

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Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs as follows:

- ESD (electrostatic discharge), positive and negative: applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB (fast transient voltage burst), positive and negative: applied to V_{DD} and V_{SS} pins through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 71*. They are based on the EMS levels and classes defined in AN1709 "*EMC design guide for STM8, STM32 and legacy MCUs*".

Table 71. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25°C, f_{HCLK1} = 100 MHz, UFQFPN48 conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to apply through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25°C, f_{HCLK1} = 100 MHz, UFQFPN48 conforming to IEC 61000-4-4	5A

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software.

Good EMC performance is highly dependent on the user application, and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the requested EMC level.

Software recommendations

The software flow must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or on the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specified values. When an unexpected behavior is detected, the software can be hardened to prevent the occurrence of unrecoverable errors. See AN1015 "*Software techniques for improving microcontrollers EMC performance*" for more details.

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Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 72. EMI characteristics for f_{HSE} = 32 MHz and f_{HCLK} = 100 MHz(1)

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak level(2)	V_{DD} = 3.6 V, T_A = 25°C, UFQFPN48 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	23	dBµV
			30 MHz to 130 MHz	21	
			130 MHz to 1 GHz	13	
			1 GHz to 2 GHz	15	
	Level(3)		EMI level	3.5	-

1. Evaluated by characterization, not tested in production.
2. Refer to AN1709, “EMI radiated test” section.
3. Refer to AN1709, “EMI level classification” section.

5.3.15 Electrical sensitivity characteristics

Based on three different tests (ESD, latch-up) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 73. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Package	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C, conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25°C, conforming to ANSI/ESDA/JEDEC JS-002	WLCSP41	C1	250	
			UFQFPN32	C2A	500	
			UFQFPN48			
			UFBGA59			

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

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These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 74. Electrical sensitivity(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 130 °C conforming to JESD78E	2

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller if abnormal injection accidentally happens, some susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter, such as an ADC error above a certain limit (higher than 5 LSB ET), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA / 0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 75*. The negative/positive induced leakage current is caused by the negative/positive injection.

Table 75. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins	5	N/A	mA

1. Evaluated by characterization, not tested in production, unless otherwise specified.

5.3.17 I/O port characteristics

General input/output characteristics

The parameters given in *Table 76* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 31*. All I/Os are designed as CMOS- and TTL-compliant.

Note: For information on I/O configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”.

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Table 76. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	1.58 V ≤ V_{DD} ≤ 3.6 V	-	-	0.3 x V_{DD}	V
V_{IH}	I/O input high level voltage		0.7 x V_{DD}	-	-	
V_{hys}(1)	Input hysteresis	-	-	250	-	mV
I_{lkg}(1)	I/O input leakage current(2)(3)	V_{IN} ≤ Max(V_{DD}, V_{DDA})	-	-	150	nA
		Max(V_{DD}, V_{DDA}) < V_{IN} ≤ Max(V_{DD}, V_{DDA}) + 1 V	-	-	2000	
		Max(V_{DD}, V_{DDA}) + 1 V < V_{IN} ≤ 5.5 V	-	-	500	
R_{PU}	Weak pull-up equivalent resistor(4)	-	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	-	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Specified by design, not tested in production.
2. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x I_{lkg} max.
3. To sustain a voltage higher than Min (V_{DD}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.
4. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).

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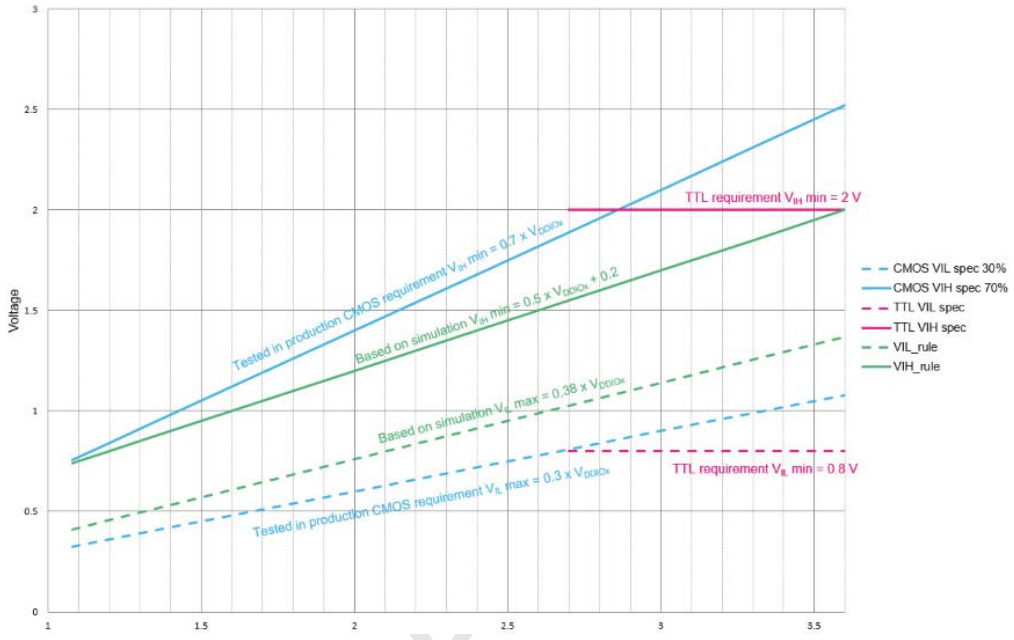
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22*.

Figure 22. I/O input characteristics (all I/Os except PH3)



Output driving current

The I/Os can sink or source up to ±8 mA, up to ±20 mA with a relaxed V_{OL} / V_{OH}.

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 28*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 28*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 77* are at ambient temperature and under the supply voltage conditions summarized in *Table 31*. All I/Os are CMOS- and TTL-compliant.

Table 77. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage	$\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage		V_{DD} - 0.4	-	
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(2)	Output high level voltage		V_{DD} - 1.3	-	
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 4 mA, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage		V_{DD} - 0.4	-	
V_{OLFM+}(2)	Output low level voltage for an I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 27*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{(PIN)}$.
2. Specified by design, not tested in production.

Output AC characteristics

Unless otherwise specified, the parameters given in *Table 78* are at ambient temperature and under the supply voltage conditions summarized in *Table 31*.

The definition and values of output AC characteristics are given, respectively, in *Figure 23* and in *Table 78*.

Table 78. Output AC characteristics(1)(2)

Speed(3)	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C_L = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	MHz
			C_L = 50 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	5	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	5	
	t_r/t_f	Output rise and fall time	C_L = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	ns
			C_L = 50 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	33	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	25	
01	Fmax	Maximum frequency	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	MHz
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	12.5	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	12.5	
	t_r/t_f	Output rise and fall time	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	10	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.2	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	7.5	

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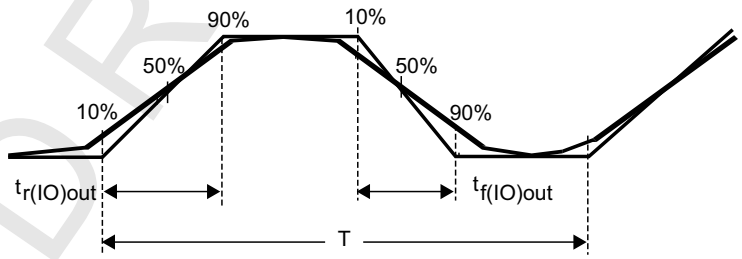
Table 78. Output AC characteristics(1)(2) (continued)

Speed(3)	Symbol	Parameter	Conditions	Min	Max	Unit
10(4)	Fmax	Maximum frequency	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	33	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	100	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	40	
	t_r/t_f	Output rise and fall time	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	6.0	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.0	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	4.1	
Fm+	Fmax	Maximum frequency	C_L = 550 pF, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	1	MHz
	t_f	Output fall time(5)	C_L = 550 pF, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	100	ns
			C_L = 100 pF, 1.58 V ≤ V_{DD} < 3.6 V	-	50	

1. Specified by design, not tested in production.
2. PB15 and PH3 output and input frequency must not exceed 16 kHz, PC14 and PC15 output and input frequency must not exceed 250 kHz, for these IOs OSPEED must be kept at low speed.
3. The I/O speed is configured using the OSPEED bits, Fm+ is configured in SYSCFG. Refer to the product reference manual for the description.
4. I/O compensation system enabled.
5. The fall time is defined between 70% and 30% of the output waveform according to the I^2C specification.

Figure 23. Output AC characteristics definition



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

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5.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

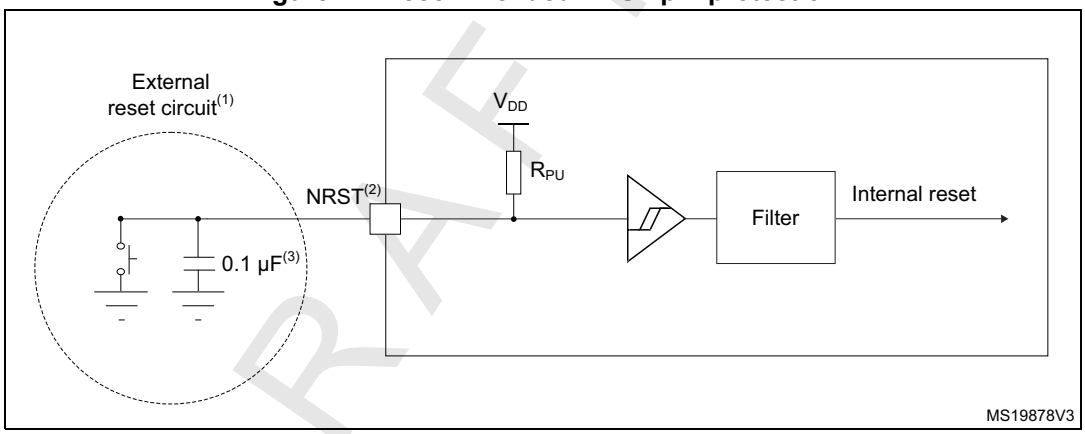
Unless otherwise specified, the parameters given in *Table 79* are at ambient temperature and under the supply voltage conditions summarized in *Table 31*.

Table 79. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	Input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	Input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{F(NRST)}$	Input filtered pulse	-	-	-	50	ns
$t_{NF(NRST)}$	Input not-filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	330	-	-	
		1.58 V ≤ V_{DD} < 1.71 V	1000	-	-	

1. Specified by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS, whose contribution to the series resistance is minimal (~10%).

Figure 24. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ maximum level specified in *Table 79*, or the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.19 Extended interrupt and event controller input (EXTI) characteristics

Pulses on the extended interrupt and event controller inputs must have a minimal length, to guarantee they are detected.

Table 80. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(EXTI)}$	Pulse length to event controller	-	20	-	-	ns

1. Specified by design, not tested in production.

5.3.20 Wake-up pin (WKUP) characteristics

Pulses on the wake-up pin inputs must have a minimal length, to ensure their detection.

Table 81. WKUP input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(WKUP)}$	Pulse length to wake up	-	20	-	-	ns

1. Specified by design, not tested in production.

5.3.21 Analog switch booster

Table 82. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.6	1.8	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	-	-	125	µA

1. Specified by design, not tested in production.

5.3.22 12-bit Analog-to-Digital converter (ADC4) characteristics

Unless otherwise specified, the parameters given in the following tables are derived at ambient temperature, and under the f_{HCLK} frequency and supply voltage conditions summarized in *Table 31*.

Note: It is recommended to perform a calibration after each power-up.

Table 83. 12-bit ADC4 characteristics (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
f_{ADC}	ADC clock frequency	-	0.14	-	55	MHz
$DuCy_{ADC}$	ADC clock duty cycle	-	45	-	55	%
f_s	Sampling rate	Resolution 12 bits	0.01	-	2.75	Msps
		Resolution 10 bits	0.0120	-	3.05	
		Resolution 8 bits	0.0140	-	3.43	
		Resolution 6 bits	0.0175	-	3.92	
t_{TRIG}	External trigger period	Resolution 12 bits	16	-	-	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(4)	External input impedance	Resolution 12 bits, T_j = 130°C	-	-	2.2	kΩ
		Resolution 10 bits, T_j = 130°C	-	-	6.8	
		Resolution 8 bits, T_j = 130°C	-	-	33.0	
		Resolution 6 bits, T_j = 130°C	-	-	47.0	

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Table 83. 12-bit ADC4 characteristics (1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
$t_{ADCVREG_STUP}$	ADC voltage regulator startup time	-	-	-	25	µs
t_{STAB}	ADC power-up time	-	(3 x 1/f_{ADC}) + 1 conversion			cycle
t_{OFF_CAL}	Offset calibration time	-	82			1/f_{ADC}
t_{LATR}	Trigger conversion latency	WAIT = 0, AUTOFF = 0, DPD = 0, f_{ADC} = HCLK	4			
		WAIT = 0, AUTOFF = 1, DPD = 0, f_{ADC} = HCLK/2	4			
		WAIT = 0, AUTOFF = 1, DPD = 1, f_{ADC} = HCLK/4	3.75			
t_s	Sampling time	-	1.5	-	814.5	
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits, VREFPROTEN = 0	t_s + N + 0.5			
		Resolution = N bits, VREFPROTEN = 1, VREFSECSMP = 0	t_s + N + 0.5	-	t_s + N + 1.5	
		Resolution = N bits, VREFPROTEN = 1, VREFSECSMP = 1	t_s + N + 0.5	-	t_s + N + 2.5	
$I_{DDA(ADC)}$	ADC consumption on V_{DDA}	f_s = 2.5 Msps	-	378	-	µA
		f_s = 1 Msps	-	190	-	
		f_s = 10 ksps	-	10	-	
		AUTOFF = 1, DPD = 0, no conversion	-	9	-	
		AUTOFF = 1, DPD = 1, no conversion	-	0.11	-	

1. Specified by design, not tested in production.
2. The voltage booster on the ADC switches must be used when V_{DDA} < 2.4 V (embedded I/O switches).
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. The tolerance is two LSBs.

Table 84. Maximum R_{AIN} for 12-bit ADC4(1) (2) (3)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
12 bits	47	276	12.5	19.5
	68	288		
	100	306		
	150	336		

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Table 84. Maximum R_{AIN} for 12-bit ADC4(1) (2) (3) (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
12 bits (continued)	220	377	19.5	39.5
	330	442		
	470	526		
	680	650	39.5	
	1000	840		79.5
	1500	1134		
	2200	1643	79.5	814.5
	3300	2395	814.5	
	4700	3342		
	6800	4754		
	10000	6840		
	15000	9967		
	22000	14068		
	33000	19933		N/A
10 bits	47	86	3.5	7.5
	68	90		
	100	95		
	150	108	7.5	
	220	116		
	330	136		
	470	161		12.5
	680	212		
	1000	276	12.5	19.5
	1500	376	19.5	39.5
	2200	516		79.5
	3300	735	39.5	
	4700	1012		
	6800	1423	79.5	814.5
	10000	2040	814.5	814.5
	15000	2978		
	22000	4356		
	33000	6443		
	47000	8925		

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Table 84. Maximum R_{AIN} for 12-bit ADC4(1) (2) (3) (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
8 bits	47	45	3.5	3.5
	68	46		
	100	48		
	150	53		
	220	59		
	330	69		7.5
	470	81		
	680	101	7.5	
	1000	130		
	1500	177		12.5
	2200	242	12.5	19.5
	3300	345		
	4700	475	19.5	39.5
	6800	670	39.5	
	10000	963		79.5
	15000	1417	79.5	
	22000	2040		814.5
	33000	2995	814.5	
	47000	4158		
6 bits	47	32	1.5	3.5
	68	32		
	100	33		
	150	35		
	220	37		
	330	41		
	470	49	3.5	
	680	61		
	1000	79		7.5
	1500	106	7.5	
	2200	146		12.5
	3300	207		
	4700	286	12.5	19.5
	6800	404	19.5	39.5
	10000	584	39.5	

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Table 84. Maximum R_{AIN} for 12-bit ADC4(1) (2) (3) (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
6 bits (continued)	22000	1250	79.5	79.5
	33000	1853		814.5
	47000	2607	814.5	

1. Specified by design, not tested in production.
2. BOOSTEN and ANASWVDD configured according to V_{DD} and V_{DDA} levels.
3. Values without external capacitance.

Table 85. 12-bit ADC4 accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	-	-	±3	±7.5	LSB
EO	Offset error		-	±2	±5.5	
EG	Gain error		-	±2	±6.5	
ED	Differential linearity error		-	-0.9/+1.0	-0.9/+1.5	
EL	Integral linearity error		-	±2	±3.5	
ENOB	Effective number of bits		9.9	10.9	-	bits
SINAD	Signal-to-noise and distortion ratio		61.4	67.4	-	dB
SNR	Signal-to-noise ratio		61.6	67.5	-	
THD	Total harmonic distortion		-	-74	-70	

1. Evaluated by characterization, not tested in production.
2. DC accuracy values are measured after internal calibration.
3. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (resolution = 12 bits, no oversampling).

Figure 25. ADC accuracy characteristics

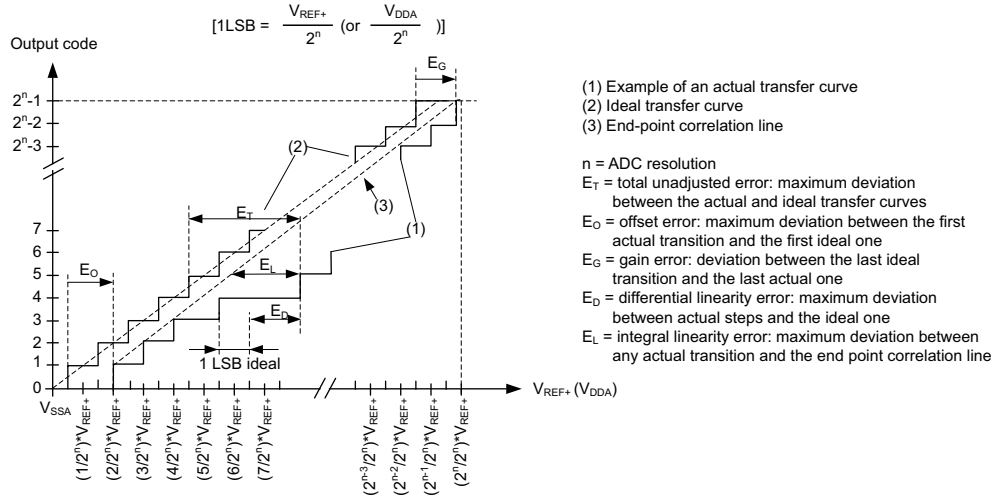

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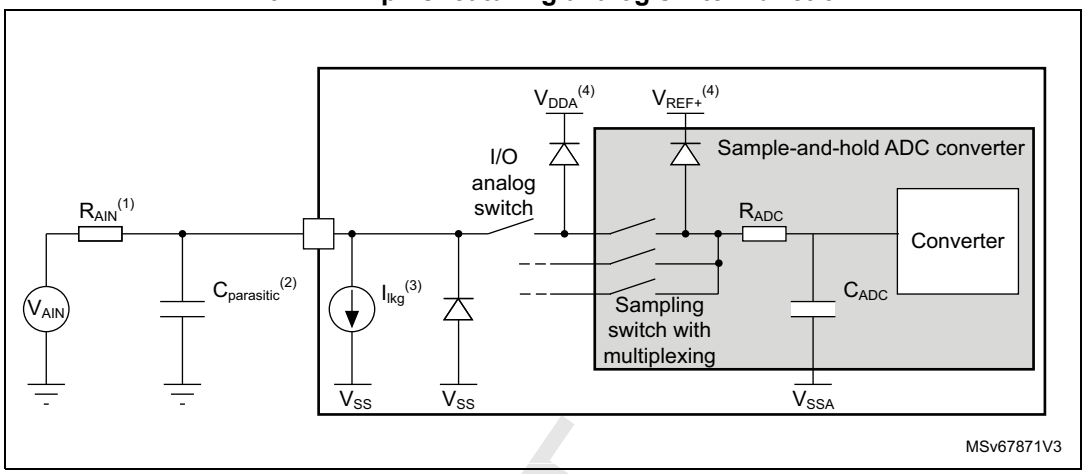
Figure 26. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. Refer to *Table 83* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the PCB capacitance (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 76* for its values). A high $C_{parasitic}$ value downgrades the conversion accuracy. As a remedy, reduce f_{ADC}.
3. Refer to *Table 76* for the values of I_{lkg}.
4. Refer to *Figure 14*, *Figure 15*, and *Figure 16*.

5.3.23 Temperature sensor characteristics

Table 86. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)(2)	V_{SENSE} linearity with temperature	-	-	1.3	°C
Avg_Slope(3)	Average slope	2	2.5	3.0	mV/°C
$V_{SENSE30}$(4)	V_{SENSE} voltage at V_{DDA} = 3.0 V (±10 mV) and 30 °C (±1°C)	700	742	800	mV
($V_{continous0}$ - $V_{sampling}$)(2)	Voltage difference between continuous and sampling modes(5)	-10	-	+4	mV
$t_{START(TS_BUF)}$(2)	Sensor buffer startup time	-	1	10	µs
t_{S_temp}(2)	ADC sampling time when reading the temperature	13	-	-	µs
$I_{DD(TS)}$(2)	Consumption from V_{DD}, when selected by ADC	-	14	20	µA

1. V_{SENSE} linearity depends upon calibration points. When using TS_CALx calibration points, linearity within the calibration limits is degraded by ±5°C. Linearity outside the calibration limits is degraded more, due to the extrapolation.
2. Specified by design, not tested in production.
3. Evaluated by characterization, not tested in production, unless otherwise specified.
4. The $V_{SENSE30}$ ADC4 conversion result is stored in the TS_CAL1 field.
5. The temperature sensor is in continuous mode when the regulator is in range 1, in sampling mode when the regulator is in range 2 or the device is in Stop 1 mode.

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5.3.24 V_{CORE} monitoring characteristics

Table 87. V_{CORE} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. Specified by design, not tested in production.

5.3.25 Comparator characteristics

Table 88. COMP characteristics(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.58	-	3.6	V
V_{IN}	Input voltage range	-		0	-	V_{DDA}	V
t_{START}(3)	Startup time to reach propagation delay specification	High-speed mode		-	-	8	µs
		Intermediate mode		-	-	12	
		Medium mode		-	-	16	
		Ultra-low-power mode		-	-	60	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode		-	50	100	ns
		Intermediate mode		-	240	490	
		Medium mode		-	400	740	
		Ultra-low-power mode		-	4	7.5	µs
V_{offset}(3)	Offset error	Full common mode range		-	±8	±20	mV
V_{hys}(3)	Hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	13	-	
		Medium hysteresis		-	26	-	
		High hysteresis		-	39	-	
I_{bias}(3)	Input bias current	-			(4)		nA
$I_{DDA(COMP)}$(3)	Consumption from V_{DDA}	High-speed mode	Static	-	43	72	µA
			With 50 kHz ±100 mV overdrive square signal	-	44	73	
		Intermediate mode	Static	-	8.5	14	
			With 50 kHz ±100 mV overdrive square signal	-	9	15	
		Medium mode	Static	-	4.0	7.0	
			With 50 kHz ±100 mV overdrive square signal	-	4.5	7.5	
		Ultra-low power mode	Static	-	0.38	1.05	
			With 50 kHz ±100 mV overdrive square signal	-	1.5	2.5	

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1. Specified by design, not tested in production, unless otherwise specified.
2. Input capacitance is negligible when compared to the I/O capacitance.
3. Evaluated by characterization, not tested in production.
4. Mostly I/O leakage when used in analog mode. Refer to I_{lkg} parameter in *Table 76: I/O static characteristics*.

5.3.26 Timer characteristics

The parameters given in the following tables are specified by design. Refer to *Section 5.3.17* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 89. TIMx(1) characteristics(2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	10	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 100 MHz	0	50	
Res_{TIM}	Timer resolution	TIM1, TIM3, TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER16}$	16-bit counter period	-	1	2^{16}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 100 MHz	0.01	655.36	µs
$t_{COUNTER32}$	32-bit counter period	-	1	2^{32}	$t_{TIMxCLK}$
		$f_{TIM2CLK}$ = 100 MHz	0,01	42.94	s

1. TIMx, is used as a general term, where x stands for 1, 2, 3, 16, or 17.
2. Specified by design, not tested in production.

Table 90. IWDG min/max timeout period at 32 kHz(1)(2)

Prescaler divider	PR[3:0] bits	Min timeout RL[11:0] = 0x002	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.325	512	ms
/8	1	0.750	1024	
/16	2	1.500	2048	
/32	3	3.0	4096	
/64	4	6.0	8192	
/128	5	12.0	16384	
/256	6	24.0	32768	
/512	7	48.0	65536	
/1024	Others	96.0	131072	

1. The exact timings depend upon the phasing of the APB interface clock vs. the IWDG kernel clock, hence there is always a full kernel clock period of uncertainty.
2. Specified by design, not tested in production.

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Table 91. WWDG min/max timeout value at 100 MHz (PCLK)

Prescaler divider	WDGTB[2:0]	Min timeout value	Max timeout value	Unit
/1	0	0.040	1.621	ms
/2	1	0.081	5.242	
/4	2	0.163	10.485	
/8	3	0.327	20.971	
/16	4	0.655	41.943	
/32	5	1.310	83.886	
/64	6	2.621	167.772	
/128	7	5.242	335.544	

5.3.27 I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

The I²C timings are valid when the I2C peripheral is properly configured (see the reference manual).

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. I²C SDA and SCL use I/O FT structure with _f option supporting Fm+ low-level output-current maximum requirement. Refer to *Section 5.3.17* for I²C I/O characteristics.

All I²C SDA and SCL I/Os embed an analog filter, refer to *Table 92* for its characteristics.

Table 92. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by the analog filter	50(2)	190(3)	ns

1. Specified by design, not tested in production.
2. Spikes with widths below t_{AF} min are filtered.
3. Spikes with widths above t_{AF} max are not filtered.

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5.3.28 USART characteristics

Unless otherwise specified, the parameters given in *Table 93* are derived under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 31*, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell activated
- Voltage scaling range 1

Refer to *Section 5.3.17* for more details on the I/O input/output characteristics (NSS, CK, TX, RX for USART).

Table 93. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	12.5	MHz
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	33.0	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	35.5	
		Slave transmitter, 1.71 V ≤ V_{DD} < 2.7 V	-	-	25.0	
$t_{su(NSS)}$	NSS setup time	Slave mode(2)	t_{ker} + 2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	4	-	-	
$t_{w(CKH)}$ $t_{w(CKL)}$	SCK high and low time	Master mode	(1 / f_{CK}) / 2 - 1	(1 / f_{CK}) / 2	(1 / f_{CK}) / 2 + 1	
$t_{su(RX)}$	Data input setup time	Master mode	18.5	-	-	
		Slave mode	1.5	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0.5	-	-	
		Slave mode	2.0	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	14	
		Slave mode, 1.71 V ≤ V_{DD} < 2.7 V	-	12	20	
		Master mode	-	0.5	1	
$t_{h(TX)}$	Data output hold time	Slave mode	10	-	-	
		Master mode	0	-	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. t_{ker} is the usart_ker_ck_pres clock period.

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Figure 27. USART timing diagram in master mode

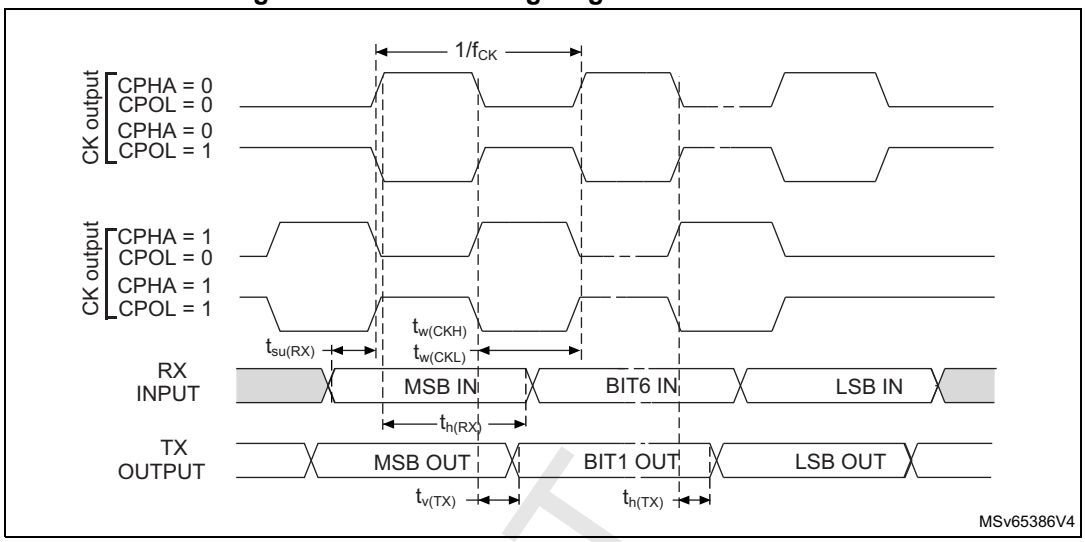
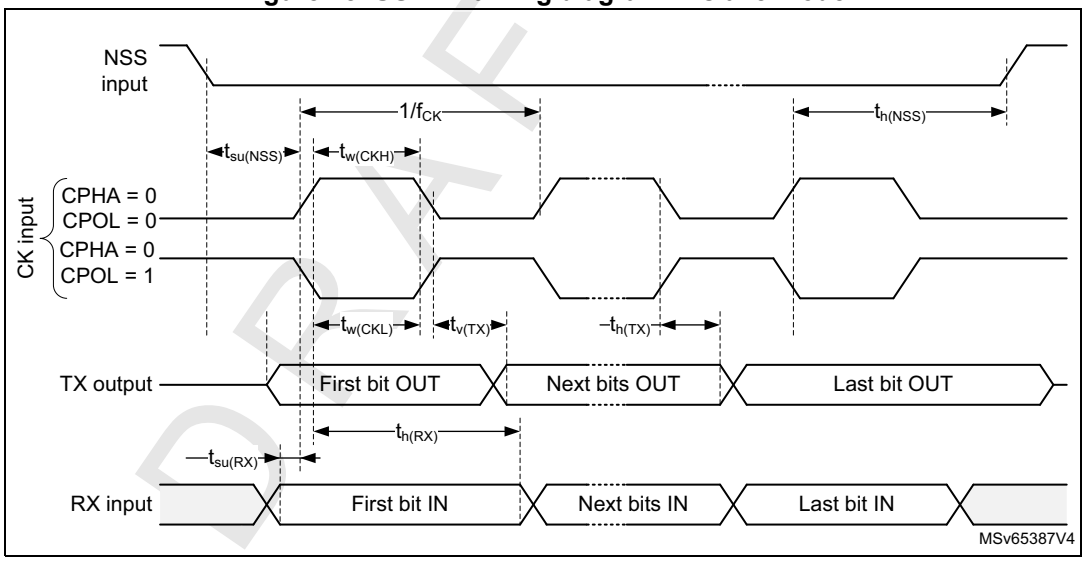


Figure 28. USART timing diagram in slave mode



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5.3.29 SPI characteristics

Unless otherwise specified, the parameters given in *Table 94* are under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 31*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell activated

Refer to *Section 5.3.17* for more details on the I/O input/output characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 94. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{SCK}$	Clock frequency	Master receiver mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	50	MHz
		Master receiver mode 1.71 V ≤ V_{DD} < 2.7 V			33	
		Master transmitter mode 2.7 V ≤ V_{DD} < 3.6 V			50	
		Master transmitter mode 1.71 V ≤ V_{DD} < 2.7 V			33	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V			100	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1			35.5(2)	
		Slave transmitter mode 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1			24(2)	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2			16	
$t_{su(NSS)}$	NSS setup time	Slave mode	$4*T_{pclk}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2*T_{pclk}$	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode(3)	$t_{SCK}/2 - 1$	$t_{SCK}/2$	$t_{SCK}/2 + 1$	
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	2.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2.0	-	-	
$t_{h(SI)}$		Slave mode	1.0	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	10.5	21.0	
$t_{dis(SO)}$	Data output disable time		10.5	13.0	21.0	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1	-	10.5	14.0	ns
		Slave mode (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1	-	16.5	20.5	
		Slave mode (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2	-	14.0	18.5	
		Slave mode (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V, voltage range 2	-	21.0	25.5	
$t_{v(MO)}$		Master mode	-	0.5	2.0	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Evaluated by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

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3. $t_{SCK} = t_{spi_ker_ck}$ x baudrate prescaler

Figure 29. SPI timing diagram - Slave mode and CPHA = 0

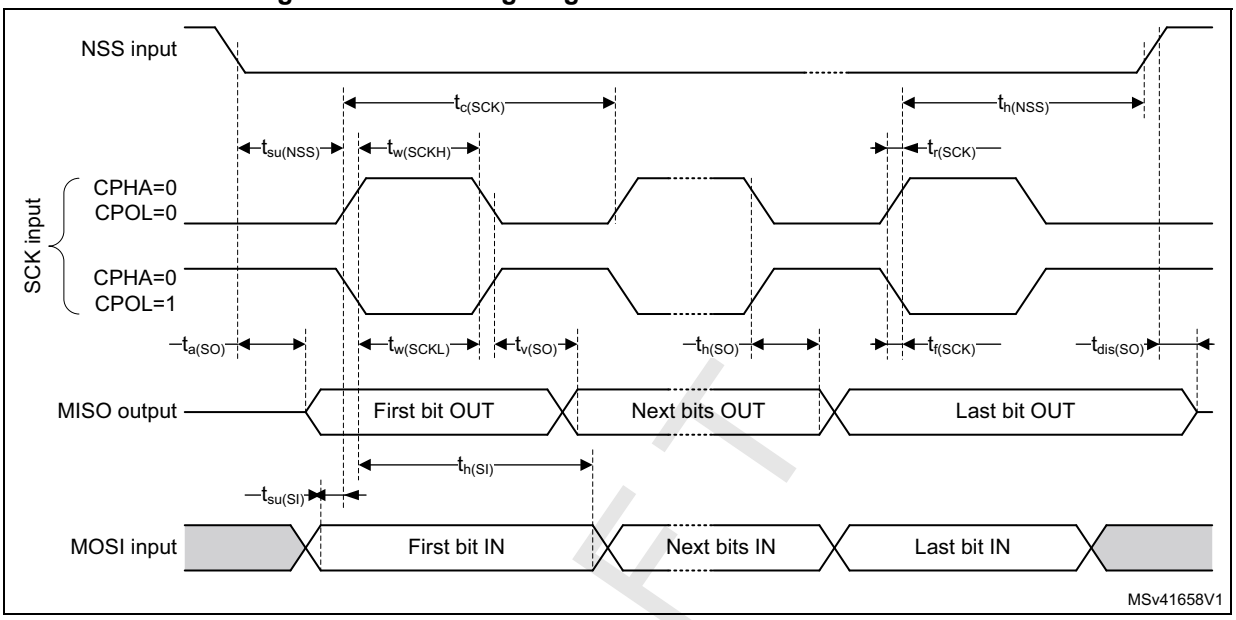

Figure 30. SPI timing diagram - Slave mode and CPHA = 1

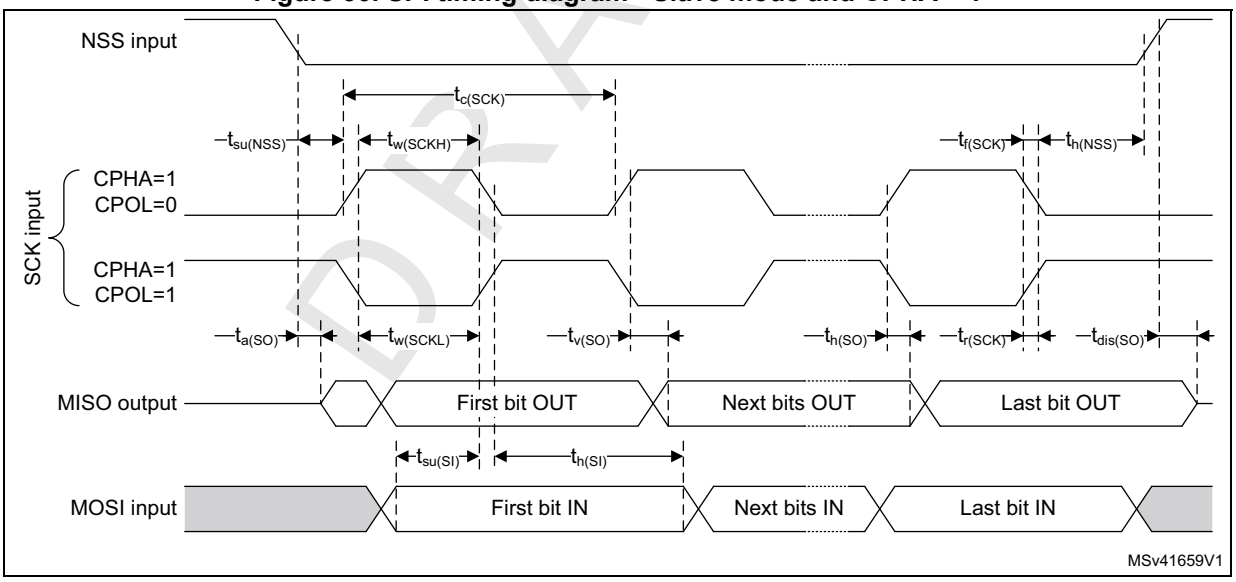

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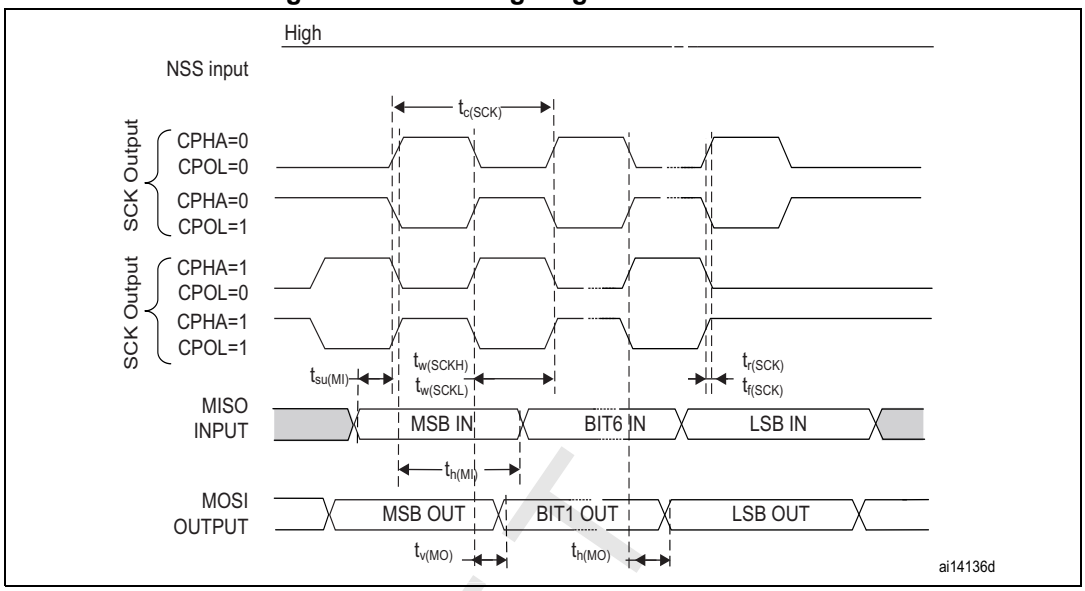
Figure 31. SPI timing diagram - Master mode



5.3.30 SAI characteristics

Unless otherwise specified, the parameters given in *Table 95* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 31*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- I/O compensation cell activated
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 3.14* and to *Section 4.1* for more details on the input/output alternate function characteristics (SCK, SD, WS).

Table 95. SAI characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	Main clock output	-	-	50	MHz
f_{CK}	Clock frequency	Master transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	25	
		Master transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	17	
		Master receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	17	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 1	-	26	
		Slave transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage range 1	-	18.5	
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage range 2	-	14	
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage range 2	-	50	

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Table 95. SAI characteristics[(1)(2)] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(FS)}$	F_S valid time	Master mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19	ns
		Master mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	29	
$t_{su(FS)}$	F_S setup time	Slave mode	1.5	-	
$t_{h(FS)}$	F_S hold time	Master mode	10	-	
		Slave mode	1.5	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	5.0	-	
$t_{su(SD_B_SR)}$		Slave receiver	3.5	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	1.5	-	
$t_{h(SD_B_SR)}$		Slave receiver	0.5	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1	-	19	
		Slave transmitter (after enable edge), 1.71 V ≤ V_{DD} ≤ 3.6 V, voltage range 1	-	27	
		Slave transmitter (after enable edge), 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2	-	27	
		Slave transmitter (after enable edge), 1.71 V ≤ V_{DD} ≤ 3.6 V, voltage range 2	-	35	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge) Voltage range 1	10.5	-	
		Slave transmitter (after enable edge) Voltage range 2	16	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	20	
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} ≤ 3.6 V	-	29	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	8.5	-	

1. Evaluated by characterization - Not tested in production.
2. APB clock frequency must be at least two times the SAI clock frequency.

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Figure 32. SAI master timing waveforms

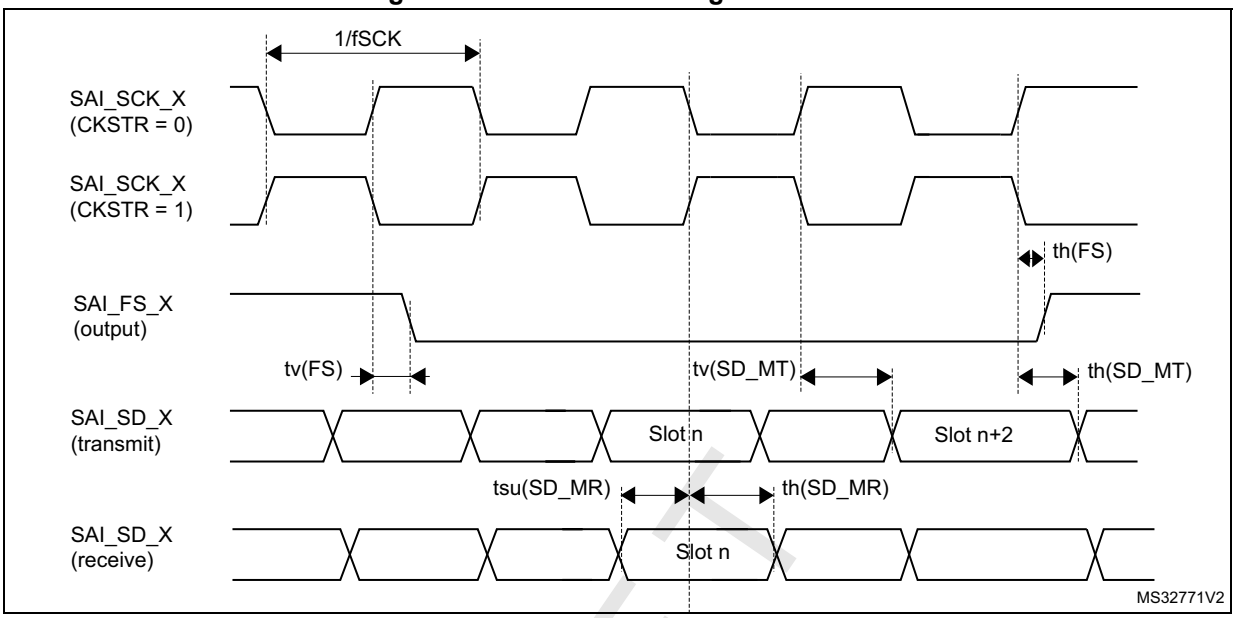
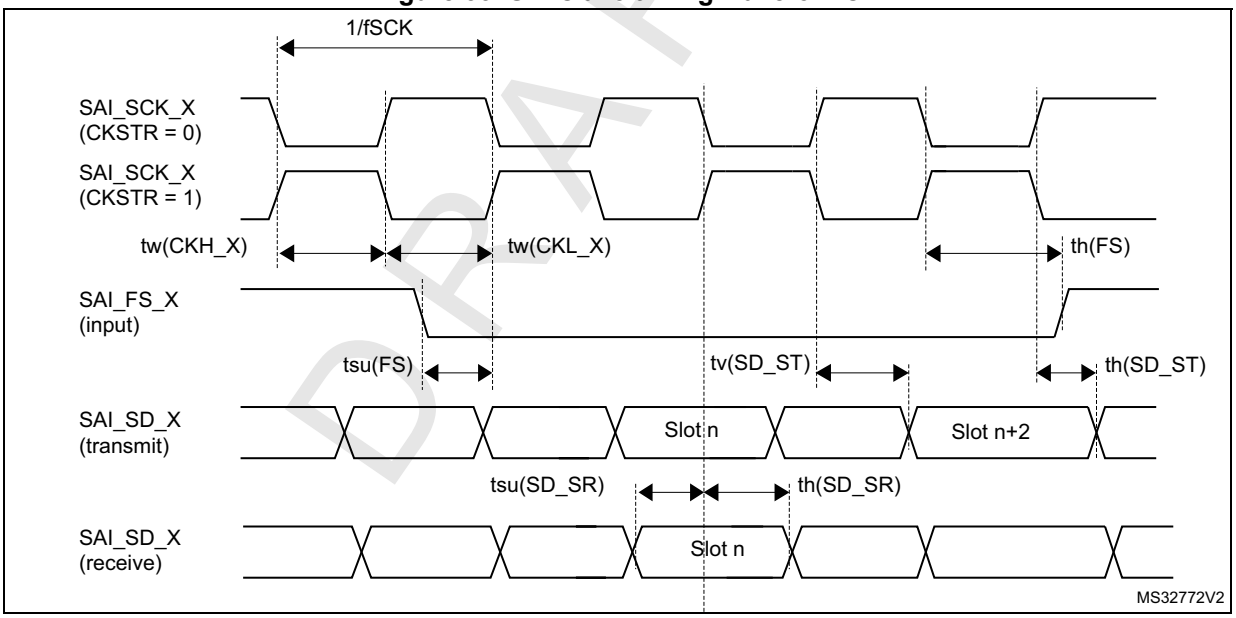


Figure 33. SAI slave timing waveforms



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5.3.31 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in the tables below are with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 00
- Capacitive load C = 30 pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell disabled

Table 96. JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TCK} $1/t_{c(TCK)}$	TCK clock frequency	$2.7 \le V_{DD} \le 3.6$ V	-	-	30	MHz
		$1.71 \le V_{DD} < 2.7$ V	-	-	20.5	
$t_{isu(TMS)}$	TMS input setup time	-	1.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	3	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	9	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	0	-	-	
$t_{ov(TDO)}$	TDO output valid time	$2.7 \le V_{DD} \le 3.6$ V	-	13	16.5	
		$1.71 \le V_{DD} < 2.7$ V	-	13	24	
$t_{oh(TDO)}$	TDO output hold time	-	10	-	-	

1. Evaluated by characterization, not tested in production.

Table 97. SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SWCLK} $1/t_{c(SWCLK)}$	SWCLK clock frequency	$2.7 \le V_{DD} \le 3.6$ V	-	-	62.5	MHz
		$1.71 \le V_{DD} < 2.7$ V	-	-	34	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	1	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	2.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	$2.7 \le V_{DD} \le 3.6$ V	-	12	16	
		$1.71 \le V_{DD} < 2.7$ V	-	12	29	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8.5	-	-	

1. Evaluated by characterization, not tested in production.

Figure 34. JTAG timing diagram

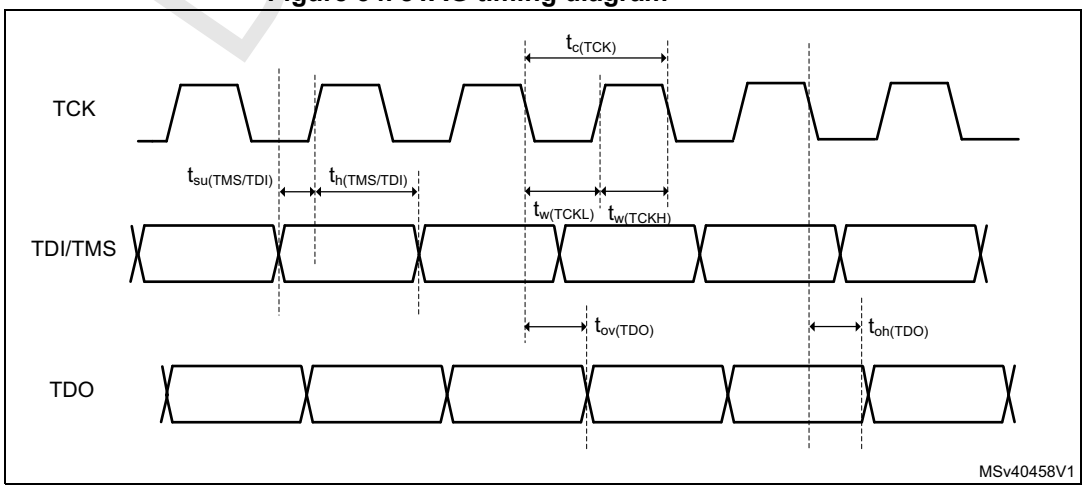

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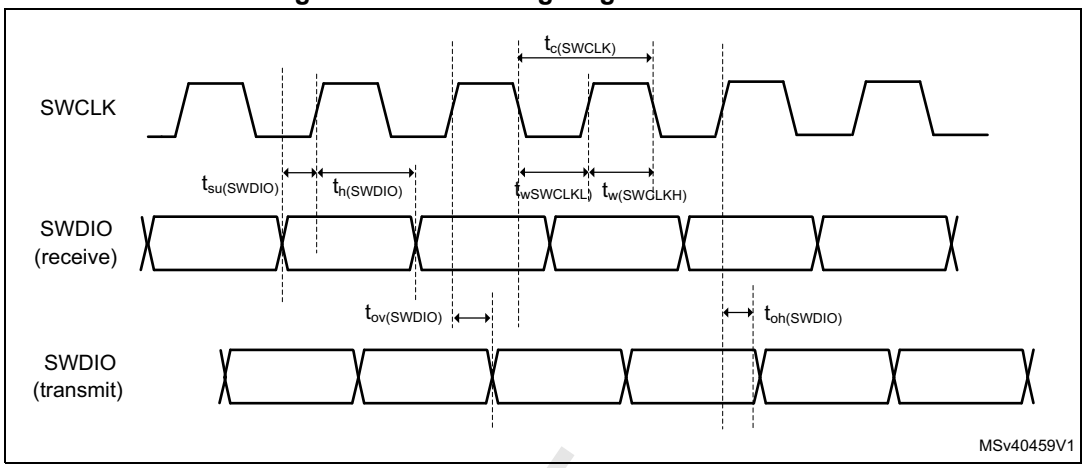
Figure 35. SWD timing diagram



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6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to "*Reference device marking schematics for STM32 microcontrollers and microprocessors*" (TN1433), available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

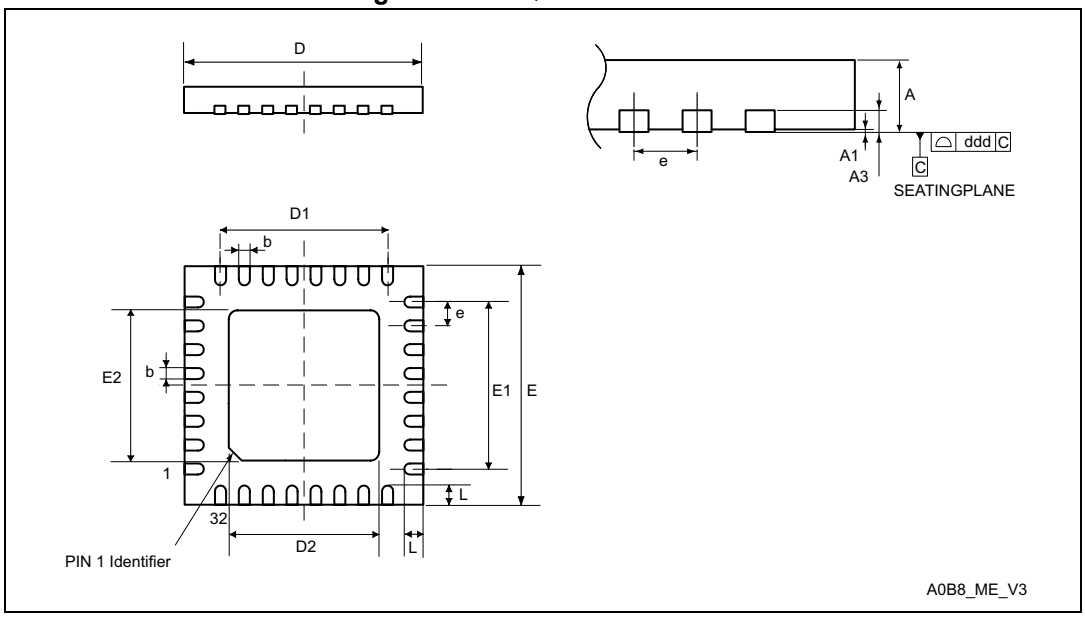
Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

6.2 UFQFPN32 package information (A0B8)

This UFQFPN is a 32-pin, 5 x 5 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 36. UFQFPN32 - Outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is mandatory to connect and

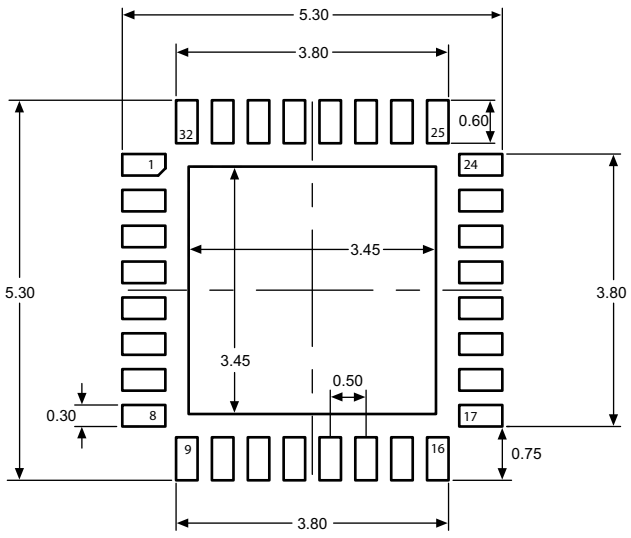
solder this back-side pad to PCB ground.

Table 98. UFQFPN32 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	-	0.300	0.0071	-	0.0118
D[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	-	3.700	0.1339	-	0.1457
D2	3.400	-	3.600	0.1339	-	0.1417
E[2]	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	-	3.700	0.1339	-	0.1457
E2	3.400	-	3.700	0.1339	-	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not to exceed 0.15 mm.

Figure 37. UFQFPN32 - Recommended footprint

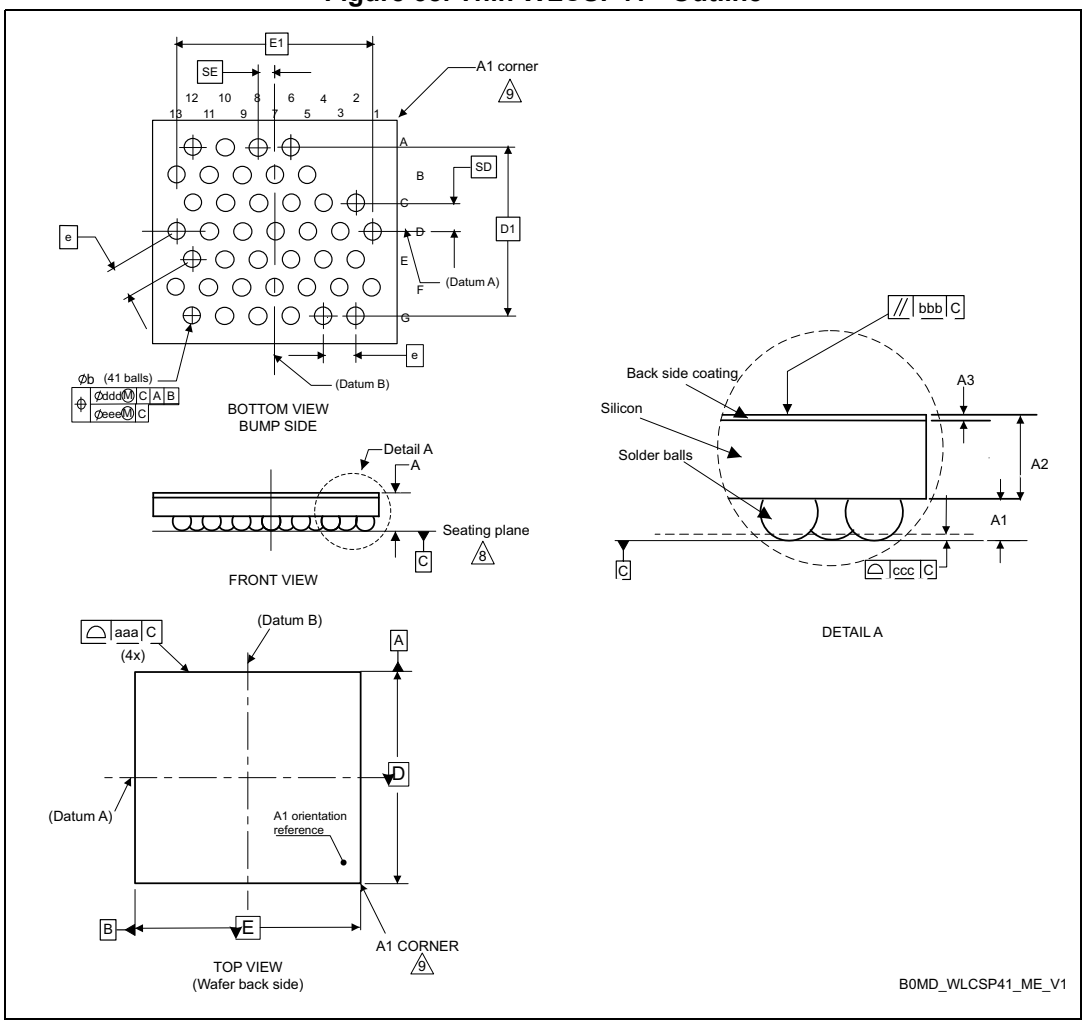


1. Dimensions are expressed in millimeters.

6.3 Thin WLCSP41 package information (B0MD)

This WLCSP is a 41-ball, 2.76 x 2.98 mm, thin wafer level chip scale package.

Figure 38. Thin WLCSP41 - Outline



1. Drawing is not to scale.

Table 99. Thin WLCSP41 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.5	-	-	0.0197
A1[3]	0.14	-	-	0.0055	-	-
A2	-	0.31	-	-	0.0122	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.20	0.23	0.25	0.0079	0.0091	0.0098
D	2.76 BSC[5]			0.1087 BSC		
D1	2.08 BSC			0.0819 BSC		
E	2.98 BSC			0.1173 BSC		
E1	2.40 BSC			0.0945 BSC		
e[6]	0.40 BSC			0.0157 BSC		
N[7]	41					
SD[8]	0.35 BSC			0.0138 BSC		
SE[8]	0.20 BSC			0.0079 BSC		
aaa[9]	0.02			0.0008		
bbb[9]	0.06			0.0024		
ccc[9]	0.03			0.0012		
ddd[9]	0.015			0.0006		
eee[9]	0.05			0.0020		

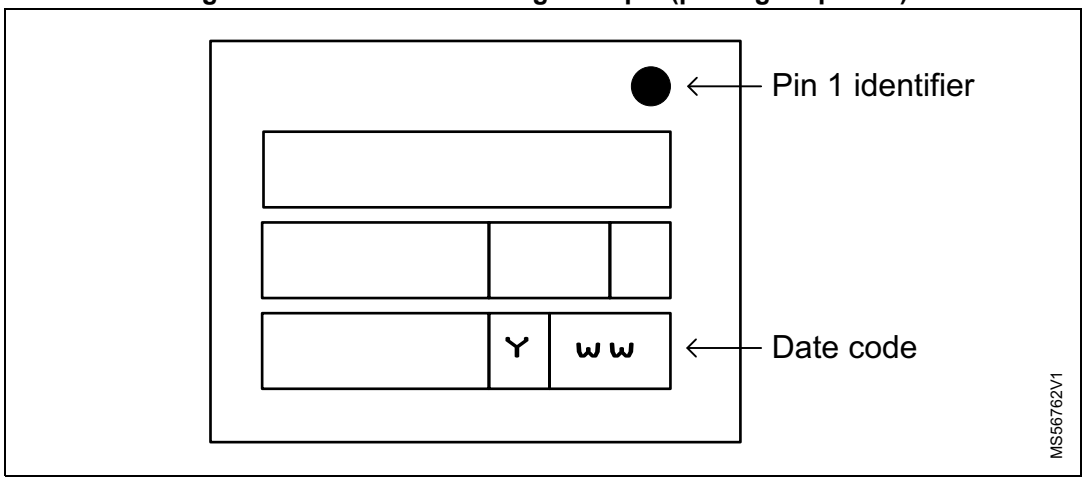
1. Values in inches are converted from mm and rounded to four decimal digits.
2. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
5. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance.
6. e represents the solder ball grid pitch.
7. N represents the total number of balls on the BGA.
8. Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.
9. Tolerance of form and position definitions.

Device marking for thin WLCSP41

Figure 39 gives an example of topside marking orientation versus pin 1 identifier location. The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 39. WLCSP41 marking example (package top view)

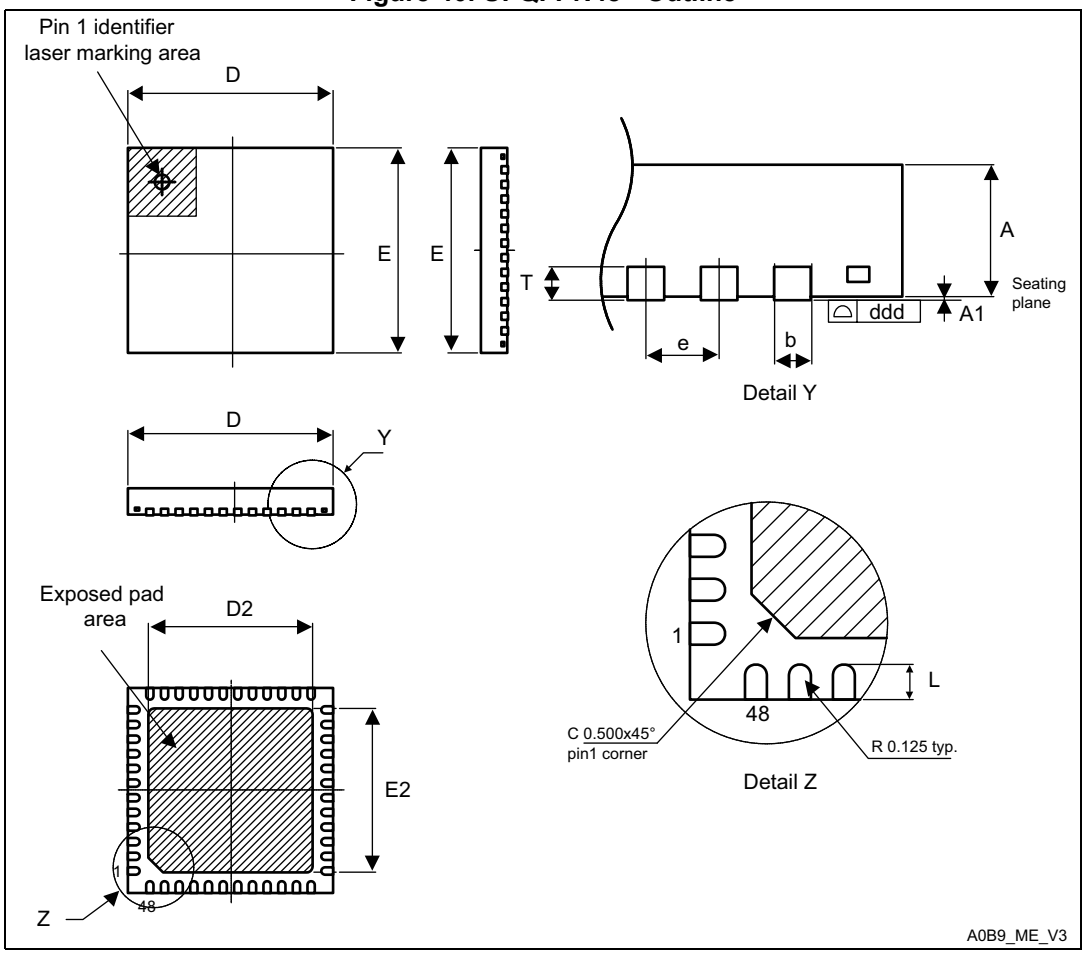


1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6.4 UFQFPN48 package information (A0B9)

UFQFPN48 is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 40. UFQFPN48 - Outline



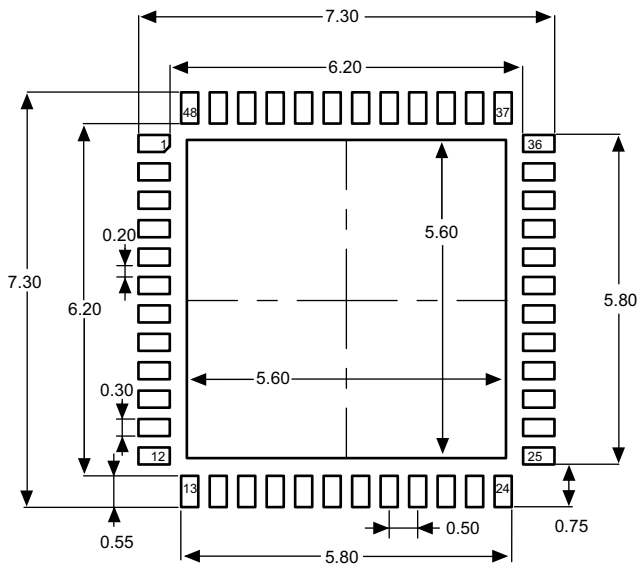
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is mandatory to connect and solder this back-side pad to PCB ground.

Table 100. UFQFPN48 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 41. UFQFPN48 - Recommended footprint

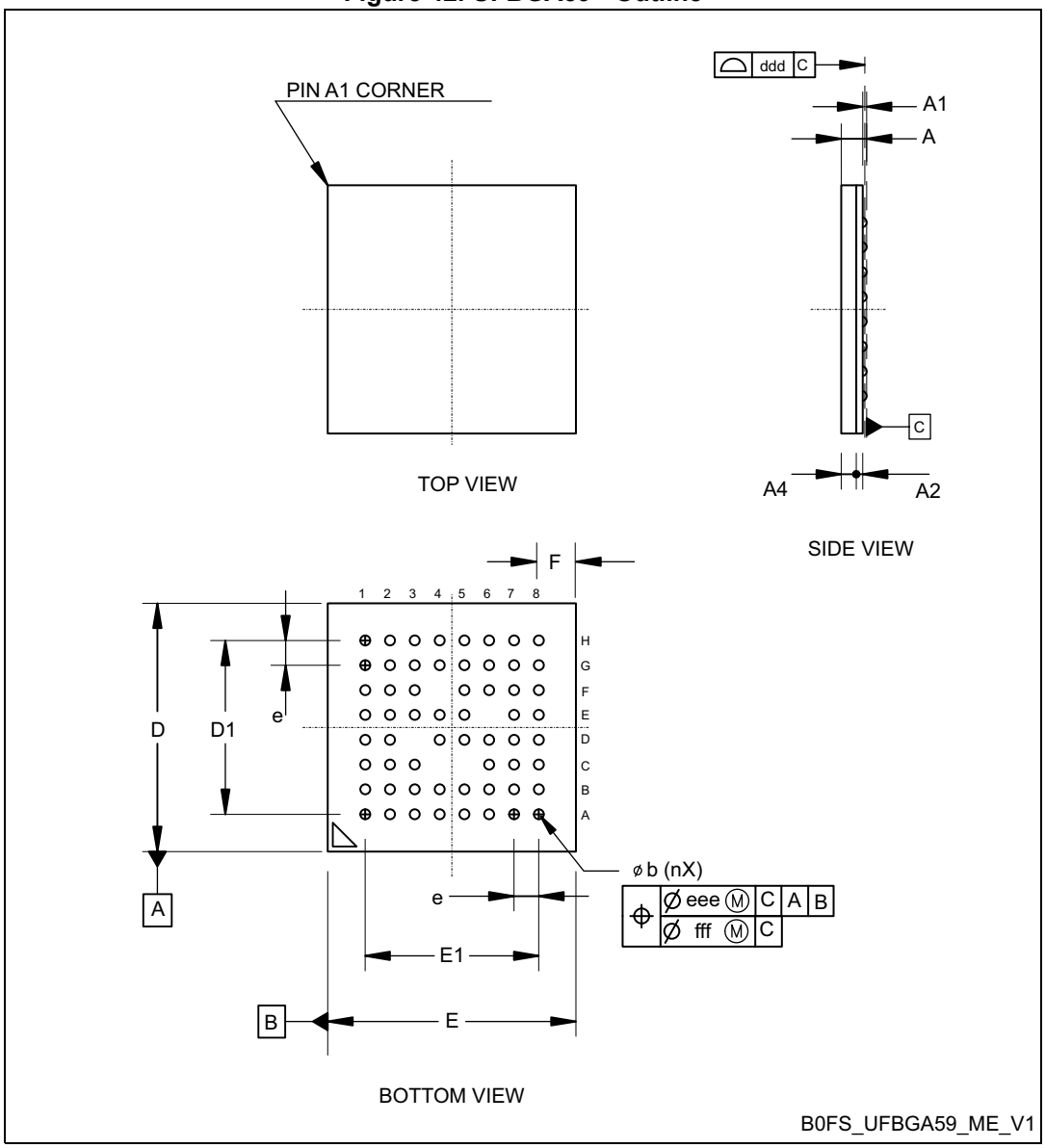


1. Dimensions are expressed in millimeters.

6.5 UFBGA59 package information (B0FS)

This UFBGA is a 59-ball, 5 x 5 mm, 0.5 mm pitch, fine pitch, square ball grid array package.

Figure 42. UFBGA59 - Outline



1. Drawing is not to scale.
2. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug.
   A distinguishing feature is available on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
3. The typical ball diameter before mounting is 0.20 mm.

Table 101. UFBGA59 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.60	-	-	0.024
A1	-	-	0.11	-	-	0.004
A2	-	0.13	-	-	0.005	-
A4	-	0.32	-	-	0.012	-
b[3]	0.24	0.29	0.34	0.009	0.011	0.013
D	4.85	5.00	5.15	0.191	0.197	0.203
D1	-	3.50	-	-	0.138	-
E	4.85	5.00	5.15	0.191	0.197	0.203
E1	-	3.50	-	-	0.138	-
e	-	0.50	-	-	0.020	-
F	-	0.75	-	-	0.029	-
ddd	-	-	0.08	-	-	0.003
eee[4]	-	-	0.15	-	-	0.006
fff[5]	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Ultra thin profile: 0.50 ≤ 0.65 mm / Fine pitch: e < 1.00 mm pitch.
   - The total profile height (Dim A) is measured from the seating plane to the top of the component.
   - The maximum total package height is calculated by the following methodology:
   A Max = A1 Typ + A2 Typ + A4 Typ + $\sqrt{(A1^2 + A2^2 + A4^2 \text{ tolerance values})}$
3. The typical ball diameter before mounting is 0.20 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 43. UFBGA59 - Recommended footprint

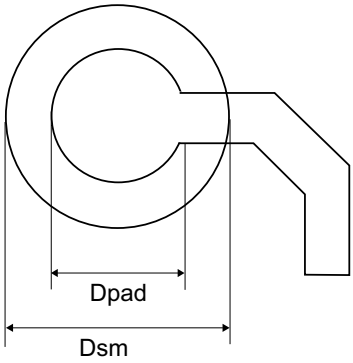


Table 102. UFBGA59 - Recommended PCB design rules

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0,300 mm
Dsm	0.400 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	0.100 mm

6.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the specified values.

T_J max (in Celsius degrees), can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

where:

- T_A max is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max)
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt (this is the maximum chip internal power)

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 103. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient**	UFQFPN32 - 5 mm x 5 mm	36.6	°C / W
		WLCSP41 - 2.76 mm x 2.98 mm	59.2	
		UFQFPN48 - 7 mm x 7 mm	28.4	
		UFBGA59 - 5 mm x 5 mm	56.6	
Θ_{JB}	**Thermal resistance junction-board**	UFQFPN32 - 5 mm x 5 mm	18.3	
		WLCSP41 - 2.76 mm x 2.98 mm	34.0	
		UFQFPN48 - 7 mm x 7 mm	12.8	
		UFBGA59 - 5 mm x 5 mm	39.4	
Θ_{JC}	**Thermal resistance junction-case**	UFQFPN32 - 5 mm x 5 mm	14.3	
		WLCSP41 - 2.76 mm x 2.98 mm	3.8	
		UFQFPN48 - 7 mm x 7 mm	10.0	
		UFBGA59 - 5 mm x 5 mm	15.6	

7 Ordering information

Example: STM32 WB A52 C G U 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth®

Device subfamily

A52 = Reduced set of features

A54 = Full set of features, LDO

A55 = Full set of features, SMPS

Pin count

K = 32 pins

H = 41 balls

C = 48 pins

U = 59 pins

Flash memory size

G = 1 Mbyte

E = 512 Kbytes

Package

U = UFQFPN

I = UFBGA

F = Thin WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)

7 = Industrial temperature range, -40 to 105 °C (120 °C junction)

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (memory, package, and so on), or for further information on any aspect of this device, contact your nearest ST sales office.

8 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on *www.st.com* for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

9 Revision history

Table 104. Document revision history

Date	Revision	Changes
13-Dec-2022	1	Initial release.
19-Dec-2022	2	Changed document classification, from ST restricted to Public.
27-Feb-2023	3	Document scope restricted to STM32WBA52Cx devices, hence: – updated image on cover page – updated *Table 1: Device summary*, *Table 1: STM32WBA52xx device features and peripheral counts*, *Table 24: Device pin definitions*, *Table 25: General operating conditions*, *Table 35: Embedded internal voltage reference*, *Table 58: ESD absolute maximum ratings*, and *Table 103: Package thermal characteristics* – removed former *Figure 6: UFQFPN32 pinout*(1) (2) – removed former *Section 6.1: UFQFPN32 package information* – updated *Section 7: Ordering information*. Updated *Section 5.1.2: Typical values* and note in *Section 5.3.9: External clock source characteristics*. Updated *Table 24: Main performance at VDD = 3.3 V*, *Table 30: RF receiver Bluetooth LE characteristics* and *Table 57: EMI characteristics for fHSE = 32 MHz and fHCLK = 100 MHz*. Removed former footnote *4* of *Table 70: 12-bit ADC4 accuracy*. Minor text edits across the whole document.
16-Jun-2023	4	Reintroduced STM32WBA52Kx devices, hence: – updated image on cover page – updated *Table 1: Device summary*, *Table 1: STM32WBA52xx device features and peripheral counts*, *Table 24: Device pin definitions*, and *Table 103: Package thermal characteristics* – added *Figure 6: UFQFPN32 pinout*(1) (2) – added *Section 6.2: UFQFPN32 package information (A0B8)* – updated *Section 7: Ordering information*. Updated *Section 1: Introduction*, *Section 2: Description*, *Section 3.12.1: Power supply schemes*, *Section 3.29: Tamper and backup registers (TAMP)*, *Device marking for UFQFPN32*, and *Device marking for UFQFPN48*. Updated *Table 10: Functionalities depending on the working mode*. Updated *Figure 9: Power supply scheme*. Minor text edits across the whole document.

Table 104. Document revision history (continued)

Date	Revision	Changes
26-Feb-2024	5	Document scope extended to STM32WBA54xx and STM32WBA55xx devices, hence updated image on cover page, *Table 1: Device summary*, and *Section 7: Ordering information*. Updated document title, *Features*, *Section 2: Description*, *Section 3.10: 2.4 GHz RADIO*, *Section 3.11: PTA interface*, *Section 3.12: Power supply management*, *Section 3.12.1: Power supply schemes*, *PWR background autonomous mode (BAM)*, *Section 3.13: Reset and clock controller (RCC)*, and *Section 5.1.6: Power supply scheme*. Added *Section 3.11: PTA interface*, *Section 3.21: Comparators (COMP)*, *Section 3.33: Serial audio interfaces (SAI)*, *Section 5.3.4: RF IEEE802.15.4 characteristics*, *Section 5.3.30: SAI characteristics*, *Section 6.1: Device marking*, and *Section 6.5: UFBGA59 package information (B0FS)*. Removed former *High-speed external clock security*, *Low-speed external clock security*, *Device marking for UFQFPN32*, and *Device marking for UFQFPN48*. Updated *Figure 1: Block diagram*, *Figure 2: 2.4 GHz RADIO block diagram*, *Figure 6: Clock tree*, and *Figure 10: Current consumption measurement scheme*. Added *Figure 3: Power supply overview with SMPS, Figure 10: UFQFPN48 SMPS pinout*[(1) (2)], *Figure 11: UFBGA59 SMPS ballout*[(1)], *Figure 15: Power supply scheme with SMPS*, and *Figure 16: Power supply scheme with SMPS (high RF power)*. Updated *Table 9: Operating modes overview*, *Table 10: Functionalities depending on the working mode*, *Table 24: Device pin definitions*, *Table 21: Voltage characteristics*, tables *24* to *26*, tables *28* to *39*, tables in *Section 5.1.7: Current consumption measurement*, tables *47* to *49*, *Table 58: ESD absolute maximum ratings*, *Table 77: USART characteristics*, *Table 78: SPI characteristics*, and *Table 103: Package thermal characteristics*. Added *Table 2: STM32WBA54/55xx device features and peripheral counts*, *Table 57: Low-power mode wake-up timings - SMPS*, *Table 67: LSI2 oscillator characteristics*, and *Table 88: COMP characteristics*. Removed former *Table 55: Current under reset condition*. Minor text edits across the whole document.

Table 104. Document revision history (continued)

Date	Revision	Changes
17-Sep-2024	6	Introduced STM32WBA55HG devices, hence updated image on cover page, *Table 1: Device summary* and *Section 7: Ordering information*. Updated *Figure 6: Clock tree*. Updated *Section 3.18.1: Nested vectored interrupt controller (NVIC)*. Added *Figure 8: WLCSP41 pinout*[(1)]. Added *Section 6.3: Thin WLCSP41 package information (B0MD)*. Updated *Table 2: STM32WBA54/55xx device features and peripheral counts*, *Table 10: Functionalities depending on the working mode*, *Table 13: ADC features*, *Table 24: Device pin definitions*, *Table 32: Generic RF transmitter characteristics*, *Table 35: RF transmitter Bluetooth LE characteristics*, *Table 36: RF receiver Bluetooth LE characteristics*, *Table 39: RF transmitter IEEE802.15.4 characteristics*, *Table 41: RF IEEE802.15.4 power consumption for VDD = 3.3 V*, *Table 51: Current consumption in Stop 0 mode*, *Table 54: Current consumption in Standby mode*, *Table 60: HSE32 crystal requirements*, *Table 61: HSE32 clock source requirements*, *Table 68: PLL characteristics*, *Table 69: Flash memory characteristics*, *Table 81: WKUP input characteristics*, *Table 93: USART characteristics*, and *Table 103: Package thermal characteristics*. Minor text edits across the whole document.
16-Dec-2024	7	Updated *Section 3.10: 2.4 GHz RADIO* and *Section 3.12.1: Power supply schemes*. Updated *Table 31: General operating conditions*, *Table 37: RF Bluetooth LE power consumption for VDD = 3.3 V*, *Table 41: RF IEEE802.15.4 power consumption for VDD = 3.3 V*, *Table 53: Current consumption in Standby retention mode*, *Table 56: Low-power mode wake-up timings - LDO*, *Table 57: Low-power mode wake-up timings - SMPS*, *Table 58: Regulator modes transition times*, and *Table 103: Package thermal characteristics*. Updated footnotes of *Table 35: RF transmitter Bluetooth LE characteristics* and of *Table 36: RF receiver Bluetooth LE characteristics*. Minor text edits across the whole document.
21-Aug-2025	8	Updated document title, *Features*, *Section 2: Description*, and *Section 3.10: 2.4 GHz RADIO*. Updated *Table 44: Embedded internal voltage reference*, *Table 47: Current consumption in Run mode on LDO, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF*, *Table 48: Current consumption in Run mode on SMPS, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF*, *Table 66: LSI1 oscillator characteristics*, *Table 72: EMI characteristics for fHSE = 32 MHz and fHCLK = 100 MHz*, and *Table 73: ESD absolute maximum ratings*. Updated *Figure 18: VREFINT vs. temperature*. Minor text edits across the whole document.

Table 104. Document revision history (continued)

Date	Revision	Changes
1-Apr-2026	9	Updated: – *Figure 6: Clock tree* – *Table 25: Alternate function AF0 to AF7* – *Table 26: Alternate function AF8 to AF15* – *Table 31: General operating conditions*

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