SIG5532B/34B: 1.875 to 3840SPS, 32-bit Sigma-Delta ADC with PGA and Reference

FEATURES

Programmable Gain: 1/2/4/8/16/32/64
Selectable Data Rates: 1.875 to 3840SPS
RMS Noise: 11nV at 7.5SPS (Gain=64)
22.8 Noise-Free Bits at 7.5SPS (Gain=1)
Offset Drift: 5nV/°C (Gain=64)
Gain Drift: 0.5ppm/°C
2.5V Internal Reference with 5ppm/°C Drift
Integral Non-Linearity: 3ppm
Internal or External Clock
Automatic Channel Sequencer
Burnout Current Sources
Low-Side Power Switch
Parity Check
Power Supply
- **AVDD: 4.75V to 5.25V or ±2.5V**
- **DVDD: 2.7V to 5.25V**

Current: 6.0mA
Package: 20/24-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Pressure Sensors
Temperature Measurement
Industrial Process Control

DESCRIPTION

The SIG5532B/34B is a low noise, low drift, and high-resolution 32-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

The device contains a low noise PGA with gains selected from 1, 2, 4, 8 16, 32, and 64, a delta-sigma (Δ-Σ) modulator, and a programmable SINC3/SINC1 digital filter. A low drift 2.5V reference is integrated on chip for accurate measurement. The output data rate from the device can be configured to 1.875, 3.75, 7.5, 15, 30, 60, 120, 240, 480, 960, 1920, and 3840SPS. This device provides channel sequencer feature to measure the differential inputs automatically. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

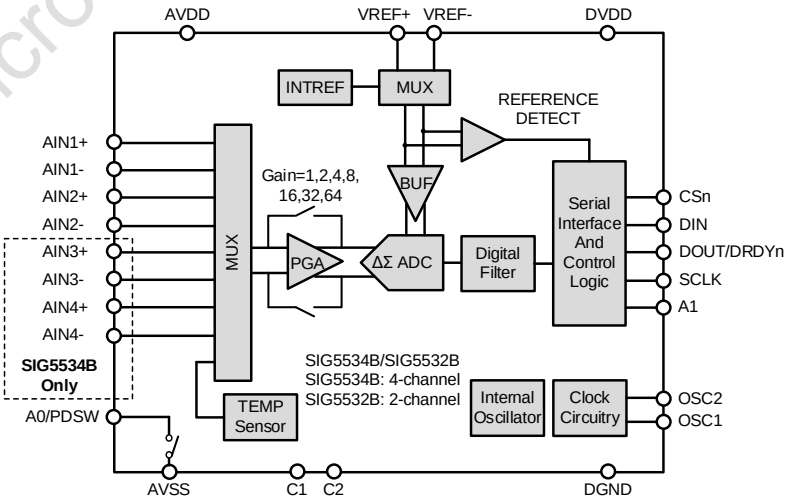
Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

The on-chip oscillator, an external clock, or an external crystal can be used as the clock source to the device.

The device can operate with bipolar ±2.375V to ±2.625V analog power supplies, or with a single 4.75V to 5.25V analog power supply.

The SIG5532B is available in 20-lead TSSOP package and the SIG5534B is available in 24-lead TSSOP package. These devices are fully specified over the -40°C to +125°C temperature range.

Function Block Diagram



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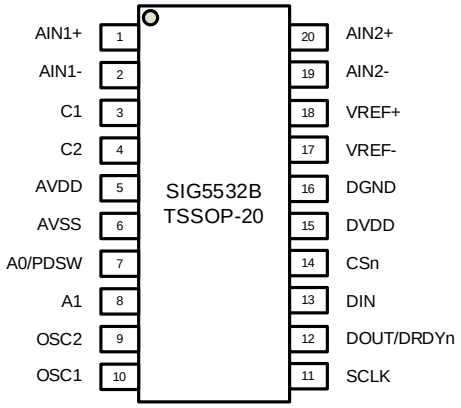
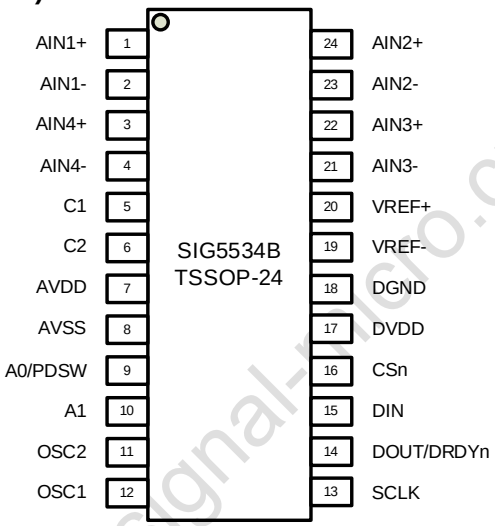
PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)





PIN		NAME	FUNCTION	DESCRIPTION
SIG5534B	SIG5532B			
1	1	AIN1+	Analog Input	Positive analog input channel 1.
2	2	AIN1-	Analog Input	Negative analog input channel 1.
3	-	AIN4+	Analog Input	Positive analog input channel 4.
4	-	AIN4-	Analog Input	Negative analog input channel 4.
5	3	C1	Analog Output	Amplifier analog output. Connect a COG cap with size 4.7~22nF between C1 and C2.
6	4	C2	Analog Output	Amplifier analog output. Connect a COG cap with size 4.7~22nF between C1 and C2.
7	5	AVDD	Analog	Positive analog power supply. 4.75V to 5.25V relative to AVSS.
8	6	AVSS	Analog	Negative analog power supply.
9	7	A0/PDSW	Analog Output	Analog logic output or bridge power down switch.
10	8	A1	Analog Output	Analog logic output.
11	9	OSC2	Digital Input/Output	Master clock input or Crystal Connection.
12	10	OSC1	Digital Input	Crystal Connection.
13	11	SCLK	Digital Input	Serial data clock.
14	12	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.
15	13	DIN	Digital Input	Serial data input.
16	14	CSn	Digital Input	Serial chip select. Active low.
17	15	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
18	16	DGND	Digital	Digital ground reference point.
19	17	REF-	Analog Input	Negative reference input.
20	18	REF+	Analog Input	Positive reference input.
21	-	AIN3-	Analog Input	Negative analog input channel 3.
22	-	AIN3+	Analog Input	Positive analog input channel 3.
23	19	AIN2-	Analog Input	Negative analog input channel 2.
24	20	AIN2+	Analog Input	Positive analog input channel 2.

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PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG5532B	TSSOP-20	-40°C to +125°C	SIG5532B-ITSP20-RL	Reel, 4500
SIG5534B	TSSOP-24	-40°C to +125°C	SIG5534B-ITSP24-RL	Reel, 3000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	–0.3	6.5	V
	AVSS to DGND	–3	0.3	V
	DVDD to DGND	–0.3	6.5	V
	Analog input	V_{AVSS} – 0.3	V_{AVDD} + 0.3	V
	Digital input	V_{DGND} – 0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{AVSS}=0V, V_{DVDD}=3.3V, V_{REF}=2.5V, f_{CLK}=4.9152MHz, data rate=60SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–V_{REF}/(2xGain)$		$+V_{REF}/(2xGain)$	V
Absolute Input Voltage	PGA bypass	$V_{AVSS} – 0.05$		$V_{AVDD} + 0.05$	V
	PGA enabled	$V_{AVSS} + 0.5$		$V_{AVDD} – 0.5$	
Common Mode Input Range	PGA enabled	$V_{AVSS} + 0.5 + \lvert V_{INMAX}\rvert \cdot Gain/2$		$V_{AVDD} – 0.5 – \lvert V_{INMAX}\rvert \cdot Gain/2$	V
Absolute Input Current	PGA bypass		±20		nA
	PGA enabled		±2		nA
SYSTEM PERFORMANCE					
PGA Gain			1/2/4/8/16/32/64		V/V
Resolution			32		Bits
Data Rate		1.875		3840	SPS
Noise		See Noise Table			
Integral Nonlinearity (INL)			±3		ppm
Offset Error	All PGA gains		±200/Gain		µV
	After calibration		In order of noise		
Offset Drift vs. Temperature	All PGA gains		±200/Gain ± 3		nV/°C
Gain Error(2)	All PGA gains	-350	±100	350	ppm
Gain Mismatch(2)	All PGA gains		150	350	ppm
Gain Drift vs. Temperature	All PGA gains	-3	±0.5	3	ppm/°C
Common Mode Rejection (CMRR)	f_{IN}=50/60Hz, data rate=960SPS	100	120		dB
Power Supply Rejection(2) (PSRR)	AVDD, AVSS	75	90		dB
	DVDD	80	120		dB
EXTERNALREFERENCE INPUT					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5		$V_{AVDD} – V_{AVSS} + 0.1$	V
Absolute Negative Reference Voltage (V_{REFN})		$V_{AVSS} – 0.05$		$V_{REFP} – 0.5$	V
Absolute Positive Reference Voltage (V_{REFP})		$V_{REFN} + 0.5$		$V_{AVDD} + 0.05$	V
Average Voltage Input Current			500		nA
INTERNAL VOLTAGE REFERENCE					
Reference Voltage			2.5		V
Initial Accuracy	T_A = 25˚C	-0.1%	±0.01%	+0.1%	
Voltage Temperature Drift	T_A = -40˚C to 125˚C		5	20	ppm/°C
Power Supply Rejection			90		dB
Burnout Current Sources					
Current Setting			1		µA
ADC CLOCK					
External Clock	Frequency Range	1	4.9152	5	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		4.9152		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	$0.8 \cdot V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			$0.2 \cdot V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7 \cdot V_{DVDD}$		V_{DVDD}	V

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Low-level Input Voltage (V_{IL})		V_{DGND}		$0.3 \cdot V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				±10	µA
POWER SUPPLY					
AVSS Voltage (V_{AVSS})		–2.625		0	V
AVDD Voltage (V_{AVDD})		V_{AVSS} + 4.75		V_{AVSS} + 5.25	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD, AVSS Current (I_{AVDD})	PGA Bypass		3.3	4.0	mA
	PGA Enabled		5.6	7.0	mA
	Sleep Mode		1		µA
DVDD Current (I_{DVDD})	Active Mode		0.4	0.6	mA
	Sleep Mode		40		µA
Total Power Dissipation	PGA Bypass		18.0		mW
	PGA Enabled		30.0		mW
	Sleep Mode		0.15		mW
TEMPERATURE RANGE					
Specified temperature range		–40		105	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) MIN and MAX values listed for gain error are for +25˚C room temperature only.

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Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

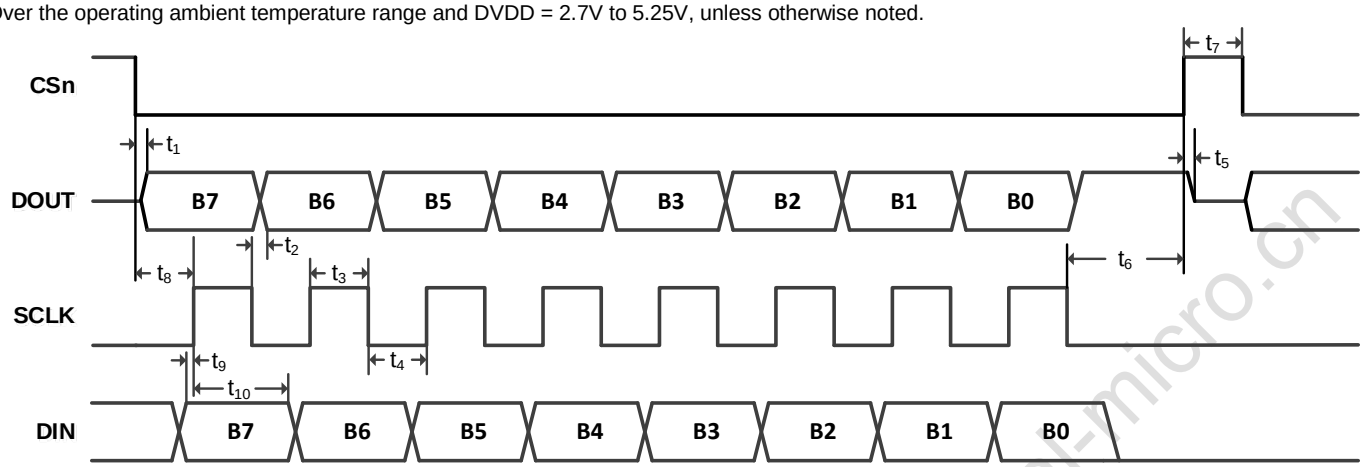

Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to valid DOUT/DRDYn: propagation delay(1)		20	ns
t_2	SCLK falling edge to valid DOUT/DRDYn: propagation delay(1)		20	ns
t_3	SCLK high pulse width	50		ns
t_4	SCLK low pulse width	50		ns
	SCLK period	100	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		20	ns
t_6	Last SCLK falling edge to CSn rising edge: delay time	20		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK rising edge: setup time(2)	50		ns
t_9	Valid DIN to SCLK rising edge: setup time	20		ns
t_{10}	Valid DIN to SCLK rising edge: hold time	20		ns

(1) DOUT load = 20pF || 100kΩ to DGND.
(2) CSn can be tied low.

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NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC3 and SINC1 filters. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF}/\text{Gain}/V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF}/\text{Gain}/V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

Table 1. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 2.5 V, SINC3 Filter

Data Rate (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
1.875	0.050(0.315)	0.027(0.171)	0.016(0.109)	0.011(0.065)	0.008(0.051)	0.006(0.040)	0.005(0.035)
3.75	0.070(0.446)	0.039(0.242)	0.023(0.154)	0.015(0.091)	0.011(0.072)	0.009(0.057)	0.008(0.049)
7.5	0.099(0.630)	0.055(0.343)	0.033(0.217)	0.021(0.129)	0.015(0.102)	0.012(0.080)	0.011(0.070)
15	0.141(0.891)	0.078(0.484)	0.046(0.307)	0.030(0.182)	0.022(0.144)	0.017(0.113)	0.015(0.099)
30	0.199(1.26)	0.110(0.685)	0.065(0.434)	0.042(0.258)	0.030(0.204)	0.025(0.160)	0.021(0.140)
60	0.281(1.78)	0.155(0.969)	0.092(0.614)	0.060(0.365)	0.043(0.288)	0.035(0.226)	0.030(0.197)
120	0.398(2.52)	0.219(1.37)	0.131(0.869)	0.084(0.516)	0.061(0.407)	0.049(0.320)	0.042(0.279)
240	0.562(3.56)	0.310(1.94)	0.185(1.23)	0.119(0.730)	0.086(0.576)	0.069(0.453)	0.060(0.395)
480	0.795(5.04)	0.439(2.74)	0.262(1.74)	0.169(1.03)	0.122(0.814)	0.098(0.640)	0.085(0.559)
960	1.12(7.13)	0.620(3.87)	0.370(2.46)	0.239(1.46)	0.172(1.15)	0.139(0.905)	0.120(0.790)
1920	1.58(11.0)	0.854(5.80)	0.508(3.33)	0.351(2.42)	0.255(1.78)	0.203(1.41)	0.171(1.15)
3840	2.27(16.5)	1.24(9.39)	0.748(5.92)	0.491(3.64)	0.360(2.91)	0.280(1.78)	0.243(1.85)

Table 2. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 5 V, SINC3 Filter

Data Rate (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
1.875	26.3(23.8)	26.2(23.7)	26.1(23.4)	25.8(23.1)	25.2(22.6)	24.6(21.9)	23.8(21.2)
3.75	25.8(23.3)	25.7(23.2)	25.6(22.9)	25.3(22.6)	24.7(22.1)	24.1(21.4)	23.3(20.7)
7.5	25.3(22.8)	25.2(22.7)	25.1(22.4)	24.8(22.1)	24.2(21.6)	23.6(20.9)	22.8(20.2)
15	24.8(22.3)	24.7(22.2)	24.6(21.9)	24.3(21.6)	23.7(21.1)	23.1(20.4)	22.3(19.7)
30	24.3(21.8)	24.2(21.7)	24.1(21.4)	23.8(21.1)	23.2(20.6)	22.6(19.9)	21.8(19.2)
60	23.8(21.3)	23.7(21.2)	23.6(20.9)	23.3(20.6)	22.7(20.1)	22.1(19.4)	21.3(18.7)
120	23.3(20.8)	23.2(20.7)	23.1(20.4)	22.8(20.1)	22.2(19.6)	21.6(18.9)	20.8(18.2)
240	22.8(20.3)	22.7(20.2)	22.6(19.9)	22.3(19.6)	21.7(19.1)	21.1(18.4)	20.3(17.7)
480	22.3(19.8)	22.2(19.7)	22.1(19.4)	21.8(19.1)	21.2(18.6)	20.6(17.9)	19.8(17.2)
960	21.8(19.3)	21.7(19.2)	21.6(18.9)	21.3(18.6)	20.7(18.1)	20.1(17.4)	19.3(16.7)
1920	21.4(18.6)	21.4(18.5)	21.1(18.3)	20.7(18.0)	20.2(17.4)	19.5(16.6)	18.8(16.0)
3840	21.0(18.2)	20.9(17.9)	20.6(17.7)	20.3(17.5)	19.7(16.8)	19.1(16.3)	18.3(15.5)

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Table 3. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 2.5 V, SINC1 Filter

Data Rate (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
1.875	0.068(0.474)	0.036(0.228)	0.022(0.149)	0.015(0.097)	0.010(0.068)	0.008(0.050)	0.007(0.049)
3.75	0.096(0.670)	0.051(0.323)	0.031(0.211)	0.021(0.137)	0.015(0.096)	0.012(0.071)	0.010(0.069)
7.5	0.136(0.948)	0.072(0.457)	0.044(0.299)	0.029(0.194)	0.021(0.136)	0.016(0.100)	0.014(0.097)
15	0.192(1.34)	0.101(0.646)	0.063(0.423)	0.041(0.274)	0.029(0.192)	0.023(0.141)	0.020(0.137)
30	0.271(1.90)	0.143(0.913)	0.089(0.598)	0.058(0.387)	0.041(0.272)	0.033(0.200)	0.029(0.194)
60	0.384(2.68)	0.203(1.29)	0.126(0.845)	0.082(0.548)	0.058(0.385)	0.046(0.282)	0.041(0.275)
120	0.543(3.79)	0.287(1.83)	0.178(1.20)	0.117(0.774)	0.082(0.544)	0.066(0.399)	0.058(0.389)
240	0.768(5.36)	0.405(2.58)	0.251(1.69)	0.165(1.10)	0.117(0.769)	0.093(0.564)	0.082(0.550)
480	1.09(7.58)	0.573(3.65)	0.355(2.39)	0.233(1.55)	0.165(1.09)	0.131(0.798)	0.116(0.777)
960	1.54(10.7)	0.810(5.17)	0.502(3.38)	0.330(2.19)	0.233(1.54)	0.186(1.13)	0.163(1.10)
1920	2.04(14.2)	1.18(8.12)	0.689(4.83)	0.606(4.35)	0.319(2.14)	0.251(1.70)	0.224(1.61)
3840	2.82(19.5)	1.57(11.7)	0.935(6.97)	0.612(4.23)	0.443(3.00)	0.345(2.25)	0.304(2.18)

Table 4. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 5 V, SINC1 Filter

Data Rate (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
1.875	26.0(23.2)	25.9(23.4)	25.7(22.9)	25.4(22.6)	24.8(22.2)	24.2(21.5)	23.3(20.6)
3.75	25.5(22.7)	25.4(22.9)	25.2(22.4)	24.9(22.1)	24.3(21.7)	23.7(21.0)	22.8(20.1)
7.5	25.0(22.2)	24.9(22.4)	24.7(21.9)	24.4(21.6)	23.8(21.2)	23.2(20.5)	22.3(19.6)
15	24.5(21.7)	24.4(21.9)	24.2(21.4)	23.9(21.1)	23.3(20.7)	22.7(20.0)	21.8(19.1)
30	24.0(21.2)	23.9(21.4)	23.7(20.9)	23.4(20.6)	22.8(20.2)	22.2(19.5)	21.3(18.6)
60	23.5(20.7)	23.4(20.9)	23.2(20.4)	22.9(20.1)	22.3(19.7)	21.7(19.0)	20.8(18.1)
120	23.0(20.2)	22.9(20.4)	22.7(19.9)	22.4(19.6)	21.8(19.2)	21.2(18.5)	20.3(17.6)
240	22.5(19.7)	22.4(19.9)	22.2(19.4)	21.9(19.1)	21.3(18.7)	20.7(18.0)	19.8(17.1)
480	22.0(19.2)	21.9(19.4)	21.7(18.9)	21.4(18.6)	20.8(18.2)	20.2(17.5)	19.3(16.6)
960	21.5(18.7)	21.4(18.9)	21.2(18.4)	20.9(18.1)	20.3(17.7)	19.7(17.0)	18.8(16.1)
1920	21.1(18.3)	21.0(18.4)	20.7(17.8)	20.3(17.8)	19.8(17.0)	19.2(16.4)	18.4(15.5)
3840	20.6(17.9)	20.5(17.6)	20.3(17.5)	19.9(17.1)	19.4(16.7)	18.8(15.8)	18.0(15.1)

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REGISTER MAPS

There are total thirteen 32-bit registers inside the device. These registers are used to configure and control the ADC to the desired mode of operation. These registers can be accessed through the SPI-compatible serial interface by using register read and write commands. At power-on or reset, the registers default to their initial settings, as shown in the *Reset Value* column of Table 5.

Table 5. Register map

ADDR. RS[2:0]	NAME	RESET VALUE	BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT26	BIT 25	BIT 24
			BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
			BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
			BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3'b001	OFFSET	0x00000000	OFFSET[31:24]							
			OFFSET[23:16]							
			OFFSET[15:8]							
			OFFSET[7:0]							
3'b010	GAIN	0x01000000	GAIN[23:16]							
			GAIN[23:16]							
			GAIN[15:8]							
			GAIN[7:0]							
3'b011	CONF	0x00000000	PSS	PDW	RS	RV	SHORT	A0_PSW	VRS	A1
			A0	OLS	BUF	OGS	FRS	FILTER	TPS	INTREF
			CHKSUM	LATENCY	CLK[1:0]		LOOPEN	DELAY[2:0]		
			CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
3'b101	CSR	0x00000000	CS1]	CS[0]	PGA[2]	PGA[1]	PGA[0]	DR[3]	DR[2]	DR[1]
			DR[0]	FORMAT	OL1	OL0	DT	BCS	OG[1]	OG[0]
			CS[1]	CS[0]	PGA[2]	PGA[1]	PGA[0]	DR[3]	DR[2]	DR[1]
			DR[0]	FORMAT	OL1	OL0	DT	BCS	OG[1]	OG[0]

OFFSET Register

The device has four OFFSET registers #1, #2, #3, and #4. Each register can be accessed by setting CS[1:0] bits in the register read and write commands. User can choose which one to use by controlling CONF bit OGS and CSR register bits OG[1:0] or OL[1:0].

Table 6. OFFSET Register (Address = 3'b001)

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFFSET[31]	OFFSET[30]	OFFSET[29]	OFFSET[28]	OFFSET[27]	OFFSET[26]	OFFSET[25]	OFFSET[24]
OFFSET[23]	OFFSET[22]	OFFSET[21]	OFFSET[20]	OFFSET[19]	OFFSET[18]	OFFSET[17]	OFFSET[16]
OFFSET[15]	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]	OFFSET[9]	OFFSET[8]
OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]	OFFSET[2]	OFFSET[1]	OFFSET[0]

Power-On/Reset value = 0x00000000

Bits	Bit Name	Access	Reset	Description
31:0	OFFSET[31:0]	R/W	0x00000000	**Offset Calibration Bits:** The 32-bit word is signed number in 2's complement format. See Calibration section for more information.

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GAIN Register

The device has four GAIN registers #1, #2, #3, and #4. Each register can be accessed by setting CS[1:0] bits in the register read and write commands. User can choose which one to use by controlling CONF bit OGS and CSR register bits OG[1:0] or OL[1:0].

Table 7. GAIN Register (Address = 3'b010)

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GAIN[31]	GAIN[30]	GAIN[29]	GAIN[28]	GAIN[27]	GAIN[26]	GAIN[25]	GAIN[24]
GAIN[23]	GAIN[22]	GAIN[21]	GAIN[20]	GAIN[19]	GAIN[18]	GAIN[17]	GAIN[16]
GAIN[15]	GAIN[14]	GAIN[13]	GAIN[12]	GAIN[11]	GAIN[10]	GAIN[9]	GAIN[8]
GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]

Power-On/Reset value = 0x01000000

Bits	Bit Name	Access	Reset	Description
31:0	GAIN[31:0]	R/W	0x01000000	**Gain Calibration Bits:** The 32-bit word is unsigned positive number in binary format. See Calibration section for more information.

Configuration Register (CONF)

Table 8. CONF Register (Address = 3'b011)

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PSS	PDW	RS	RV	SHORT	A0_PSW	VRS	A1
A0	OLS	BUF	OGS	FRS	FILTER	TPS	INTREF
CHKSUM	LATENCY	CLK[1:0]		LOOPEN	DELAY[2:0]		
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Power-On/Reset value = 0x00000000

Bits	Bit Name	Access	Reset	Description
31	PSS	R/W	1'b0	**Power Save Select:** 0: Standby Mode (default) 1: Sleep Mode
30	PDW	R/W	1'b0	**Power Down Mode:** 0: Normal Mode (default) 1: Power Down Mode
29	RS	R/W	1'b0	**Reset System:** 0: Normal Operation (default) 1: Activate a Reset cycle.
28	RV	R	1'bx	**Reset Indicator:** Read only. Bit is cleared to logic zero after the CONF register is read. 0: Normal Operation (default) 1: System was reset.
27	SHORT	R/W	1'b0	**Input Short:** 0: Normal Input (default) 1: Analog Inputs are disconnected from the pins and shorted

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				internally to mid-supply (V_{AVDD}+V_{AVSS})/2.
26	A0_PSW	R/W	1'b0	**Bridge Power-down Switch Function:** When this bit is set to 1, the output latch bit A0 or OL0 is served as the switch control bit. The switch is closed to short pin A0 to AVSS with low on-resistor of typical 3 Ohms if the output latch bit is set to 1. The switch is open if the output latch bit is cleared. The switch remains active in standby mode and is forced to open in sleep mode. 0: Disabled (default) 1: Enabled
25	VRS	R/W	1'b0	**Voltage Reference Select:** The input full-scale range is [-V_{REF}/(2xgain), V_{REF}/(2xgain)] with VRS=0, and is [-V_{REF}/gain, V_{REF}/gain] with VRS=1. 0: 2.5V<V_{REF}<(V_{AVDD}-V_{AVSS}) (default) 1: 0.5V<V_{REF}<2.5V
24	A1	R/W	1'b0	**Output Latch Bit:** This bit sets the value of the A1 output pin if OLS bit is set to 1. During register read, this bit reflects the status of the A1 pin. 0: AVSS (default) 1: AVDD
23	A0	R/W	1'b0	**Output Latch Bit:** This bit sets the value of the A0 output pin if OLS bit is set to 1. During register read, this bit reflects the status of the A0 pin. 0: AVSS (default) 1: AVDD
22	OLS	R/W	1'b0	**Output Latch Select:** This bit decides which register bits are used as the source of output pin A1 and A0. 0: CSR register bits OL1 and OL0(default) 1: CONF register bits A1 and A0
21	BUF	R/W	1'b0	**Buffer Enable Bit:** When this bit is set, analog input is buffered. Otherwise the input buffer is bypassed for gain bits PGA[2:0]=3'b000.
20	OGS	R/W	1'b0	**Offset and Gain Select:** This bit decides the source bits in CSR register used to control which OFFSET and GAIN registers are used. 0: Bits CS[1:0] (default) 1: Bits OG[1:0]
19	FRS	R/W	1'b0	**Filter Rate Select:** 0: Default output data rates. (default) 1: Scale the output data rate by a factor of 5/6.
18	FILTER	R/W	1'b0	**Digital Filter Configuration:** Configures the ADC digital filter 0: SINC5/SINC3 filter (default) 1: SINC5/SINC1 filter
17	TPS	R/W	1'b0	**Temperature Sensor Enable Bit:** The voltage output is about 125.4mV at room temp and the rate of change over temperature is about 420uV/°C. PGA gain is internally forced to 1 with buffer on for temperature sensor measurement. 0: Disabled (default) 1: Enabled
16	INTREF	R/W	1'b0	**Internal Reference Enable Bit**: 0: REFP, REFN (default) 1: 2.5V internal reference.
15	CHKSUM	R/W	1'b0	**ADC Data Checksum Enable Bit:** 0: Disabled (default) 1: Enabled

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14	LATENCY	R/W	1'b0	**Zero Latency Bit:** When this bit is set, the ADC settles in one conversion cycle so that it functions as a zero latency ADC.
13:12	CLK[1:0]	R/W	2'b00	**Clock Select Bits:** These bits select the clock source for SYSCLK. 00: External crystal applied between OSC1 and OSC2. (default) 01: External clock applied to the OSC2 pin. 10: Internal 4.9152MHz clock with OSC2 tristated. 11: Internal 4.9152MHz clock with its output on OSC2 pin.
11	LOOPEN	R/W	1'b0	**Channel Sequence Enable Bit:** With this bit as default logic 0, CRSP[2:0] bits in command byte are used to select the single channel for ADC conversion. When this bit is set to logic 1, CONF[7:0] bits are used disregarding CRSP[2:0] in command byte to select the channels for ADC conversion. CONF[10:8] are used to provide additional delay before each channel conversion to ensure fully settled analog input signal during channel switching.
10:8	DELAY[2:0]	R/W	3'b000	**Conversion Delay:** Only effective if LOOPEN bit is set to logic 1. Provides additional delay from conversion start to the beginning of the actual conversion for each channel enabled in bits CH0-CH7. 000: 0µs (default) 001: 104.2µs 010: 416.7µs 011: 1.667ms 100: 6.667ms 101: 26.67ms 110: 106.7ms 111: 426.7ms
7:0	CH7 to CH0	R/W	0x00	**Channel Select Bits:** Only effective if LOOPEN bit is set to logic 1. These bits select which channels are enabled for ADC conversion. When more than one channel are enabled, ADC automatically sequences them and place the data into data buffer with corresponding channel information appended. CH0 is selected if These bits are all logic 0. For calibrations, only one channel can be selected and the lowest bit channel is selected if more than one channels are enabled.

Table 9. Channel Selection Bits with LOOPEN=1

Channel	Channel Setup Information	Channel Indicator Bits CL[2:0] in Output Data
CH0=1	CSR0[31:16]	000
CH1=1	CSR0[15:0]	001
CH2=1	CSR1[31:16]	010
CH3=1	CSR1[15:0]	011
CH4=1	CSR2[31:16]	100
CH5=1	CSR2[15:0]	101
CH6=1	CSR3[31:16]	110
CH7=1	CSR3[15:0]	110

Table 10. Channel Selection Bits with LOOPEN=0

CRSP[2:0]	Channel Setup Information	Channel Indicator Bits CL[1:0] in Output Data
000	CSR0[31:16]	CSR0[31:30]
001	CSR0[15:0]	CSR0[15:14]
010	CSR1[31:16]	CSR1[31:30]

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011	CSR1[15:0]	CSR1[15:14]
100	CSR2[31:16]	CSR2[31:30]
101	CSR2[15:0]	CSR2[15:14]
110	CSR3[31:16]	CSR3[31:30]
110	CSR3[15:0]	CSR3[15:14]

Channel-Setup Register (CSR)

The device has four CSR registers: CRS0/CRS1/CRS2/CRS3. Each register can be accessed by setting CS[1:0] bits in the register read and write commands. Each CSR contains two 16-bit setups with bits [31:16] as setup #1/#3/#5/#7 and bits [15:0] as setup #2/#4/#6/#8. User can select which setup to use by controlling CSRP[2:0] bits in the command if LOOPEN bit is logic 0 or CH0-CH7 bits in CONF register if LOOPEN bit is logic 1 when performing conversion or calibration.

Table 11. CSR Register (Address = 3'b101)

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CS[1]	CS[0]	PGA[2]	PGA[1]	PGA[0]	DR[3]	DR[2]	DR[1]
DR[0]	FORMAT	OL1	OL0	DT	BCS	OG[1]	OG[0]
CS[1]	CS[0]	PGA[2]	PGA[1]	PGA[0]	DR[3]	DR[2]	DR[1]
DR[0]	FORMAT	OL1	OL0	DT	BCS	OG[1]	OG[0]

Power-On/Reset value = 0x0000000

Bits	Bit Name	Access	Reset	Description
31:30 or 15:14	CS[1:0]	R/W	2'b00	**Channel Select Bits:** 00: Select physical channel 1: AIN1+/AIN1- (default) 01: Select physical channel 2: AIN2+/AIN2- 10: Select physical channel 3: AIN3+/AIN3- (SIG5534B only) 11: Select physical channel 4: AIN4+/AIN4- (SIG5534B only)
29:27 or 13:11	PGA[2:0]	R/W	3'b000	**PGA Gain Configuration:** Selects the PGA gain. If PGA gain is set to other than 1, the BUF bit setting on CONF register is ignored with PGA always enabled. 000: Gain=1 (default) 001: Gain=2 010: Gain=4 011: Gain=8 100: Gain=16 101: Gain=32 110: Gain=64 111: Reserved
26:23 or 10:7	DR[3:0]	R/W	4'b0000	**Data Rate Configuration:** Selects the ADC data rate. 0000: 120SPS (default) 0001: 60SPS 0010: 30SPS 0011: 15SPS 0100: 7.5SPS 1000: 3840SPS 1001: 1920SPS 1010: 960SPS 1011: 480SPS 1100: 240SPS 1101: 3.75SPS

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				1110: 1.875SPS
22 or 6	FORMAT	R/W	1'b0	**Data Format Bit:** This bit sets the ADC data format. 0: Bipolar mode (default) 1: Unipolar mode
21 or 5	OL1	R/W	1'b0	**Output Latch Bit:** This bit sets the value of the A1 output pin if OLS bit is set to 0. During register read, this bit reflects the status of the A1 pin. 0: AVSS (default) 1: AVDD
20 or 4	OL0	R/W	1'b0	**Output Latch Bit:** This bit sets the value of the A0 output pin if OLS bit is set to 0. During register read, this bit reflects the status of the A0 pin. 0: AVSS (default) 1: AVDD
19 or 3	DT	R/W	1'b0	**Delay Time Bit:** When set, the converter will wait for a delay time before starting a conversion. The delay time is 1280 SYSCLK cycles when FRS=0. And 1536 SYSCLK cycles when FRS=1. DT bit is only effective if LOOPEN bit in CONF Register is logic 0, otherwise DLY[2:0] bits in CONF Register are used to control the delay time. 0: No delay (default) 1: Delay time added
18 or 2	BCS	R/W	1'b0	**Burnout Current Sources:** When this bit is enabled, a pair of 1μA current sources are applied to analog inputs. 0: Disabled (default) 1: Enabled
17:16 or 1:0	OG[1:0]	R/W	2'b00	**Offset/Gain Register Pointer Bits:** These bits are effective and used to select the offset and gain register to use while performing a conversion or calibration while OGS bit in CONF register is logic 1. Otherwise CS[1:0] bits are used if OGS bit in CONF register is logic 0. 00: Use offset and gain register #1 (default) 01: Use offset and gain register #2 10: Use offset and gain register #3 11: Use offset and gain register #4

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Conversion Data Output Descriptions

Table 12. 32-bit Conversion Data Output

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT26	BIT 25	BIT 24
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA[31]	DATA[30]	DATA[29]	DATA[28]	DATA[27]	DATA[26]	DATA[25]	DATA[24]
DATA[23]	DATA[22]	DATA[21]	DATA[20]	DATA[19]	DATA[18]	DATA[17]	DATA[16]
DATA[15]	DATA[14]	DATA[13]	DATA[12]	DATA[11]	DATA[10]	DATA[9]	DATA[8]
DATA[7]	DATA[6]	DATA[5]	DATA[4]	CL[2]	OF	CL[1]	CL[0]

Bits	Bit Name	Description
31:4	DATA[31:4]	**28-bit Conversion Data**
3	CI[2]	**Channel Indicator Bit:** This bit is used together with CI[1:0] bits if LOOPEN bit in CONF Register is logic 1.
2	OF	**Over-range Flag indicator Bit:** 0: Over-range not occurred. 1: Over-range occurred.
1:0	CI[1:0]	**Channel Indicator Bits:** These bits indicate the input channel used to get the ADC conversion data output.

Table 13. Channel Indicator Bits

Channel Indicator Bits CL[2:0]	LOOPEN=0	LOOPEN=1
000	Select physical channel 1: AIN1+/AIN1-	CH0
001	Select physical channel 2: AIN2+/AIN2-	CH1
010	Select physical channel 3: AIN3+/AIN3- (SIG5534B only)	CH2
011	Select physical channel 4: AIN4+/AIN4- (SIG5534B only)	CH3
100	N/A	CH4
101	N/A	CH5
110	N/A	CH6
110	N/A	CH7

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REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 20, 2022		Initial release.

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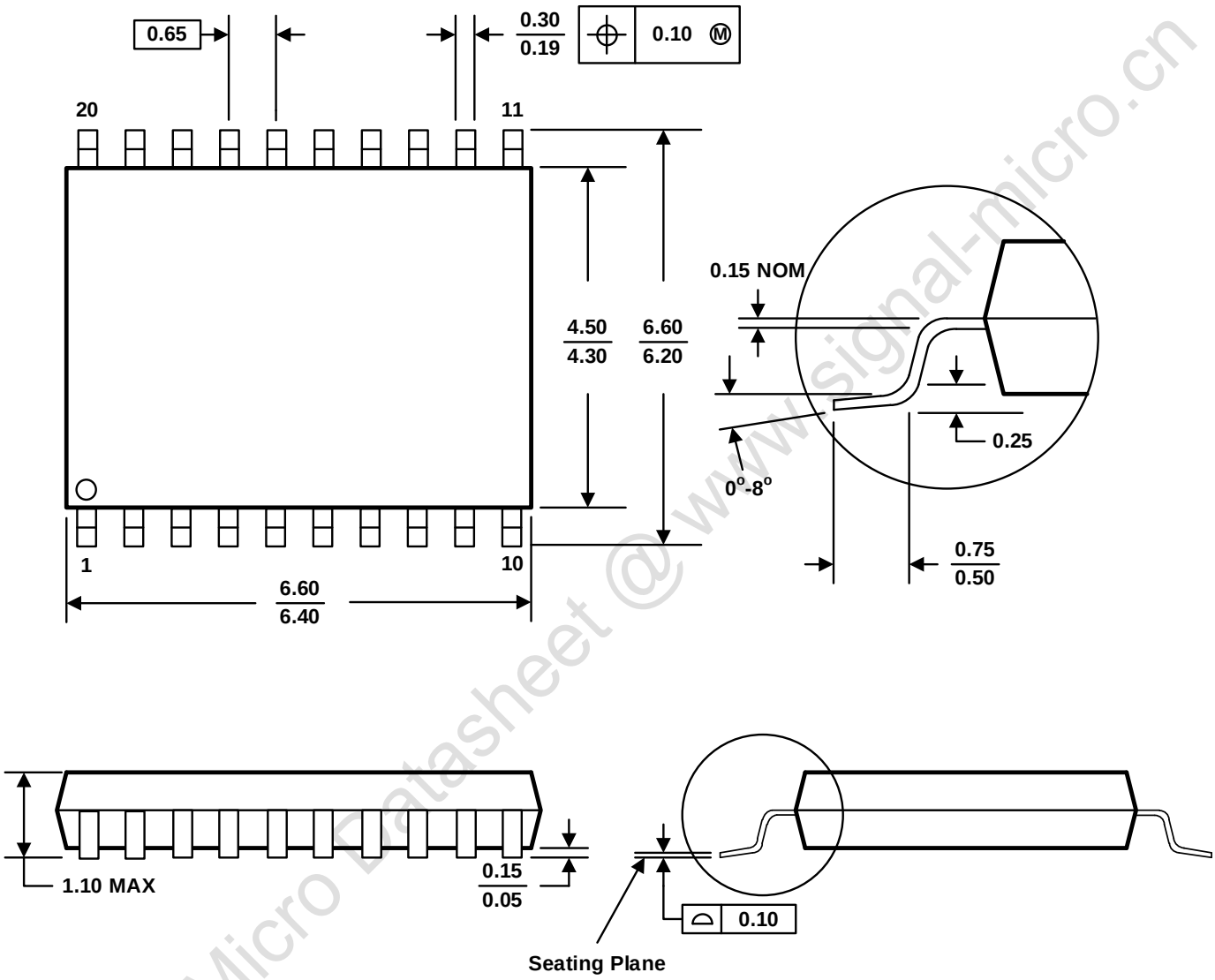
PACKAGE OUTLINE DIMENSIONS

TSSOP-20



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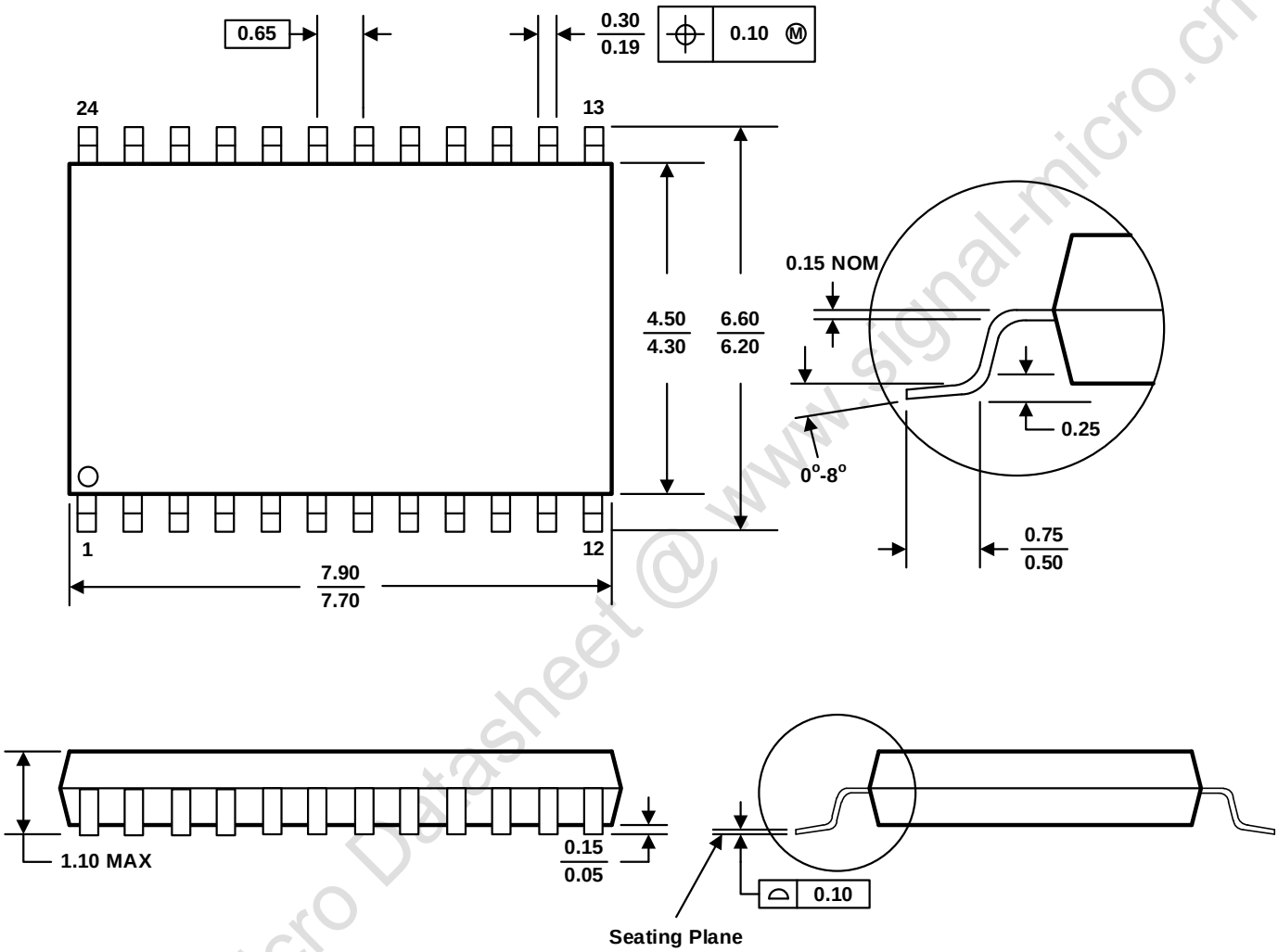

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