Si53320-28 Data Sheet

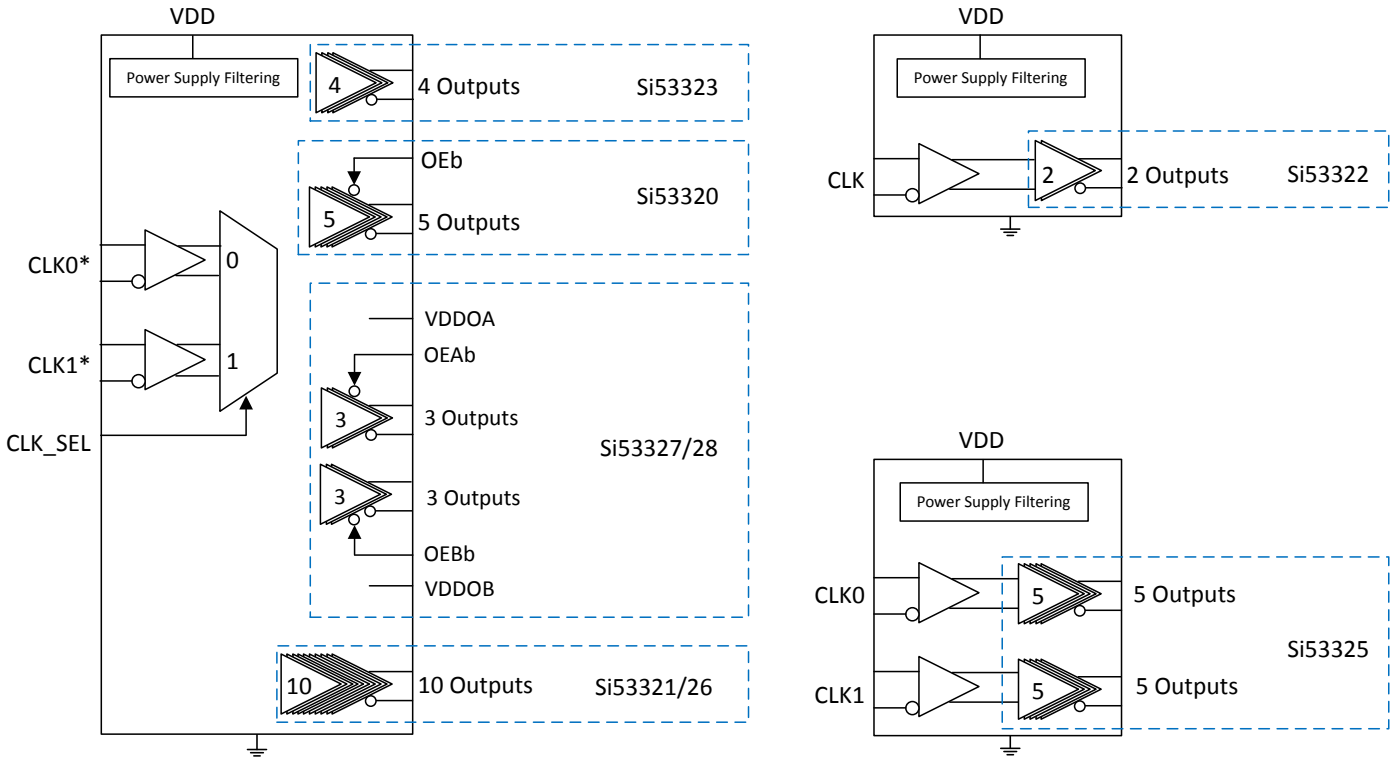
Low-Jitter LVPECL Fanout Clock Buffers with up to 10 LVPECL Outputs from Any-Format Input and Wide Frequency Range from DC up to 1250 MHz

The Si53320–28 family of LVPECL fanout buffers is ideal for clock/data distribution and redundant clocking applications. These devices feature typical ultra-low jitter characteristics of 50 fs and operate over a wide frequency range from dc to 725/1250 MHz. Built-in LDOs deliver high PSRR performance and reduce the need for external components, simplifying low-jitter clock distribution in noisy environments.

The Si53320–28 family is available in multiple configurations, with some versions offering a selectable input clock using a 2:1 input mux. Other features include independent output enable and built-in format translation. These buffers can be paired with the Si534x clocks and Si5xx oscillators to deliver end-to-end clock tree performance.

KEY FEATURES

- Ultra-low additive jitter: 50 fs rms
- Built-in LDOs for high PSRR performance
- Up to 10 LVPECL Outputs
- Any-format Inputs (LVPECL, Low-power LVPECL, LVDS, CML, HCSL, LVCMOS)
- Wide frequency range: dc to 1250 MHz
- Output Enable option
- Multiple configuration options
  - Dual Bank option
  - 2:1 Input Mux operation
- RoHS compliant, Pb-free
- Temperature range: –40 to +85 °C



*Si53326/28 require Single-ended Inputs

1. Ordering Guide

Table 1.1. Si5332x Ordering Guide

Part Number	Input	LVPECL Output	Output Enable	Frequency Range	Package
Si53320-B-GT	2:1 selectable MUX Any-format	1 bank / 5 Outputs	Single	dc to 725 MHz	20-TSSOP
Si53321-B-GM	2:1 selectable MUX Any-format	1 bank / 10 Outputs	—	dc to 1250 MHz	32-QFN 5 x 5 mm
Si53321-B-GQ	2:1 selectable MUX Any-format	1 bank / 10 Outputs	—	dc to 1250 MHz	32-eLQFP 7 x 7 mm
Si53322-B-GM	1 bank / 1 Input Any-format	1 bank / 2 Outputs	—	dc to 1250 MHz	16-QFN 3 x 3 mm
Si53323-B-GM	2:1 selectable MUX Any-format	1 bank / 4 Outputs	—	dc to 1250 MHz	16-QFN 3 x 3 mm
Si53325-B-GM	2 banks / 2 Inputs Any-format	2 banks / 5 Outputs	—	dc to 1250 MHz	32-QFN 5 x 5 mm
Si53325-B-GQ	2 banks / 2 Inputs Any-format	2 banks / 5 Outputs	—	dc to 1250 MHz	32-eLQFP 7 x 7 mm
Si53326-B-GM	2:1 selectable MUX LVCMOS	1 bank / 10 Outputs	—	dc to 200 MHz	32-QFN 5 x 5 mm
Si53327-B-GM	2:1 selectable MUX Any-format	2 banks / 3 Outputs	1 per bank	dc to 1250 MHz	24-QFN 4 x 4 mm
Si53328-B-GM	2:1 selectable MUX LVCMOS	2 banks / 3 Outputs	1 per bank	dc to 200 MHz	24-QFN 4 x 4 mm

2. Functional Description

The Si53320-28 are a family of low-jitter, low-skew, fixed-format (LVPECL) buffers. All devices except the Si53326 and Si53328 have a universal input that accepts most common differential or LVCMOS input signals. The Si53326 and Si53328 accept only single-ended LVCMOS inputs. These devices are available in multiple configurations customized for the end application (refer to 1. Ordering Guide for more details on configurations).

2.1 Universal, Any-Format Input Termination (Si53320/21/22/23/25/27)

The universal input stage enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. The tables below summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended since low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.

Table 2.1. Clock Input Options

Clock Format	1.8 V	2.5/3.3 V
AC-Coupled		
LVPECL/Low-power LVPECL	N/A	Yes
LVCMOS	No	Yes
LVDS	Yes	Yes
HCSL	No	Yes (3.3 V)
CML	Yes	Yes
DC-Coupled		
LVPECL/Low-power LVPECL	N/A	Yes
LVCMOS	No	Yes
LVDS	No	Yes
HCSL	No	Yes (3.3 V)
CML	No	No

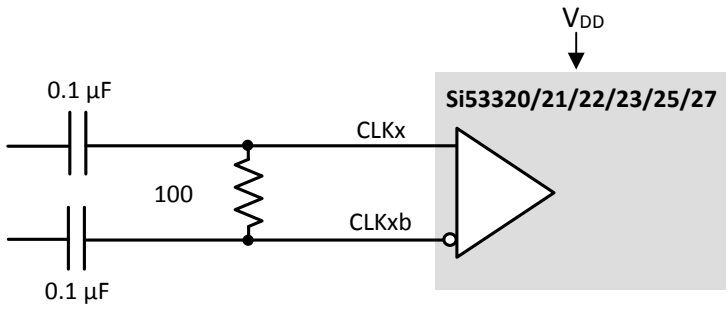


Figure 2.1. Differential (HCSL, LVPECL, Low-Power LVPECL, LVDS, CML) AC-Coupled Input Termination

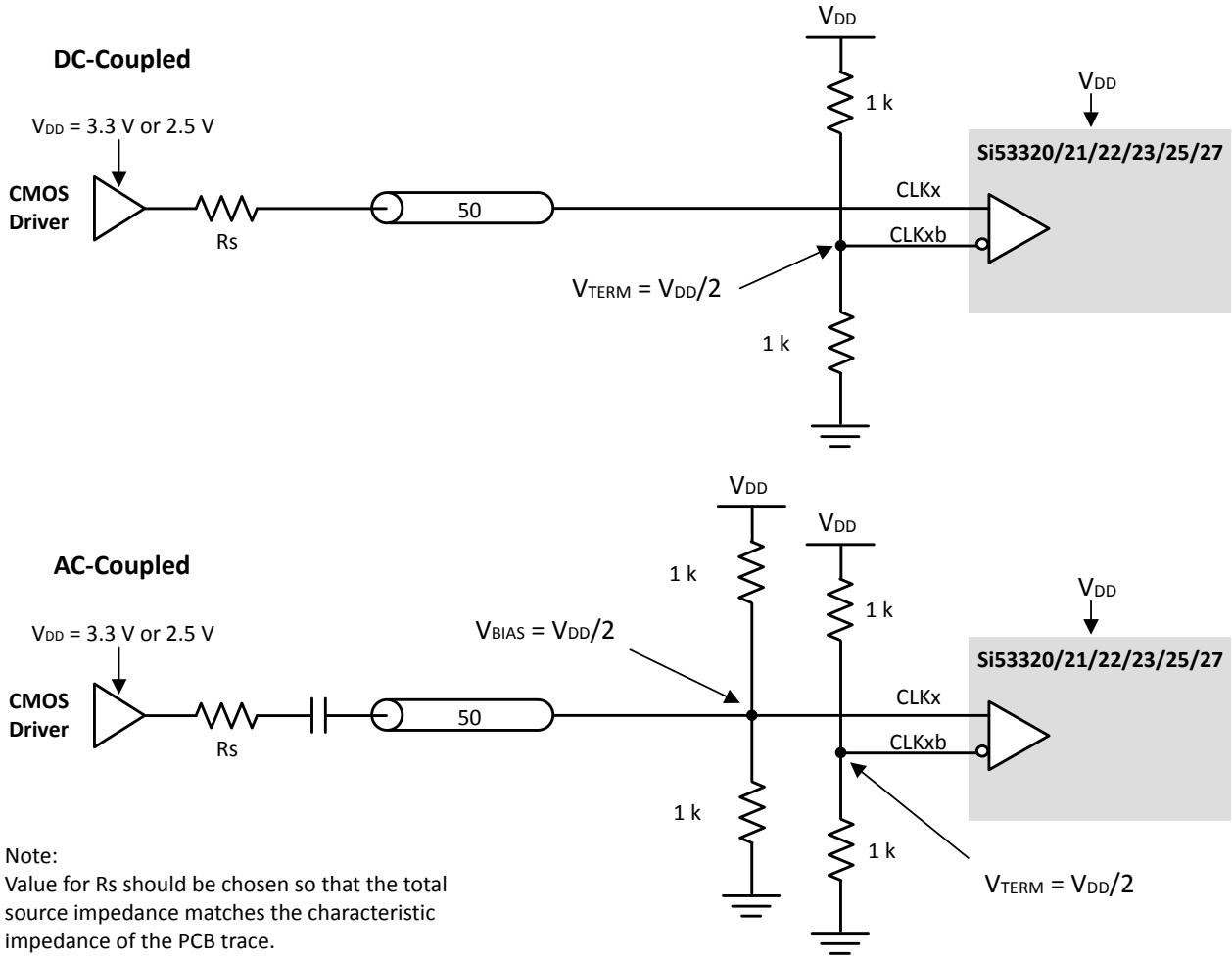


Figure 2.2. Single-Ended (LVCMOS) Input Termination

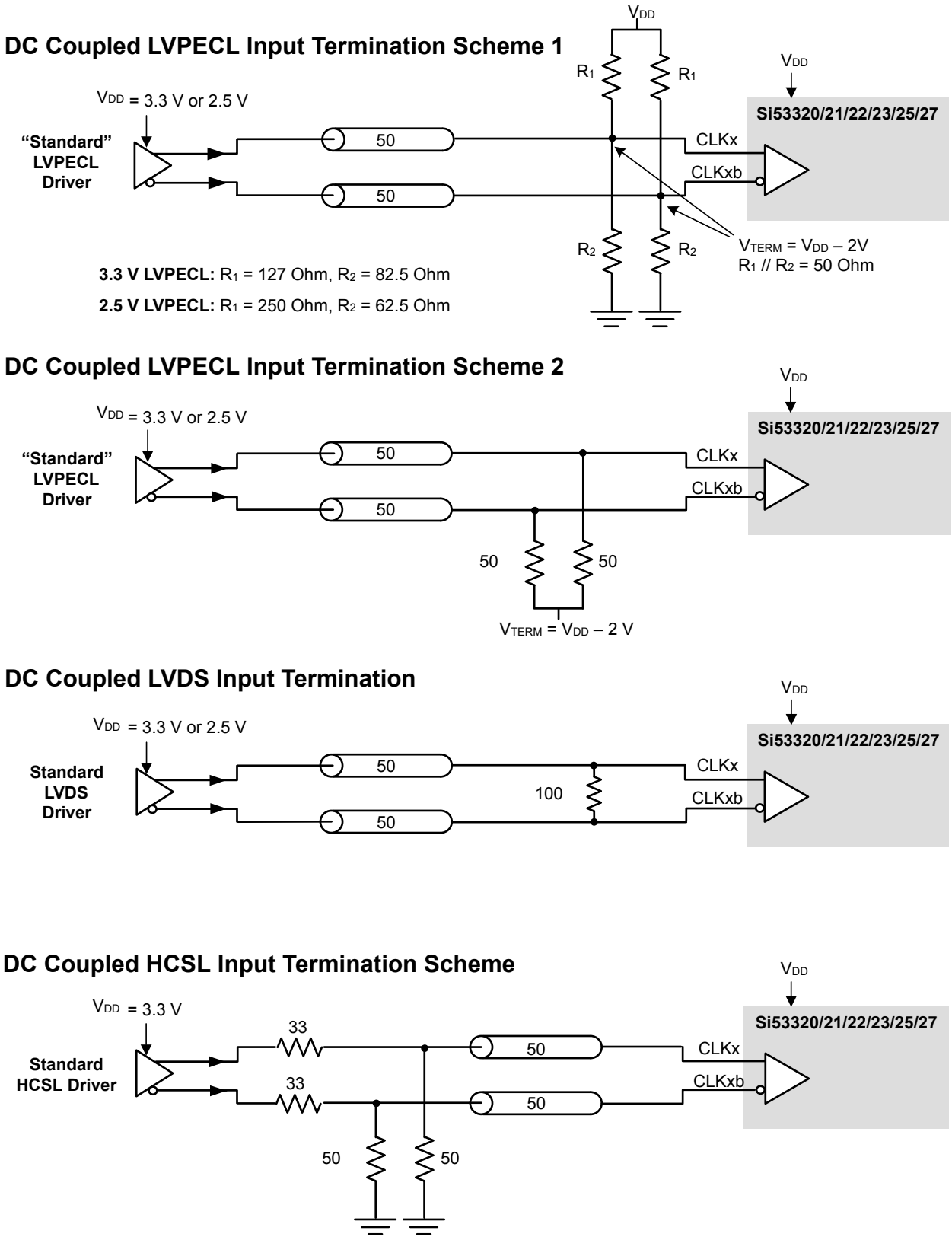


Figure 2.3. Differential DC-Coupled Input Terminations (Si53320/21/22/23/25/27)

2.2 LVCMOS Input Termination (Si53326/28 Only)

The table below summarizes the various ac- and dc-coupling options supported by the LVCMOS device, and the figure shows the recommended input clock termination.

Note: 1.8 V LVCMOS inputs are not supported for Si53326/28.

Table 2.2. LVCMOS Input Clock Options

	LVCMOS	
	AC-Coupled	DC-Coupled
1.8 V	No	No
2.5/3.3 V	Yes	Yes

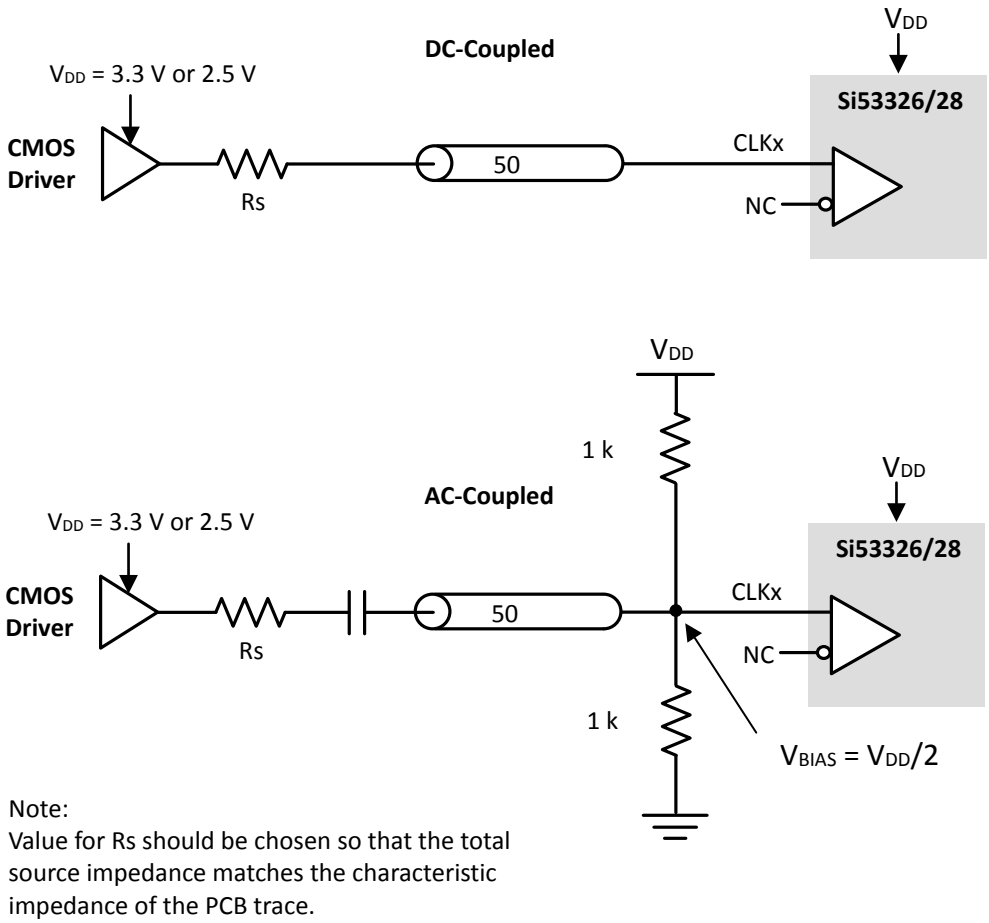


Figure 2.4. Recommended Input Clock Termination (Si53326/28)

2.3 Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The non-inverting input is biased with a 18.75 kΩ pull-down to GND and a 75 kΩ pull-up to V_{DD}. The inverting input is biased with a 75 kΩ pull-up to V_{DD}.

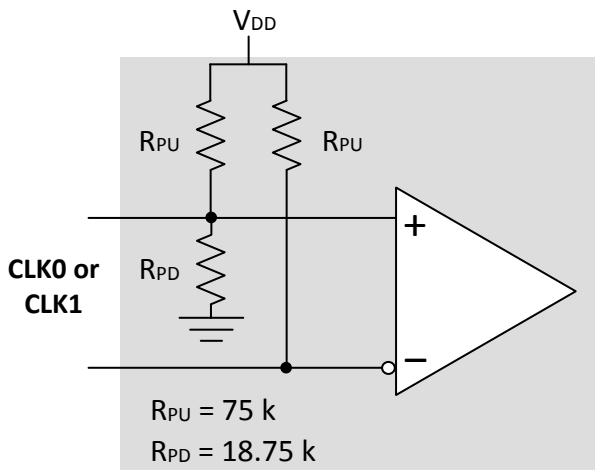


Figure 2.5. Input Bias Resistors

Note: To minimize the possibility of system noise coupling into the Si5332x differential inputs and adversely affecting the buffered output, Silicon Labs recommends 1 PPS clocks and disabled/gapped clocks be dc-coupled and driven “stop-low”.

2.4 Input Mux

The Si53320/21/23/26/27/28 provide two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The following table summarizes the input and output clock based on the input mux and output enable pin settings.

Table 2.3. Input Mux Logic

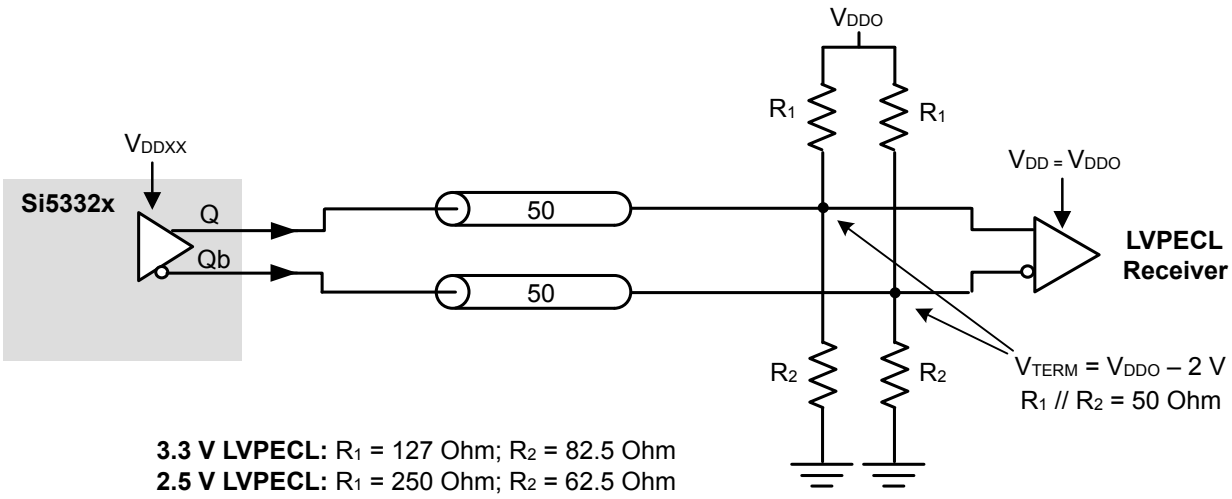
CLK_SEL	CLK0	CLK1	Q[1]	Qb
L	L	X	L	H
L	H	X	H	L
H	X	L	L	H
H	X	H	H	L

Note:
1. On the next negative transition of CLK0 or CLK1.

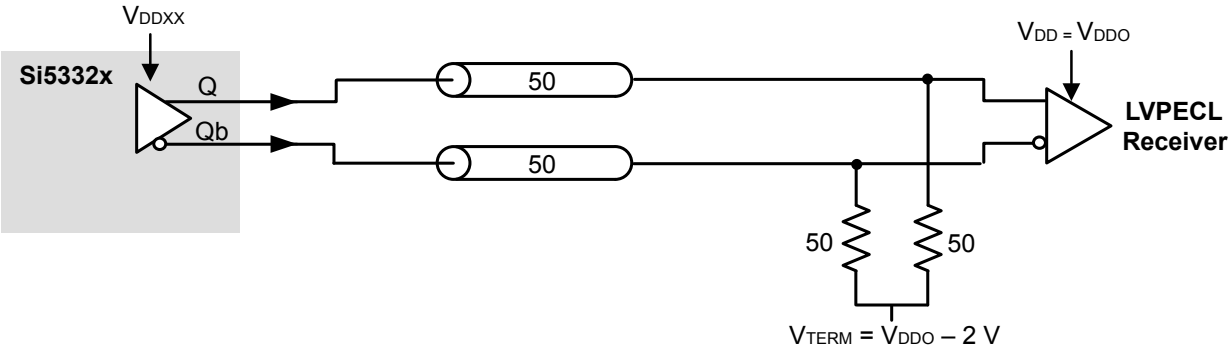
2.5 Output Clock Termination Options

The recommended output clock termination options for dc and ac are shown below. Unused outputs should be left unconnected.

DC Coupled LVPECL Output Termination Scheme 1



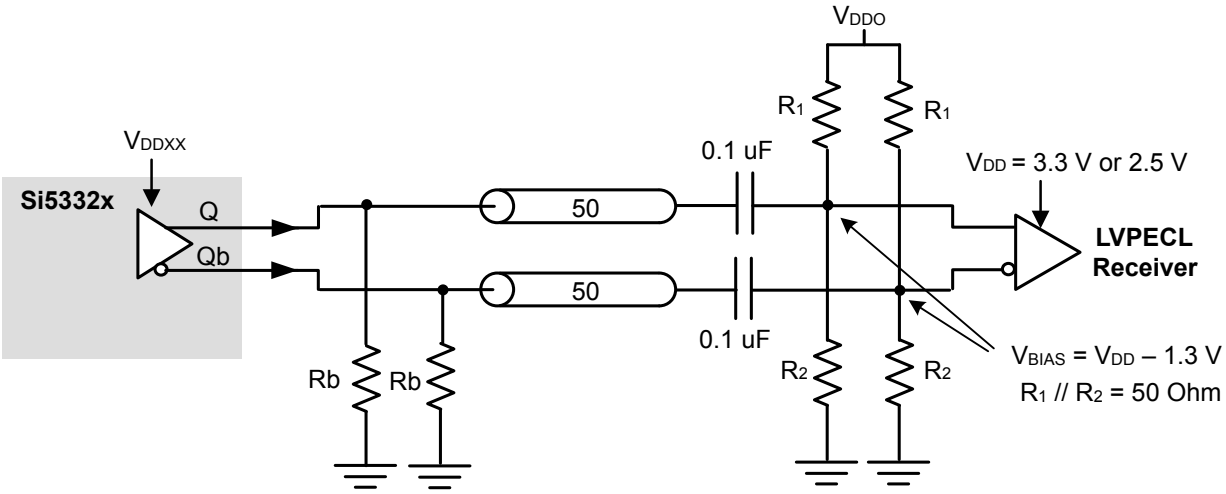
DC Coupled LVPECL Output Termination Scheme 2



Note:
For Si53320/21/22/23/25/26, $V_{DDXX} = V_{DD}$ = 3.3 V, 2.5 V
For Si53327/28, $V_{DDXX} = V_{DDOA}$ or V_{DDOB} = 3.3 V, 2.5 V

Figure 2.6. LVPECL DC Output Terminations

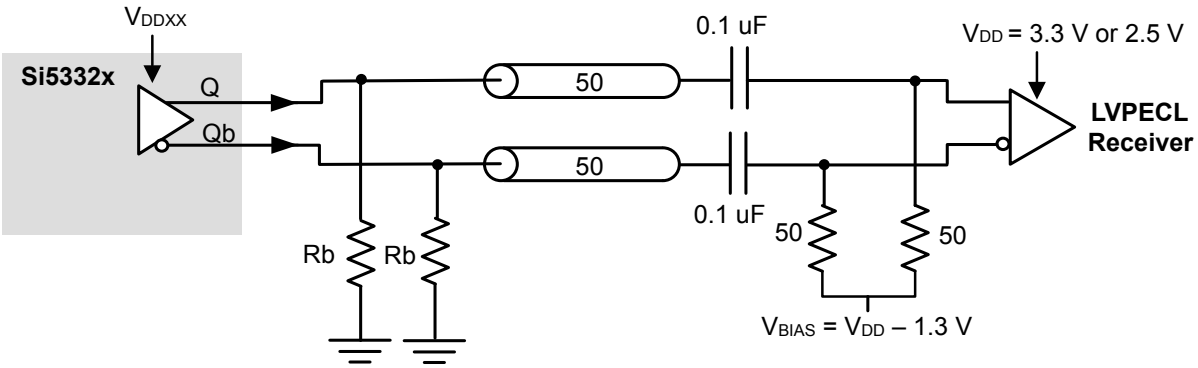
AC Coupled LVPECL Output Termination Scheme 1



3.3 V LVPECL: R_1 = 82.5 Ohm; R_2 = 127 Ohm; Rb = 120 Ohm

2.5 V LVPECL: R_1 = 62.5 Ohm; R_2 = 250 Ohm; Rb = 90 Ohm

AC Coupled LVPECL Output Termination Scheme 2



3.3 V LVPECL: Rb = 120 Ohm

2.5 V LVPECL: Rb = 90 Ohm

Note:
For Si53320/21/22/23/25/26, V_{DDXX} = V_{DD} = 3.3 V, 2.5 V
For Si53327/28, V_{DDXX} = V_{DDOA} or V_{DDOB} = 3.3 V, 2.5 V

Figure 2.7. LVPECL AC Output Terminations

2.6 AC Timing Waveforms

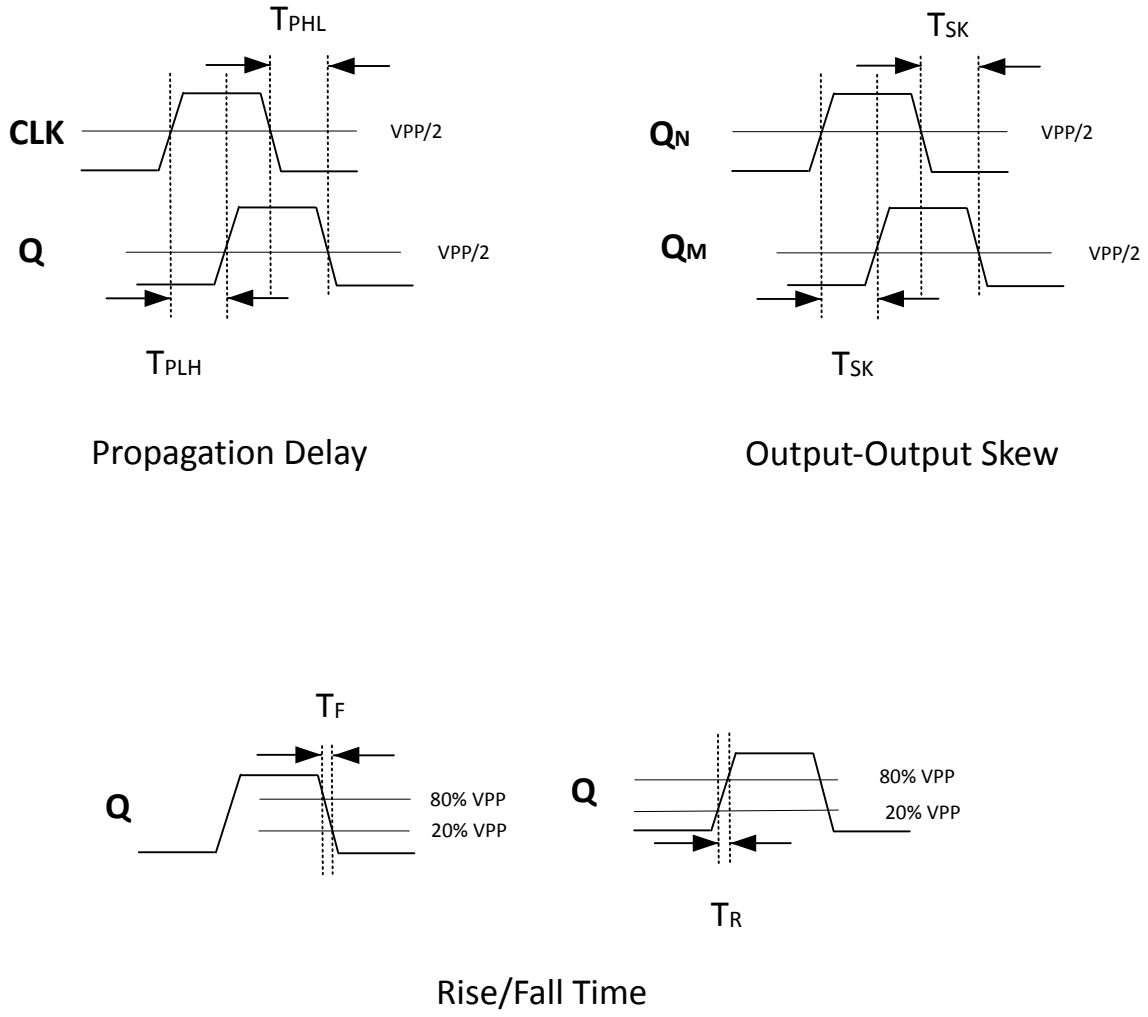


Figure 2.8. AC Timing Waveforms

2.7 Typical Phase Noise Performance: Differential Input Clock

Each of the phase noise plots superimposes Source Jitter, Total SE Jitter, and Total Diff Jitter on the same diagram.

- **Source Jitter**—Reference clock phase noise (measured Single-ended to PNA).
- **Total Jitter (SE)**—Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.
- **Total Jitter (Diff)**—Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. For more information, see 3. Electrical Specifications.

Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

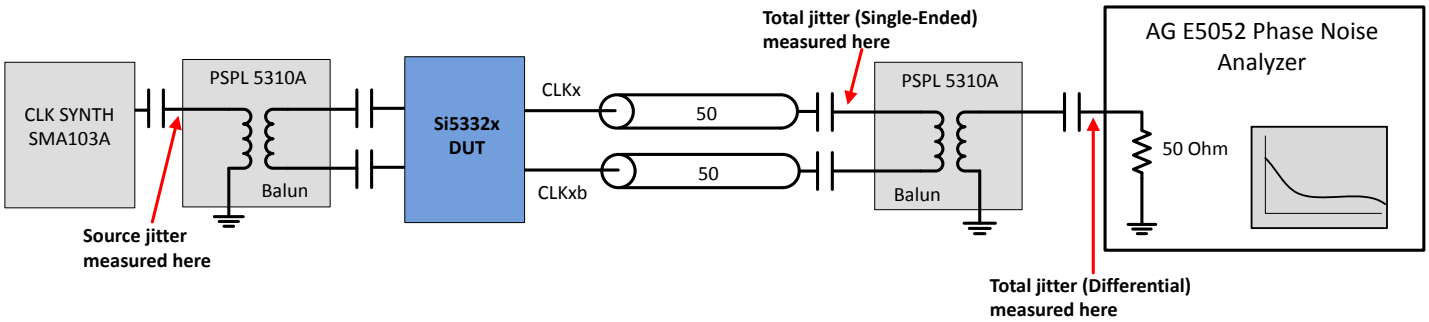
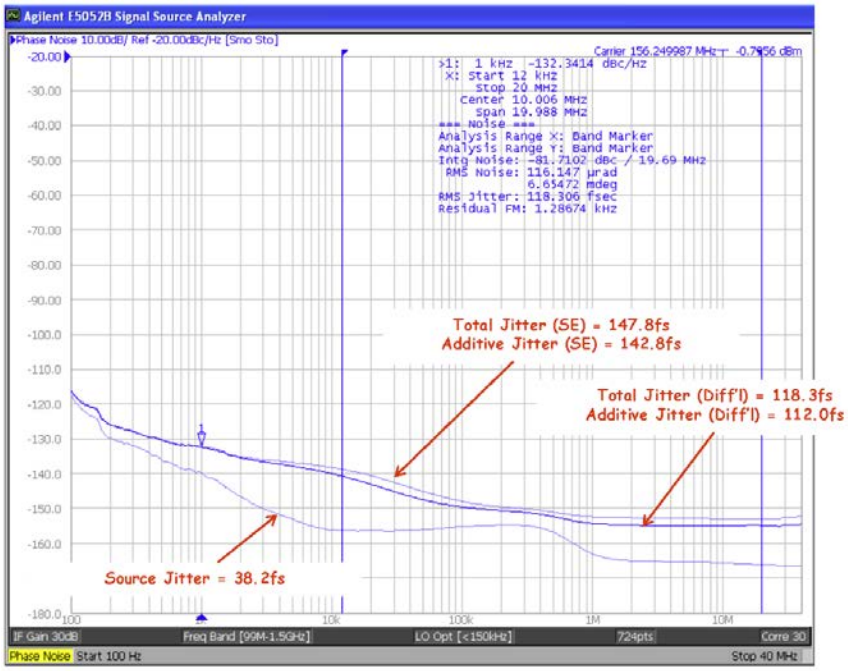


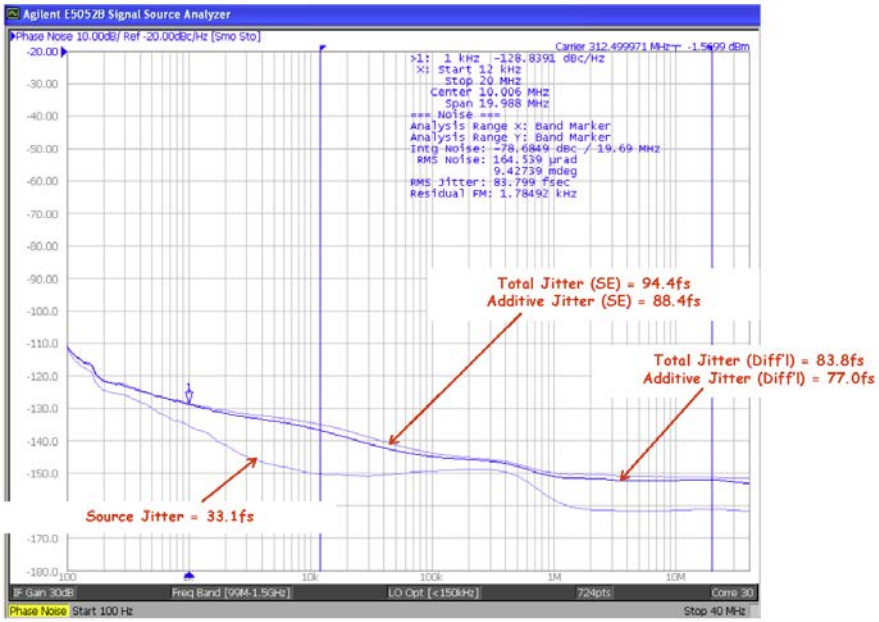
Figure 2.9. Differential Measurement Method Using a Balun

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



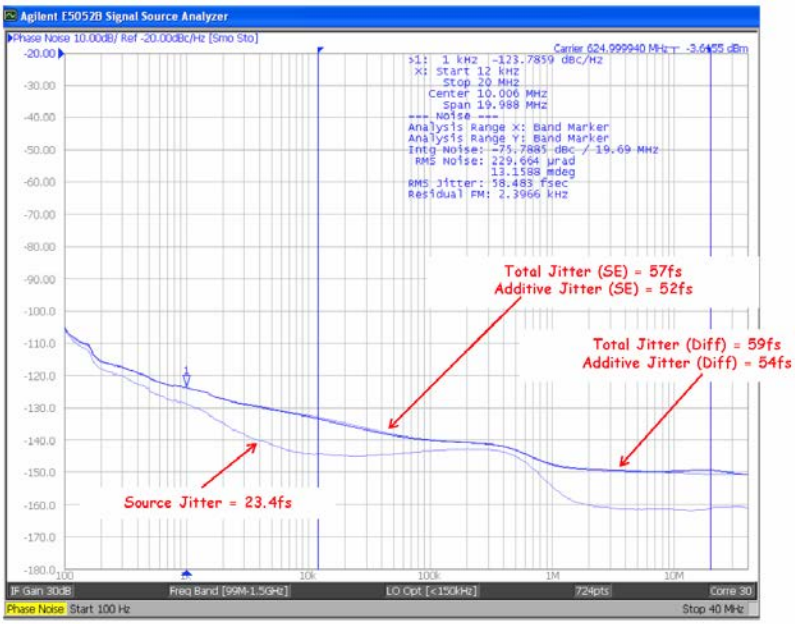
Frequency (MHz)	Differential Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Differential) (fs)	Additive Jitter (Differential) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

Figure 2.10. Total Jitter Differential Input (156.25 MHz)



Frequency (MHz)	Differential Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Differential) (fs)	Additive Jitter (Differential) (fs)
312.5	1.0	33.10	94.39	88.39	83.80	76.99

Figure 2.11. Total Jitter Differential Input (312.5 MHz)



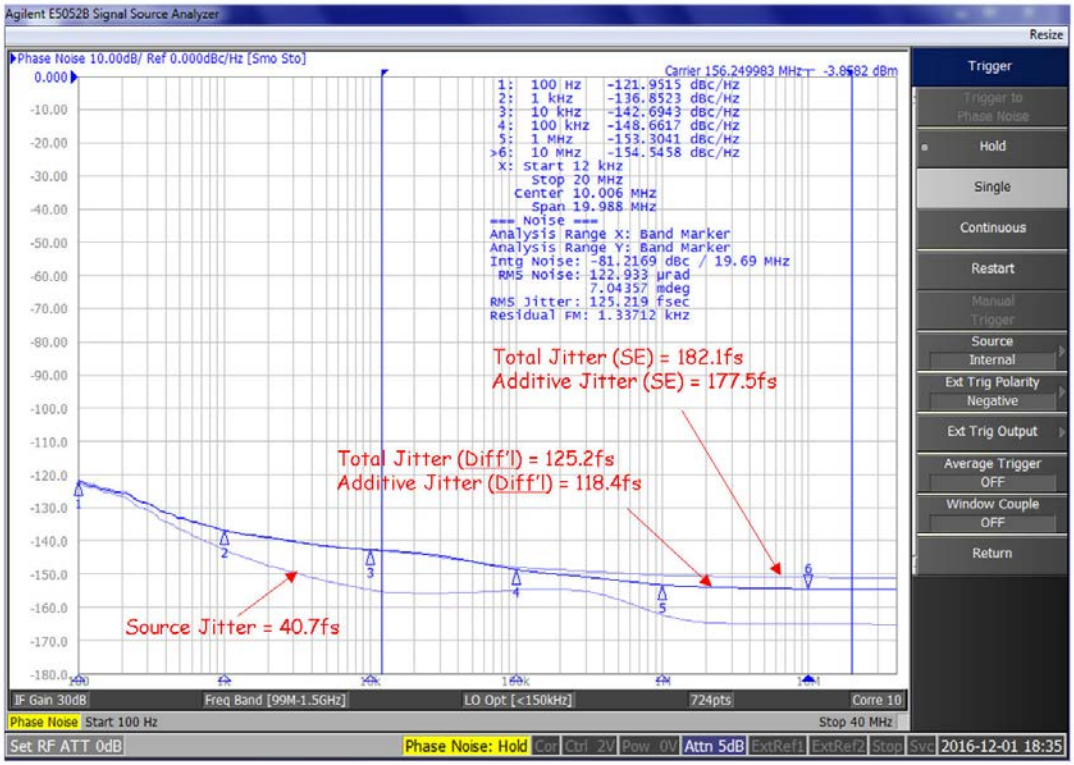
Frequency (MHz)	Differential Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Differential) (fs)	Additive Jitter (Differential) (fs)
625	1.0	23	57	52	59	54

Figure 2.12. Total Jitter Differential Input (625 MHz)

2.8 Typical Phase Noise Performance: Single-Ended Input Clock

For single-ended input phase noise measurements, the input was connected directly without the use of a balun.

The following figure shows three phase noise plots superimposed on the same diagram.



Frequency (MHz)	Single-Ended Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Differential) (fs)	Additive Jitter (Differential) (fs)
156.25	1.0	40.74	182.12	177.51	125.22	118.41

Figure 2.13. Total Jitter Single-Ended Input (156.25 MHz)

2.9 Input Mux Noise Isolation

The input clock mux is designed to minimize crosstalk between the CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. The following figure shows a measurement of the input mux's noise isolation.

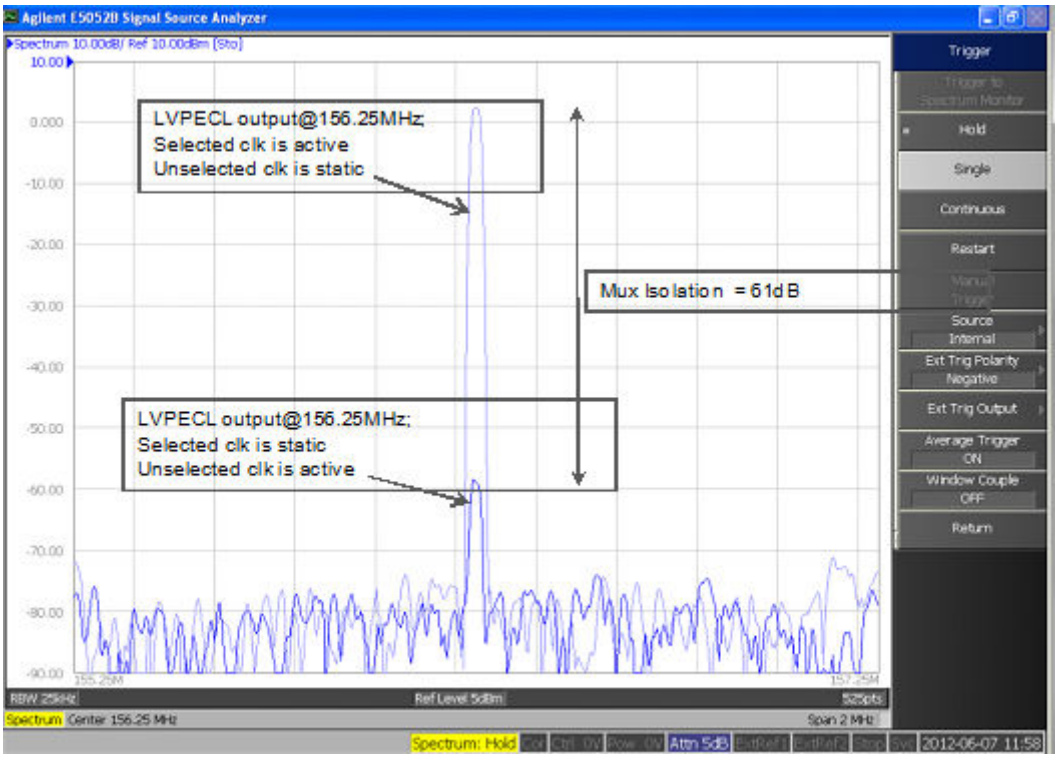


Figure 2.14. Input Mux Noise Isolation (Differential Input Clock, 44-QFN Package)

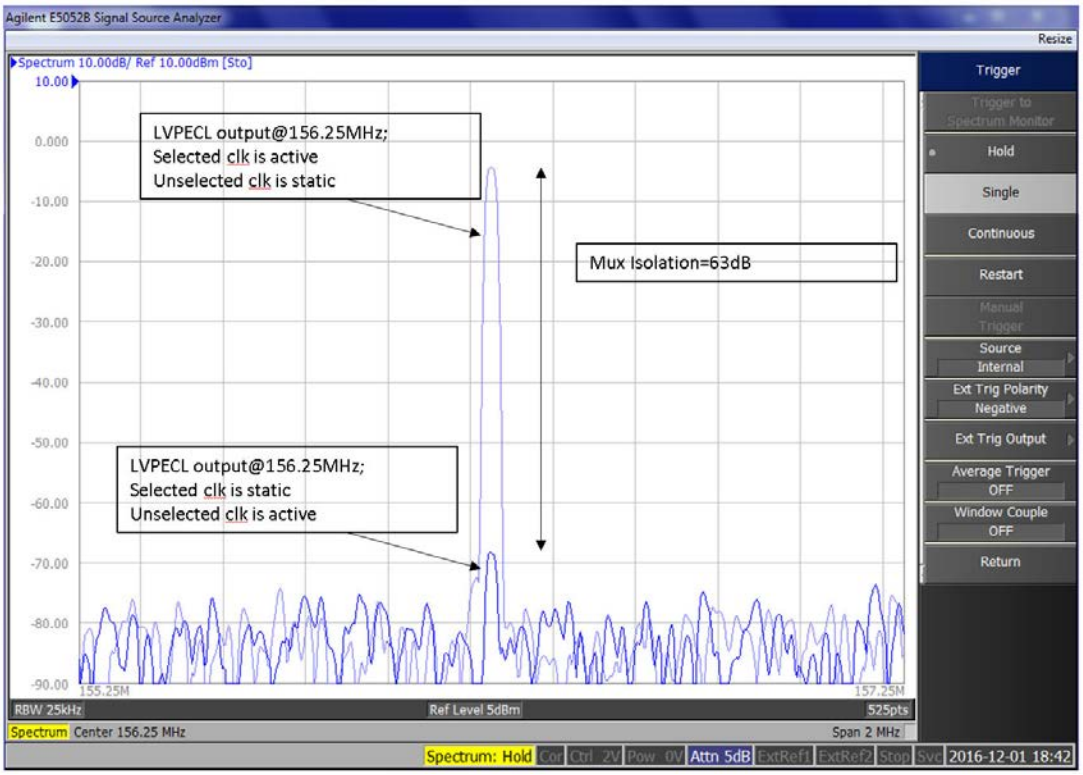


Figure 2.15. Input Mux Noise Isolation (Single-Ended Input Clock, 24-QFN Package)

2.10 Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject power supply noise and simplify low-jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for more information.

3. Electrical Specifications

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range	V_{DD}	LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V

Table 3.2. Input Clock Specifications

V_{DD} = 2.5 V ± 5% or 3.3 V ± 10%; T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}		0.05	—	—	V
Differential Input Swing (peak-to-peak)	V_{IN}		0.2	—	2.2	V
LVCMOS Input High Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
LVCMOS Input Low Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Capacitance	C_{IN}	CLK0 and CLK1 pins with respect to GND	—	5	—	pF

Table 3.3. DC Common Characteristics

V_{DD} = 2.5 V ± 5% or 3.3 V ± 10%; T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}[1]	Si53320	—	260	—	mA
		Si53321/25/26	—	440	—	mA
		Si53322	—	130	—	mA
		Si53323	—	210	—	mA
		Si53327/28	—	80	—	mA
Output Supply Current (Per Clock Output)	I_{DDOx}[1]	Si53327/28	—	35	—	mA
Input High Voltage	V_{IH}	CLK_SEL, OExb	V_{DD} x 0.8	—	—	V
Input Low Voltage	V_{IL}	CLK_SEL, OExb	—	—	V_{DD} x 0.2	V
Internal Pull-down Resistor	R_{DOWN}	CLK_SEL, OExb	—	25	—	kΩ

Note:
1. Measured using ac-coupled termination at V_{DD}/V_{DDOX} = 3.3 V.

Table 3.4. Output Characteristics (LVPECL)

V_{DD} = 2.5 V ± 5% or 3.3 V ± 10%; T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing[1]	V_{SE}		0.55	0.80	1.05	V
Output Common Mode Voltage	V_{COM}		V_{DD} – 1.595	—	V_{DD} – 1.245	V

Note:
1. Unused outputs can be left floating. Do not short unused outputs to ground.

Table 3.5. AC Characteristics

V_{DD} = 2.5 V ± 5% or 3.3 V ± 10%; T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	Si53326/28	dc	—	200	MHz
		Si53320	dc	—	725	MHz
		Si53321/22/23/25/27	dc	—	1250	MHz
Duty Cycle (50% input duty cycle)	D_C	20/80% T_R/T_F<10% of period (Differential input clock)	47	50	53	%
		20/80% T_R/T_F<10% of period (Single-Ended input clock)	45	50	55	%
Minimum Input Clock Slew Rate	SR_{diff}	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
	SR_{se}		1.00	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	20–80%	—	—	350	ps
Minimum Input Pulse Width	T_W		360	—	—	ps
Propagation Delay	T_{PLH}, T_{PHL}		600	800	1000	ps
Output-to-Output Skew[1]	T_{SK}		—	25	60	ps
Part-to-Part Skew[2]	T_{PS}		—	—	150	ps
Power Supply Noise Rejection[3]	PSRR	10 kHz sinusoidal noise	—	–65	—	dBc
		100 kHz sinusoidal noise	—	–62.5	—	dBc
		500 kHz sinusoidal noise	—	–60	—	dBc
		1 MHz sinusoidal noise	—	–55	—	dBc

Note:
1. Output-to-output skew specified for outputs with identical configuration.
2. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
3. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DD} (3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for more information.

Table 3.6. Additive Jitter, Differential Clock Input

V_{DD}	Input[1, 2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (Single-Ended, Peak-to-Peak)	Differential 20% to 80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	725	Differential	0.15	0.637	LVPECL	45	95
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
2.5	725	Differential	0.15	0.637	LVPECL	45	95
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185

Note:

1. For best additive jitter results, use the fastest slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 2.9 Differential Measurement Method Using a Balun on page 10.

Table 3.7. Additive Jitter, Single-Ended Clock Input

V_{DD}	Input[1, 2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (Single-Ended, Peak-to-Peak)	Single-Ended 20% to 80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185

Note:

1. For best additive jitter results, use the fastest slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 2.9 Differential Measurement Method Using a Balun on page 10.

Table 3.8. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
16-QFN Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	57.6	°C/W
16-QFN Thermal Resistance, Junction to Case	θ_{JC}	Still air	41.5	°C/W
20-TSSOP Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	93.88	°C/W
24-QFN Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	37	°C/W
24-QFN Thermal Resistance, Junction to Case	θ_{JC}	Still air	25	°C/W
32-eLQFP Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	54.9	°C/W
32-eLQFP Thermal Resistance, Junction to Case	θ_{JC}	Still air	10.0	°C/W
32-QFN Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	99.6	°C/W
32-QFN Thermal Resistance, Junction to Case	θ_{JC}	Still air	10.3	°C/W

Table 3.9. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	V_{DD}		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	V_{DD} + 0.3	V
Output Voltage	V_{OUT}		—	—	V_{DD} + 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	—	—	2000	V
	CDM		—	—	500	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C

Note:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

4. Detailed Block Diagrams

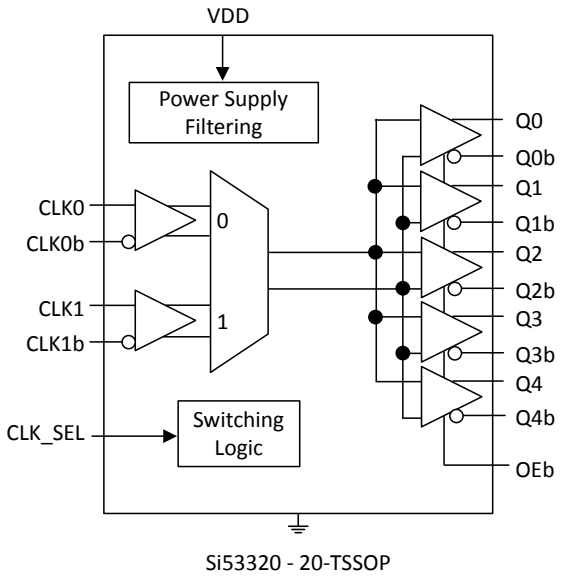


Figure 4.1. Si53320 Block Diagram

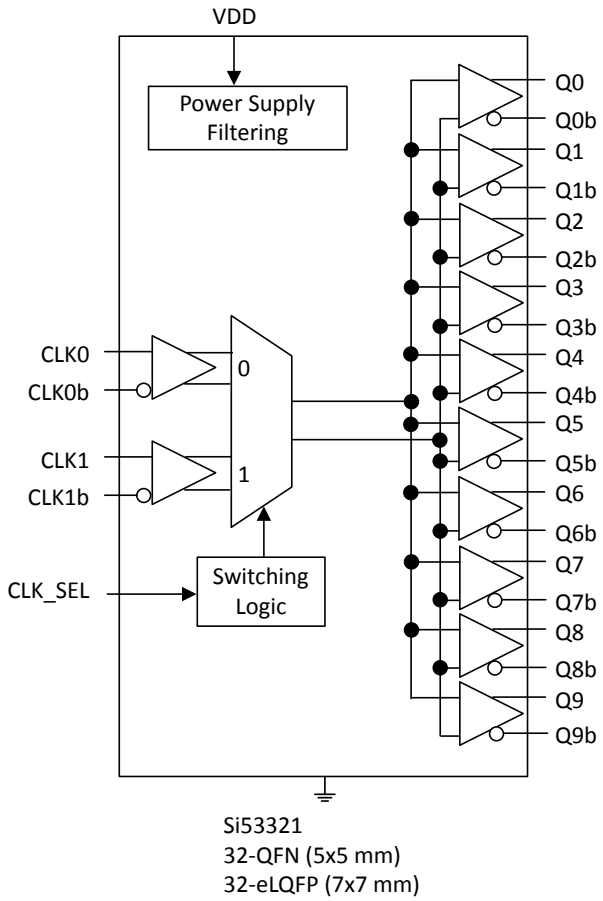


Figure 4.2. Si53321 Block Diagram

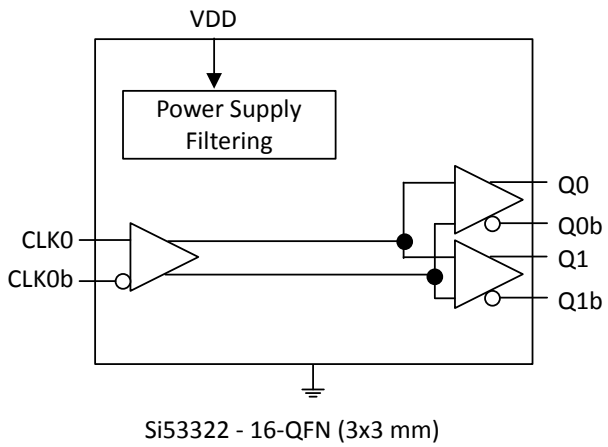


Figure 4.3. Si53322 Block Diagram

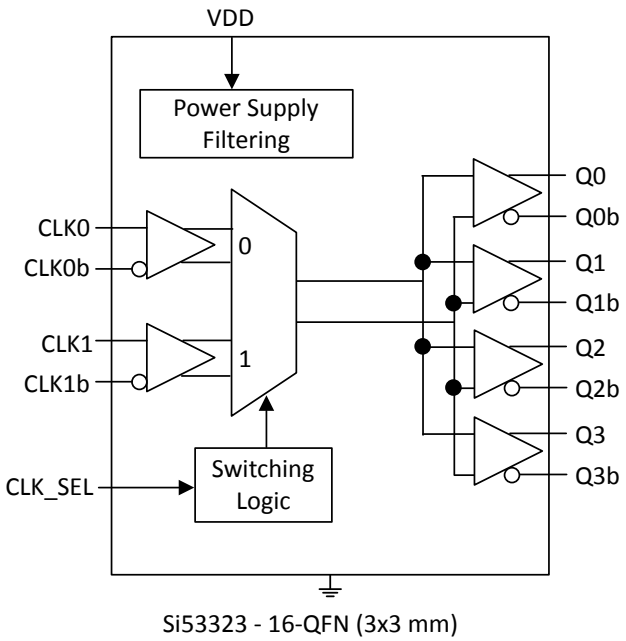


Figure 4.4. Si53323 Block Diagram

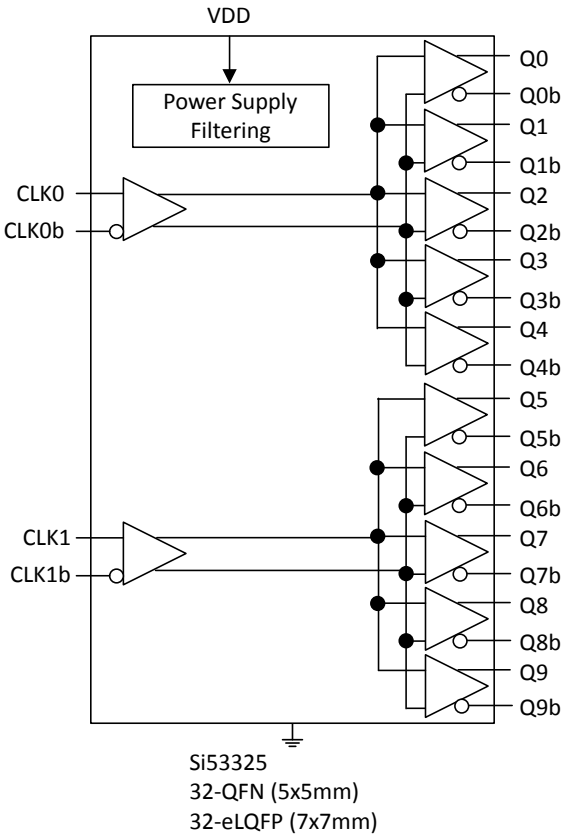


Figure 4.5. Si53325 Block Diagram

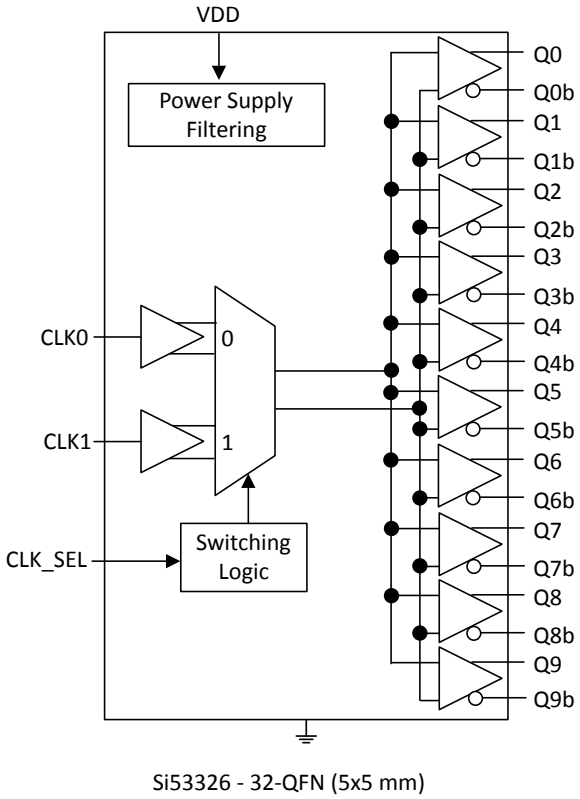


Figure 4.6. Si53326 Block Diagram

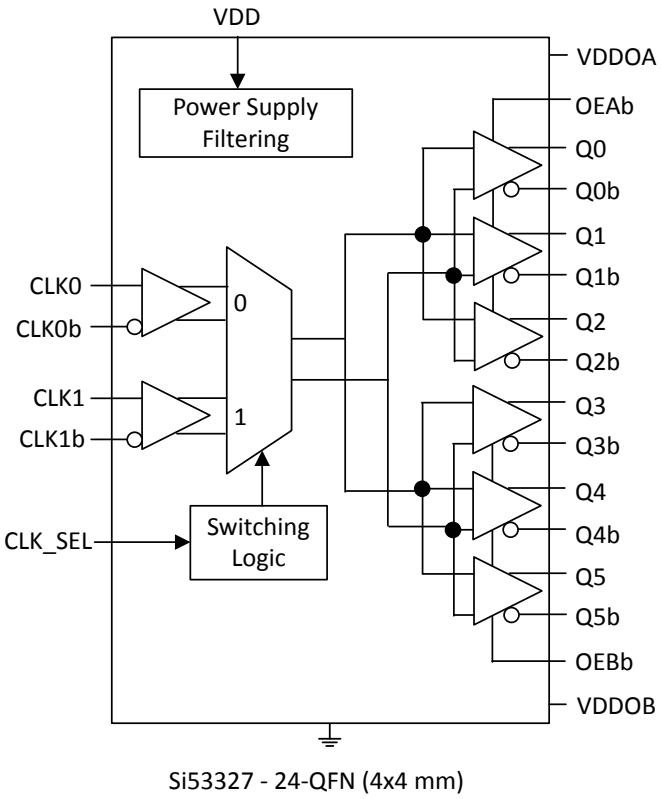


Figure 4.7. Si53327 Block Diagram

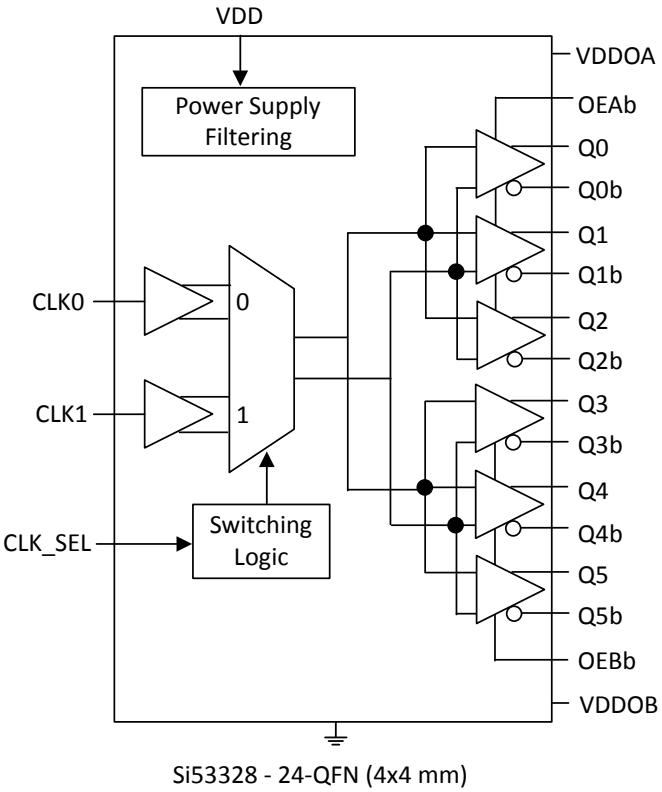


Figure 4.8. Si53328 Block Diagram

5. Pin Descriptions

5.1 Si53320 Pin Descriptions

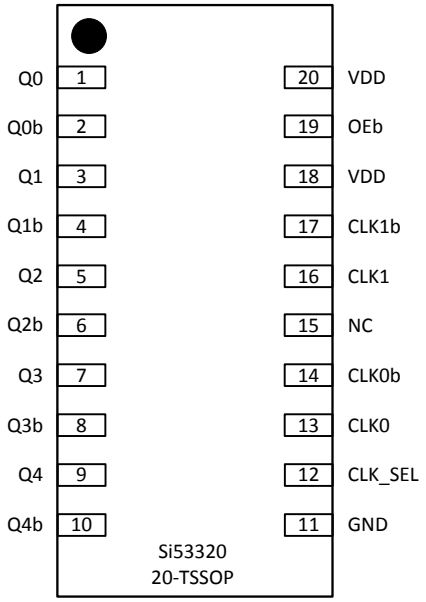


Table 5.1. Si53320 20-Pin TSSOP Descriptions

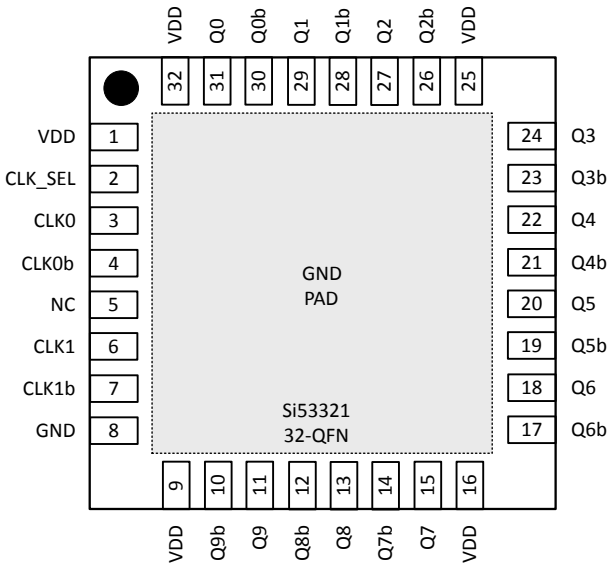
Pin #	Name	Type[1]	Description
1	Q0	O	Output clock 0.
2	Q0b	O	Output clock 0 (complement).
3	Q1	O	Output clock 1.
4	Q1b	O	Output clock 1 (complement).
5	Q2	O	Output clock 2.
6	Q2b	O	Output clock 2 (complement).
7	Q3	O	Output clock 3.
8	Q3b	O	Output clock 3 (complement).
9	Q4	O	Output clock 4.
10	Q4b	O	Output clock 4 (complement).
11	GND	GND	Ground.
12	CLK_SEL	I	Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
13	CLK0	I	Input clock 0.
14	CLK0b	I	Input clock 0 (complement). When CLK0 is driven by a single-ended input, connect CLK0b to an appropriate bias voltage (e.g., for a CMOS input apply $V_{DD}/2$).
15	NC	—	No connect. Leave this pin unconnected.
16	CLK1	I	Input clock 1.

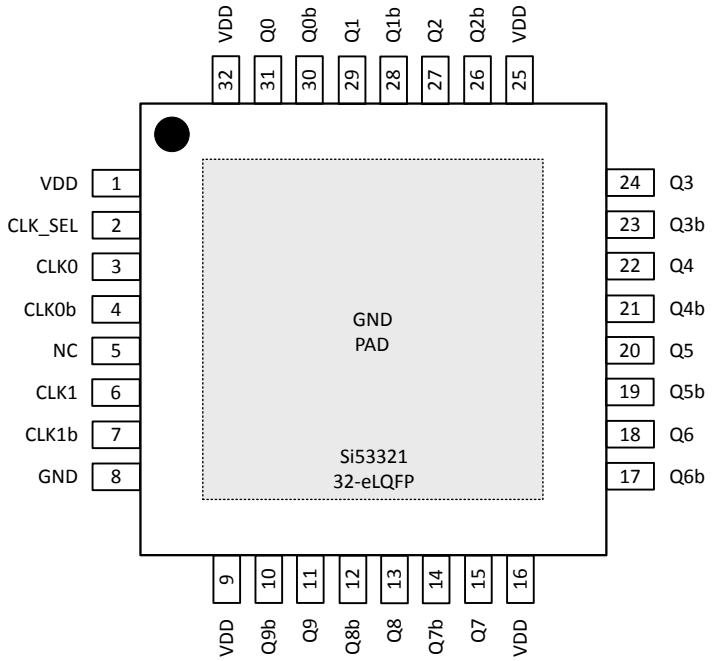
Pin #	Name	Type[1]	Description
17	CLK1b	I	Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect CLK1b to an appropriate bias voltage (e.g., for a CMOS input apply $V_{DD}/2$).
18	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
19	OEb	I	Output enable. When OEb = low, the clock outputs are enabled. When OEb = high, Qx is held low and Qxb is held high. OEb features an internal pull-down resistor and may be left unconnected.
20	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.

Note:

1. I = Input; O = Output; P = Power; GND = Ground.

5.2 Si53321 and Si53326 Pin Descriptions





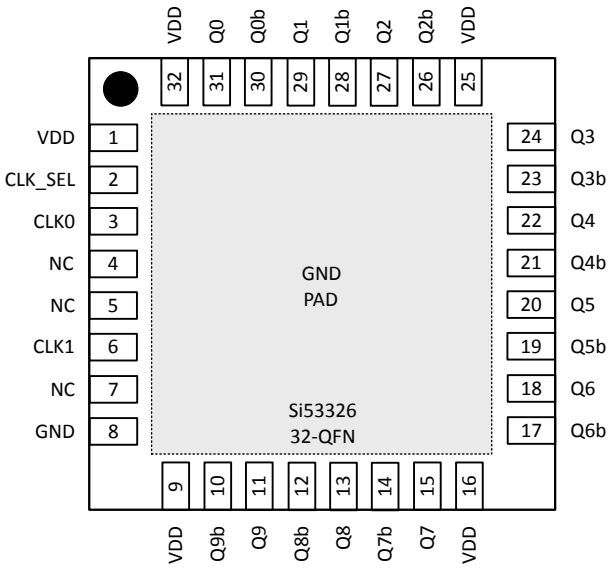


Table 5.2. Si53321 32-QFN/32-eLQFP and Si53326 32-QFN Pin Descriptions

Pin #	Name	Type[1]	Description
1	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
2	CLK_SEL	I	Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
3	CLK0	I	Input clock 0.
4	CLK0b (Si53321 only)	I	Input clock 0 (complement). When CLK0 is driven by a single-ended LVCMOS input, connect CLK0b to an appropriate bias voltage (e.g. $V_{DD}/2$).
	NC (Si53326 only)	—	No connect. Leave this pin unconnected.
5	NC		No connect. Leave this pin unconnected.
6	CLK1	I	Input clock 1.
7	CLK1b (Si53321 only)	I	Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect CLK1b to $V_{DD}/2$.
	NC (Si53326 only)	—	No connect. Leave this pin unconnected.
8	GND	GND	Ground.
9	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
10	Q9b	O	Output clock 9 (complement).
11	Q9	O	Output clock 9.
12	Q8b	O	Output clock 8 (complement).
13	Q8	O	Output clock 8.
14	Q7b	O	Output clock 7 (complement).
15	Q7	O	Output clock 7.
16	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
17	Q6b	O	Output clock 6 (complement).
18	Q6	O	Output clock 6.
19	Q5b	O	Output clock 5 (complement).
20	Q5	O	Output clock 5.
21	Q4b	O	Output clock 4 (complement).
22	Q4	O	Output clock 4.
23	Q3b	O	Output clock 3 (complement).
24	Q3	O	Output clock 3.
25	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
26	Q2b	O	Output clock 2 (complement).

Pin #	Name	Type[1]	Description
27	Q2	O	Output clock 2.
28	Q1b	O	Output clock 1 (complement).
29	Q1	O	Output clock 1.
30	Q0b	O	Output clock 0 (complement).
31	Q0	O	Output clock 0.
32	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
GND Pad	Exposed ground pad	GND	Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

Note:

1. I = Input; O = Output; P = Power; GND = Ground.

5.3 Si53322 Pin Descriptions

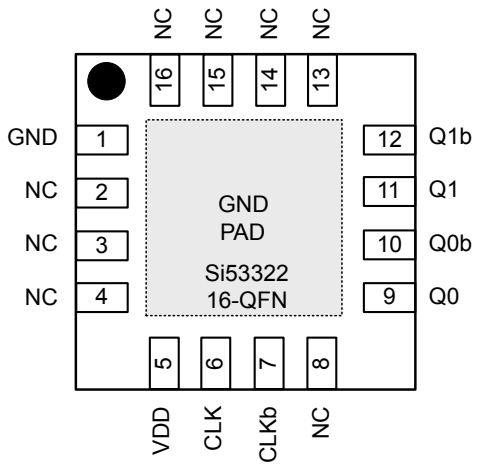


Table 5.3. Si53322 16-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	GND	GND	Ground.
2	NC	—	No connect. Leave this pin unconnected.
3	NC	—	No connect. Leave this pin unconnected.
4	NC	—	No connect. Leave this pin unconnected.
5	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
6	CLK	I	Input Clock
7	CLKb	I	Input clock (complement). When CLK is driven by a single-ended LVCMOS input, connect CLKb to an appropriate bias voltage (e.g. $V_{DD}/2$).
8	NC	—	No connect. Leave this pin unconnected.
9	Q0	O	Output Clock 0.
10	Q0b	O	Output Clock 0 (complement).
11	Q1	O	Output Clock 1.
12	Q1b	O	Output Clock 1 (complement).
13	NC	—	No connect. Leave this pin unconnected.
14	NC	—	No connect. Leave this pin unconnected.
15	NC	—	No connect. Leave this pin unconnected.
16	NC	—	No connect. Leave this pin unconnected.
GND Pad	Exposed ground pad	GND	Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

Note:
1. I = Input; O = Output; P = Power; GND = Ground.

5.4 Si53323 Pin Descriptions

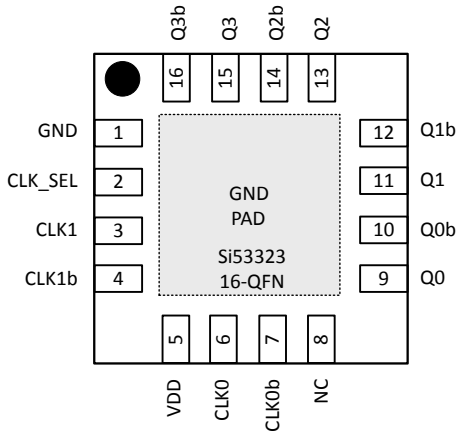
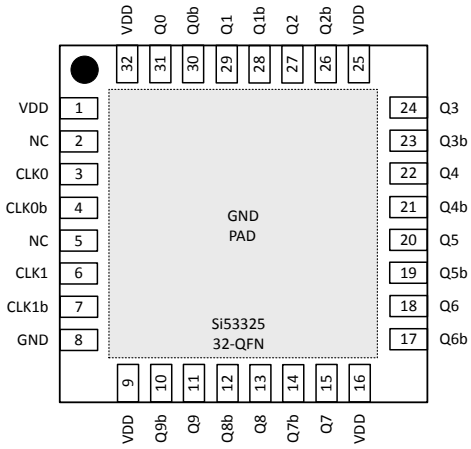


Table 5.4. Si53323 16-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	GND	GND	Ground.
2	CLK_SEL	I	Mux input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
3	CLK1	I	Input clock 1.
4	CLK1b	I	Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect CLK1b to an appropriate bias voltage (e.g., for a CMOS input apply $V_{DD}/2$).
5	VDD	P	Core and Output Voltage Supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
6	CLK0	I	Input Clock 0.
7	CLK0b	I	Input Clock 0 (complement). When CLK0 is driven by a single-ended input, connect CLK0b to an appropriate bias voltage (e.g., for a CMOS input apply $V_{DD}/2$).
8	NC	—	No connect. Leave this pin unconnected.
9	Q0	O	Output Clock 0.
10	Q0b	O	Output Clock 0 (complement).
11	Q1	O	Output Clock 1.
12	Q1b	O	Output Clock 1 (complement).
13	Q2	O	Output Clock 2.
14	Q2b	O	Output Clock 2 (complement).
15	Q3	O	Output Clock 3.
16	Q3b	O	Output Clock 3 (complement).
GND Pad	Exposed ground pad	GND	Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

Note:
1. I = Input; O = Output; P = Power; GND = Ground.

5.5 Si53325 Pin Descriptions



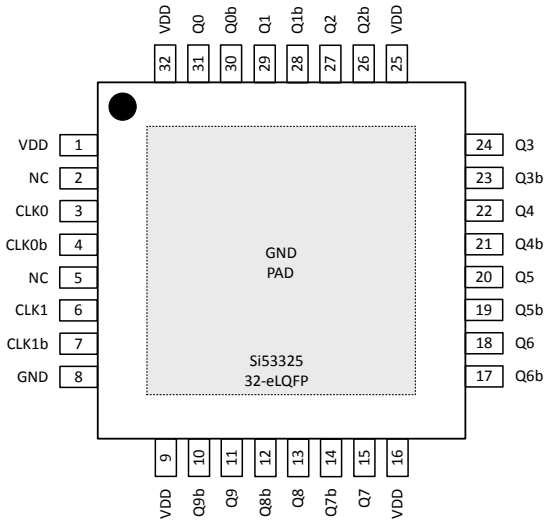


Table 5.5. Si53325 32-QFN and 32-eLQFP Pin Descriptions

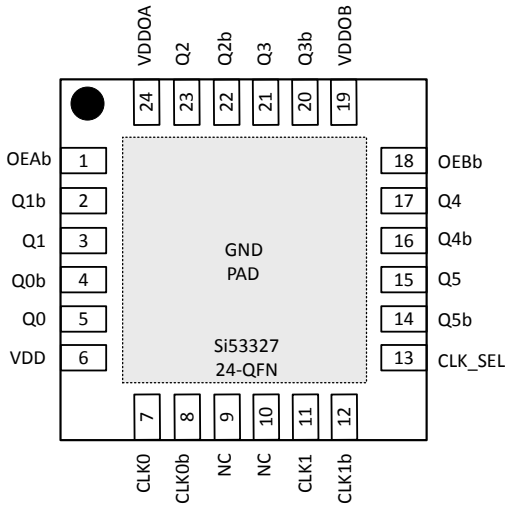
Pin #	Name[1]	Type	Description
1	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
2	NC	—	No connect. Leave this pin unconnected.
3	CLK0	I	Input clock 0.
4	CLK0b	I	Input clock 0 (complement).
5	NC	—	No connect. Leave this pin unconnected.
6	CLK1	I	Input clock 1.
7	CLK1b	I	Input clock 1 (complement).
8	GND	GND	Ground.
9	VDD	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
10	Q9b	O	Output clock 9 (complement).
11	Q9	O	Output clock 9.
12	Q8b	O	Output clock 8 (complement).
13	Q8	O	Output clock 8.
14	Q7b	O	Output clock 7 (complement).
15	Q7	O	Output clock 7.
16	VDD	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
17	Q6b	O	Output clock 6 (complement).
18	Q6	O	Output clock 6.
19	Q5b	O	Output clock 5 (complement).
20	Q5	O	Output clock 5.

Pin #	Name[1]	Type	Description
21	Q4b	O	Output clock 4 (complement).
22	Q4	O	Output clock 4.
23	Q3b	O	Output clock 3 (complement).
24	Q3	O	Output clock 3.
25	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
26	Q2b	O	Output clock 2 (complement).
27	Q2	O	Output clock 2.
28	Q1b	O	Output clock 1 (complement).
29	Q1	O	Output clock 1.
30	Q0b	O	Output clock 0 (complement).
31	Q0	O	Output clock 0.
32	VDD	P	Core and Output voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
GND Pad	Exposed ground pad	GND	Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

Note:

1. I = Input; O = Output; P = Power; GND = Ground.

5.6 Si53327 and Si53328 Pin Descriptions



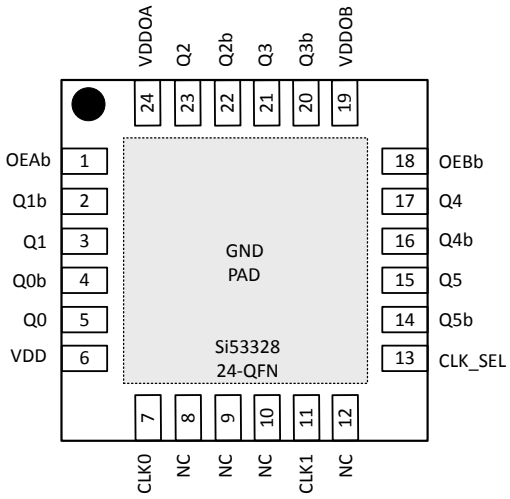


Table 5.6. Si53327 and Si53328 24-QFN Pin Descriptions

Pin	Name	Type[1]	Description
1	OEAb	I	Output Enable for Bank A (Q0, Q1, Q2). When OEAb = LOW, outputs Q0, Q1, and Q2 are enabled. This pin contains an active pull-down resistor, and leaving the pin disconnected enables the outputs. When OEAb = HIGH, Q0, Q1, and Q2 are disabled.
2	Q1b	O	Output clock 1 (Complement).
3	Q1	O	Output clock 1.
4	Q0b	O	Output clock 0 (complement).
5	Q0	O	Output clock 0.
6	VDD	P	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
7	CLK0	I	Input clock 0. Bypass with 1.0 µF capacitor and place as close to the VDD pin as possible.
8	CLK0b (Si53327 only)	O	Input clock 0 (complement). When CLK0 is driven by a single-ended input, connect CLK0b to $V_{DD}/2$.
	NC (Si53328 only)	—	No connect. Leave this pin unconnected.
9	NC	—	No connect. Leave this pin unconnected.
10	NC	—	No connect. Leave this pin unconnected.
11	CLK1	I	Input clock 1.
12	CLK1b (Si53327 only)	I	Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect CLK1b to VDD/2.
	NC (Si53328 only)	—	No connect. Leave this pin unconnected.
13	CLK_SEL	I	Mux input select pin. When CLK_SEL=HIGH, CLK1 is selected. When CLK_SEL=LOW, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
14	Q5b	O	Output clock 5 (complement).
15	Q5	O	Output clock 5.

Pin	Name	Type[1]	Description
16	Q4b	O	Output clock 4 (complement).
17	Q4	O	Output clock 4.
18	OEBb	I	Output Enable for Bank B (Q3, Q4, Q5). When OEBb = LOW, outputs Q3, Q4, and Q5 are enabled. This pin contains an active pull-down resistor, and leaving the pin disconnected enables the outputs. When OEBb = HIGH, Q3, Q4, and Q5 are disabled.
19	VDDOB	P	Output voltage supply—Bank B (Outputs: Q3 to Q5). Bypass with 1.0 µF capacitor and place as close to the VDDOB pin as possible.
20	Q3b	O	Output clock 3 (complement).
21	Q3	O	Output clock 3.
22	Q2b	O	Output clock 2 (complement).
23	Q2	O	Output clock 2.
24	VDDOA	P	Output voltage supply—Bank A (Outputs: Q0 to Q2). Bypass with 1.0 µF capacitor and place as close to the VDDOA pin as possible.
GND Pad	Exposed ground pad	GND	Ground Pad—Power supply ground and thermal relief. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

Note:

1. I = Input; O = Output; P = Power; GND = Ground.

6. Package Outlines

6.1 16-Pin QFN Package

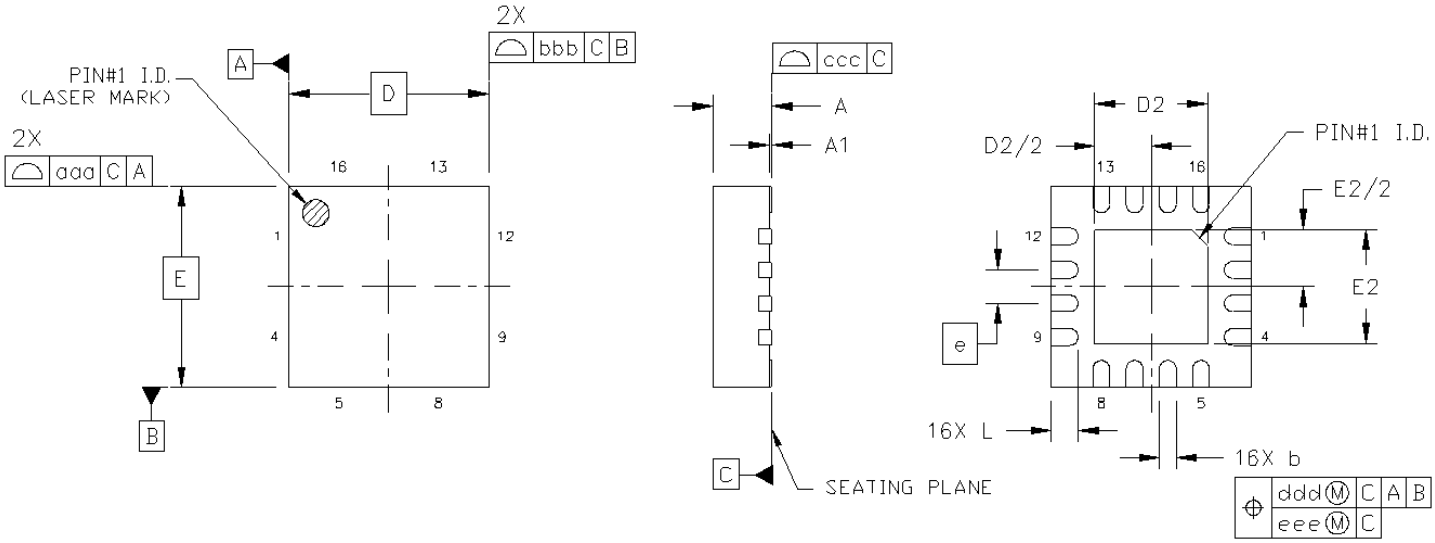


Figure 6.1. 16-Pin QFN Package

Table 6.1. 16-QFN Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		3.00 BSC.	
D2	1.65	1.70	1.75
e		0.50 BSC.	
E		3.00 BSC.	
E2	1.65	1.70	1.75
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6.2 20-Pin TSSOP Package

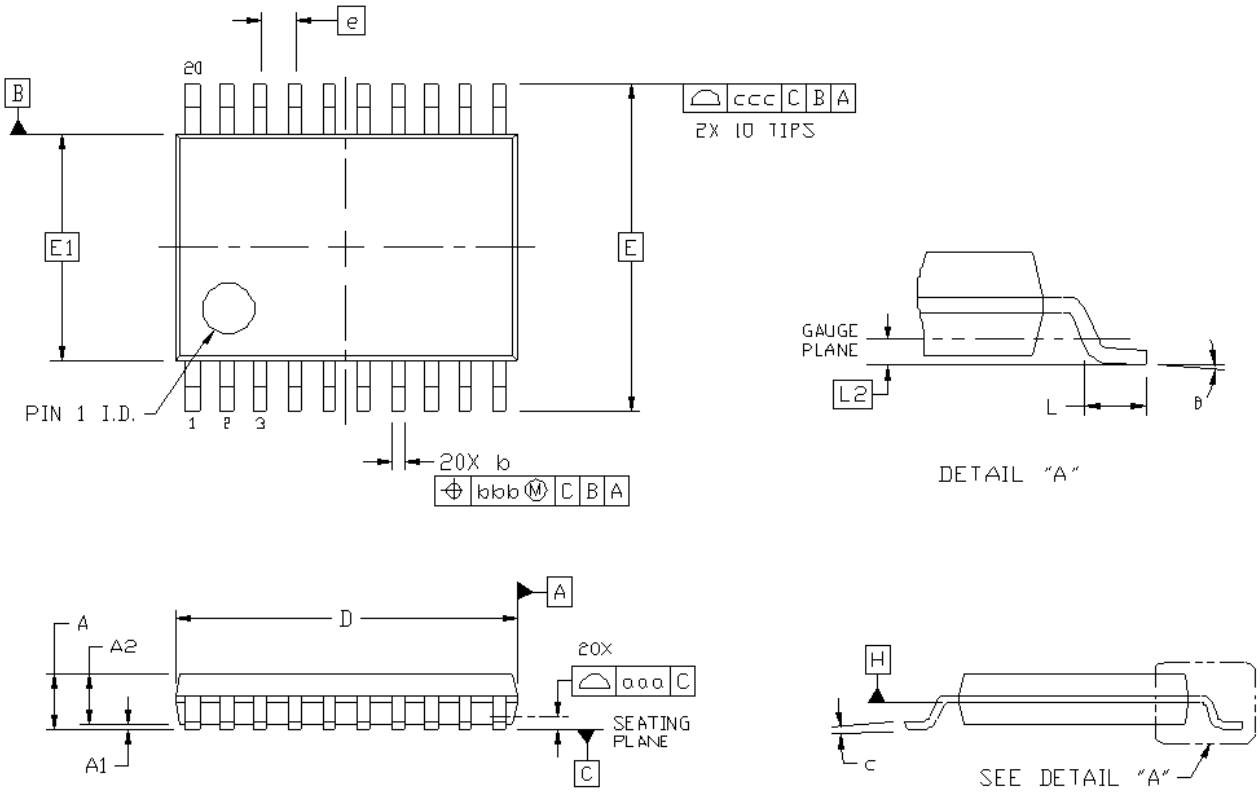


Figure 6.2. 20-Pin TSSOP Package

Table 6.2. 20-TSSOP Package Dimensions

Dimension	Min	Nom	Max		Dimension	Min	Nom	Max
A	—	—	1.20		e		0.65 BSC	
A1	0.05	—	0.15		L	0.45	0.60	0.75
A2	0.80	1.00	1.05		L2		0.25 BSC	
b	0.19	—	0.30		q	0°	—	8°
c	0.09	—	0.20		aaa		0.10	
D	6.40	6.50	6.60		bbb		0.10	
E		6.40 BSC			ccc		0.20	
E1	4.30	4.40	4.50					

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-153, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3 24-Pin QFN Package

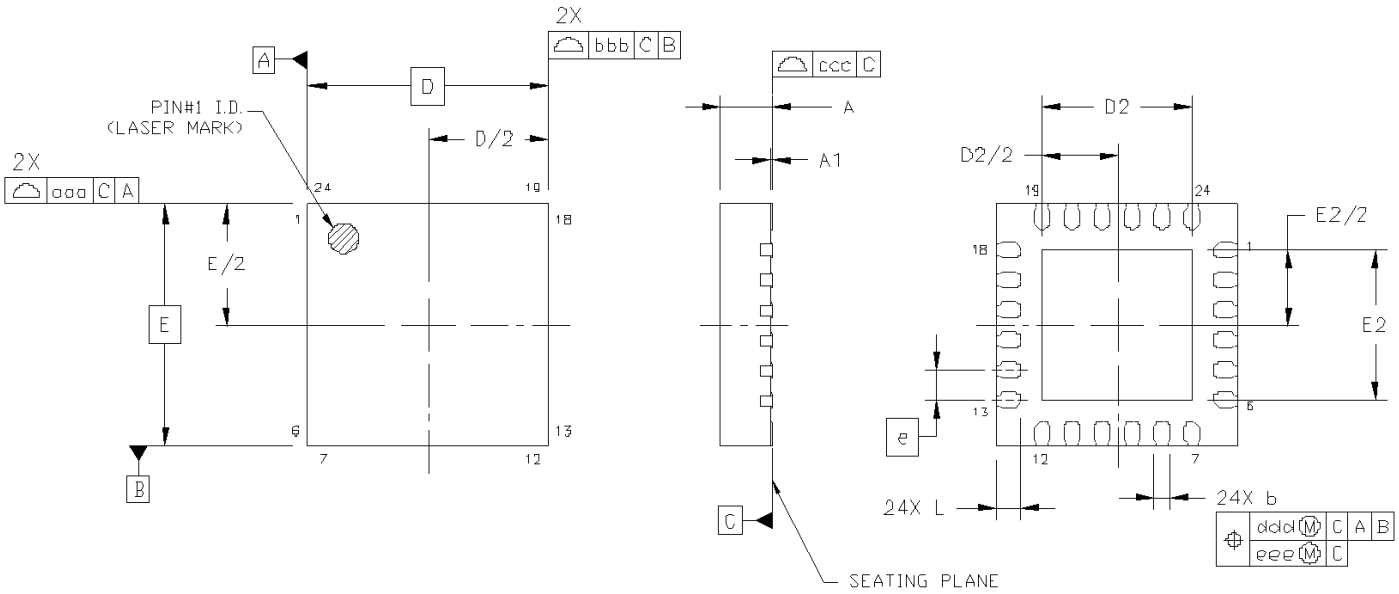


Figure 6.3. 24-Pin QFN Package

Table 6.3. 24-QFN Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6.4 32-Pin QFN Package

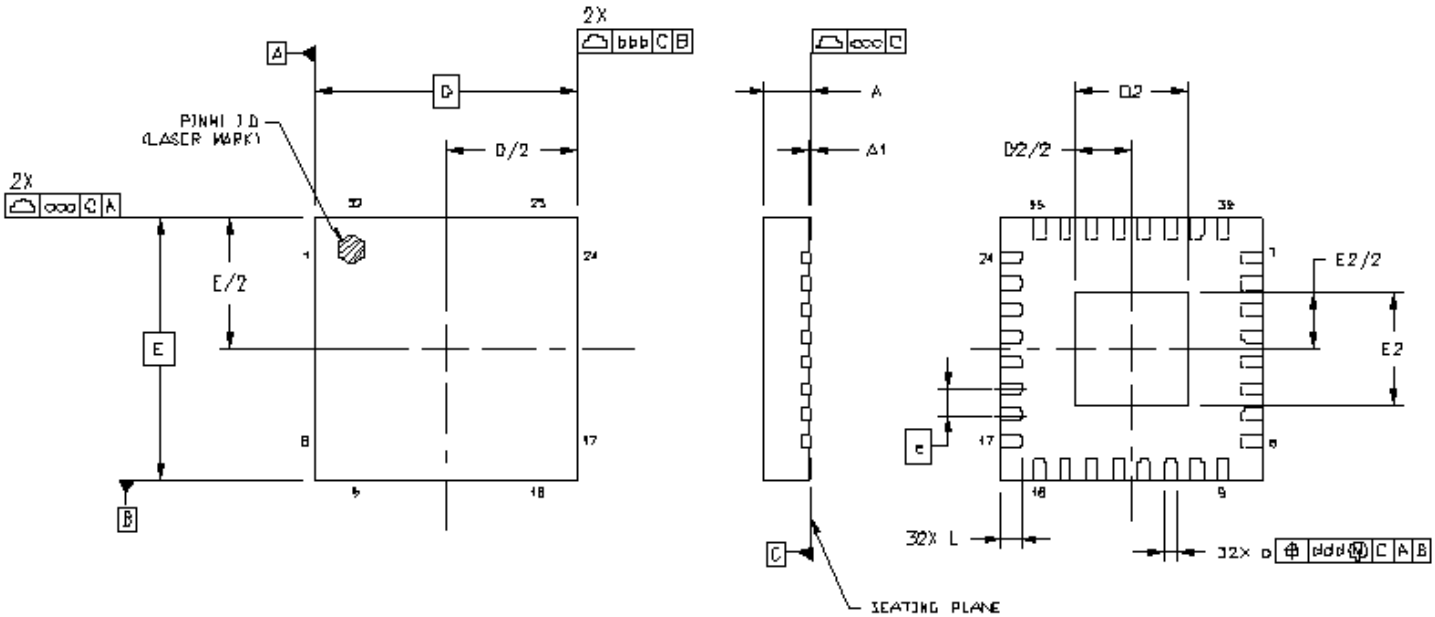


Figure 6.4. 32-Pin QFN Package

Table 6.4. 32-QFN Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.20	0.25	0.30
D		5.00 BSC	
D2	2.00	2.15	2.30
e		0.50 BSC	
E		5.00 BSC	
E2	2.00	2.15	2.30
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.

6.5 32-Pin eLQFP Package

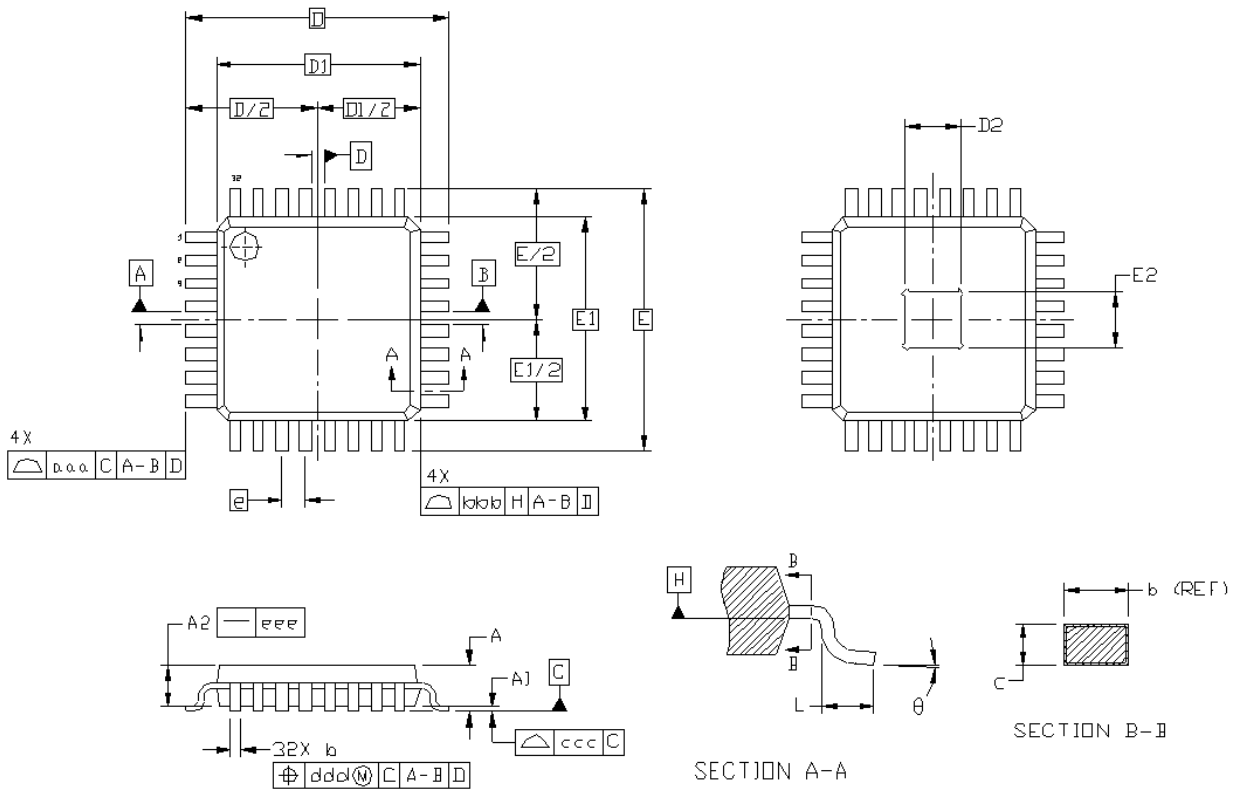


Figure 6.5. 32-Pin eLQFP Package

Table 6.5. 32-eLQFP Package Dimensions

Dimension	Min	Nom	Max		Dimension	Min	Nom	Max
A	—	—	1.60		E1		7.00 BSC	
A1	0.05	—	0.15		E2	1.87	1.92	1.97
A2	1.35	1.40	1.45		L	0.45	0.60	0.75
b	0.30	0.37	0.45		θ	0°	3.5°	7°
c	0.09	—	0.20		aaa		0.20	
D		9.00 BSC			bb	0.20		
D1		7.00 BSC			ccc	0.10		
D2	1.87	1.92	1.97		dddd		0.20	
e		0.80 BSC			eee	0.05		
E		9.00 BSC						

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Land Patterns

7.1 16-Pin QFN Land Pattern

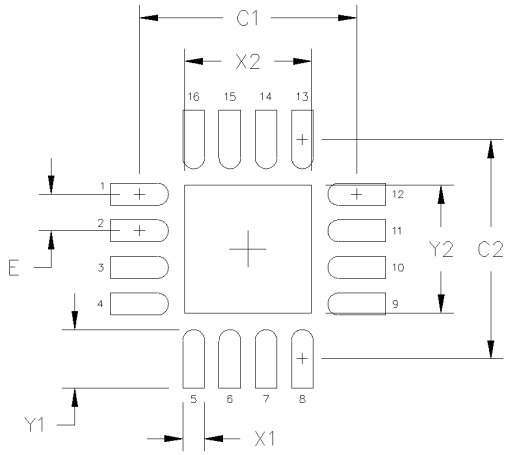


Figure 7.1. 16-Pin QFN Land Pattern

Table 7.1. 16-QFN Land Pattern Dimensions

Dimension	mm
C1	3.00
C2	3.00
E	0.50
X1	0.30
Y1	0.80
X2	1.75
Y2	1.75

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2 x 2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 20-Pin TSSOP Land Pattern

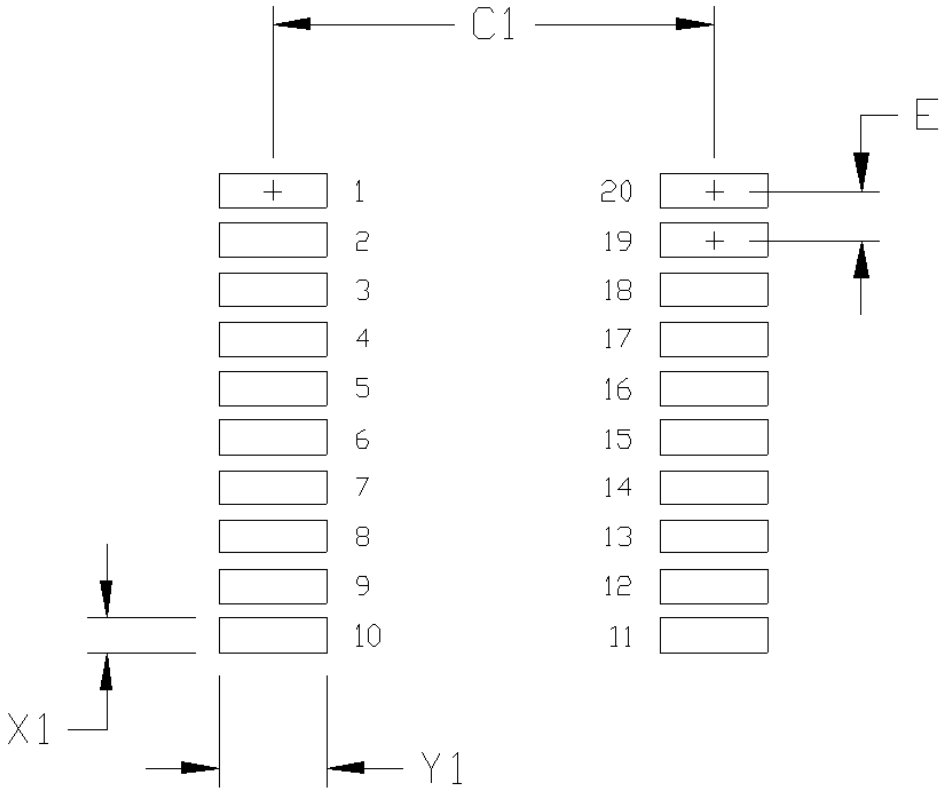


Figure 7.2. 20-Pin TSSOP Land Pattern

Table 7.2. 20-TSSOP Land Pattern Dimensions

Dimensions	Feature	(mm)
C1	Pad Column Spacing	5.80
E	Pad Row Pitch	0.65
X1	Pad Width	0.45
Y1	Pad Length	1.40

Note:

1. This Land Pattern Design is based on IPC-7351 specifications for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.3 24-Pin QFN Land Pattern

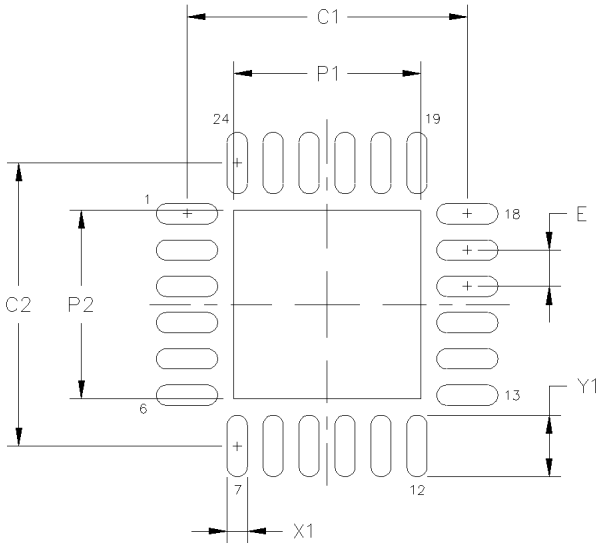


Figure 7.3. 24-Pin QFN Land Pattern

Table 7.3. 24-QFN Land Pattern Dimensions

Dimension	mm
P1	2.55
P2	2.55
X1	0.25
Y1	0.80
C1	3.90
C2	3.90
E	0.50

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.4 32-Pin QFN Land Pattern

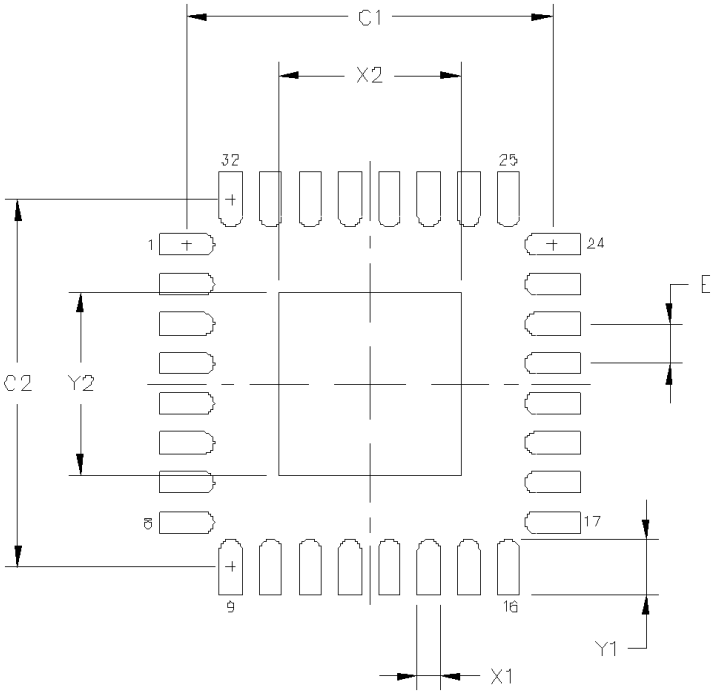


Figure 7.4. 32-Pin QFN Land Pattern

Table 7.4. 32-QFN Land Pattern Dimensions

Dimension	Min	Max		Dimension	Min	Max
C1	4.52	4.62		X2	2.20	2.30
C2	4.52	4.62		Y1	0.59	0.69
E	0.50 BSC			Y2	2.20	2.30
X1	0.20	0.30				

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2 x 2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.5 32-Pin eLQFP Land Pattern

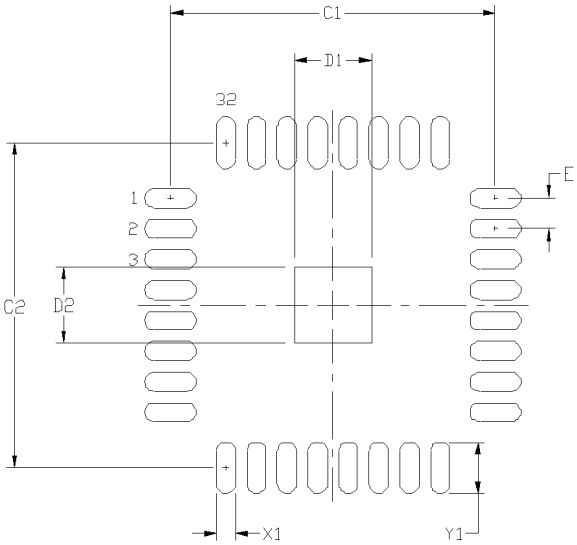


Figure 7.5. 32-Pin eLQFP Land Pattern

Table 7.5. 32-eLQFP Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
D1	1.84	2.00
D2	1.84	2.00
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A single 1.5 x 1.5 mm stencil aperture should be used for the center ground pad to achieve between 50-60% solder coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Markings

8.1 Si53320 Top Marking

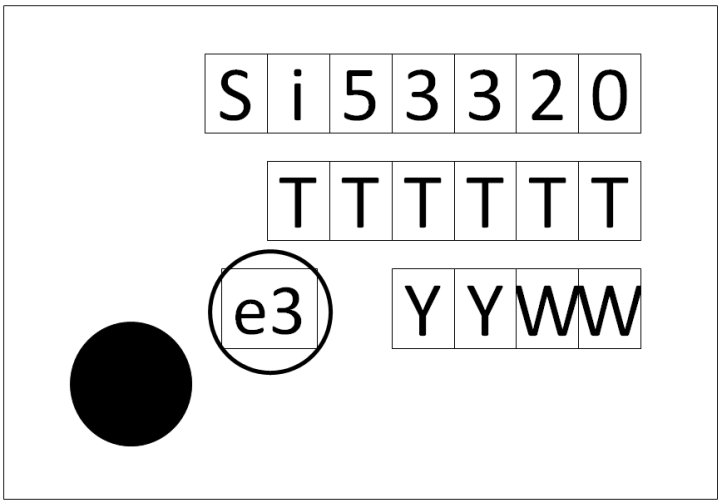


Figure 8.1. Si53320 Top Marking

Table 8.1. Si53320 Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (0.71 mm) Right-Justified	
Line 1 Marking:	Customer Part Number	Si53320
Line 2 Marking:	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to year and work week of the build date.

8.2 Si53321/25/26 Top Markings

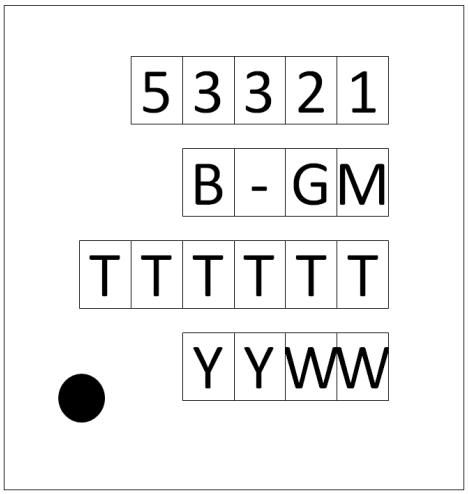


Figure 8.2. Si53321 Top Marking

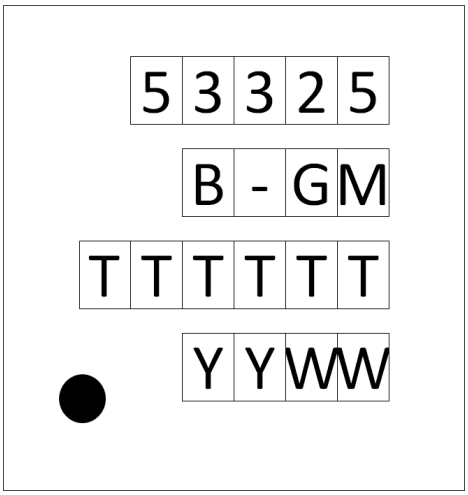


Figure 8.3. Si53325 Top Marking

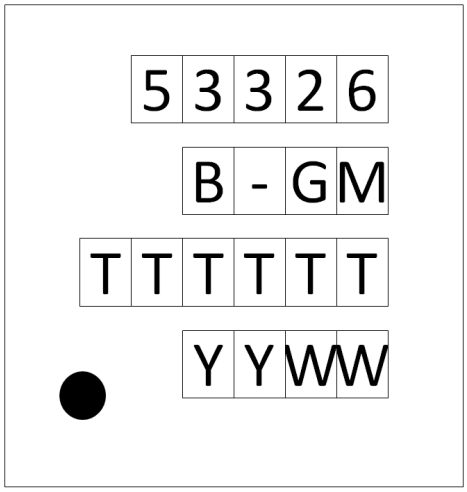


Figure 8.4. Si53326 Top Marking

Table 8.2. Si53321/25/26 Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (28 mils) Center-Justified	
Line 1 Marking:	Device Part Number	53321 for Si53321 53325 for Si53325 53326 for Si53326
Line 2 Marking:	Device Revision/Type	B-GM for Si53321 and Si53325. Blank for Si53326.
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 4 Marking	Circle = 0.50 mm Diameter Lower-Left Justified	Pin 1 Identifier
	YY = Year WW = Work Week	Corresponds to the year and work week of the mold date.

8.3 Si53322/23 Top Markings

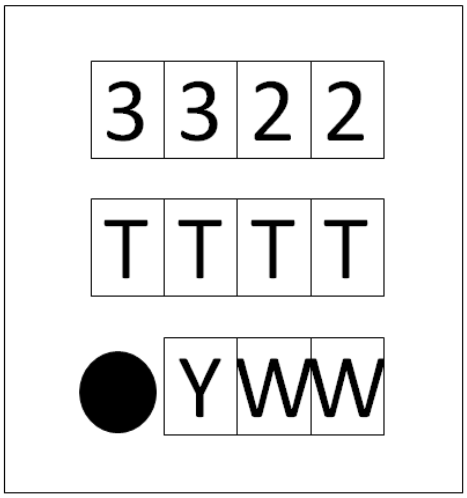


Figure 8.5. Si53322 Top Marking

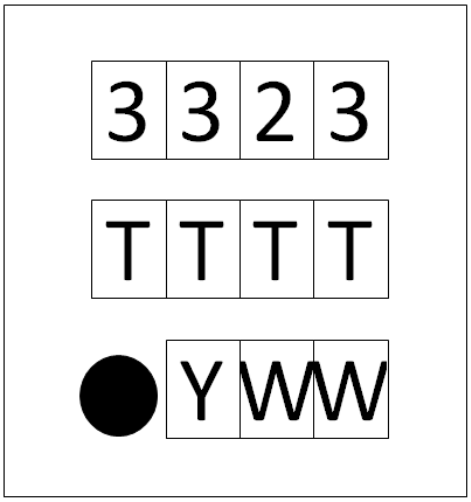


Figure 8.6. Si53323 Top Marking

Table 8.3. Si53322/23 Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.635 mm (25 mils) Right-Justified	
Line 1 Marking:	Product ID	3322 for Si53322 3323 for Si53323
Line 2 Marking:	TTTT = Mfg Code	Manufacturing Code
Line 3 Marking	Circle = 0.5 mm Diameter Bottom-Left Justified	Pin 1 Identifier
	YWW = Date Code	Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date.

8.4 Si53327/28 Top Markings

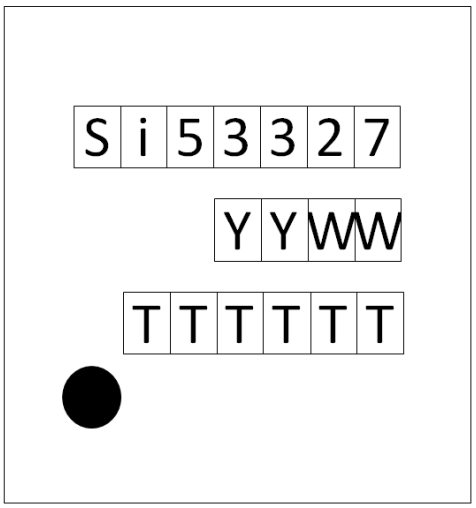


Figure 8.7. Si53327 Top Marking

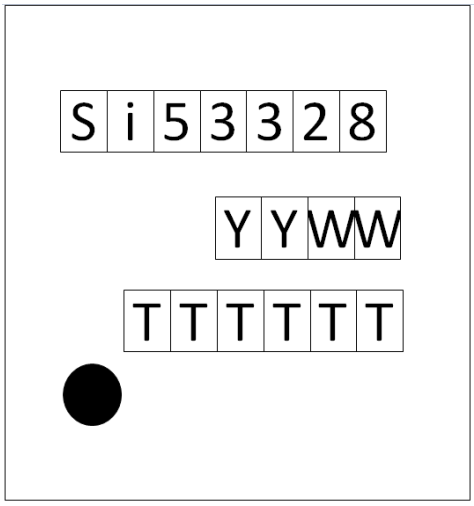


Figure 8.8. Si53328 Top Marking

Table 8.4. Si53327/28 Top Marking Explanation

Mark Method:	Laser	
Font Size:	2.0 Point (28 mils) Center-Justified	
Line 1 Marking:	Device Part Number	53327 for Si53327 53328 for Si53328
Line 2 Marking:	Device Revision/Type	B-GM
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 4 Marking:	Circle = 0.5 mm Diameter Lower-Left Justified	Pin 1 Identifier
	YY = year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

Table of Contents

1. Ordering Guide . . . 1

2. Functional Description . . . 2

2.1 Universal, Any-Format Input Termination (Si53320/21/22/23/25/27) . . . 2

2.2 LVCMOS Input Termination (Si53326/28 Only) . . . 5

2.3 Input Bias Resistors . . . 6

2.4 Input Mux . . . 6

2.5 Output Clock Termination Options . . . 7

2.6 AC Timing Waveforms . . . 9

2.7 Typical Phase Noise Performance: Differential Input Clock . . . 10

2.8 Typical Phase Noise Performance: Single-Ended Input Clock . . . 12

2.9 Input Mux Noise Isolation . . . 13

2.10 Power Supply Noise Rejection . . . 14

3. Electrical Specifications . . . 15

4. Detailed Block Diagrams . . . 19

5. Pin Descriptions . . . 23

5.1 Si53320 Pin Descriptions . . . 23

5.2 Si53321 and Si53326 Pin Descriptions . . . 25

5.3 Si53322 Pin Descriptions . . . 28

5.4 Si53323 Pin Descriptions . . . 29

5.5 Si53325 Pin Descriptions . . . 30

5.6 Si53327 and Si53328 Pin Descriptions . . . 32

6. Package Outlines . . . 34

6.1 16-Pin QFN Package . . . 34

6.2 20-Pin TSSOP Package . . . 35

6.3 24-Pin QFN Package . . . 36

6.4 32-Pin QFN Package . . . 37

6.5 32-Pin eLQFP Package . . . 38

7. Land Patterns . . . 39

7.1 16-Pin QFN Land Pattern . . . 39

7.2 20-Pin TSSOP Land Pattern . . . 40

7.3 24-Pin QFN Land Pattern . . . 41

7.4 32-Pin QFN Land Pattern . . . 42

7.5 32-Pin eLQFP Land Pattern . . . 43

8. Top Markings . . . 44

8.1 Si53320 Top Marking 44
8.2 Si53321/25/26 Top Markings 45
8.3 Si53322/23 Top Markings 46
8.4 Si53327/28 Top Markings 47
Table of Contents 48

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