Not Recommended For New Designs

24-BIT 192-kHz SAMPLING 8-CHANNEL ENHANCED MULTILEVEL DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **24-Bit Resolution**
- **Analog Performance**
  - **Dynamic Range: 105 dB Typical**
  - **SNR: 105 dB Typical**
  - **THD+N: 0.002% Typical**
  - **Full-Scale Output: 3.1 Vp-p, Typical**
- **4×/8× Oversampling Interpolation Filter**
  - **Stop-Band Attenuation: –55 dB**
  - **Pass-Band Ripple: ±0.03 dB**
- **Sampling Frequency: 5 kHz to 200 kHz**
- **Accepts 16-, 18-, 20-, and 24-Bit Audio Data**
- **Data Formats: Standard, I^2S, and Left-Justified**
- **System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S**
- **User-Programmable Functions**
  - **Digital Attenuation: 0 dB to –63 dB, 0.5 dB/Step**
  - **Soft Mute**
  - **Zero Flags Can Be Used as General-Purpose Logic Output**
  - **Digital De-Emphasis**
  - **Digital Filter Rolloff: Sharp or Slow**
- **Dual-Supply Operation**
  - **5-V Analog**
  - **3.3-V Digital**
- **5-V Tolerant Digital Logic Inputs**
- **Package: LQFP-48**

APPLICATIONS

- **Integrated A/V Receivers**
- **DVD Movie and Audio Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **DVD Add-On Cards for High-End PCs**
- **Digital Audio Workstations**
- **Other Multichannel Audio Systems**

DESCRIPTION

The PCM1609A is a CMOS, monolithic integrated circuit that features eight 24-bit audio digital-to-analog converters (DACs) and support circuitry in a small LQFP-48 package. The DACs use Texas Instruments (TI) enhanced multilevel delta-sigma architecture that employs fourth-order noise shaping and 8-level amplitude quantization to achieve excellent signal-to-noise performance and a high tolerance to clock jitter.

The PCM1609A accepts industry-standard audio data formats with 16- to 24-bit audio data. Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through a 4-wire serial control port that supports register write and read functions.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Power-supply voltage range	–0.3 V to 4 V
V_{CC}		–0.3 V to 6.5 V
V_{CC}, V_{DD}	Supply voltage difference	$V_{CC} – V_{DD} < 3$ V
	Ground voltage differences	±0.1 V
	Digital input voltage range	–0.3 V to 6.5 V
	Input current (except power supply pins)	±10 mA
	Operating temperature range under bias	–40°C to 125°C
	Storage temperature range	–55°C to 150°C
	Junction temperature	150°C
	Lead temperature (soldering)	260°C, 5 s
	Package temperature (reflow, peak)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Digital supply voltage, V_{DD}		3	3.3	3.6	V
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		36.864	MHz
	Sampling clock	32		192	kHz
Analog output load resistance		5			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	°C

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ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, system clock = 384 f_S (f_S = 44.1 kHz), and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				24		Bits
DATA FORMAT						
	Audio data interface formats			Standard, I^2S, left-justified		
	Audio data bit length			16/18/20/24 bit, selectable		
	Audio data format			MSB first, binary 2s complement		
f_S	Sampling frequency		5		200	kHz
	System clock frequency			128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2			Vdc
V_{IL}					0.8	
I_{IH} (1)	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL} (1)		V_{IN} = 0 V			–10	
I_{IH} (2)		$V_{IN} = V_{DD}$		65	100	
I_{IL} (2)		V_{IN} = 0 V			–10	
V_{OH}	Output logic level	I_{OH} = –4 mA	2.4			Vdc
V_{OL}		I_{OL} = 4 mA			1	
DYNAMIC PERFORMANCE (3)(4)						
THD+N	Total harmonic distortion + noise	V_{OUT} = 0 dB, f_S = 44.1 kHz		0.002%	0.008%	
		V_{OUT} = 0 dB, f_S = 96 kHz		0.004%		
		V_{OUT} = 0 dB, f_S = 192 kHz		0.005%		
		V_{OUT} = –60 dB, f_S = 44.1 kHz		0.7%		
		V_{OUT} = –60 dB, f_S = 96 kHz		0.9%		
		V_{OUT} = –60 dB, f_S = 192 kHz		1%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	98	105		dB
		A-weighted, f_S = 96 kHz		103		
		A-weighted, f_S = 192 kHz		102		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	98	105		dB
		A-weighted, f_S = 96 kHz		103		
		A-weighted, f_S = 192 kHz		102		
	Channel separation	f_S = 44.1 kHz	94	103		dB
		f_S = 96 kHz		101		
		f_S = 192 kHz		100		
	Level linearity error	V_{OUT} = –90 dB		±0.5		dB
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Bipolar zero error	V_{OUT} = 0.5 V_{CC} at bipolar zero		±30	±60	mV

(1) Pins 31, 38, 40, 41, 45–47 (DATA4, SCKI, BCK, LRCK, DATA1, DATA2, DATA3)
(2) Pins 34–37 (MDI, MC, ML, $\overline{RST}$)
(3) Analog performance specifications are tested using a System Two™ Cascade audio measurement system by Audio Precision™ with 400-Hz HPF on, 30-kHz LPF on, average mode with 20-kHz bandwidth limiting. The load connected to the analog output is 5 kΩ or larger via capacitive loading.
(4) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S in register 12.

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, system clock = 384 f_S (f_S = 44.1 kHz), and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
Output voltage		Full scale (–0 dB)		0.62 V_{CC}		Vp-p
Center voltage				0.5 V_{CC}		Vdc
Load impedance		AC load	5			kΩ
DIGITAL FILTER PERFORMANCE						
Group delay time				20/f_S		
De-emphasis error				±0.1		dB
Filter Characteristics 1, Sharp Rolloff						
Pass band		±0.03 dB			0.454 f_S	
Pass band		–3 dB			0.487 f_S	
Stop band			0.546 f_S			
Pass-band ripple					±0.03	dB
Stop-band attenuation		Stop band = 0.546 f_S	–50			dB
Stop-band attenuation		Stop band = 0.567 f_S	–55			dB
Filter Characteristics 2, Slow Rolloff						
Pass band		±0.5 dB			0.198 f_S	
Pass band		–3 dB			0.39 f_S	
Stop band			0.884 f_S			
Pass-band ripple					±0.5	dB
Stop-band attenuation		Stop band = 0.884 f_S	–40			dB
ANALOG FILTER PERFORMANCE						
Frequency response		f = 20 kHz		–0.03		dB
		f = 44 kHz		–0.2		
POWER-SUPPLY REQUIREMENTS (5)						
V_{DD}	Voltage range		3	3.3	3.6	Vdc
V_{CC}			4.5	5	5.5	
I_{DD} (6)	Supply current	f_S = 44.1 kHz		18	25	mA
		f_S = 96 kHz		40		
		f_S = 192 kHz		40		
I_{CC}		f_S = 44.1 kHz		33	46	
		f_S = 96 kHz		36		
		f_S = 192 kHz		36		
Power dissipation		f_S = 44.1 kHz		224	313	mW
		f_S = 96 kHz		312		
		f_S = 192 kHz		312		
TEMPERATURE RANGE						
T_A	Operating temperature		–25		85	°C
θ_{JA}	Thermal resistance			100		°C/W

(5) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S in register 12.
(6) SCKO is disabled.

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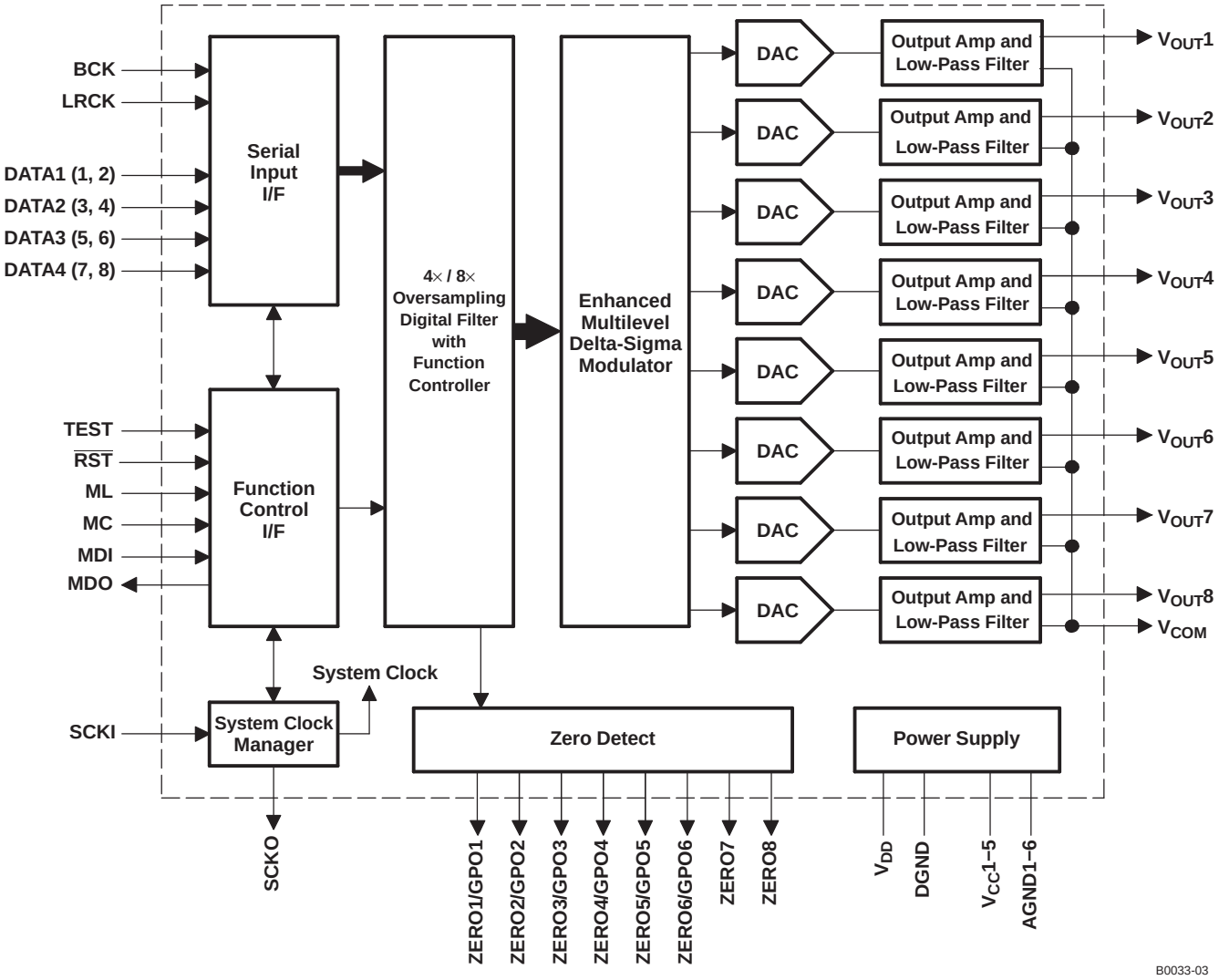
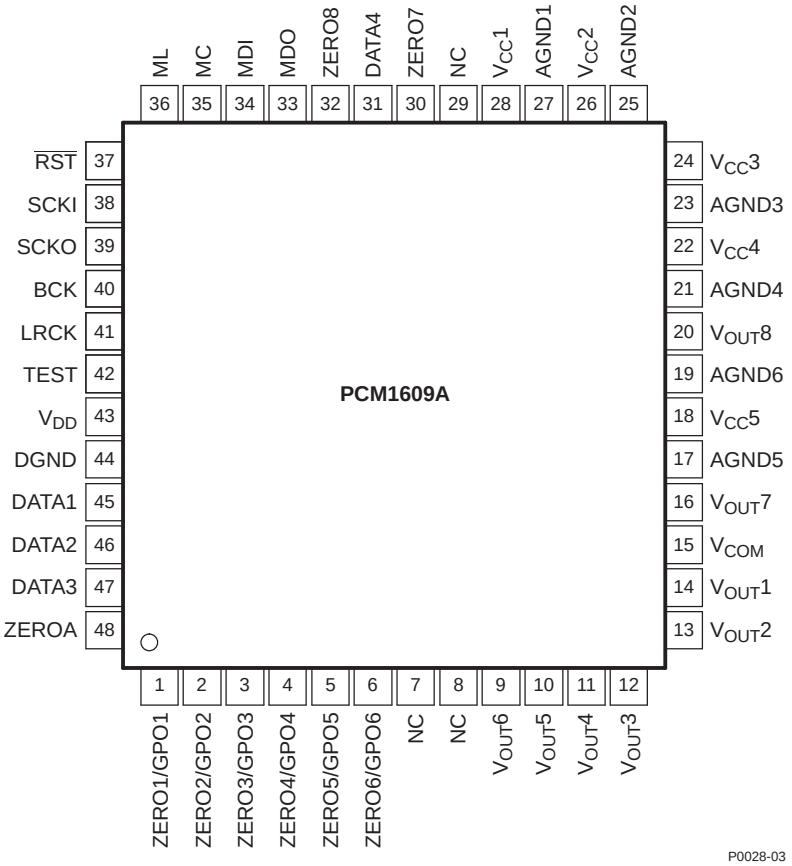
FUNCTIONAL BLOCK DIAGRAM



PT PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND1	27	–	Analog ground
AGND2	25	–	Analog ground
AGND3	23	–	Analog ground
AGND4	21	–	Analog ground
AGND5	17	–	Analog ground
AGND6	19	–	Analog ground
BCK	40	I	Shift clock input for serial audio data. Clock must be one of 32 f_S, 48 f_S, or 64 f_S. (1)
DATA1	45	I	Serial audio data for $V_{OUT}1$ and $V_{OUT}2$ (1)
DATA2	46	I	Serial audio data for $V_{OUT}3$ and $V_{OUT}4$ (1)
DATA3	47	I	Serial audio data for $V_{OUT}5$ and $V_{OUT}6$ (1)
DATA4	31	I	Serial audio data for $V_{OUT}7$ and $V_{OUT}8$ (1)
DGND	44	–	Digital ground
LRCK	41	I	Left and right clock. This clock is equal to the sampling rate, f_S. (1)
MC	35	I	Shift clock for serial control port (2)
MDI	34	I	Serial data input for serial control port (2)
MDO	33	O	Serial data output for serial control port (3)

(1) Schmitt-trigger input, 5-V tolerant
(2) Schmitt-trigger input with internal pulldown, 5-V tolerant
(3) 3-state output

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ML	36	I	Latch enable for serial control port (2)
NC	7, 8, 29	–	No connection
$\overline{RST}$	37	I	System reset, active low (2)
SCKI	38	I	System clock input. Input frequency is one of 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S. (1)
SCKO	39	O	Buffered clock output. Output frequency is one of 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S, or one-half of 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, or 768 f_S.
TEST	42	–	Test. This pin should be connected to DGND. (2)
$V_{CC}1$	28	–	Analog power supply, 5 V
$V_{CC}2$	26	–	Analog power supply, 5 V
$V_{CC}3$	24	–	Analog power supply, 5 V
$V_{CC}4$	22	–	Analog power supply, 5 V
$V_{CC}5$	18	–	Analog power supply, 5 V
V_{COM}	15	O	Common voltage. This pin should be bypassed with a 10-µF capacitor to AGND.
V_{DD}	43	–	Digital power supply, 3.3 V
$V_{OUT}1$	14	O	Voltage output of audio signal corresponding to left channel on DATA1
$V_{OUT}2$	13	O	Voltage output of audio signal corresponding to right channel on DATA1
$V_{OUT}3$	12	O	Voltage output of audio signal corresponding to left channel on DATA2
$V_{OUT}4$	11	O	Voltage output of audio signal corresponding to right channel on DATA2
$V_{OUT}5$	10	O	Voltage output of audio signal corresponding to left channel on DATA3
$V_{OUT}6$	9	O	Voltage output of audio signal corresponding to right channel on DATA3
$V_{OUT}7$	16	O	Voltage output of audio signal corresponding to left channel on DATA4
$V_{OUT}8$	20	O	Voltage output of audio signal corresponding to right channel on DATA4
ZERO1/GPO1	1	O	Zero-data flag for $V_{OUT}1$. Can also be used as GPO pin.
ZERO2/GPO2	2	O	Zero-data flag for $V_{OUT}2$. Can also be used as GPO pin.
ZERO3/GPO3	3	O	Zero-data flag for $V_{OUT}3$. Can also be used as GPO pin.
ZERO4/GPO4	4	O	Zero-data flag for $V_{OUT}4$. Can also be used as GPO pin.
ZERO5/GPO5	5	O	Zero-data flag for $V_{OUT}5$. Can also be used as GPO pin.
ZERO6/GPO6	6	O	Zero-data flag for $V_{OUT}6$. Can also be used as GPO pin.
ZERO7	30	O	Zero-data flag for $V_{OUT}7$
ZERO8	32	O	Zero-data flag for $V_{OUT}8$
ZEROA	48	O	Zero-data flag. Logical AND of ZERO1 through ZERO8.

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TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit input data (unless otherwise noted)

Digital Filter (De-Emphasis Off)

FREQUENCY RESPONSE (SHARP ROLLOFF)

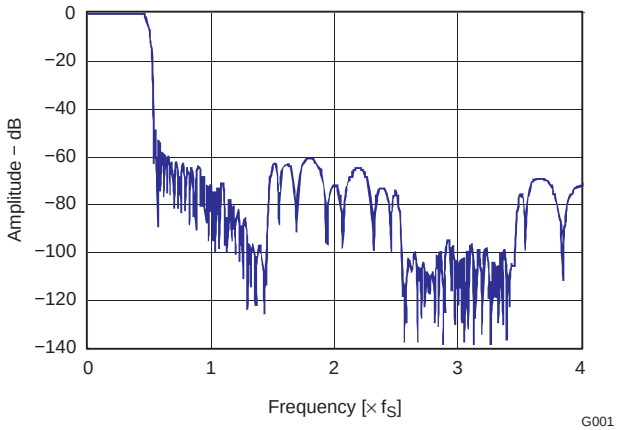

Figure 1.

PASS-BAND FREQUENCY RESPONSE (SHARP ROLLOFF)

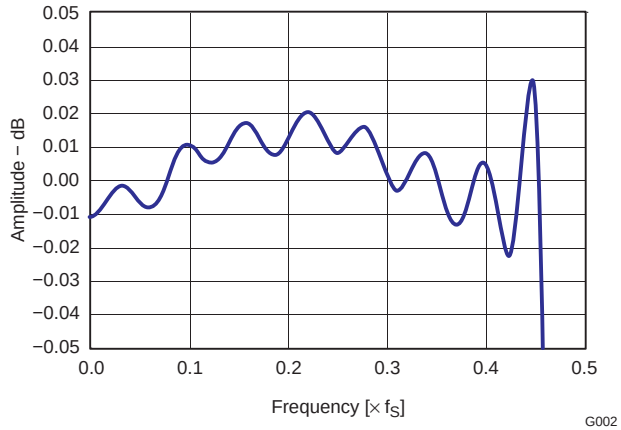

Figure 2.

FREQUENCY RESPONSE (SLOW ROLLOFF)

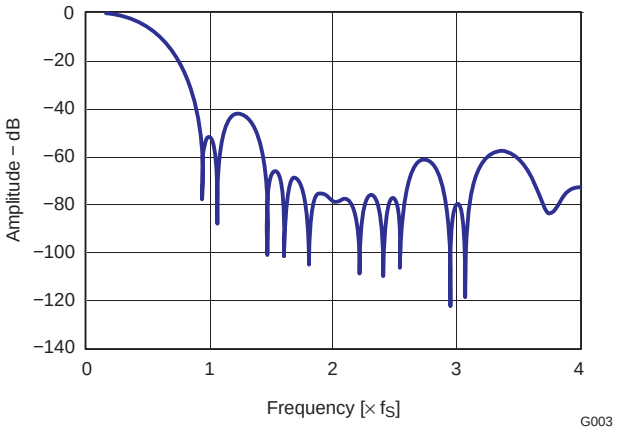

Figure 3.

TRANSITION CHARACTERISTICS (SLOW ROLLOFF)

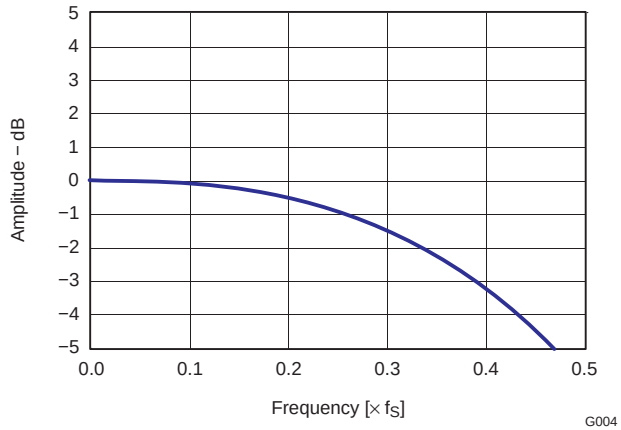

Figure 4.

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TYPICAL PERFORMANCE CURVES (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit input data (unless otherwise noted)

Digital Filter (De-Emphasis Curves)

DE-EMPHASIS (f_S = 32 kHz)

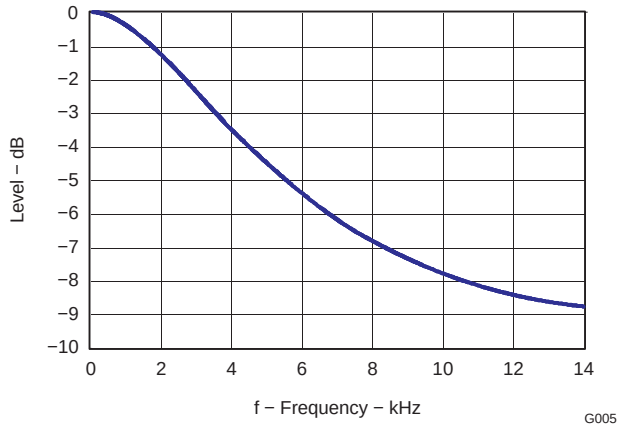

Figure 5.

DE-EMPHASIS ERROR (f_S = 32 kHz)

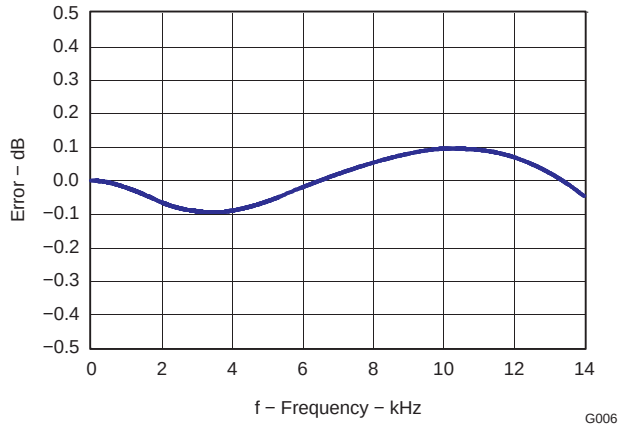

Figure 6.

DE-EMPHASIS (f_S = 44.1 kHz)

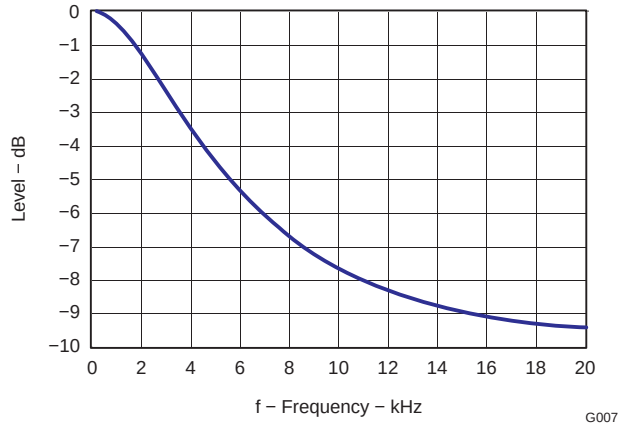

Figure 7.

DE-EMPHASIS ERROR (f_S = 44.1 kHz)

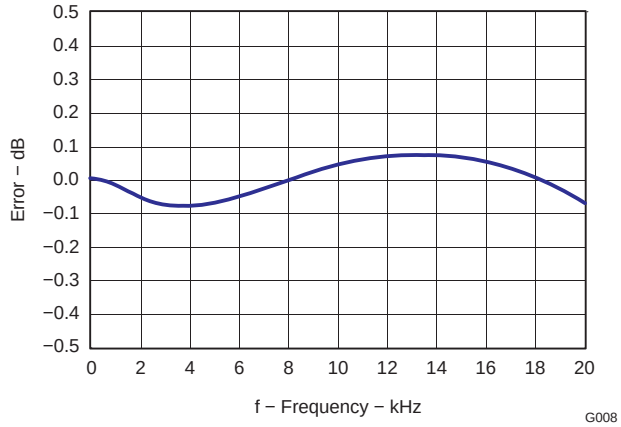

Figure 8.

DE-EMPHASIS (f_S = 48 kHz)

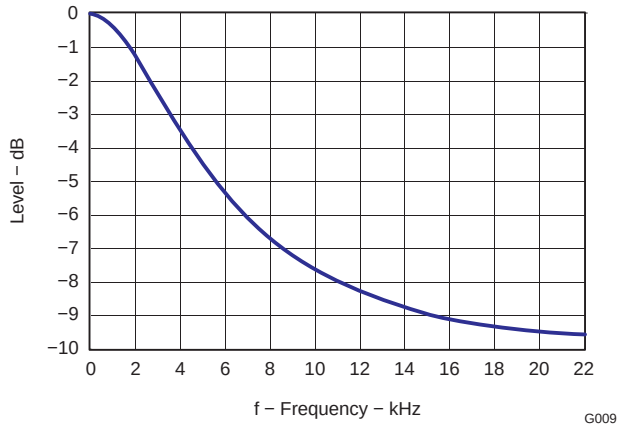

Figure 9.

DE-EMPHASIS ERROR (f_S = 48 kHz)

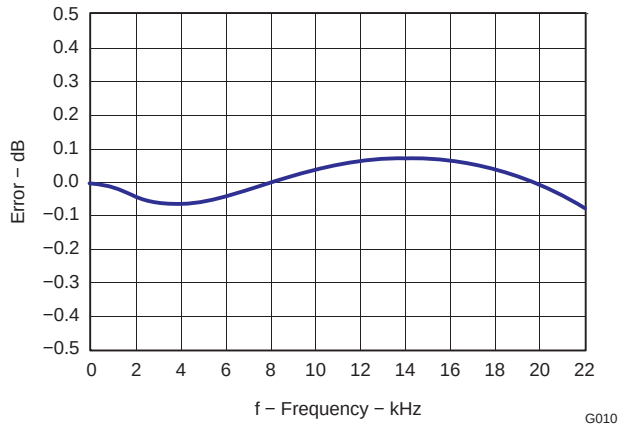

Figure 10.

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TYPICAL PERFORMANCE CURVES (continued)

ANALOG DYNAMIC PERFORMANCE

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, and 24-bit input data (unless otherwise noted). Conditions in 192-kHz operation are system clock = 128 f_S, DAC3 through DAC6 disabled in register 8, and oversampling rate = 64 f_S (set by OVER bit in register 12).

Supply Voltage Characteristics

TOTAL HARMONIC DISTORTION + NOISE vs SUPPLY VOLTAGE (V_{DD} = 3.3 V)

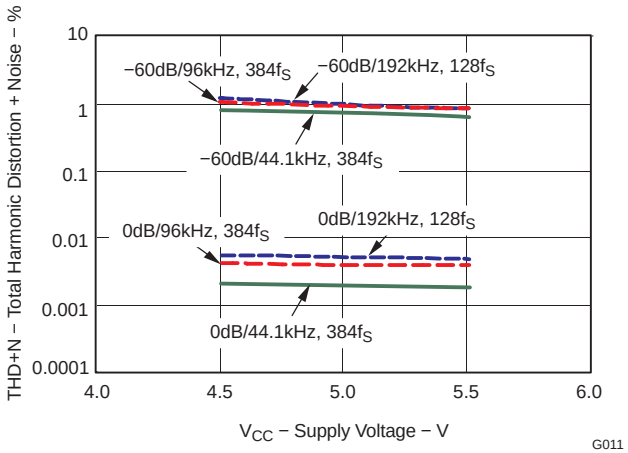

Figure 11.

DYNAMIC RANGE vs SUPPLY VOLTAGE (V_{DD} = 3.3 V)

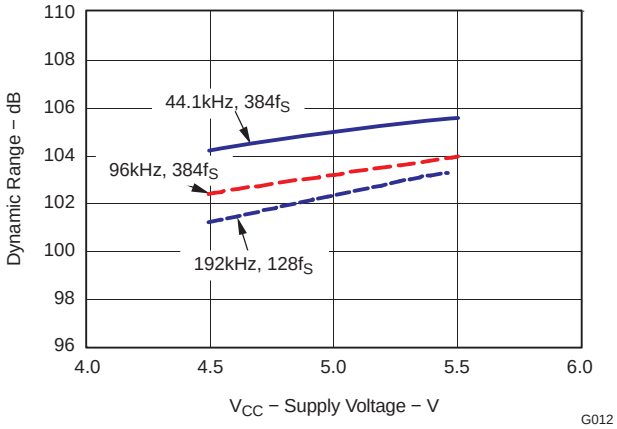

Figure 12.

SIGNAL-TO-NOISE RATIO vs SUPPLY VOLTAGE (V_{DD} = 3.3 V)

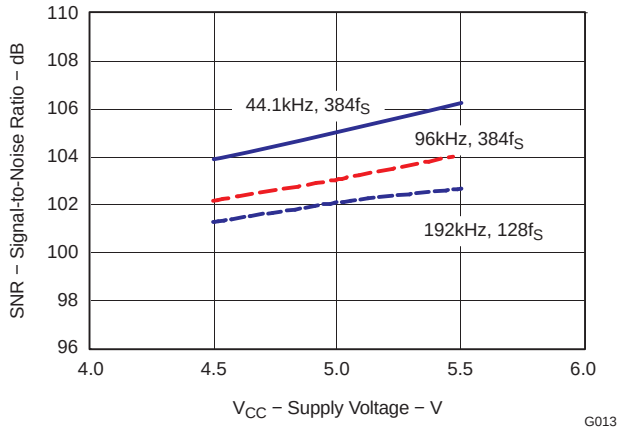

Figure 13.

CHANNEL SEPARATION vs SUPPLY VOLTAGE (V_{DD} = 3.3 V)

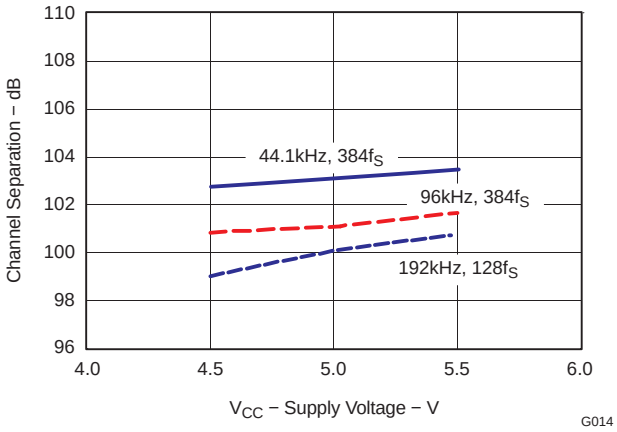

Figure 14.

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TYPICAL PERFORMANCE CURVES (continued)

ANALOG DYNAMIC PERFORMANCE (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, and 24-bit input data (unless otherwise noted). Conditions in 192-kHz operation are system clock = 128 f_S, DAC3 through DAC6 disabled in register 8, and oversampling rate = 64 f_S (set by OVER bit in register 12).

Temperature Characteristics

TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE

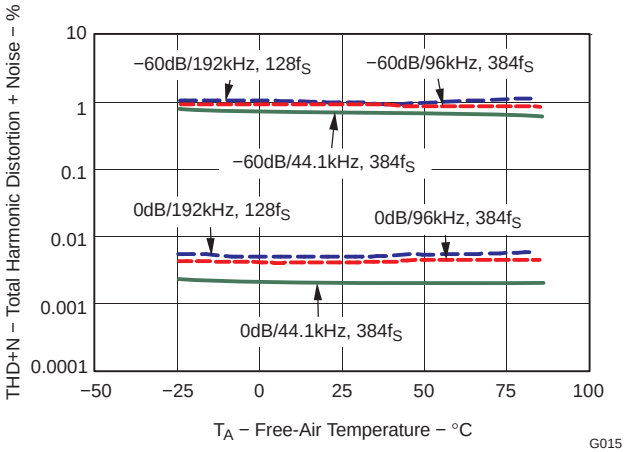


Figure 15.

DYNAMIC RANGE vs TEMPERATURE

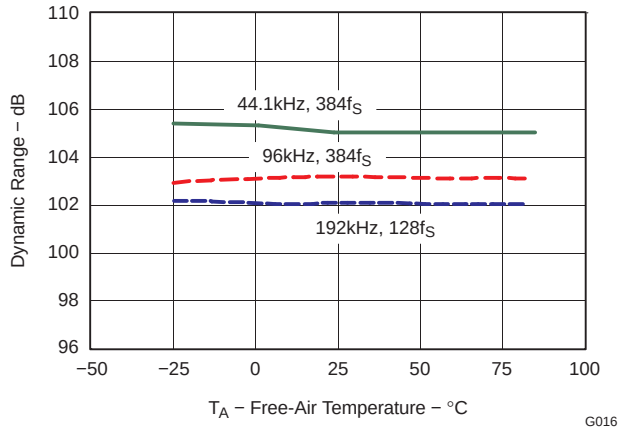


Figure 16.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

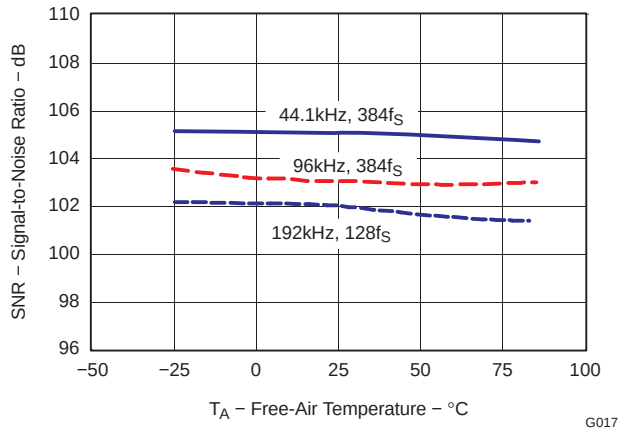


Figure 17.

CHANNEL SEPARATION vs TEMPERATURE

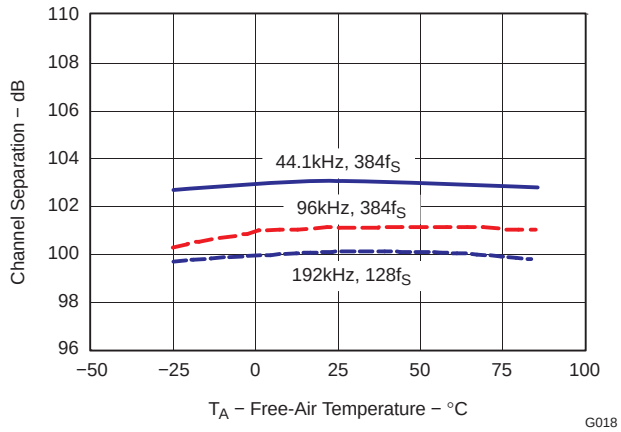


Figure 18.

SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

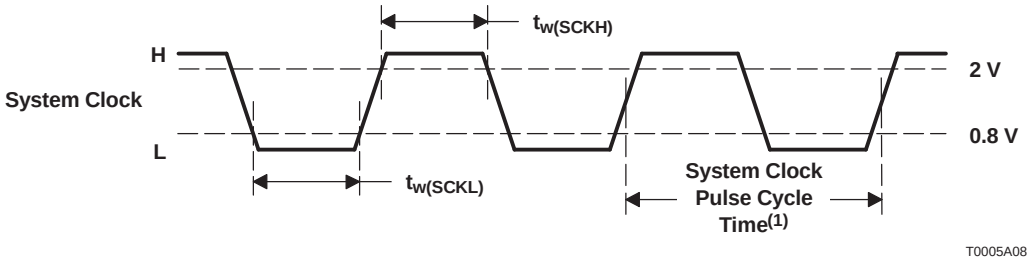
The PCM1609A requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCKI input (pin 38). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 19 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The PLL170x multiclock generator from Ti is an excellent choice for providing the PCM1609A system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
8	(1)	(1)	2.048	3.072	4.096	6.144
16	(1)	(1)	4.096	6.144	8.192	12.288
32	(1)	(1)	8.192	12.288	16.384	24.576
44.1	(1)	(1)	11.2896	16.9344	22.5792	33.8688
48	(1)	(1)	12.288	18.432	24.576	36.864
96	(1)	(1)	24.576	36.864	49.152	(1)
192	24.576	36.864	(1)	(1)	(1)	(1)

(1) This system clock is not supported for the given sampling frequency.



SYMBOL		MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	7		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	7		ns

(1) 1/128 f_S, 56 f_S, 1/384 f_S, 1/512 f_S, and 1/768 f_S.

Figure 19. System Clock Timing

SYSTEM CLOCK OUTPUT

A buffered version of the system clock input is available at the SCKO output (pin 39). SCKO can operate at either full (f_{SCKI}) or half ($f_{SCKI}/2$) rate. The SCKO output frequency can be programmed using the CLKD bit of register 9. The SCKO output pin can also be enabled or disabled using the CLKE bit of register 9. If the SCKO output is not required, it is recommended to disable it using the CLKE bit. The default is SCKO enabled.

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POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1609A includes a power-on reset function (see Figure 20). With the system clock active, and V_{DD} > 2 V (typical, 1.6 V to 2.4 V), the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V. After the initialization period, the PCM1609A is set to its reset default state, as described in the Mode Control Registers section of this data sheet.

The PCM1609A also includes an external reset capability using the $\overline{RST}$ input (pin 37). This allows an external controller or master reset circuit to force the PCM1609A to initialize to its reset default state. For normal operation, $\overline{RST}$ should be set to a logic 1.

The external reset operation and timing is shown in Figure 21. The $\overline{RST}$ pin is set to logic-0 for a minimum of 20 ns. After the initialization sequence is completed, the PCM1609A is set to its reset default state, as described in the Mode Control Registers section of this data sheet.

During the reset period (1024 system clocks), the analog outputs are forced to the bipolar zero level (or $V_{CC}/2$). After the reset period, the internal registers are initialized in the next $1/f_S$ period and, if SCKI, BCK, and LRCK are provided continuously, the PCM1609A provides proper analog output with the group delay time given in the Electrical Characteristics section of this data sheet.

The external reset is especially useful in applications where there is a delay between PCM1609A power up and system-clock activation. In this case, the $\overline{RST}$ pin should be held at a logic-0 level until the system clock has been activated.

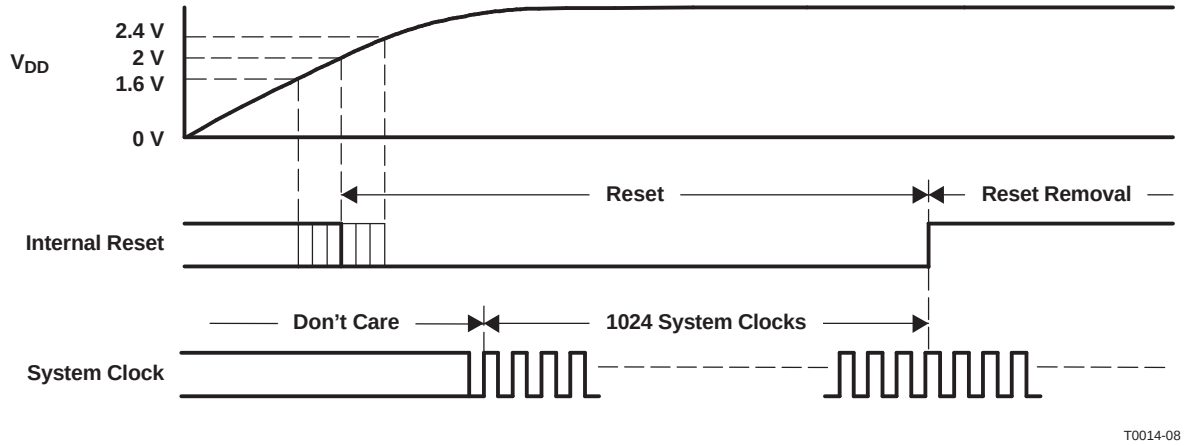

Figure 20. Power-On Reset Timing

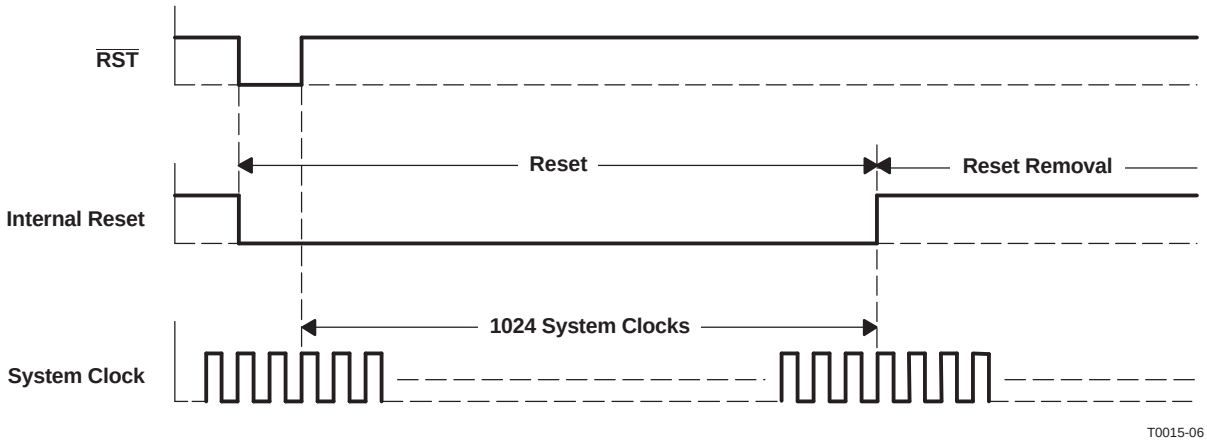

Figure 21. External Reset Timing

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1609A consists of a 5-wire synchronous serial port. It includes LRCK (pin 41), BCK (pin 40), DATA1 (pin 45), DATA2 (pin 46), DATA3 (pin 47), and DATA4 (pin 31). BCK is the serial audio bit clock, and is used to clock the serial data present on DATA1, DATA2, DATA3, and DATA4 into the audio interface serial shift register. Serial data is clocked into the PCM1609A on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface internal registers.

Both LRCK and BCK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCKI. LRCK is operated at the sampling frequency (f_S). BCK can be operated at 32, 48, or 64 times the sampling frequency (I^2S format does not support BCK = 32 f_S).

Internal operation of the PCM1609A is synchronized with LRCK. Accordingly, internal operation of the device is suspended when the sampling rate clock (LRCK) is changed, or when SCKI and/or BCK is interrupted at least for a 3-bit clock cycle. If SCKI, BCK, and LRCK are provided continuously after this suspended state, the internal operation is resynchronized automatically within a period of less than $3/f_S$. During this resynchronization period and for a $3/f_S$ time thereafter, the analog outputs are forced to the bipolar zero level, $V_{CC}/2$. External resetting is not required.

AUDIO DATA FORMATS AND TIMING

The PCM1609A supports industry-standard audio data formats, including standard, I^2S, and left-justified (see Figure 22). Data formats are selected using the format bits, FMT[2:0], in register 9. The default data format is 24-bit standard. All formats require binary 2s complement, MSB-first audio data. See Figure 23 for a detailed timing diagram of the serial audio interface.

DATA1, DATA2, DATA3, and DATA4 each carry two audio channels, designated as the left and right channels. The left-channel data always precedes the right-channel data in the serial data stream for all data formats. Table 2 shows the mapping of the digital input data to the analog output pins.

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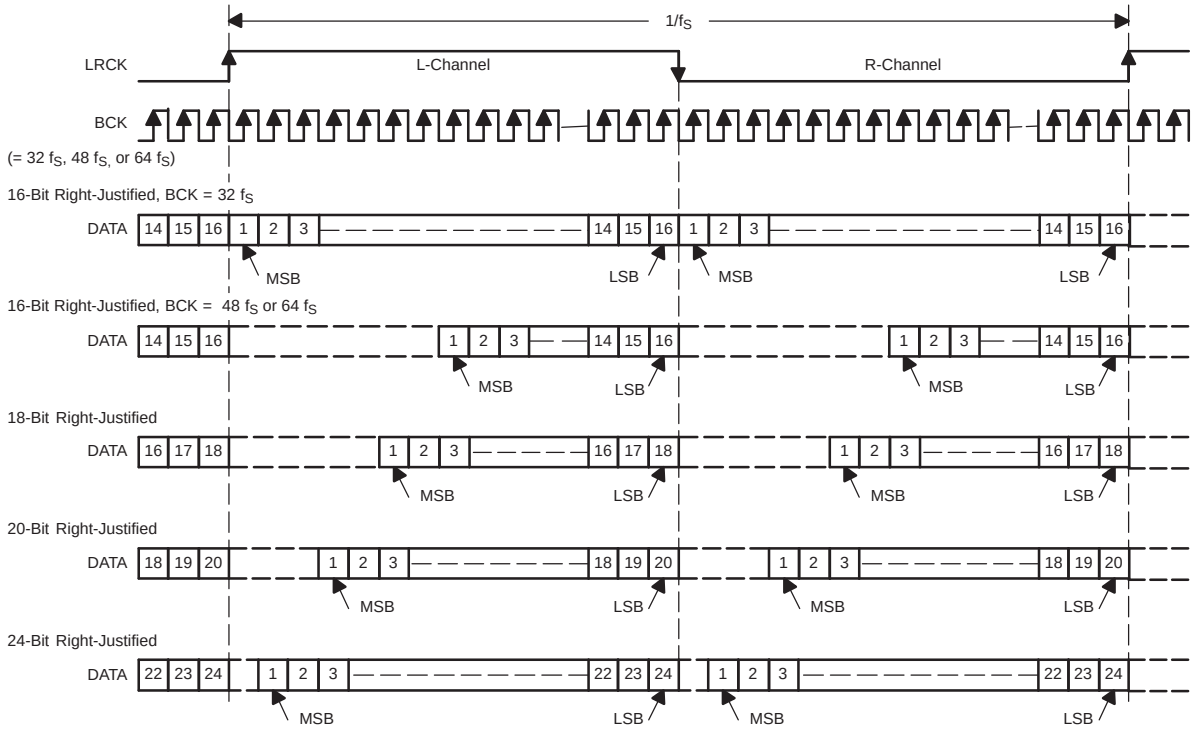
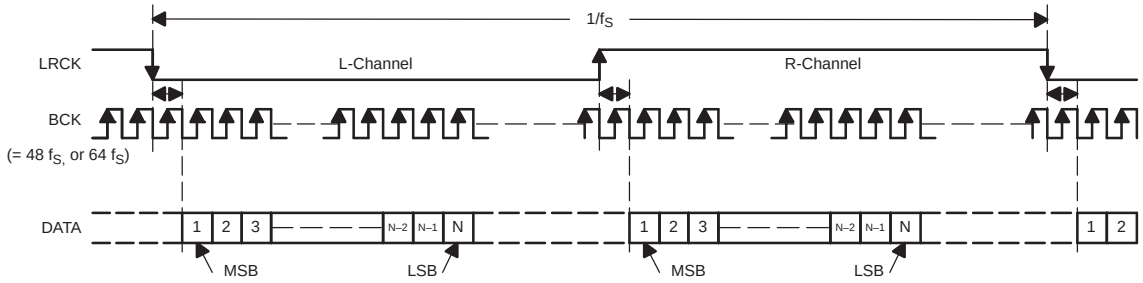
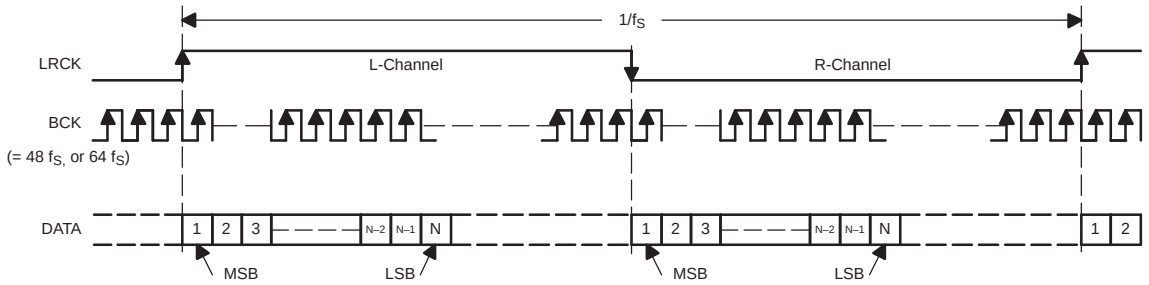
(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH

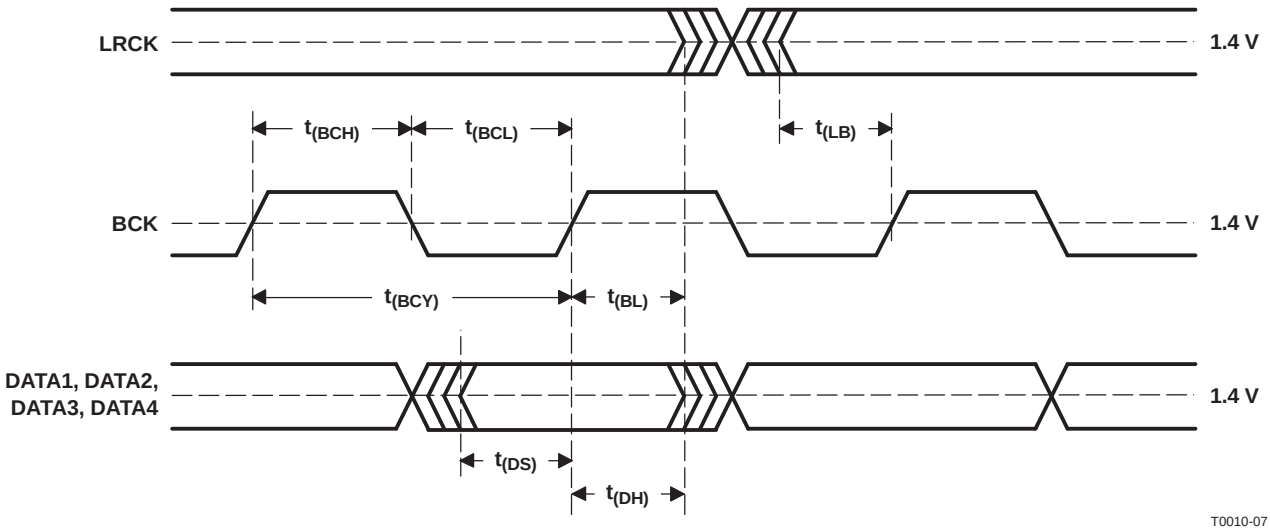


(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



T0009-05

Figure 22. Audio Data Input Formats



SYMBOL		MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	1/(64 f_S)(1)		
$t_{(BCH)}$	BCK high-level time	35		ns
$t_{(BCL)}$	BCK low-level time	35		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK falling edge to BCK rising edge	10		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns

(1) f_S is the sampling frequency (e.g., 44.1 kHz, 48 kHz, 96 kHz, etc.)

Figure 23. Audio Interface Timing

Table 2. Audio Input Data to Analog Output Mapping

DATA INPUT	CHANNEL	ANALOG OUTPUT
DATA1	Left	$V_{OUT}1$
DATA1	Right	$V_{OUT}2$
DATA2	Left	$V_{OUT}3$
DATA2	Right	$V_{OUT}4$
DATA3	Left	$V_{OUT}5$
DATA3	Right	$V_{OUT}6$
DATA4	Left	$V_{OUT}7$
DATA4	Right	$V_{OUT}8$

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SERIAL CONTROL INTERFACE

The serial control interface is a 4-wire synchronous serial port that operates asynchronously to the serial audio interface. The serial control interface is used to program and read the on-chip mode registers. The control interface includes MDO (pin 33), MDI (pin 34), MC (pin 35), and ML (pin 36). MDO is the serial data output used to read back the values of the mode registers. MDI is the serial data input used to program the mode registers. MC is the serial bit clock used to shift data in and out of the control port. ML is the control port latch clock.

REGISTER WRITE OPERATION

All write operations for the serial control port use 16-bit data words. Figure 24 shows the control data word format. The most significant bit (MSB) is the read/write (R/$\overline{W}$) bit. When set to 0, this bit indicates a write operation. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 25 shows the functional timing diagram for writing to the serial control port. ML is held at a logic-1 state until a register is to be written. To start the register write cycle, ML is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI. After the sixteenth clock cycle has completed, ML is set to logic 1 to latch the data into the indexed mode control register.

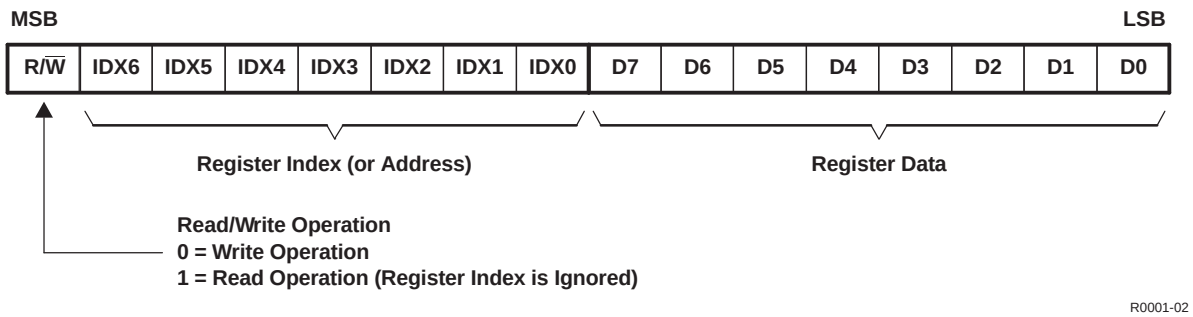

Figure 24. Control Data Word Format for MDI

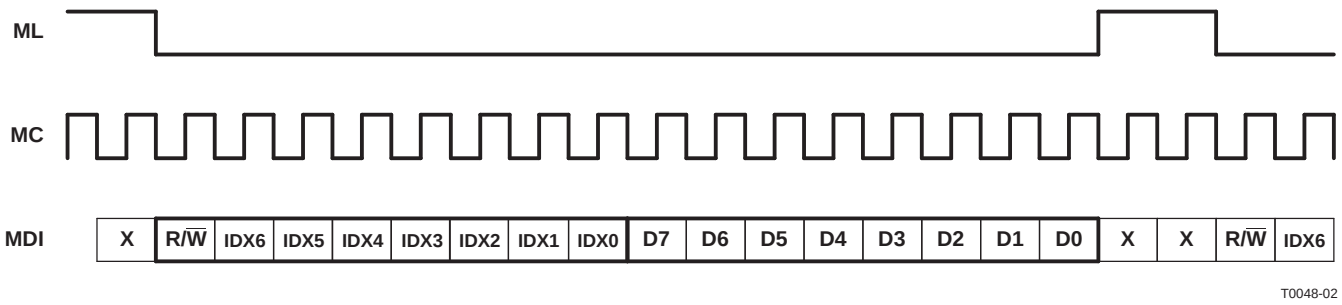

Figure 25. Write Operation Timing

SINGLE REGISTER READ OPERATION

Read operations use the 16-bit control word format shown in Figure 24. For read operations, the R/$\overline{W}$ bit is set to 1. Read operations ignore the index bits, IDX[6:0], of the control data word. Instead, the REG[6:0] bits in control register 11 are used to set the index of the register that is to be read during the read operation. Bits IDX[6:0] should be set to 00h for read operations.

The details of the read operation are shown in Figure 26. First, control register 11 must be written with the index of the register to be read back. Additionally, the INC bit must be set to logic 0 in order to disable the auto-increment read function. The read cycle is then initiated by setting ML to logic 0 and setting the R/$\overline{W}$ bit of the control data word to logic 1, indicating a read operation. MDO remains in a high-impedance state until the last eight bits of the 16-bit read cycle, which correspond to the eight data bits of the register indexed by the REG[6:0] bits of control register 11. The read cycle is completed when ML is set to 1, immediately after the MC clock cycle for the least significant bit (LSB) of the indexed control register has completed.

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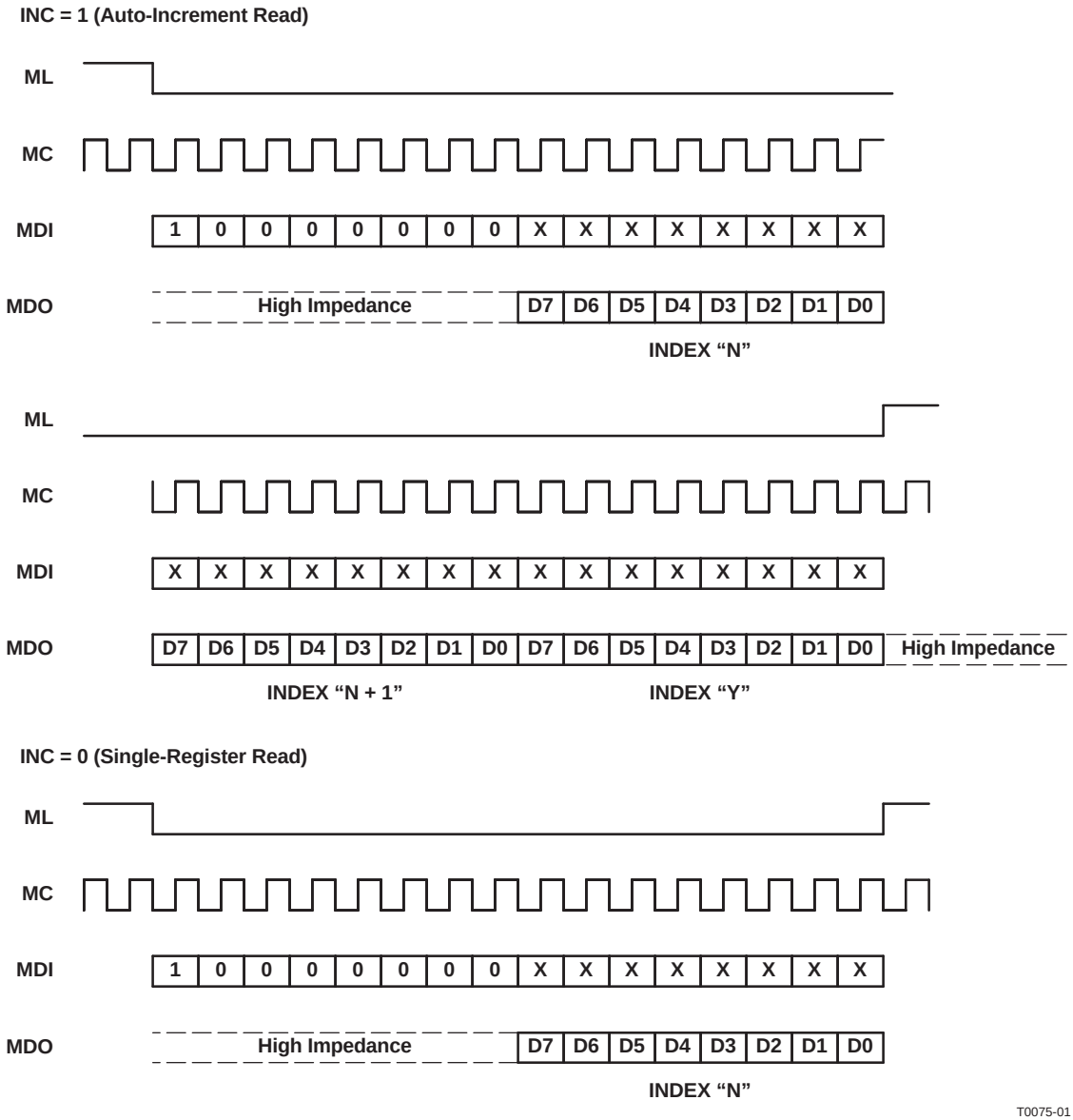

NOTES: X = Don't care

Y = Last register to be read

In single-register read (INC = 0), the index that indicates the register to be read in read operation can be set by REG[6:0] in register 11. For example, setting REG[6:0] = 000 1001b means reading from register 9.

In auto-increment read (INC = 1), the index REG[6:0] indicates the first register to be read. For example, setting REG[6:0] = 000 1001b means reading registers from 9 to Y. Y is determined by the low-to-high transition of ML in serial mode control.

Figure 26. Read Operation Timing

AUTO-INCREMENT READ OPERATION

The auto-increment read function allows for multiple registers to be read sequentially. The auto-increment read function is enabled by setting the INC bit of control register 11 to 1. The sequence always starts with the register indexed by the REG[6:0] bits in control register 11, and ends by the ML setting to 1 after MC clock cycle for the LSB of the last register.

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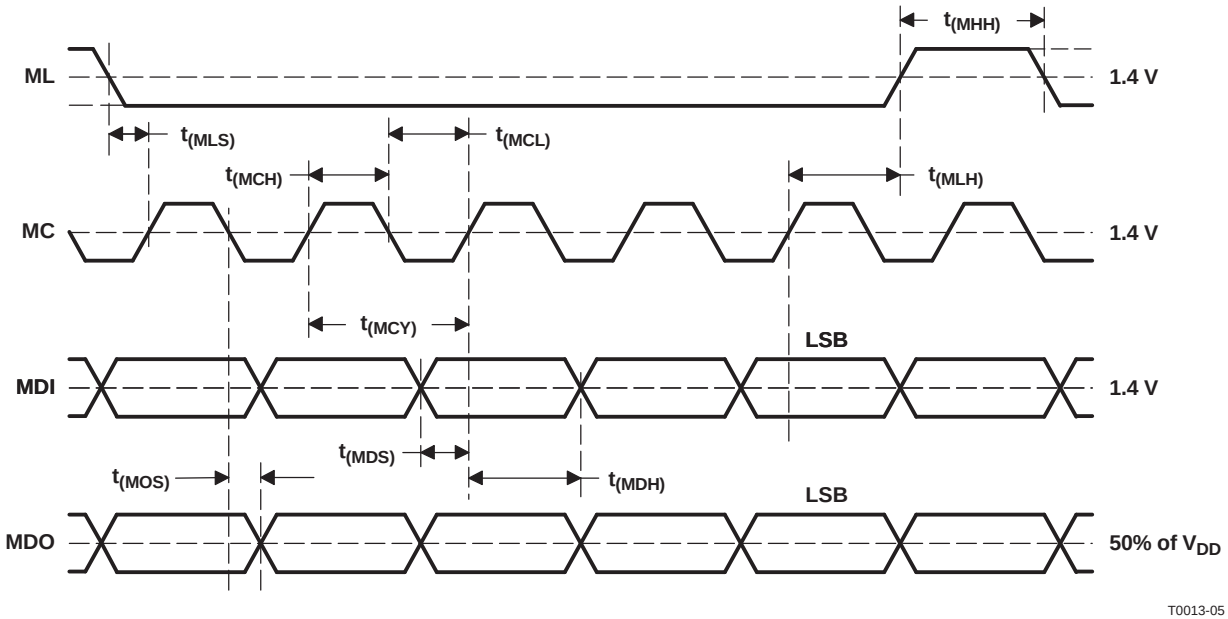
Figure 26 shows the timing of the auto-increment read operation. The operation begins by writing control register 11, setting INC to 1, and setting REG[6:0] to the first register to be read in the sequence. The actual read operation starts on the next HIGH-to-LOW transition of the ML pin.

The read cycle starts by setting the R/$\overline{W}$ bit of the control word to 1, and setting all of the IDX[6:0] bits to 0. All subsequent bits input on MDI are ignored while ML is set to 0. For the first eight clocks of the read cycle, MDO is set to the high-impedance state. This is followed by a sequence of 8-bit words, each corresponding to the data contained in control registers N through Y, where N is defined by the REG[6:0] bits in control register 11, and where Y is the last register to be read. The read cycle is completed when ML is set to 1, immediately after the MC clock cycle for the LSB of the last register has completed. If ML is held low and the MC clock continues beyond the last physical register (register 19), the read operation returns to control register 1 and subsequent control registers, continuing until ML is set to 1.

CONTROL INTERFACE TIMING REQUIREMENTS

Figure 27 shows a detailed timing diagram for the serial control interface. Pay special attention to the setup and hold times, as well as $t_{(MLS)}$ and $t_{(MLH)}$, which define minimum delays between the edges of the ML and MC clocks. These timing parameters are critical for proper control-port operation.



SYMBOL		MIN	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	100		ns
$t_{(MCL)}$	MC low-level time	50		ns
$t_{(MCH)}$	MC high-level time	50		ns
$t_{(MHH)}$	ML high-level time	300		ns
$t_{(MLS)}$	ML falling edge to MC rising edge	20		ns
$t_{(MLH)}$	ML hold time (1)	20		ns
$t_{(MDH)}$	MDI hold time	15		ns
$t_{(MDS)}$	MDL setup time	20		ns
$t_{(MOS)}$	MC falling edge to MDO stable		30	ns

(1) MC rising edge for LSB to ML rising edge

Figure 27. Control Interface Timing

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1609A includes a number of user-programmable functions that are accessed via control registers. The registers are programmed using the serial control interface that is previously discussed in this data sheet. Table 3 lists the available mode control functions, along with their reset default conditions and associated register index.

Table 3. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	CONTROL REGISTER	BIT(S) LABEL
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	1 through 6, 16, 17	AT1[7:0], AT2[7:0], AT3[7:0], AT4[7:0], AT5[7:0], AT6[7:0], AT7[7:0], AT8[7:0]
Soft mute control	Mute disabled	7, 18	MUT[8:1]
DAC1–DAC8 operation control	DAC1–DAC8 enabled	8, 19	DAC[8:1]
Audio data format control	24-bit standard format	9	FMT[2:0]
Digital filter rolloff control	Sharp rolloff	9	FLT
SCKO frequency selection	Full rate (= f_{SCKI})	9	CLKD
SCKO output enable	SCKO enabled	9	CLKE
De-emphasis all-channel function control	De-emphasis, all channels disabled	10	DMC
De-emphasis all-channel sample rate selection	44.1 kHz	10	DMF[1:0]
Output phase select	Normal phase	10	DREV
Zero-flag polarity select	High	10	ZREV
Read-register index control	REG[6:0] = 01h	11	REG[6:0]
Read auto-increment control	Auto-increment disabled	11	INC
General-purpose output enable	Zero-flag enabled	12	GPOE
General-purpose output bits (GPO1–GPO6)	Disabled	12	GPO[6:1]
Oversampling rate control	64×	12	OVER

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Reserved Registers

Registers 00h and 0Dh through 0Fh are reserved for factory use. To ensure proper operation, the user should not write to or read from these registers.

Register Map

The mode control register map is shown in Table 4. Each register includes an R/$\overline{W}$ bit that determines whether a register read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation is performed. Each register also includes an index (or address) indicated by the IDX[6:0] bits.

Table 4. Mode Control Register Map

IDX (B14 – B8)	REG	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
01h	1	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
02h	2	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
03h	3	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
04h	4	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
05h	5	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
06h	6	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
07h	7	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
08h	8	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
09h	9	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	FLT	CLKD	CLKE	FMT2	FMT1	FMT0
0Ah	10	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	ZREV	DREV	DMF1	DMF0	DMC	DMC	DMC
0Bh	11	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0
0Ch	12	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	GPOE	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1
10h	16	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT77	AT76	AT75	AT74	AT73	AT72	AT71	AT70
11h	17	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT87	AT86	AT85	AT84	AT83	AT82	AT81	AT80
12h	18	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	MUT8	MUT7
13h	19	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	DAC8	DAC7

(1) Reserved for test operation. It should be set to 0 during normal operation.

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REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 1	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
REGISTER 2	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
REGISTER 3	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
REGISTER 4	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
REGISTER 5	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
REGISTER 6	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
REGISTER 16	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT77	AT76	AT75	AT74	AT73	AT72	AT71	AT70
REGISTER 17	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT87	AT86	AT85	AT84	AT83	AT82	AT81	AT80

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

ATx[7:0] – Digital Attenuation Level Setting

Where x = 1 through 8, corresponding to the DAC output V_{OUT}x.

These bits are read/write.

Default value: 1111 1111b

Each DAC output, V_{OUT}1 through V_{OUT}8, includes a digital attenuator function. The attenuation level can be set from 0 dB to –63 dB in 0.5-dB steps. Changes in attenuation levels are made by incrementing or decrementing by one step (0.5 dB) for every $8/f_S$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation, or mute.

The attenuation level is calculated using the following formula:

$$\text{Attenuation level (dB)} = 0.5\ (\text{ATx}[7:0]_{DEC} - 255)$$

Where $\text{ATx}[7:0]_{DEC}$ = 0 through 255.

For $\text{ATx}[7:0]_{DEC}$ = 0 through 128, the attenuator is set to infinite attenuation.

The following table shows attenuation levels for various settings.

ATx[7:0]	DECIMAL VALUE	ATTENUATOR LEVEL SETTING
1111 1111b	255	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1 dB
:	:	:
1000 0011b	131	–62 dB
1000 0010b	130	–62.5 dB
1000 0001b	129	–63 dB
1000 0000b	128	Mute
:	:	:
0000 0000b	0	Mute

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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 7	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
REGISTER 18	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	MUT8	MUT7

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

MUTx – Soft Mute Control

Where x = 1 through 8, corresponding to the DAC output V_{OUT}x.

These bits are read/write.

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 through MUT8, are used to enable or disable the soft mute function for the corresponding DAC outputs, V_{OUT}1 through V_{OUT}8. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to the infinite attenuation setting, one attenuator step (0.5 dB) at a time. This provides a quiet, pop-free muting of the DAC output. On returning from soft mute, by setting MUTx = 0, the attenuator is increased one step at a time to the previously programmed attenuation level.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 8	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
REGISTER 19	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	DAC8	DAC7

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

DACx – DAC Operation Control

Where x = 1 through 8, corresponding to the DAC output V_{OUT}x.

These bits are read/write.

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, V_{OUT}1 through V_{OUT}8. When DACx = 0, the output amplifier input is connected to the DAC output. When DACx = 1, the output amplifier input is switched to the dc common-mode voltage (V_{COM}), equal to V_{CC}/2.

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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 9	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	CLKD	CLKE	FMT2	FMT1	FMT0

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

FLT – Digital Filter Rolloff Control

This bit is read/write.

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows users to select the digital filter rolloff that is best suited to their application. Two filter rolloff selections are available: sharp or slow. The filter responses for these selections are shown in the *Typical Performance Curves* section of this data sheet.

CLKD – SCKO Frequency Selection

This bit is read/write.

Default value: 0

CLKD = 0	Full-rate, $f_{SCKO} = f_{SCKI}$ (default)
CLKD = 1	Half-rate, $f_{SCKO} = f_{SCKI}/2$

The CLKD bit is used to determine the clock frequency at the system clock output pin, SCKO.

CLKE – SCKO Output Enable

This bit is read/write.

Default value: 0

CLKE = 0	SCKO enabled (default)
CLKE = 1	SCKO disabled

The CLKE bit is used to enable or disable the system clock output pin, SCKO. When SCKO is enabled, it outputs either a full- or half-rate clock, based on the setting of the CLKD bit. When SCKO is disabled, it is set to a LOW level.

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FMT[2:0] – Audio Interface Data Format

These bits are read/write.

Default value: 000b

FMT[2:0]	Audio Data Format Selection
000	24-bit standard format, right-justified data (default)
001	20-bit standard format, right-justified data
010	18-bit standard format, right-justified data
011	16-bit standard format, right-justified data
100	I^2S format, 16 bit to 24 bit
101	Left-justified format, 16 bit to 24 bit
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 10	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	ZREV	DREV	DMF1	DMF0	DMC	DMC	DMC

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

ZREV – Zero-Flag Polarity Select

Default value: 0

ZREV = 0	Zero-flag pins HIGH at a zero detect (default)
ZREV = 1	Zero-flag pins LOW at a zero detect

The ZREV bit allows the user to select the polarity of zero-flag pins.

DREV – Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit allows the user to select the phase of analog output signal.

DMF[1:0] – Sampling Frequency Selection for the De-Emphasis Function

These bits are read/write.

Default value: 00b

DMF[1:0]	**De-Emphasis Sample Rate Selection**
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled. The de-emphasis curves are shown in the Typical Performance Curves section of this data sheet. The preceding table shows the available sampling frequencies.

DMC – Digital De-Emphasis, All-Channel Function Control

This bit is read/write.

Default value: 0

DMC = 0	De-emphasis disabled for all channels (default)
DMC = 1	De-emphasis enabled for all channels

The DMC bits are used to enable or disable the de-emphasis function for all channels. The three DMC bits are ORed together. Setting any one DMC bit, any combination of two DMC bits, or all three DMC bits to 1 enables digital de-emphasis for all channels. Setting all three DMC bits to 0 disables digital de-emphasis for all channels.

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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 11	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

INC – Auto-Increment Read Control

This bit is read/write.

Default value: 0

INC = 0	Auto-increment read disabled (default)
INC = 1	Auto-increment read enabled

The INC bit is used to enable or disable the auto-increment read feature of the serial control interface. See the Serial Control Interface section of this data sheet for details regarding auto-increment read operation.

REG[6:0] – Read Register Index

These bits are read/write.

Default value: 01h

The REG[6:0] bits are used to set the index of the register to be read when performing the single-register read operation. In the case of an auto-increment read operation, the REG[6:0] bits indicate the index of the last register to be read in the auto-increment read sequence. For example, if registers 1 through 6 are to be read during an auto-increment read operation, the REG[6:0] bits would be set to 06h. See the Serial Control Interface section of this data sheet for details regarding the single-register and auto-increment read operations.

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	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 12	R/$\overline{W}$	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	GPOE	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1

R/$\overline{W}$ – Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

OVER – Oversampling Rate Control

This bit is read/write.

Default value: 0

System clock rate = 256 f_S, 384 f_S, 512 f_S, or 768 f_S:

OVER = 0	64× oversampling (default)
OVER = 1	128× oversampling

System clock rate = 128 f_S or 192 f_S:

OVER = 0	32× oversampling (default)
OVER = 1	64× oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma DACs. The OVER = 1 setting is recommended when the oversampling rate is 192 kHz (system clock rate is 128 f_S or 192 f_S).

GPOE – General-Purpose Output Enable

This bit is read/write.

Default value: 0

GPOE = 0	General-purpose outputs disabled (default) Pins default to zero-flag function (ZERO1 through ZERO6).
GPOE = 1	General-purpose outputs enabled Data written to GPO1 through GPO6 appears at the corresponding pins.

GPOx – General-Purpose Logic Output

Where: x = 1 through 6, corresponding pins GPO1 through GPO6.

These bits are read/write.

Default value: 0

GPOx = 0	Set GPOx to 0 (default)
GPOx = 1	Set GPOx to 1

The general-purpose output pins, GPO1 through GPO6, are enabled by setting GPOE = 1. These pins are used as general-purpose outputs for controlling user-defined logic functions. When general-purpose outputs are disabled (GPOE = 0), they default to the zero-flag function, ZERO1 through ZERO6.

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ANALOG OUTPUTS

The PCM1609A includes eight independent output channels, $V_{OUT}1$ through $V_{OUT}8$. These are unbalanced outputs, each capable of driving 3.1 Vp-p typical into a 5-kΩ ac load with V_{CC} = 5 V. The internal output amplifiers for $V_{OUT}1$ through $V_{OUT}8$ are dc biased to the common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise-shaping characteristics of the PCM1609A delta-sigma DACs. The frequency response of this filter is shown in Figure 28. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Application Information section of this data sheet.

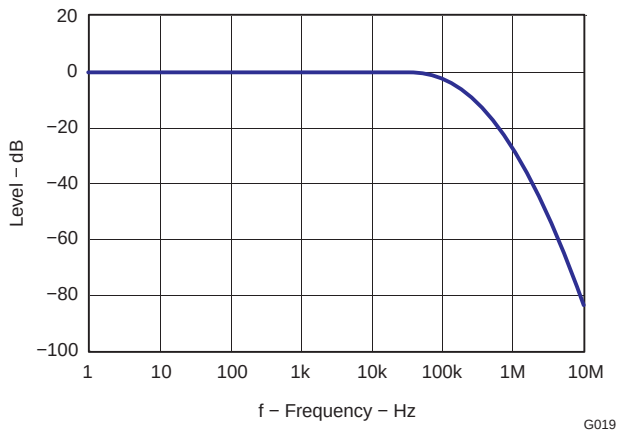

Figure 28. Output-Filter Frequency Response

V_{COM} OUTPUT

One unbuffered common-mode voltage output pin, V_{COM} (pin 15), is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to $V_{CC}/2$. If this pin is to be used to bias external circuitry, a voltage follower is required for buffering purposes. Figure 29 shows an example of using the V_{COM} pin for external biasing applications.

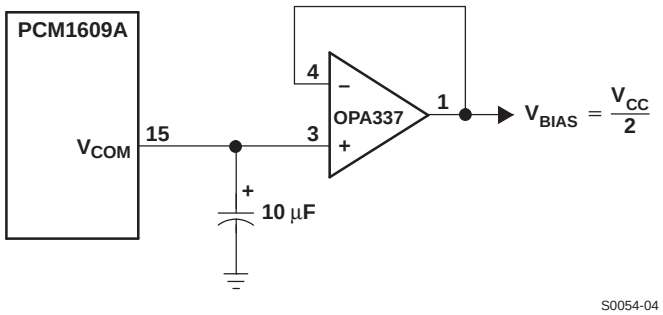

Figure 29. Biasing External Circuits Using V_{COM} Pin

ZERO FLAG

ZERO-DETECT CONDITION

Zero detection for each output channel is independent from the others. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero-detect condition exists for that channel.

ZERO OUTPUT FLAGS

Given that a zero-detect condition exists for one or more channels, the zero-flag pins for those channels are set to a logic-1 state. Each channel, ZERO1 through ZERO6 (pins 1 through 6), ZERO7 (pin 30), and ZERO8 (pin 32), has zero-flag pins. In addition, all eight zero flags are logically ANDed together, and the result is provided at the ZEROA pin (pin 48), which is set to a logic-1 state when all channels indicate a zero-detect condition. The zero-flag pins can be used to operate external mute circuits. ZERO1 through ZERO6 can be used as status indicators for a microcontroller, audio signal processor, or other digitally controlled function.

The active polarity of the zero-flag output can be inverted by setting to 1 the ZREV bit of control register 10. The reset default is active-high output, or ZREV = 0.

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APPLICATION INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram with the necessary power-supply bypassing and decoupling components is shown in Figure 30. TI recommends using the component values shown in Figure 30 for all designs.

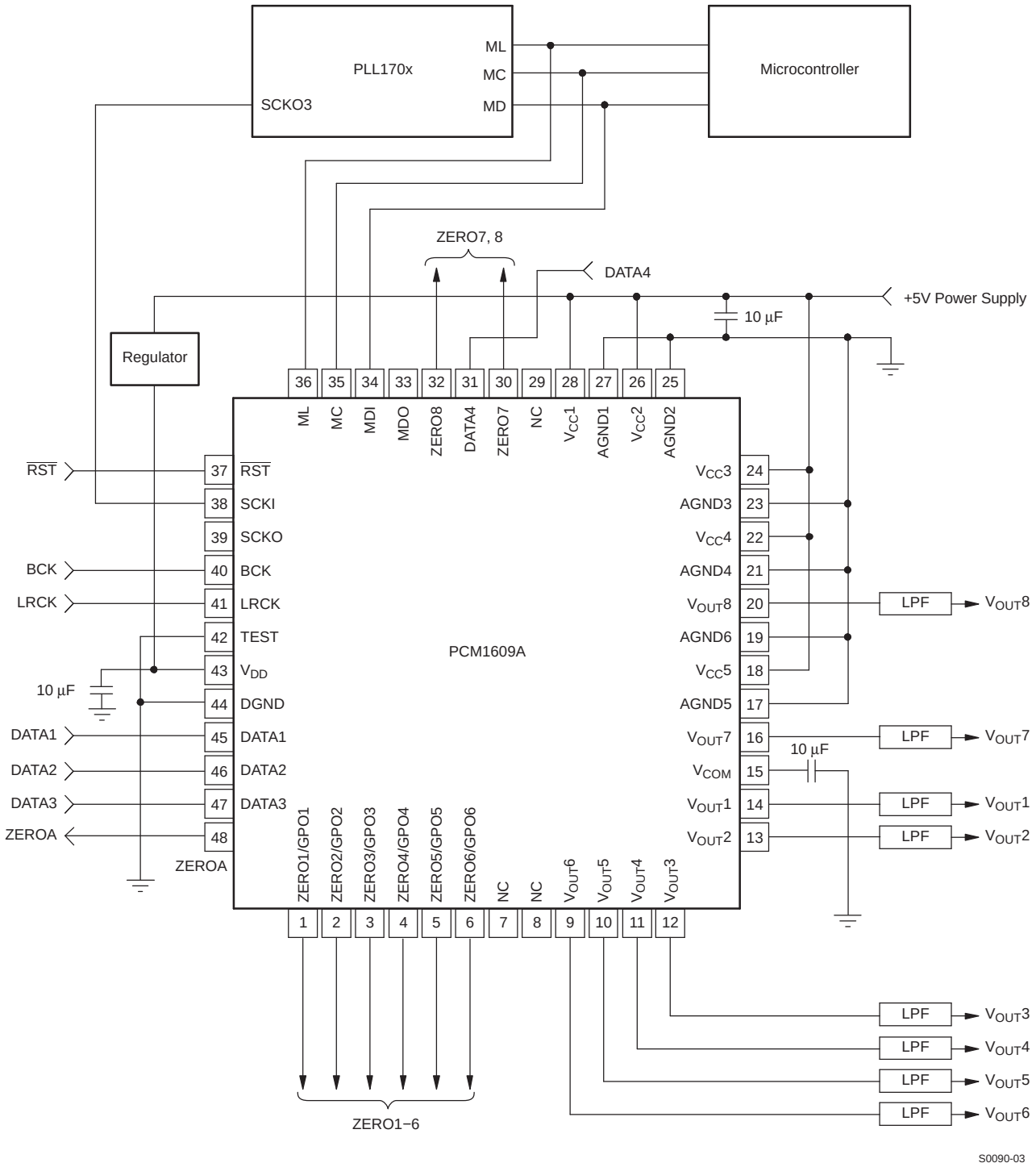
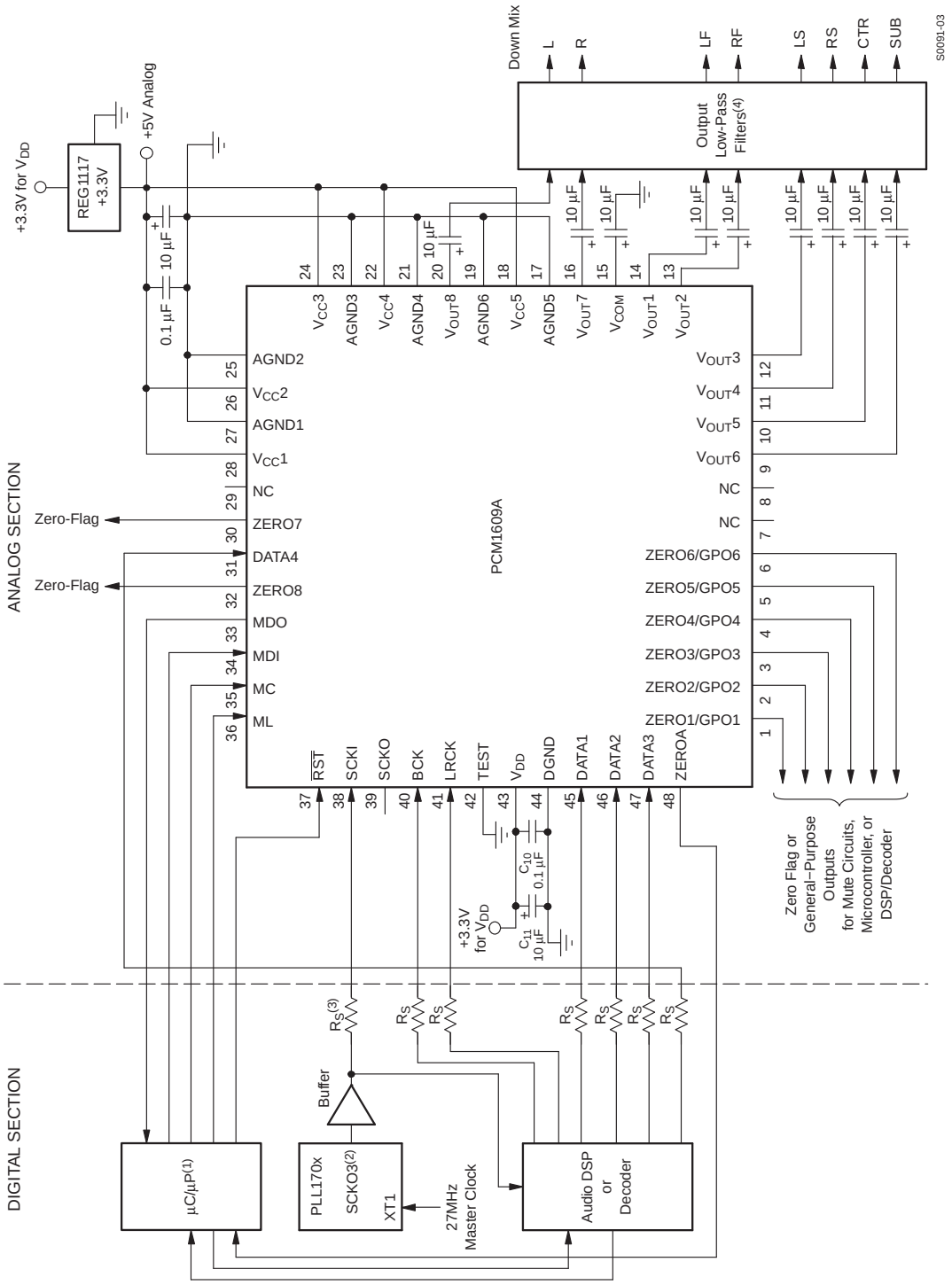


Figure 30. Basic Connection Diagram



(1) Serial control and reset functions can be provided by DSP/decoder GPIO pins.

(2) Actual clock output used is determined by the application.

(3) R_S = 22 Ω to 100 Ω

(4) See the Application Information section of this data sheet for more information

Figure 31. Typical Application Diagram

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A typical application diagram is shown in Figure 31. The REG1117-3.3 from TI is used to generate 3.3 V for V_{DD} from the 5-V analog power supply. The PLL170x from TI is used to generate the system clock input at SCKI, as well as generating the clock for the audio signal processor.

Series resistors (22 Ω to 100 Ω) are recommended for SCKI, LRCK, BCK, DATA1, DATA2, DATA3, and DATA4. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which removes high-frequency noise from the digital signal, thus reducing high-frequency emission.

POWER SUPPLIES AND GROUNDING

The PCM1609A requires a 5-V analog supply and a 3.3-V digital supply. The 5-V supply is used to power the DAC analog and output filter circuitry, whereas the 3.3-V supply is used to power the digital filter and serial interface circuitry. For best performance, the 3.3-V supply should be derived from the 5-V supply using a linear regulator (see Figure 31).

Two capacitors are required for supply bypassing (see Figure 30). These capacitors should be located as close as possible to the PCM1609A package. The 10-µF capacitors should be tantalum or aluminum electrolytic, whereas the 0.1-µF capacitors are ceramic (X7R type is recommended for surface-mount applications).

DAC OUTPUT FILTER CIRCUITS

Delta-sigma DACs use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 32 and Figure 33 show the recommended external low-pass active filter circuits for dual- and single-supply applications. These circuits are second-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see the *FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program* application report (literature number SBFA001) available from the TI web site (www.ti.com).

Because the overall system performance is defined by the quality of the DACs and their associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. The OPA2134 and OPA2353 dual operational amplifiers from TI are shown in Figure 32 and Figure 33, and are recommended for use with the PCM1609A.

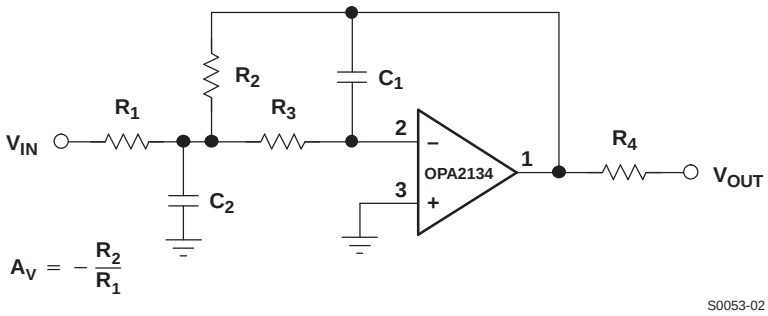

Figure 32. Dual-Supply Filter Circuit

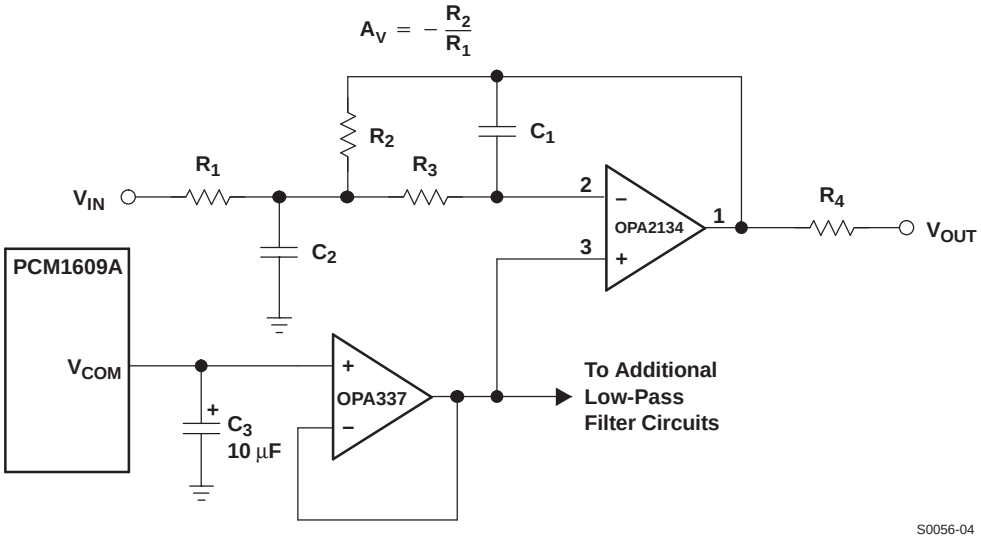

Figure 33. Single-Supply Filter Circuit

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1609A is shown in Figure 34. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1609A should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

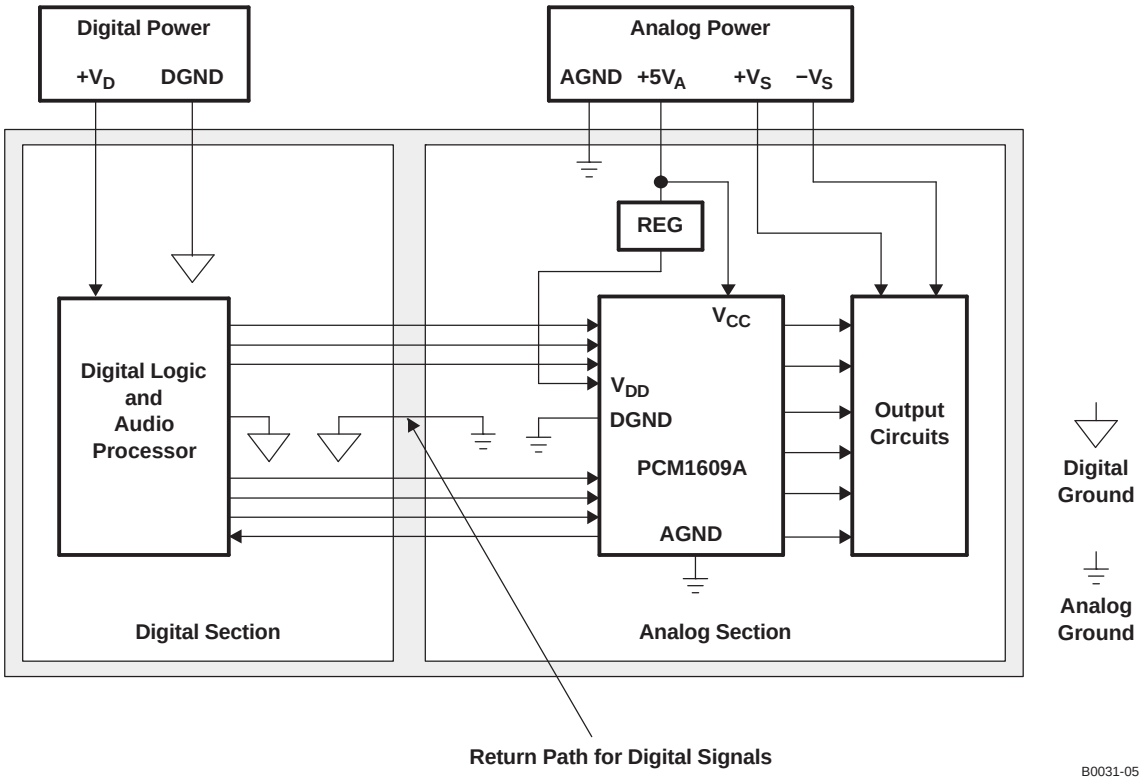

Figure 34. Recommended PCB Layout

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Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the DACs. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 35 shows the recommended approach for single-supply applications.

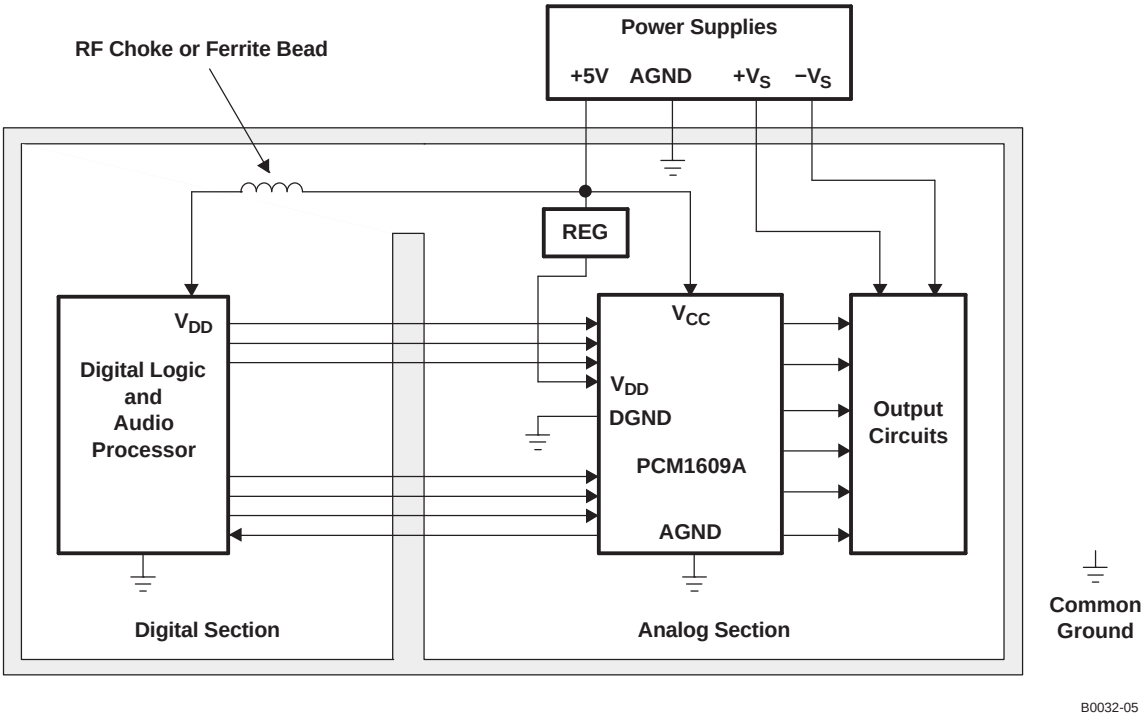

Figure 35. Single-Supply PCB Layout

THEORY OF OPERATION

The DAC section of the PCM1609A is based on a multibit delta-sigma architecture. This architecture uses a fourth-order noise shaper and an 8-level amplitude quantizer, followed by an analog low-pass filter. A block diagram of the delta-sigma modulator is shown in Figure 36. This architecture has the advantage of stability and improved jitter tolerance, when compared to traditional 1-bit (2-level) delta-sigma designs.

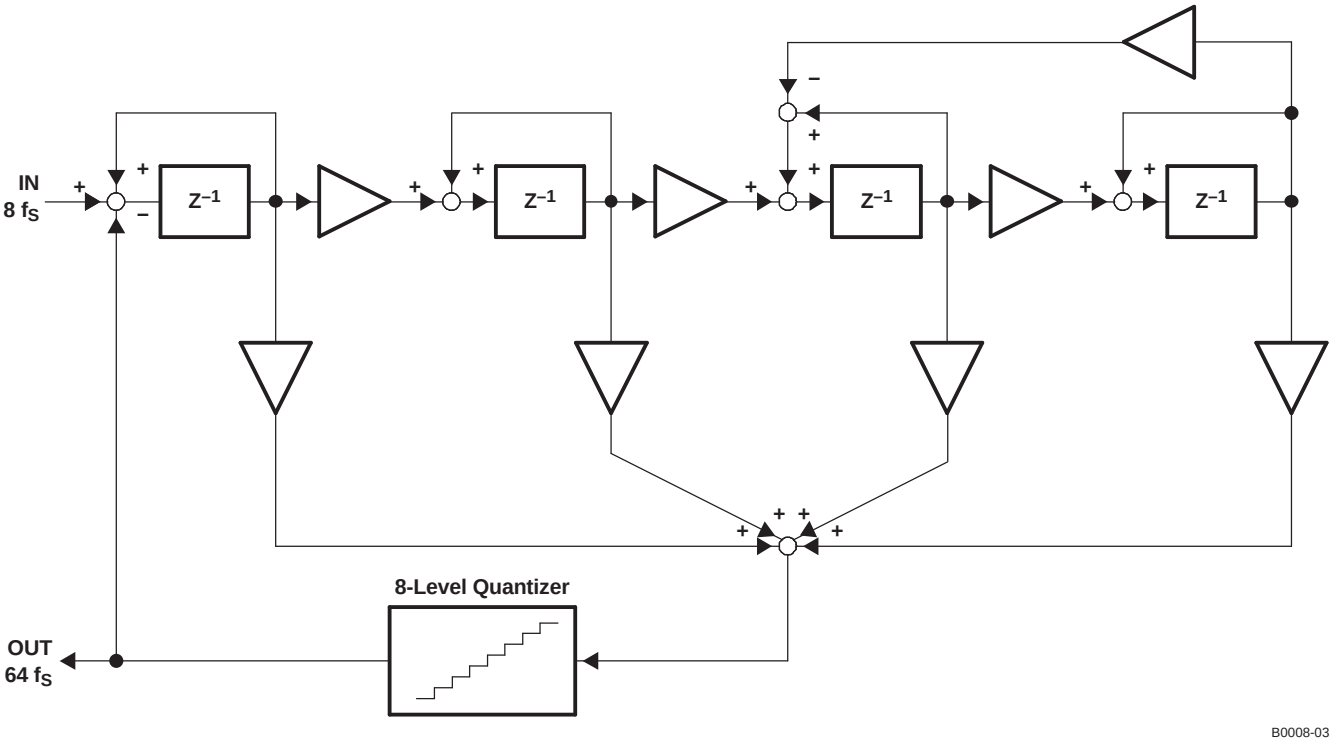

Figure 36. Eight-Level Delta-Sigma Modulator

The combined oversampling rate of the digital interpolation filter and the delta-sigma modulator is 32 f_S, 64 f_S, or 128 f_S. The total oversampling rate is determined by the desired sampling frequency. If $f_S \leq 96$ kHz, the OVER bit in register 12 can be set to an oversampling rate of 64 f_S or 128 f_S. If $f_S > 96$ kHz, the OVER bit can be used to set the oversampling rate to 32 f_S or 64 f_S. Figure 37 shows the out-of-band quantization noise plots for both the 64× and 128× oversampling scenarios. Notice that the 128× oversampling plot shows significantly improved out-of-band noise performance, allowing for a simplified low-pass filter to be used at the output of the DAC.

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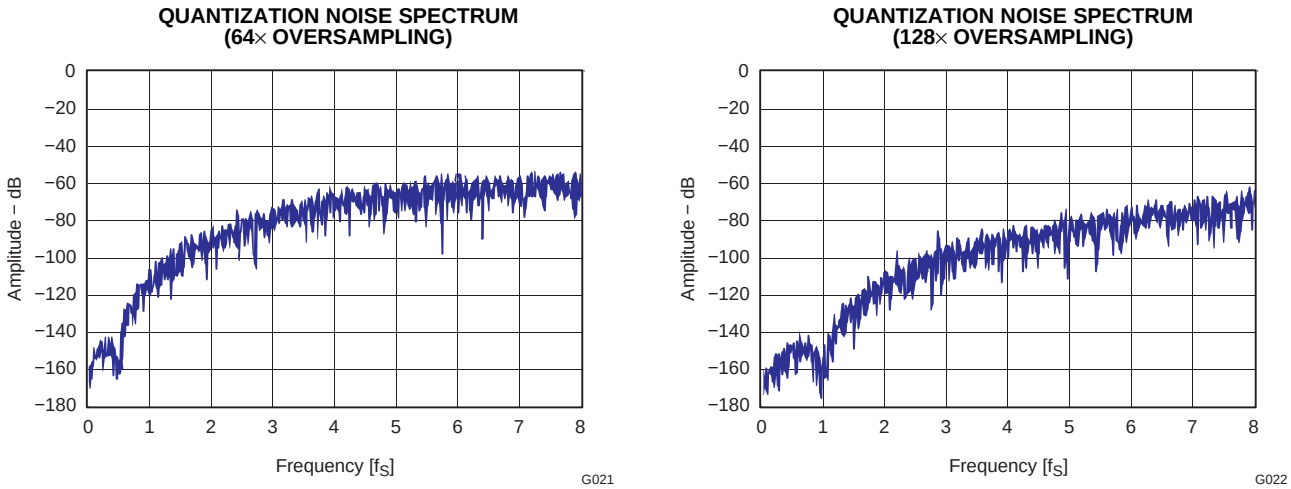


Figure 37. Quantization Noise Spectrum

Figure 38 illustrates the simulated jitter sensitivity of the PCM1609A. To achieve best performance, the system clock jitter should be less than 300 ps. This is easily achieved using a quality clock generation IC, such as the PLL170x from TI.

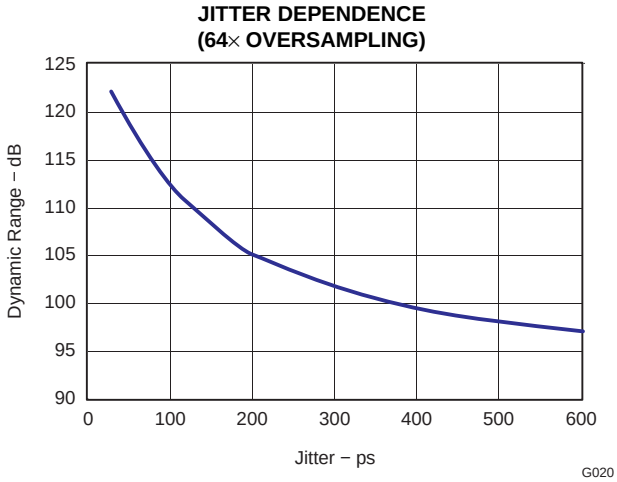


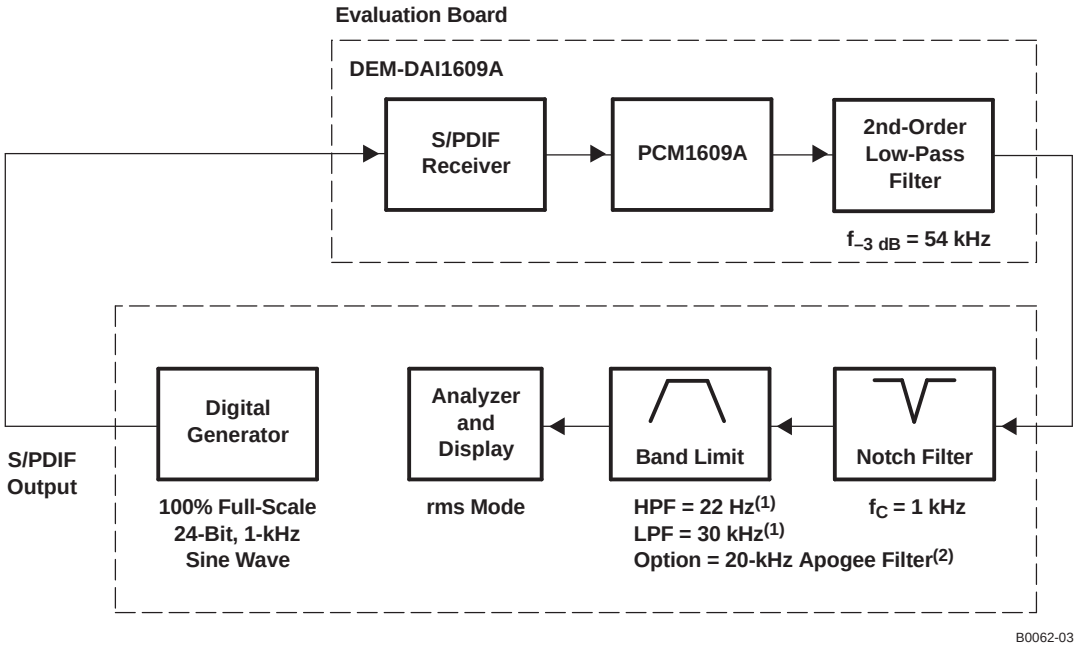
Figure 38. Jitter Sensitivity

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1609A. In all cases, a System Two™ Cascade audio measurement system by Audio Precision™ or equivalent is used to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE (THD+N)

THD+N is a significant feature of merit for audio DACs, because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N. The test setup for THD+N measurements is shown in Figure 39.



(1) There is little difference in measured THD+N when using the various settings for these filters.

(2) Required for THD+N test

Figure 39. Test Setup for THD+N Measurements

For PCM1609A DACs, THD+N is measured with a full-scale 1-kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to a 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via coaxial cable to the digital audio receiver on the DEM-DAI1602 demonstration board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited, using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

DYNAMIC RANGE

Dynamic range is specified as A-weighted THD+N measured with a –60-dBFS 1-kHz digital sine-wave stimulus at the input of the DAC. This measurement is designed to give a good indication of how the DAC performs, given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 40, and is similar to the THD+N test setup discussed previously. The differences include the band-limit filter selection, the additional A-weighting filter, and the –60-dBFS input level.

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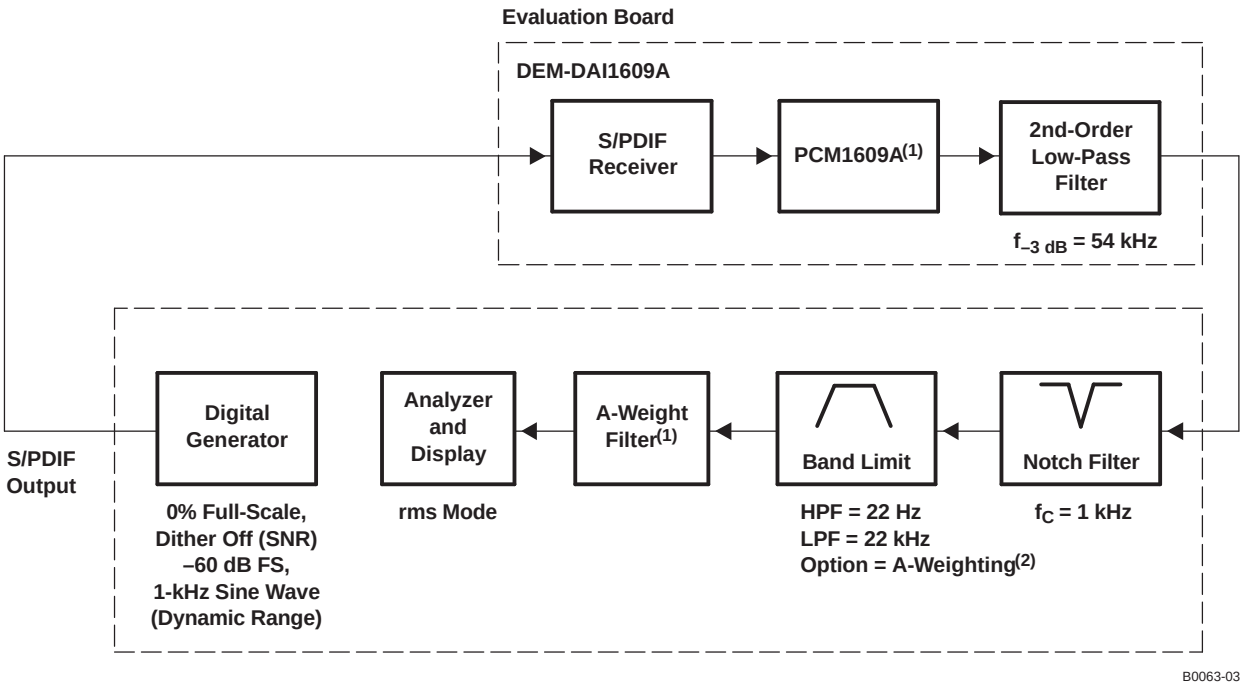

(1) Infinite-zero-detect mute disabled

(2) Results without A-weighting are approximately 3 dB worse.

Figure 40. Test Setup for Dynamic Range and SNR Measurements

IDLE-CHANNEL SIGNAL-TO-NOISE RATIO (SNR)

The SNR test provides a measure of the noise of the DAC. The input to the DAC is in all-0s data, and the DAC infinite-zero-detect mute function must be disabled (default condition at power up for the PCM1609A). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) can be observed at the output. The dither function of the digital signal generator must also be disabled to ensure an all-0s data stream at the input of the DAC.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level (see the notes in Figure 40).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1609APT	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1609A	Samples
PCM1609APTR	NRND	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1609A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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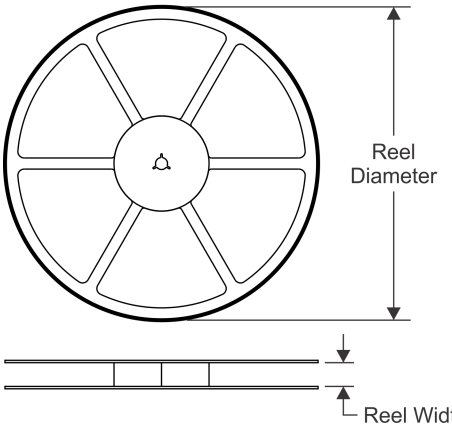
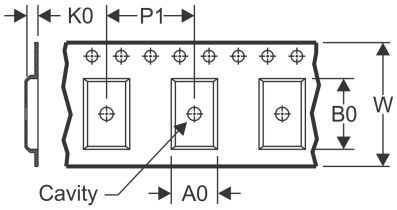
TAPE AND REEL INFORMATION

REEL DIMENSIONS

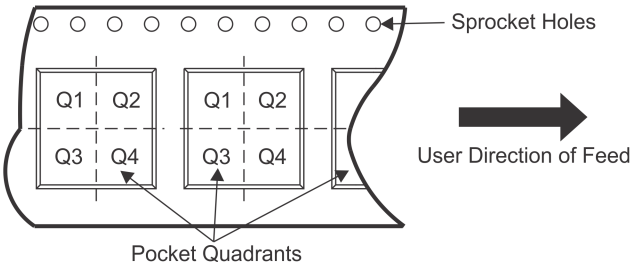


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

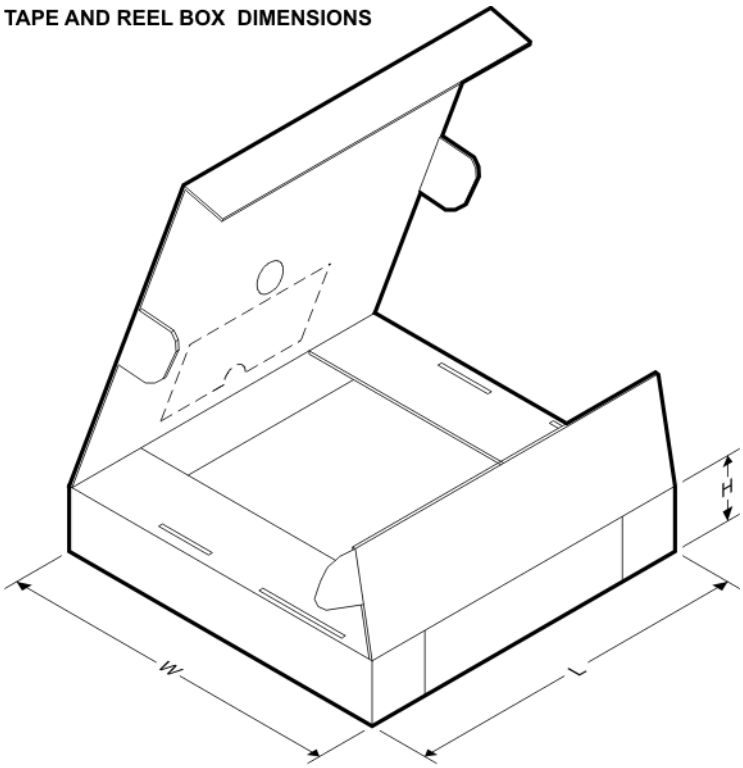
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1609APTR	LQFP	PT	48	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

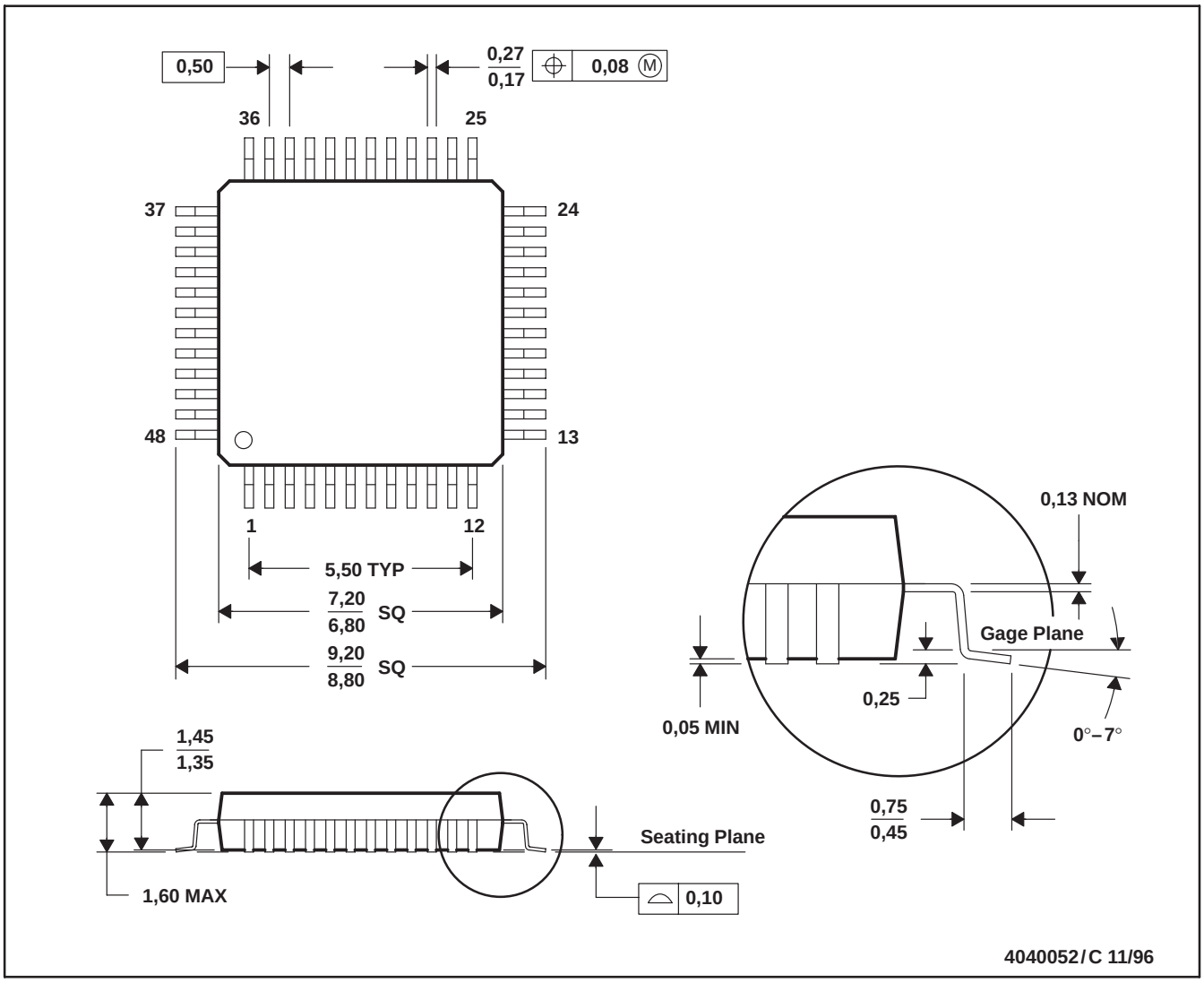
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1609APTR	LQFP	PT	48	1000	350.0	350.0	43.0

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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