

NLHV001

1-Bit Gate Pulse Modulator

The NLHV001 is a 1-bit gate pulse modulator designed to translate logic voltages for TFT LCD panels. This part translates a low voltage logic input signal to an output voltage of 15 V to 38 V. In addition, the NLV001 provides a user selectable delay and fall time on the high-to-low edge of the output signal. The delay and fall times are controlled by the magnitudes of the external and capacitor resistor, respectively.

Features

- Gate Pulse Modulation (GPM)
- TFT LCD Flicker Compensation Circuit
- Reduction of Coupling Effect Between Gate Line and Pixel
- Provides Power Sequencing Circuit for Gate Driver IC
- Wide Power Supply Operation: 15 V to 38 V
- Adjustable Output Delay and Fall Time
- This is a Pb-Free Device

Typical Applications

- TFT LCDs

Important Information

- ESD Protection for All Pins:
Human Body Model (HBM) > 3000 V

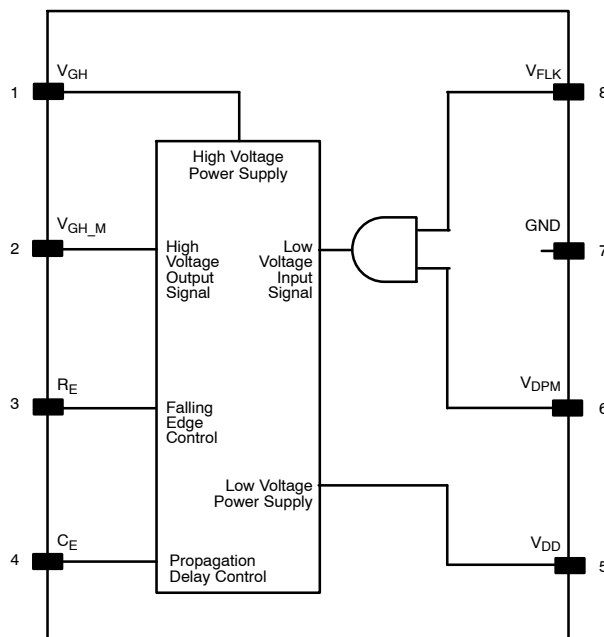
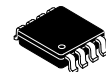


Figure 1. Block Diagram



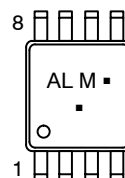
ON Semiconductor®

<http://onsemi.com>



US8
US SUFFIX
CASE 493

MARKING DIAGRAM



AL = Device Code
M = Date Code*
■ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

NLHV001

PIN DESCRIPTION

Pin	Pin Name	Pin Function	Comment
1	V_{GH}	Power Supply Input	$V_{GH} = 15$ to 38 V
2	V_{GH_M}	Output	This output directly drives the power supply of Gate Driver IC
3	R_E	R_E pin used to set the falling edge time (t_{fall})	The Delay time is programmed by connecting resistor R_E to V_{GH} and capacitor C_E to ground.
4	C_E	C_E pin used to set the propagation delay time (t_{phl})	
5	V_{DD}	Reference to input	The reference input pin is used to reduce flicker. The reference input voltage is as follows: $V_{DD} \leq V_{GH} - 8.5$ V, $V_{DD} = 0$ to 25 V
6	V_{DPM}	Signal input 1	V_{DPM} single input voltage is as follows: $V_{DPM} = 0$ V to V_{GH} . The V_{DPM} pin is used to create a delay with the V_{GH} to prevent system latch-up. V_{DPM} also determines the time V_{GH} is ON.
7	GND	Ground	
8	V_{FLK}	Signal input 2	V_{FLK} single input voltage is as follows: $V_{DPM} = 0$ V to V_{GH} . The V_{FLK} determines the ON/OFF time of the TFT LCD and is produced from LCD timing controller module.

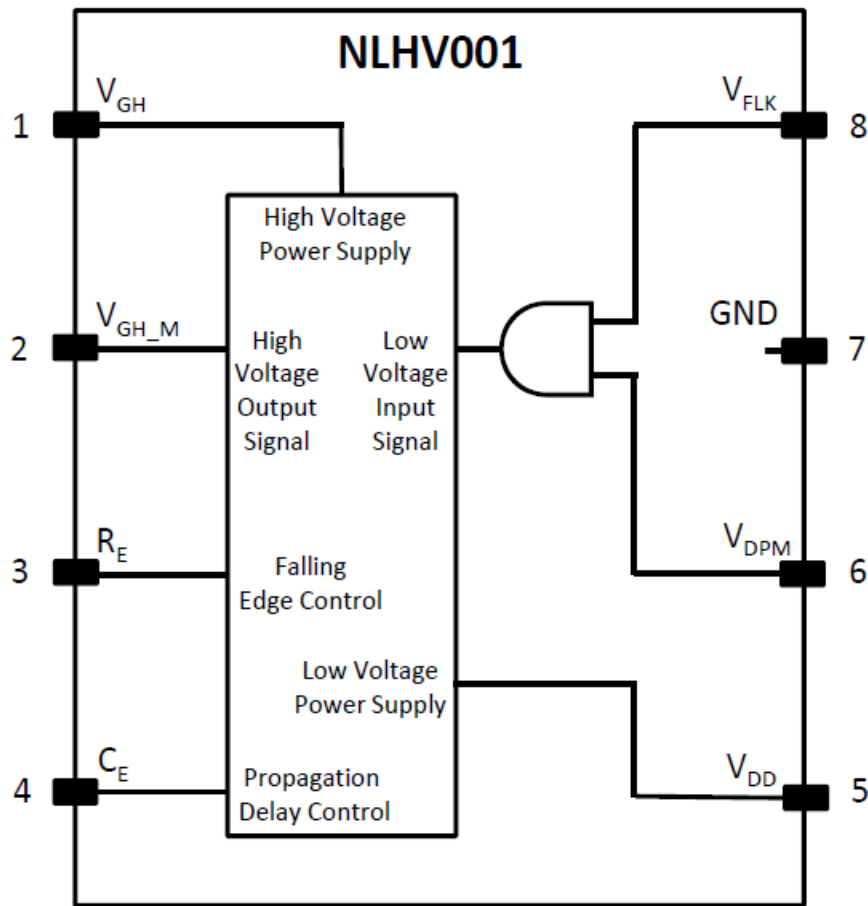


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
V_{GH}	DC Supply Voltage		-0.5 to +40	V
V_{DD}	DC Supply Voltage		-0.5 to +40	V
V_{FLK}	Input Voltage V_{FLK}		-0.5 to +40	V
V_{DPM}	Input Voltage V_{DPM}		-0.5 to +40	V
$V_{GH} - V_{CE}$	Differential Voltage Between V_{GH} and V_{CE} Pins (Note 1)		9.5	V
I_{IK}	DC Input Diode Current		50	mA
I_{OK}	DC Output Diode Current		50	mA
I_O	DC Output Current		50	mA
I_{GH}	DC Supply Current Per Supply Pin		50	mA
P_D	Power Dissipation		200	mW
T_J	Junction Temperature		95	°C
T_{STG}	Storage Temperature		-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. A differential voltage between the V_{GH} and V_{CE} pins ($V_{GH} - V_{CE}$) occurs during the power-up and power-down procedure. The voltages on the V_{GH} and C_E pins are equal at steady-state conditions after power-up.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{GH}	DC Supply Voltage (Note 2)	$V_{GH} - V_{DD} \geq 8.5 \text{ V}$	15	–	38	V
V_{DD}	DC Supply Voltage	$V_{DD} \leq V_{GH} - 8.5 \text{ V}$	0	–	25	V
V_{FLK}	Input Voltage V_{FLK}	$V_{GH_M} = V_{GH} - 1.2 \text{ V}$	1.5	–	V_{GH}	V
V_{DPM}	Input Voltage V_{DPM}	$V_{GH_M} = V_{DD} + 1.5 \text{ V}$	0	–	V_{GH}	V
T_A	Operating Temperature Range		-40	–	85	V
$V_{GH} - V_{CE}$	Differential Voltage Between V_{GH} and V_{CE} Pins (Note 3)		–	–	5.5	V
$\Delta t / \Delta V_{GH}$	Safe V_{GH} Power-Up Slew Rate (Note 4)	$C_E = 5 \text{ pF}$	–	0.2	–	$\mu\text{s} / \text{V}$
		$C_E = 10 \text{ pF}$		0.4		
		$C_E = 50 \text{ pF}$		0.6		
		$C_E = 150 \text{ pF}$		0.7		
		$C_E = 220 \text{ pF}$		0.8		
		$C_E = 500 \text{ pF}$		1.2		
		$C_E = 1000 \text{ pF}$		2.2		

2. Maximum recommended V_{GH} supply voltage guaranteed by design.
3. A differential voltage between the V_{GH} and V_{CE} pins ($V_{GH} - V_{CE}$) occurs during the power-up and power-down procedure. The voltages on the V_{GH} and C_E pins are equal at steady-state conditions after power-up.
4. It is recommended that a ceramic or tantalum decoupling capacitor of 0.1 to 1 μF is used on the V_{GH} power supply voltage. The capacitor should be placed adjacent to the NLHV001 and connected between V_{GH} and Ground.

NLHV001

ELECTRICAL CHARACTERISTICS ($V_{GH} = 20\text{ V}$, $V_{DD} = 10\text{ V}$, $V_{DPM} = 2.2\text{ V}$, $V_{FLK} = 2.2\text{ V}$, $V_{GH} - V_{DD} \geq 8.5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$, unless otherwise noted.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{FLK_H}	FLK High Voltage	$V_{GH_M} = V_{GH} - 1.6$	1.5	–	V_{GH}	V
V_{FLK_L}	FLK Low Voltage	$V_{GH_M} = V_{DD} + 1.5$	0	–	0.5	V
V_{DPM_H}	DPM High Voltage	$V_{FLK} = 0\text{ V}$, $V_{GH_M} = V_{DD} - 0.2\text{ V}$	1.5	–	V_{GH}	V
V_{DPM_L}	DPM Low Voltage	$V_{FLK} = 0\text{ V}$, $V_{GH_M} \leq 0.6\text{ V}$	0	–	0.5	V
I_{DPM}	DPM ON Current	$V_{FLK} = 3\text{ V}$, $V_{GH_M} = V_{GH}$	0.2	0.4	2	mA
R_C	R_C (Resistor of V_{DPM} pin)	$V_{GH} = 22\text{ V}$, $R_C \approx (V_{GH} - 0.9) / I_{DPM}$ (Application Circuits 2 and 3)	10	45	100	k Ω
$V_{GH_M_H}$	Output High Voltage	$I_O = 10\text{ mA}$	$V_{GH} - 1.6$	$V_{GH} - 0.7$	–	V
$V_{GH_M_R}$	Output Reset Voltage	$V_{DPM} = 0\text{ V}$, $V_{FLK} = 3\text{ V}$	–	–	0.6	V
		$V_{DPM} = 0\text{ V}$, $V_{FLK} = 0\text{ V}$				
$V_{GH_M_L}$	Output Low Voltage	$V_{DPM} = 3\text{ V}$, $V_{FLK} = 0\text{ V}$, $I_O = -1\text{ mA}$	$V_{DD} - 0.2$	$V_{DD} + 0.3$	$V_{DD} + 0.8$	V
I_{GH}	Power Supply Input Current	$V_{GH} = 35\text{ V}$, $V_{DD} = 15\text{ V}$, $V_{FLK} = V_{DPM} = 3.3\text{ V}$, $I_O = 0$	–	3.5	–	mA
I_{DD}	Reference Input Current	$V_{GH} = 35\text{ V}$, $V_{DD} = 15\text{ V}$, $V_{FLK} = 0\text{ V}$, $V_{DPM} = 3.3\text{ V}$, $I_O = 0$	–	40	–	μA

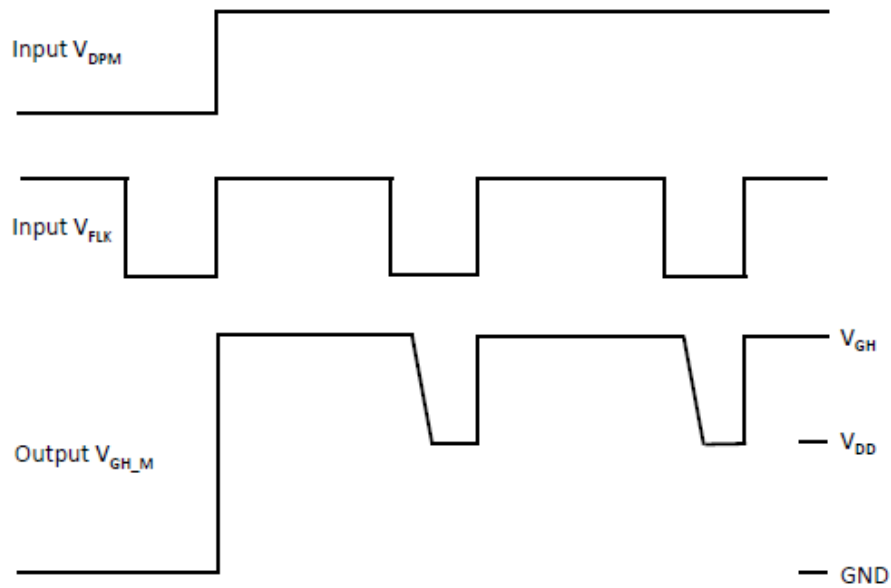


Figure 3. Input and Output Waveforms (Application Circuit #1)

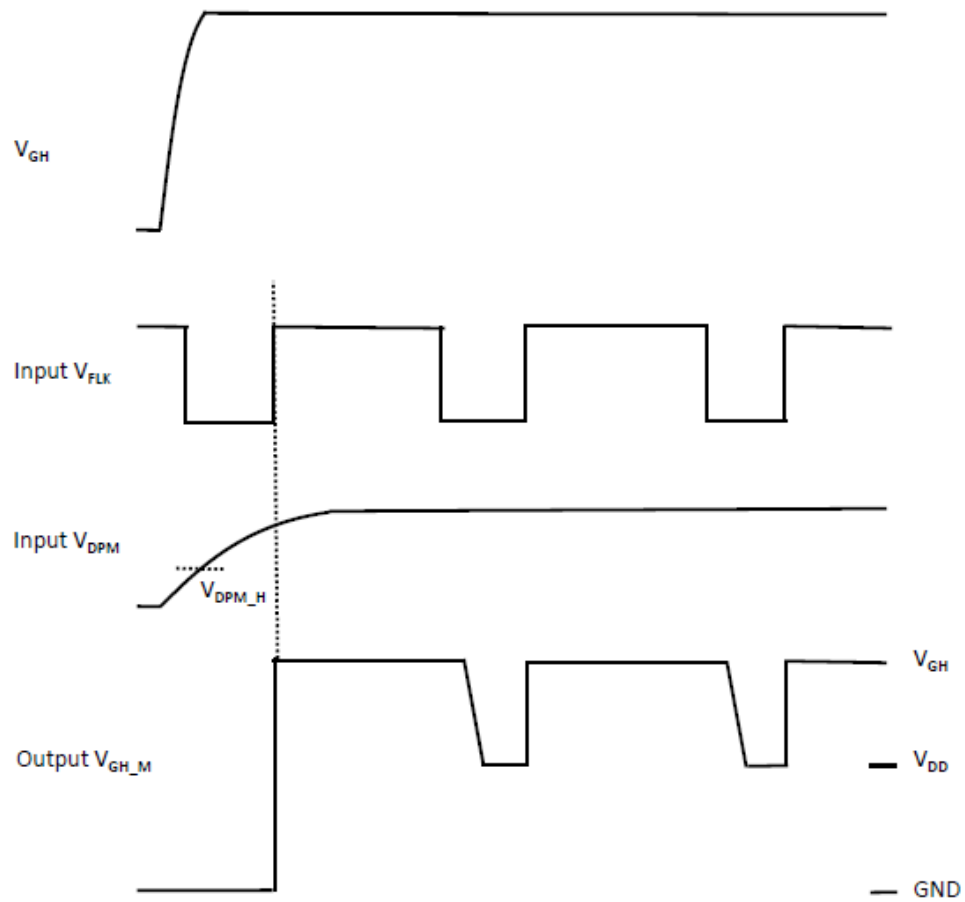


Figure 4. Input and Output Waveforms (Application Circuit #2)

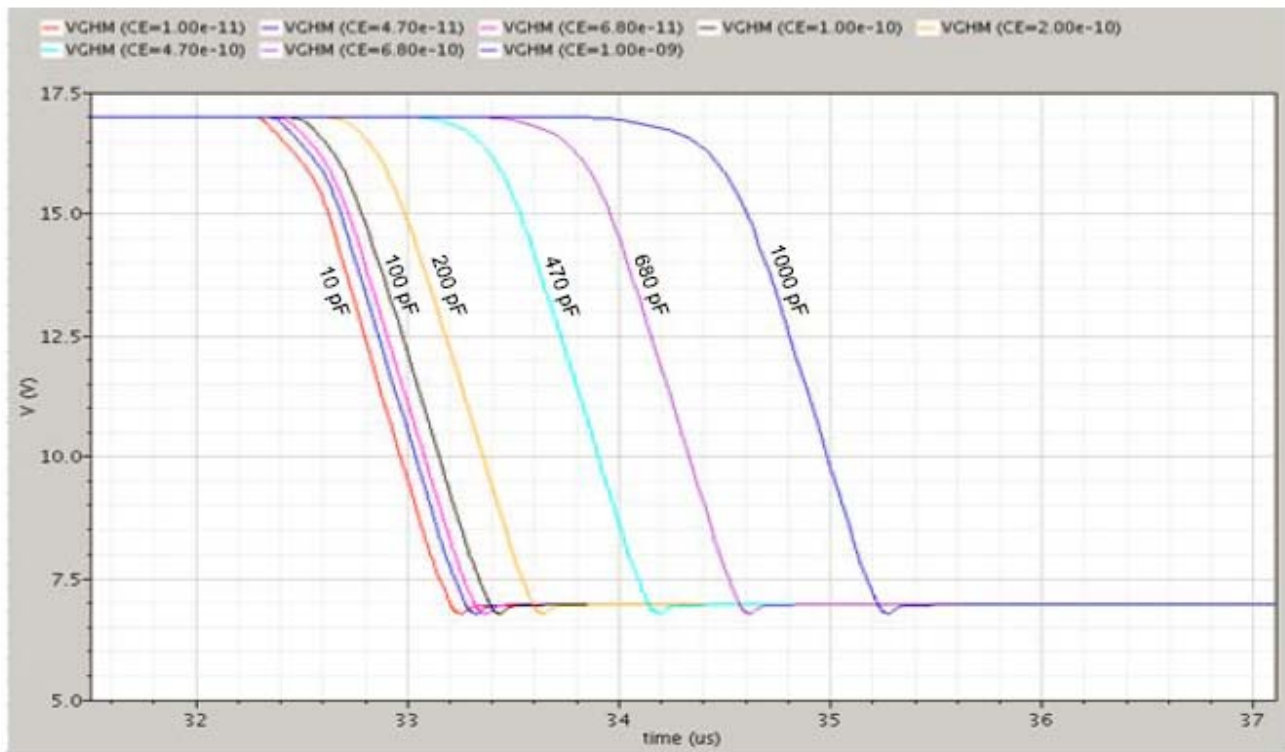


Figure 5. V_{GH_M} Output Propagation Delay (t_{phl}) is controlled by C_E
 (Application Circuit #1, $V_{GH} = 18$ V, $V_{DD} = 7$ V, $R_E = 3.9$ k Ω , $R_L = 15$ k Ω , $C_L = 220$ pF, $T_a = 25$ °C)

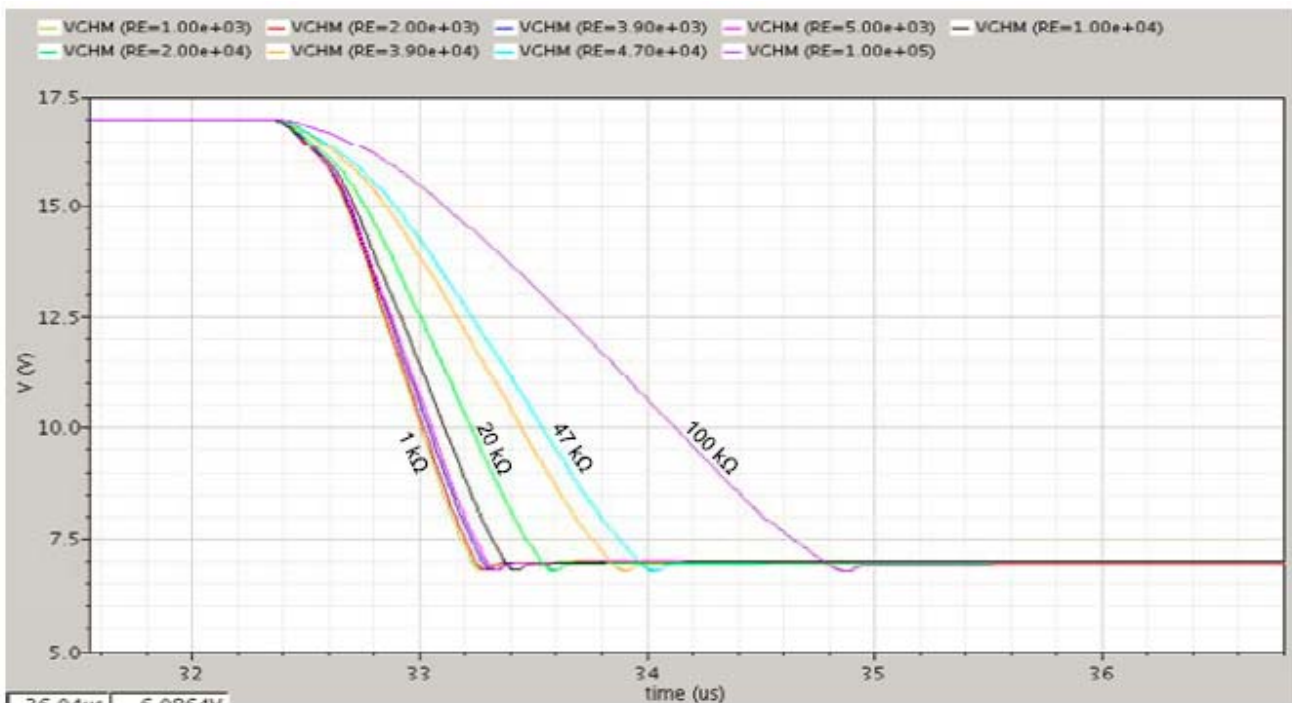


Figure 6. V_{GH_M} Output Transition Falling Edge (t_{fall}) is controlled by R_E
 (Application Circuit #1, $V_{GH} = 18$ V, $V_{DD} = 7$ V, $C_E = 47$ pF, $R_L = 15$ k Ω , $C_L = 220$ pF, $T_a = 25$ °C)

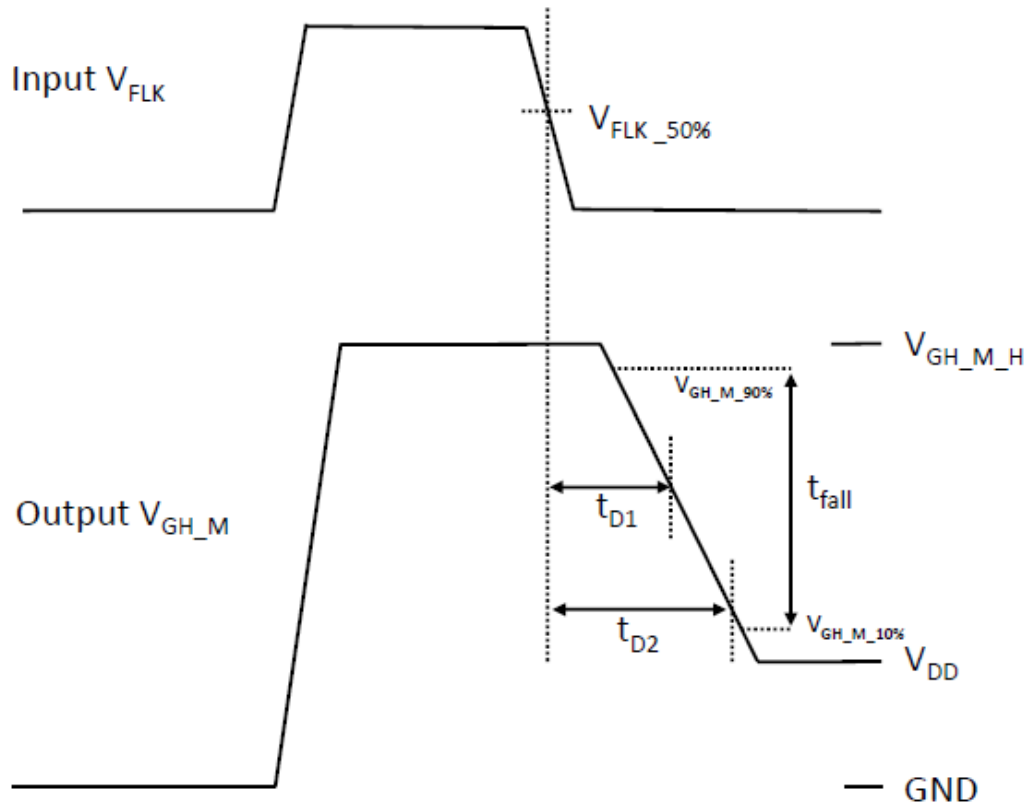


Figure 7.

Definition of Delay Time

t_{D1} = Delay Time 1 (t_{D_50-50}) = $V_{FLK_50\%}$ to $[V_{DD} + ((V_{GH_M_H} - V_{DD}) \times 0.50)]$

t_{D2} = Delay Time 2 (t_{D_50-15}) = $V_{FLK_50\%}$ to $[V_{DD} + ((V_{GH_M_H} - V_{DD}) \times 0.15)]$

t_{fall} = 90-to-10% Fall Time = $[V_{DD} + ((V_{GH_M_H} - V_{DD}) \times 0.90)] - [V_{DD} + ((V_{GH_M_H} - V_{DD}) \times 0.10)]$

DELAY TIME CHARACTERISTICS

(Application Circuit #1, $V_{DPM} = 3\text{ V}$, $V_{FLK} = 3\text{ V}$, $R_E = 15\text{ k}\Omega$, $R_L = 15\text{ k}\Omega$, $C_L = 220\text{ pF}$, $T_A = 25^\circ\text{C}$)

Parameter	Test Condition	Typ	Unit
Delay Time 2 (t_{D_50-15})	$V_{GH} = 17\text{ V}$, $V_{DD} = 6.7\text{ V}$, $C_E = 100\text{ pF}$	2.4	μs
	$V_{GH} = 17\text{ V}$, $V_{DD} = 6.7\text{ V}$, $C_E = 240\text{ pF}$	2.8	μs
	$V_{GH} = 22.4\text{ V}$, $V_{DD} = 10\text{ V}$, $C_E = 91\text{ pF}$	2.3	μs
	$V_{GH} = 22\text{ V}$, $V_{DD} = 10\text{ V}$, $C_E = 220\text{ pF}$	2.8	μs
	$V_{GH} = 25.4\text{ V}$, $V_{DD} = 15.4\text{ V}$, $C_E = 56\text{ pF}$	2.4	μs
	$V_{GH} = 25.4\text{ V}$, $V_{DD} = 15.4\text{ V}$, $C_E = 130\text{ pF}$	2.5	μs

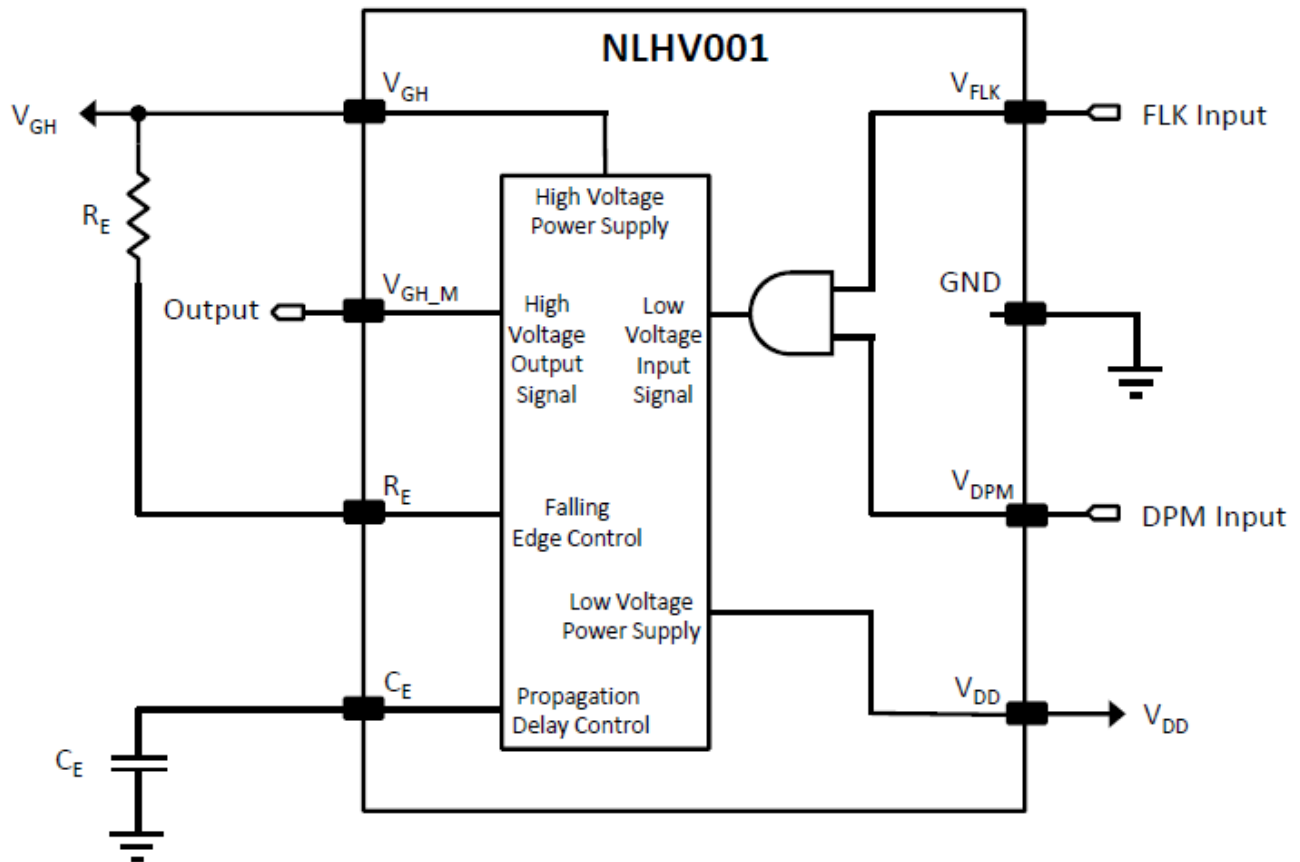


Figure 8. Application #1 Circuit Schematic

Notes:

1. V_{DPM} can rise only after V_{GH} is valid.

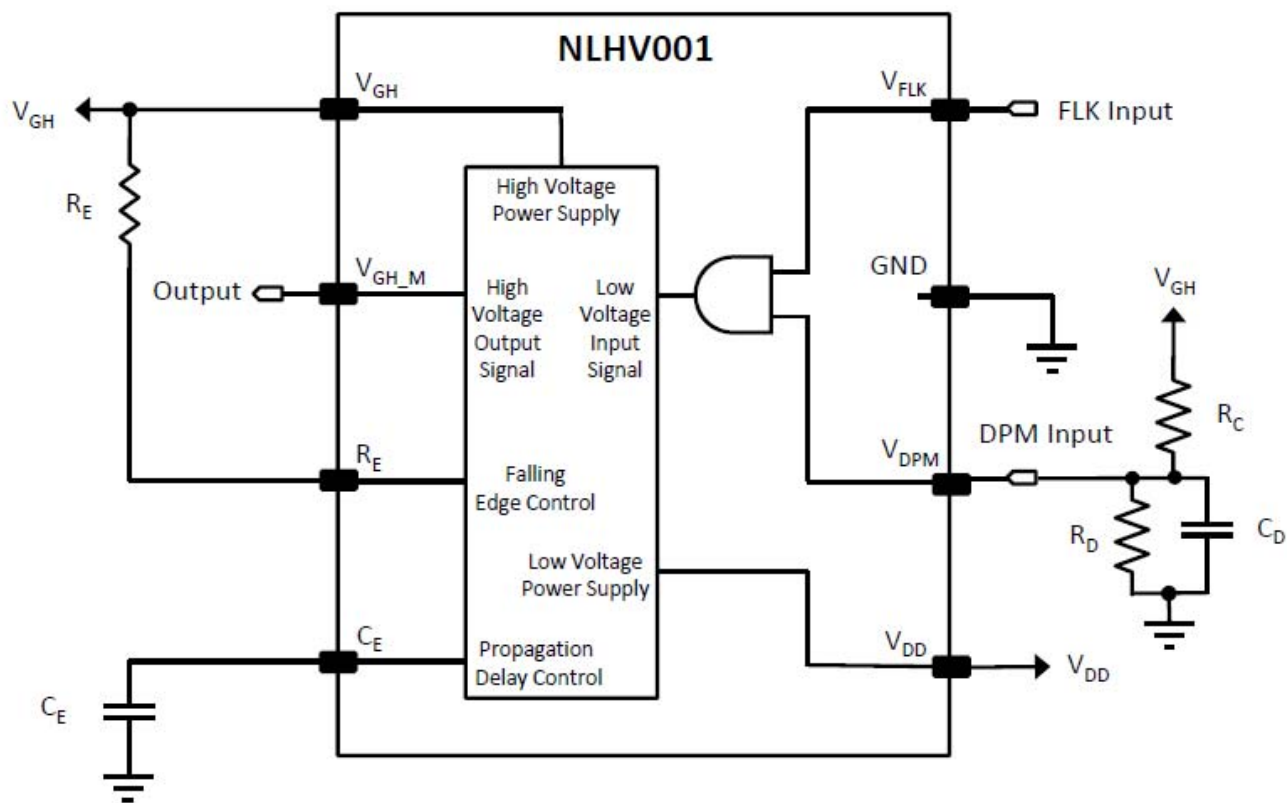


Figure 9. Application #2 Circuit Schematic

Notes:

- 1. V_{DPM} is produced by a Low Pass Filter (LPF) on V_{GH} pin with R_C and C_D .
- 2. R_D is a V_{DPM} pull-down resistor.

APPLICATION 2: V_{GH_M} SIGNAL DELAY TIME CHARACTERISTICS

V_{GH} (V)	V_{DD} (V)	C_D (μ F)	R_D (k Ω)	R_C (k Ω)	V_{GH_M} ON Delay Time (when V_{GH} ON) t_{on} (ms)	V_{DPM} Pin Discharge Time (when V_{GH} OFF) t_{off} (ms)
22	12	1	15	50	17.9	3.4
		1	1.5	20	5.5	1.4
		1	0.620	10	1.7	0.74

APPLICATION 2: FUNCTION DESCRIPTION

Name	Comment	Function
R_C	R_C and C_D determines the time when the V_{DPM} pin is charged.	t_{on} = Time when V_{GH_M} is high t_{off} = Time when V_{DPM} pin is fully discharged
C_D		
R_D	R_D determines the time when the V_{DPM} pin is discharged.	

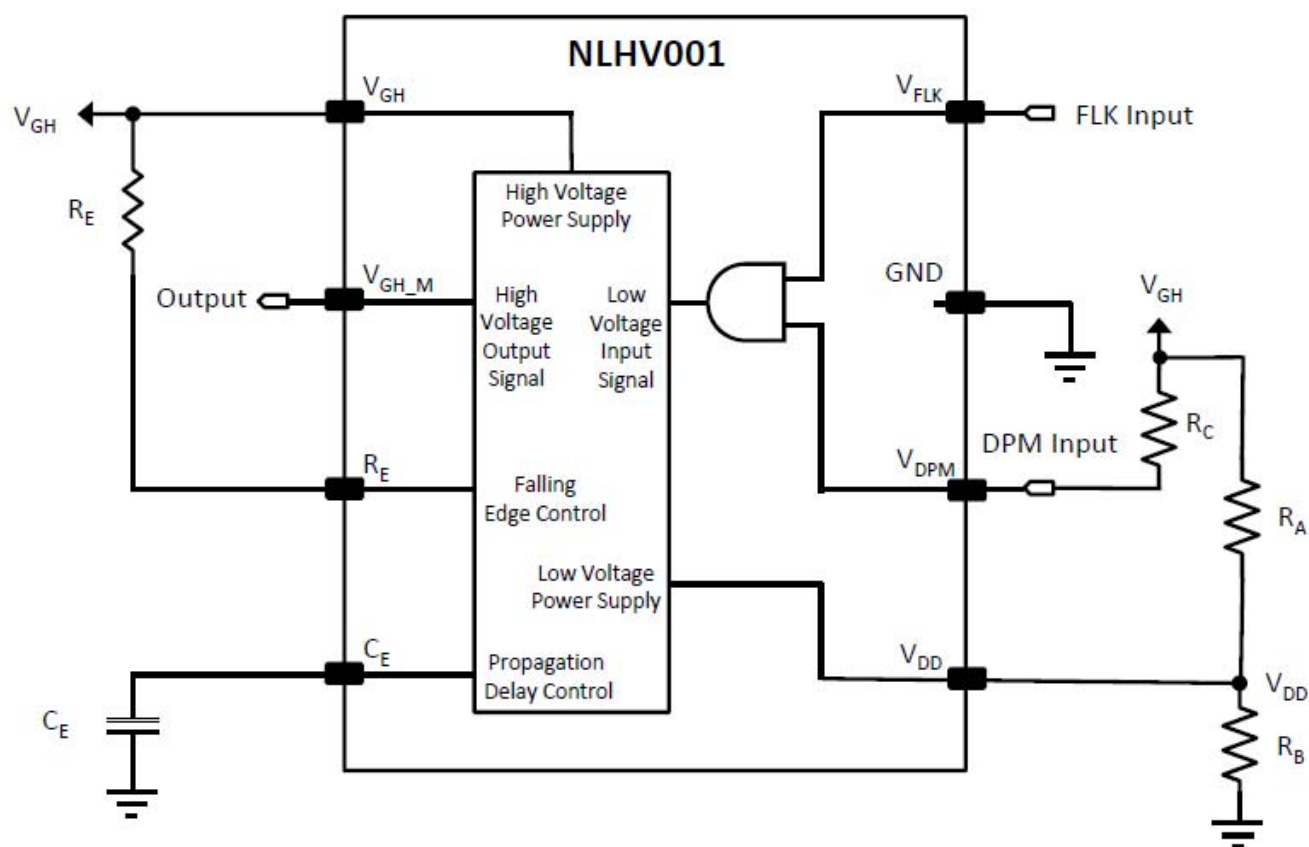


Figure 10. Application #3 Circuit Schematic

APPLICATION 3: FUNCTION DESCRIPTION

Name	Comment	Function
RA	RA and RB set the VDD voltage.	$V_{DD} = V_{GH} \times (R_B / (R_A + R_B))$
RB		
RC	RC determines the voltage that VDD pin becomes high.	

Notes:

- 1. VDD produced by external RC and internal R and C.
- 2. VDD created from external resistors RA and RB.
- 3. VGH should be higher than 18 V to meet VDD_H.
- 4. RA = 15 kΩ, RB = 10 kΩ, RC = 45 kΩ, RE = 15 kΩ, RL = 15 kΩ, CE = 220 pF, CL = 100 pF

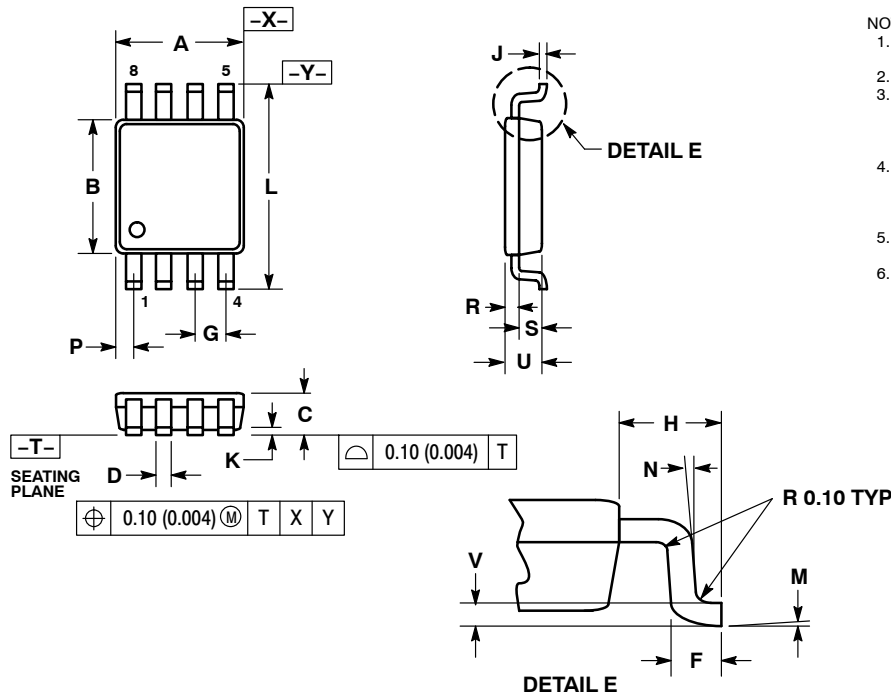
DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
NLHV001USG	US8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

US8
CASE 493-02
ISSUE B

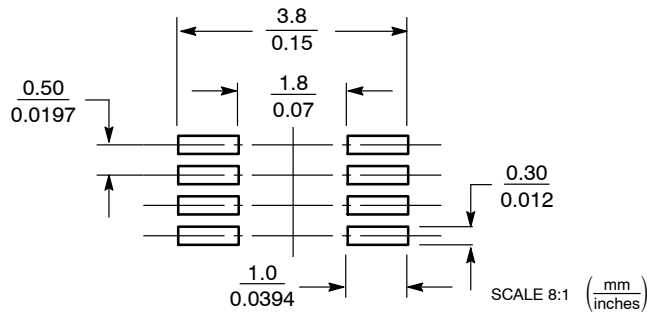


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ± 0.0508 (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0°	6°	0°	6°
N	5°	10°	5°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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