MIC502 Evaluation Board

Fan Management IC

General Description

The combination evaluation/demonstration board for the MIC502 Fan Management IC is depicted in a typical hookup in Figure 1. This dual-purpose board can be used (1) to initially evaluate the functionality of the MIC502 on the bench, and (2) as a demonstration installed in the target equipment. It is important to realize that the "evaluation board" consists of both portions of the board, intact. If it is decided to sever the smaller, right-side portion of the board to produce the "demonstration board," the remaining larger, left-side portion of the board will no longer be useful.

Inputs to the board are one or two thermistors, or one thermistor and the NLX "FanC" signal. The board operates from either a 5V or 12V power supply. A 12V supply is required for the fan. Outputs are a 30Hz pulse-width modulated (PWM) fan-drive output and an open-collector, active-low overtemperature fault (/OTF) signal. The status of the latter output is also displayed via an LED on the evaluation portion of the board. When using only one thermistor, the VT2 input should be grounded (unless using the NLX "FanC" signal). When using the demonstration board alone the VSLP input should not be left open; i.e., include R5 and R6 by populating the board with resistors to properly set VSLP.

The evaluation/demonstration board schematic is shown in Figure 3. The demonstration portion of this board consists of header J2 and those components to its right. The board is designed so it can be cut in two immediately to the left of this single-in-line header to reduce its size to a 2-inch^2 board for ease of installation in the target equipment. See Figure 2. Note that when this portion of the board is actually severed from the evaluation board, header J2 is then the electrical connection mechanism for the user of the demonstration board. There are also vias along the edge of the board that can serve as additional connection points. The preferred method of severing the boards is a sheet metal shear (before component population of the board). It is also possible to very carefully saw the board after it is populated with components using a hacksaw.

The board contains several configuration jumpers that provide flexibility in tailoring it to different supply voltage and signal environments. Table 1 lists the interconnection points found on the evaluation (larger, left side) portion of the board. Table 2 lists the interconnection points on the demonstration (smaller, right side) portion of the board. Table 3 lists all jumpers with their functions and configuration settings. Table 4 lists test points, and Table 5 is a parts list.

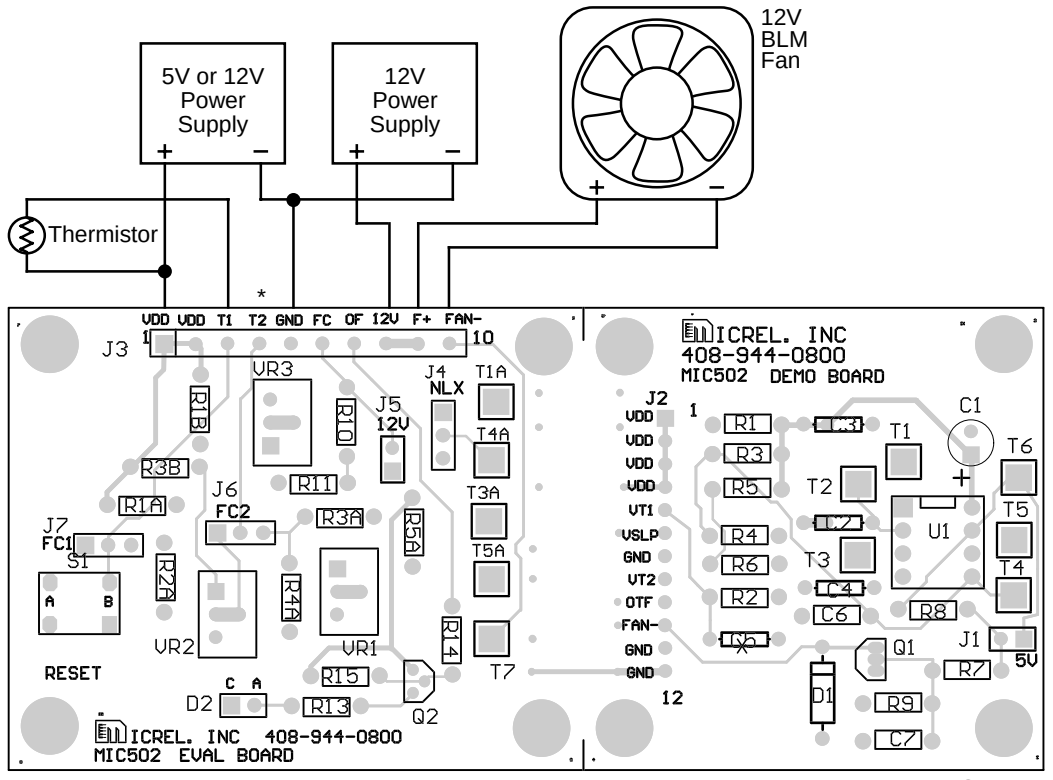


Figure 1. MIC502 Evaluation and Demonstration Board Connections

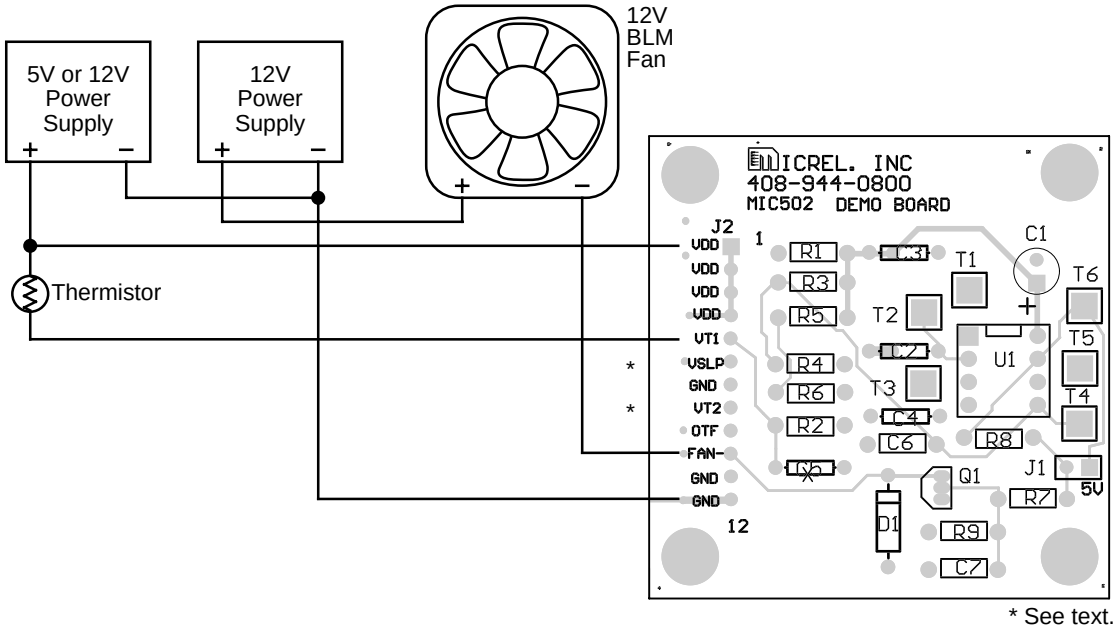


Figure 2. MIC502 Demonstration Board Connections

Circuit Description

Figure 3 reveals numerous unpopulated components. The following discussions explain these empty placeholders and their intended uses. Additionally, a description of how to use the board(s) is presented along with this discussion. Refer to Figure 1 and the MIC502 product data sheet for information pertaining to device operation. Tables 1 through 5 provide information pertinent to operation and use of the evaluation/ demonstration board(s).

Temperature Control Inputs

Three-pin jumper J7, labeled FC1, controls the Fan Control #1 input to the MIC502, VT1, pin 1. When a jumper is placed between J7-1 and J7-2, VT1 can be adjusted from 0V to about $0.9V_{DD}$ using potentiometer VR3. This simulates a voltage that would normally be produced by a thermistor and resistor interface. When J7-2 and J7-3 are connected via a jumper, VT1 is controlled by resistors on either the evaluation board or the demonstration board. The resistors for this interface are R1 and R2 on the demonstration board; they are duplicated by R1a and R2a on the evaluation board. The notion is that several values may need to be experimented with on the evaluation board and, after the correct values are established, they can be moved to the demonstration (if it is desired to sever the two boards). Also in association with input VT1 is a push-button system RESET switch, S1, which momentarily grounds VT1 to affect a reset of the MIC502.

Similarly, the above description also applies to three-pin jumper J6, labeled FC2, and the second MIC502 fan control input, VT2. This voltage is adjusted using VR2, and the corresponding resistor pairs are R3 and R4 (demonstration board) and R3a and R4a (evaluation board).

NLX “FanC” Input

Three-pin jumper J4, labeled NLX, determines whether VT2 is (1) simulated by VR2, (2) thermistor/resistor derived for a second temperature input, or (3) the “FanC” signal of an NLX motherboard computer. Jumpering J4-1 and J4-2 facilitate simulation or thermistor-derived control; jumpering J4-2 and J4-3 accommodate the "FanC" signal input (via pin 6 of terminal strip J3). The MIC502 evaluation/demonstration board can operate from either 5V or 12V, but since the NLX "FanC" signal can swing nearly to 11V, two-pin jumper J5, labeled 12V, is provided to enable an attenuator for this signal when the board is powered from 5V. The jumper should be in place (eliminating the attenuation) when the board is powered from 12V.

Sleep Voltage Input

Potentiometer VR1 adjusts the VSLP input, pin 3, from 0V to about $0.9V_{DD}$. Resistors R5 and R6 on the demonstration board are unpopulated pending determination of the desired sleep voltage setting for a given application. There are no functionally redundant resistors on the evaluation board, nor is there a jumper to disable the output VR1, so R5 and R6 apply only when using a severed demonstration board.

5V vs. 12V Operation

Two-pin jumper J1, labeled 5V, allows for tailoring the base-drive current to the motor-drive transistor, Q1. When the board is operated from 5V this jumper should be in place. It should be removed for 12V operation to reduce on-chip power dissipation.

Additional Considerations

Since the demonstration board could be placed in a noisy environment, such as in close proximity (or inside) a switch-mode power supply, placeholders are provided for potential bypass capacitors for the VSLP, VT1, and VT2 inputs; these are C4, C5, and C6. A candidate value is 0.01µF.

Thermistor Selection

The thermistor interface (choice of a particular thermistor, and calculation of R1 and R2, etc.) is the responsibility of the customer. However, the evaluation/demonstration board is shipped with a thermistor for experimentation. Because the envisioned evaluation may require the thermistor to be located remotely from the board, the thermistor is not mounted on the board (nor are there provisions for mounting it on the board. Instead, wiring to the thermistor is connected by the user between V_{DD} (J3-2) and T1 (J3-3) of the evaluation board, or counterpart connection points (J2-4 and J2-5) on the demonstration board.

The thermistor that is shipped with the board is the RL2010-54.1K-138-D1, by Keystone Thermometrics. This device has a resistance of 100kΩ at 25°C; its resistance at 70°C is about 13.6kΩ. Calculations for determining typical values for R1 and R2 for interfacing this thermistor are discussed in the MIC502 product data sheet; R1 should be about 100kΩ, and R2 should be about 33kΩ. These values provide approximately 25% RPM at 25°C and 100% RPM at 70°C.

Symbol	Label	Description	Comment
J3	J3	10-Terminal, Screw-type Terminal Block	Interconnects evaluation board to power supply(ies), thermistors, and fan.
J3-1	VDD	V_{DD} Supply Input	+5V or +12V.
J3-2	VDD	V_{DD} Supply Input	Spare terminal, useful for thermistor bias connection.
J3-3	T1	Thermistor #1 Input	Thermistor connects between here and VDD terminal.
J3-4	T2	Thermistor #2 Input	Optional input.
J3-5	GND	Supply Return Point	
J3-6	FC	NLX “FanC” Input	Optional input.
J3-7	OF	/OFT Output	Optional output.
J3-8	12V	+12V Fan Supply Tie Point	Convenience tie point.
J3-9	F+	Fan High-Side (12V) Tie Point	Fan connection tie point.
J3-10	FAN–	Fan Low-Side (Drive) Output Connection	Fan connection tie point.

Table 1. Evaluation Board Connection Points

Symbol	Label	Description	Comment
J2	J2	12-terminal, Single-Inline Header Strip	Interconnects demonstration board to power supply(ies), thermistors, and fan (if demonstration board is severed from evaluation board).
J2-1	VDD	V_{DD} Supply Input	+5V or +12V.
J2-2	VDD	V_{DD} Supply Input	Spare terminal, useful for thermistor bias connection.
J2-3	VDD	V_{DD} Supply Input	Spare terminal.
J2-4	VDD	V_{DD} Supply Input	spare terminal.
J2-5	VT1	Thermistor #1 Input	Thermistor connects between here and VDD terminal.
J2-6	VSLP	VSLP Input	VSLP set by R5 and R6.
J2-7	GND	Supply Return Point	
J2-8	VT2	Thermistor #2 Input	Optional, thermistor or NLX “FanC” input.
J2-9	OTF	/OTF Output	Optional output.
J2-10	FAN–	Fan Low-Side (Drive) Output Connection	Fan connection tie point.
J2-11	GND	Supply Return Point	
J2-12	GND	Supply Return Point	

Table 2. Demonstration Board Connection Points

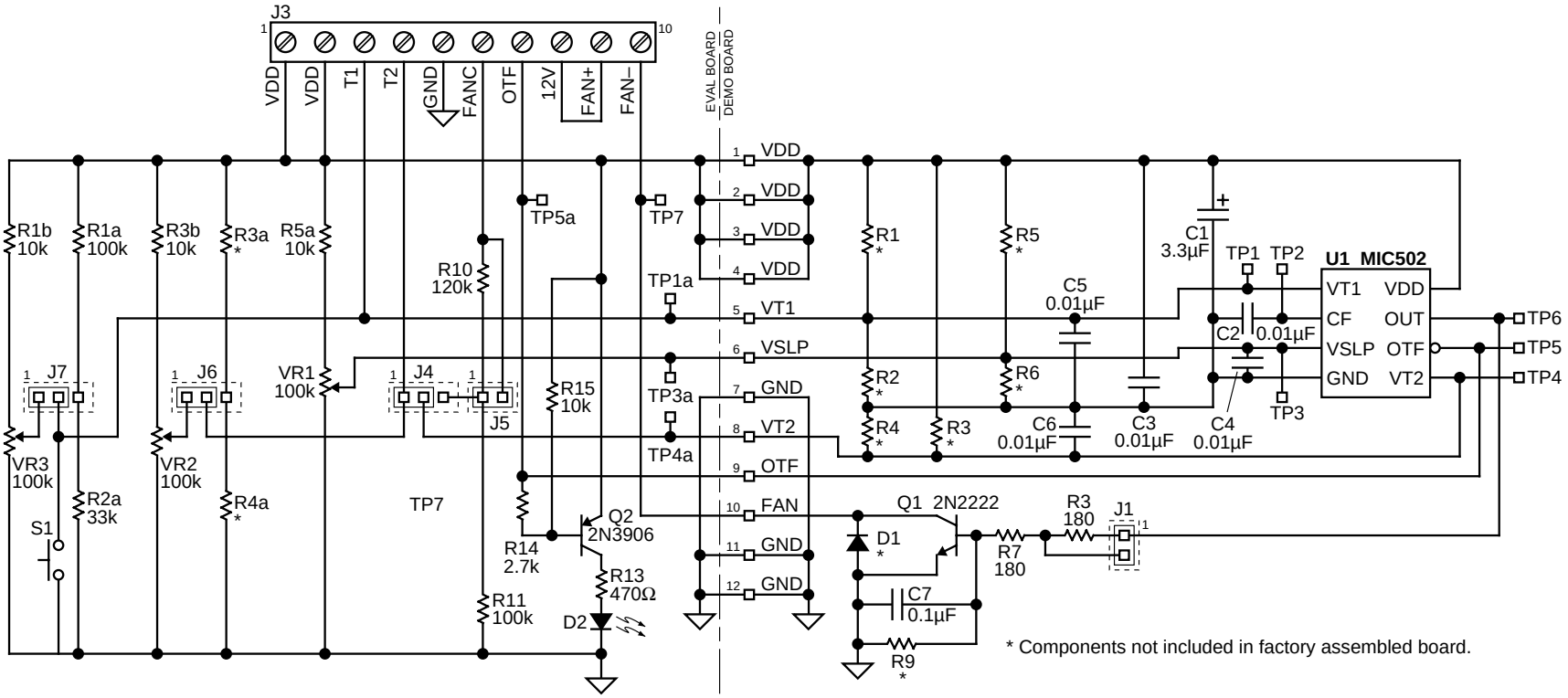


Figure 3. Evaluation/Demonstration Board Schematic

Symbol	Label	Jumper	Description	Comment
J1	5V	open	2-Pin Header	Remove jumper if V_{DD} = 12V.
J1	5V	1–2		Jumper pins 1–2 if V_{DD} = 5V.
J4	NLX	open	3-Pin Header	Remove jumper only if using 2nd thermistor and R3 and R4 are installed on demonstration board.
J4	NLX	1–2		Jumper pins 1–2 to simulate or use external thermistor #2.
J4	NLX	2–3		Jumper pins 2–3 to use NLX “FanC” input.
J5	12V	open	2-Pin Header	If using “FanC” input, remove jumper if V_{DD} = 5V.
J5	12V	1–2		If using “FanC” input, jumper pins 1–2 if V_{DD} = 12V.
J6	FC2	open	3-Pin Header	Remove jumper only if R3 and R4 are installed on demonstration board.
J6	FC2	1–2		Jumper pins 1–2 to use VR2 to simulate thermistor #2.
J6	FC2	2–3		Jumper pins 2–3 to use R3a and R4a to bias thermistor #2.
J7	FC1	open	3-Pin Header	Remove jumper only if R1 and R2 are installed on demonstration board.
J7	FC1	1–2		Jumper pins 1–2 to use VR3 to simulate thermistor #1.
J7	FC1	2–3		Jumper pins 2–3 to use R1a and R2a to bias thermistor #1.

Table 3. Configuration Jumpers and Settings

Symbol	Label	Description
TP1	T1	Access to VT1 on demostration board
TP1a	T1a	Access to VT1 on evaluation board
TP2	T2	Access to oscillator output on demostration board
TP3	T3	Access to VSLP on demostration board
TP3a	T3a	Access to VSLP on evaluation board
TP4	T4	Access to VT2 on demostration board
TP4a	T4a	Access to VT2 on evaluation board
TP5	T5	Access to /OTF on demostration board
TP5a	T5a	Access to /OTF on evaluation board
TP6	T6	Access to OUT on demostration board
TP7	T7	Access to FAN– (drive)

Table 4. Test Points

Parts List

Symbol	Type	Description	Comment
U1	MIC502BN	8-pin DIP (socketed)	8-pin DIP (socketed)
Q1	2N2222A	TO-92 NPN transistor	motor driver
Q2	2N3906	TO-92 PNP transistor	LED driver
D1	not used		
D2	LN28RP	red LED	OTF indicator
R1	*	⅛W resistor	demonstration board VT1 bias, **Note 1**
R1a	100k	⅛W resistor	evaluation board VT1 bias
R1b	10k	⅛W resistor	limits maximum VT1 to ≈ $0.9V_{DD}$
R2	*	⅛W resistor	demonstration board VT1 bias, **Note 1**
R2a	33k	⅛W resistor	evaluation board VT1 bias
R3	*	⅛W resistor	demonstration board VT2 bias, **Note 1**
R3a	*	⅛W resistor	evaluation board VT2 bias, **Note 2**
R3b	10k	⅛W resistor	limits maximum VT2 to ≈ $0.9V_{DD}$
R4	*	⅛W resistor	demonstration board VT2 bias, **Note 1**
R4a	*	⅛W resistor	evaluation board VT2 bias, **Note 2**
R5	*	⅛W resistor	demonstration board VSLP bias; **Note 1**
R5a	10k	⅛W resistor	limits maximum VSLP to ≈ $0.9V_{DD}$
R6	*	⅛W resistor	demonstration board VSLP bias; **Note 1**
R7	180Ω	⅛W resistor	base-drive current limit
R8	180Ω	⅛W resistor	base-drive current limit
R9	not used		
R10	120k	⅛W resistor	NLX "FanC" atten. resistor
R11	100k	⅛W resistor	NLX "FanC" atten. resistor
R12	symbol not used		not referenced
R13	470Ω	¼W resistor	LED current limit
R14	2.7k	⅛W resistor	base-drive current limit
R15	10k	⅛W resistor	Q2 turnoff
VR1	100k, 12-turn	potentiometer	adjusts VSLP voltage
VR2	100k, 12-turn	potentiometer	adjusts VT2 (simulated voltage)
VR3	100k, 12-turn	potentiometer	adjusts VT1 (simulated voltage)
C1	3.3µF, 16V	aluminum electrolytic	supply filter/ bypass
C2	0.1µF	ceramic bypass cap.	PWM oscillator timing
C3	0.1µF	ceramic bypass cap.	supply bypass
C4	0.1µF*	ceramic bypass cap.	optional VSLP bypass, **Note 4**
C5	0.1µF*	ceramic bypass cap.	optional VT1 bypass, **Note 4**
C6	0.1µF*	ceramic bypass cap.	optional VT2 bypass, **Note 4**
C7	0.1µF	bypass capacitor	
S1	SPST, NO	push-button switch	RESET switch

***** = not populated

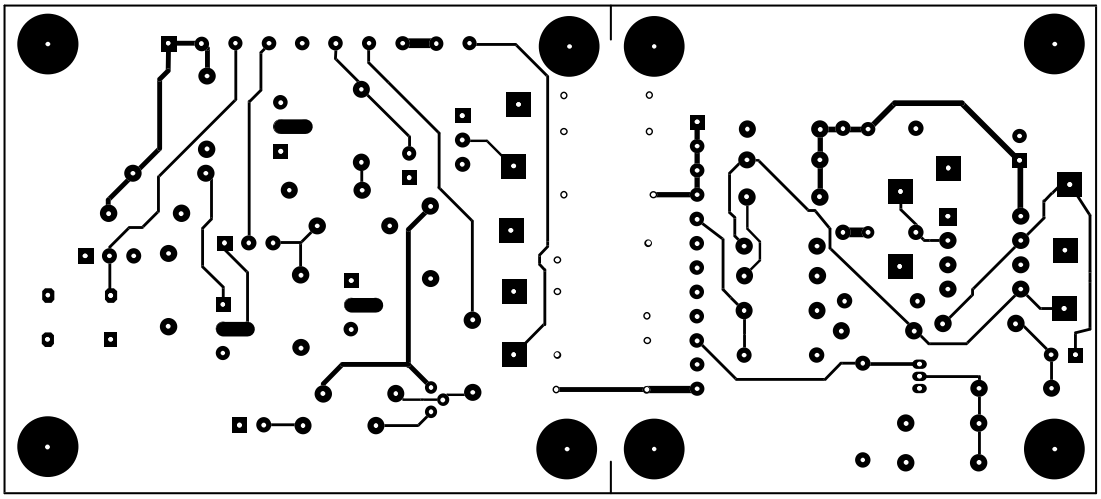
Note 1. Resistors are not populated on demonstration board because their value depends on the customer-chosen thermistor type and the desired setting for VSLP.

Note 2. Resistor is not populated on evaluation board because its value will be determined by customer-chosen thermistor type. Corresponds to functionally identical resistor on demonstration board.

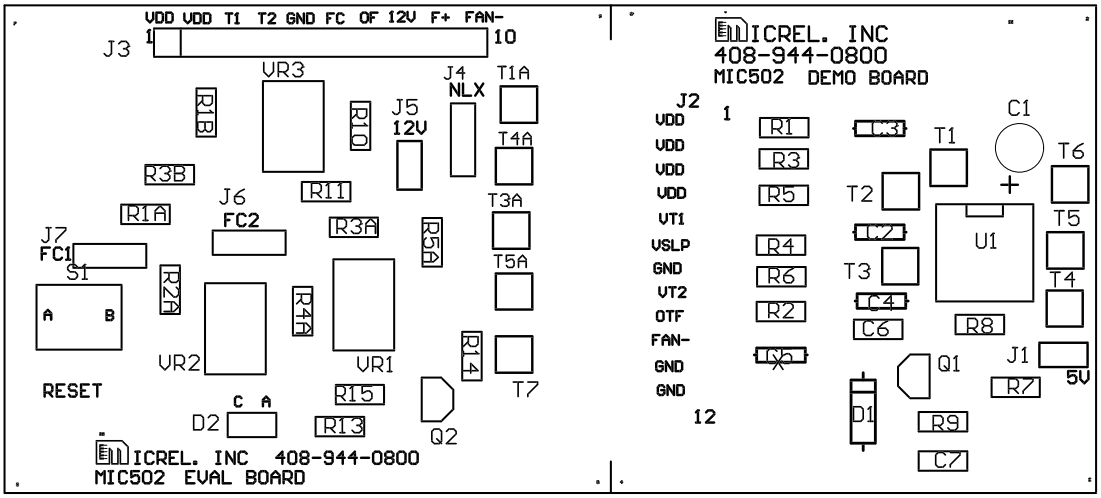
Note 3. These potentiometers adjust the VSLP voltage and the simulated thermistor voltages.

Note 4. Capacitors are not populated because they may not be required. Space is reserved for them in case there is noise pickup by any of the related MIC502 inputs.

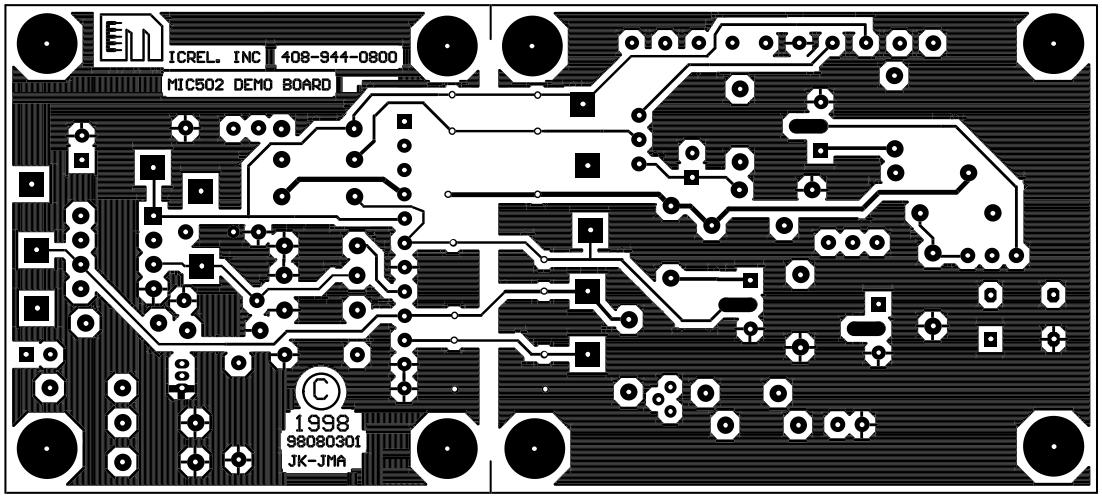
Printed Circuit Board Layouts



Component-Side Copper



Component-Side Silk Screen



Solder-Side Copper

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