

Octal 3-State Noninverting Transparent Latch

MC74HC573A, MC74HCT573A

The MC74HC573A / MC74HCT573A is identical in pinout to the LS573. The MC74HC573A device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT573A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The HC573A/HCT573A is identical in function to the HC373A/HCT373A but has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range:
2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

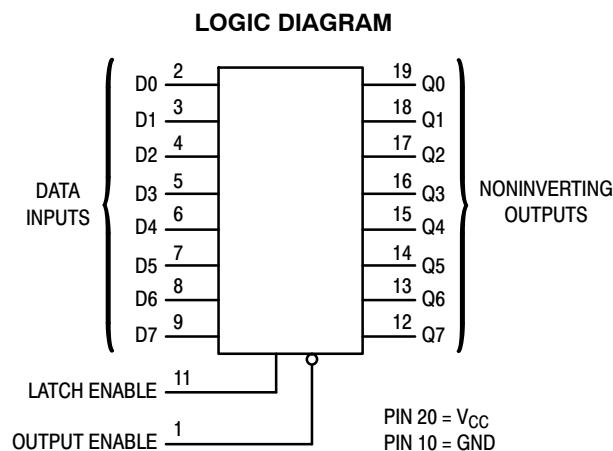
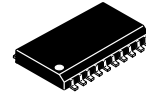


Figure 1. Logic Diagram

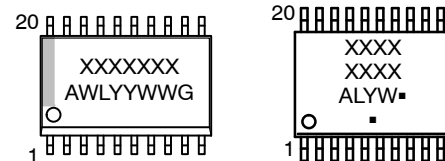


SOIC-20
DW SUFFIX
CASE 751D



TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAMS



SOIC-20

TSSOP-20

XXXXXXXX = Specific Device Code

A = Assembly Location

WL, L = Wafer Lot

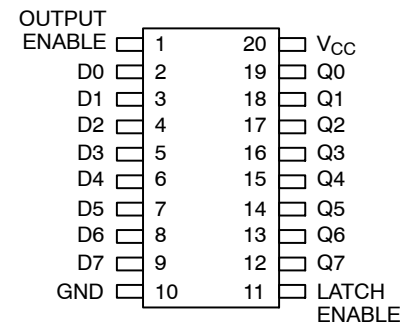
YY, Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care

Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

MC74HC573A, MC74HCT573A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_{IN}	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
I_{IK}	Input Clamp Current ($V_{IN} < 0$ or $V_{IN} > V_{CC}$)	± 20	mA
I_{OK}	Output Clamp Current ($V_{OUT} < 0$ or $V_{OUT} > V_{CC}$)	± 20	mA
T_{STG}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	± 150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC-20W WQFN20 QFN20 TSSOP-20	96 99 111 150 °C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC-20W WQFN20 QFN20 TSSOP-20	1302 1256 1127 833 mW
MSL	Moisture Sensitivity	SOIC-20W All Other Packages	Level 3 Level 1 -
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in -
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	>2000 N/A V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
--------	-----------	-----	-----	------

MC74HC

V_{CC}	DC Supply Voltage	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 3)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Time	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 1000 500 400	ns

MC74HCT

V_{CC}	DC Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 3)	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
t_r, t_f	Input Rise or Fall Time	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.



MC74HC573A, MC74HCT573A

DC ELECTRICAL CHARACTERISTICS (MC74HC573A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25 °C	≤ 85 °C	≤ 125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	
		I _{OUT} ≤ 2.4 mA I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V _{OL}	Minimum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					V
		I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	
		I _{OUT} ≤ 2.4 mA I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High Impedance; V _{IN} = V _{IH} or V _{IL} ; V _{OUT} = V _{CC} or GND	6.0	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND	6.0	4.0	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



MC74HC573A, MC74HCT573A

AC ELECTRICAL CHARACTERISTICS (MC74HC573A) (See Figures 2 and 3)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55 to 25 °C	≤ 85 °C	≤ 125 °C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	2.0	150	190	225	ns
		3.0	100	140	180	
		4.5	30	38	45	
		6.0	26	33	38	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q	2.0	160	200	240	ns
		3.0	105	145	190	
		4.5	32	40	48	
		6.0	27	34	41	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q	2.0	150	190	225	ns
		3.0	100	140	180	
		4.5	30	38	45	
		6.0	26	33	38	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q	2.0	150	190	225	ns
		3.0	100	140	180	
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output	2.0	60	75	90	ns
		3.0	23	27	32	
		4.5	12	15	18	
		6.0	10	13	15	
C _{IN}	Maximum Input Capacitance	–	10	10	10	pF
C _{OUT}	Maximum Three-State Output Capacitance (Output in High Impedance State)	–	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 4)	5.0	Typical @ 25 °C	pF
			23	

4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f + I_{CC} \times V_{CC}$.

TIMING REQUIREMENTS (MC74HC573A) (See Figures 2 and 3)

Symbol	Parameter	V _{CC} (V)	Guaranteed Limit			Unit
			-55 to 25 °C	≤ 85 °C	≤ 125 °C	
t _{SU}	Minimum Setup Time, D to Latch Enable	2.0	50	65	75	ns
		3.0	40	50	60	
		4.5	10	13	15	
		6.0	9.0	11	13	
t _H	Minimum Hold Time, Latch Enable to D	2.0	5.0	5.0	5.0	ns
		3.0	5.0	5.0	5.0	
		4.5	5.0	5.0	5.0	
		6.0	5.0	5.0	5.0	
t _W	Minimum Pulse Width, Latch Enable	2.0	75	95	110	ns
		3.0	60	80	90	
		4.5	15	19	22	
		6.0	13	16	19	
t _r , t _f	Maximum Input Rise and Fall Times	2.0	1000	1000	1000	ns
		3.0	800	800	800	
		4.5	500	500	500	
		6.0	400	400	400	

MC74HC573A, MC74HCT573A

DC ELECTRICAL CHARACTERISTICS (MC74HCT573A)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55 to 25 °C	≤ 85 °C	≤ 125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} -0.1 V; I _{OUT} ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} -0.1 V; I _{OUT} ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} ;					V
		I _{OUT} ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	
		I _{OUT} ≤ 6.0 mA	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} ;					V
		I _{OUT} ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	
		I _{OUT} ≤ 6.0 mA	4.5	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High Impedance; V _{IN} = V _{IH} or V _{IL} ; V _{OUT} = V _{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND	5.5	4.0	40	160	μA

ΔI _{CC}	Additional Quiescent Supply Current (Note 5)	V _{IN} = 2.4 V, Any One Input; V _{IN} = V _{CC} or GND, Other Inputs; I _{OUT} = 0 μA	5.5	≥ -55 °C	25 °C to 125 °C	mA
				2.9	2.4	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Total Supply Current = I_{CC} + Σ ΔI_{CC}.



MC74HC573A, MC74HCT573A

AC ELECTRICAL CHARACTERISTICS (MC74HCT573A) (See Figures 2 and 3)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			–55 to 25 °C	≤ 85 °C	≤ 125 °C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, D to Q	4.5 – 5.5	30	38	45	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Enable to Q	4.5 – 5.5	30	38	45	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to Q ENABLE B to YB	4.5 – 5.5	28	35	42	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to Q ENABLE B to YB	4.5 – 5.5	28	35	42	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output	4.5 – 5.5	12	15	18	ns
C _{IN}	Maximum Input Capacitance	–	10	10	10	pF
C _{OUT}	Maximum Three-State Output Capacitance (Output in High Impedance State)	–	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Enabled Output) (Note 6)	5.0	Typical @ 25°C	pF
			48	

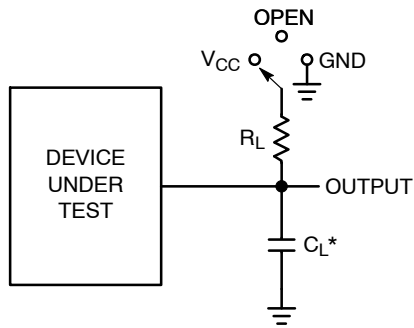
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f + I_{CC} \times V_{CC}$.

TIMING REQUIREMENTS (MC74HCT573A) (See Figures 2 and 3)

Symbol	Parameter	V _{CC} (V)	Guaranteed Limit			Unit
			–55 to 25 °C	≤ 85 °C	≤ 125 °C	
t _{SU}	Minimum Setup Time, D to Latch Enable	4.5 – 5.5	10	13	15	ns
t _H	Minimum Hold Time, Latch Enable to D	4.5 – 5.5	5.0	5.0	5.0	ns
t _W	Minimum Pulse Width, Latch Enable	4.5 – 5.5	15	19	22	ns
t _r , t _f	Maximum Input Rise and Fall Times	4.5 – 5.5	500	500	500	ns



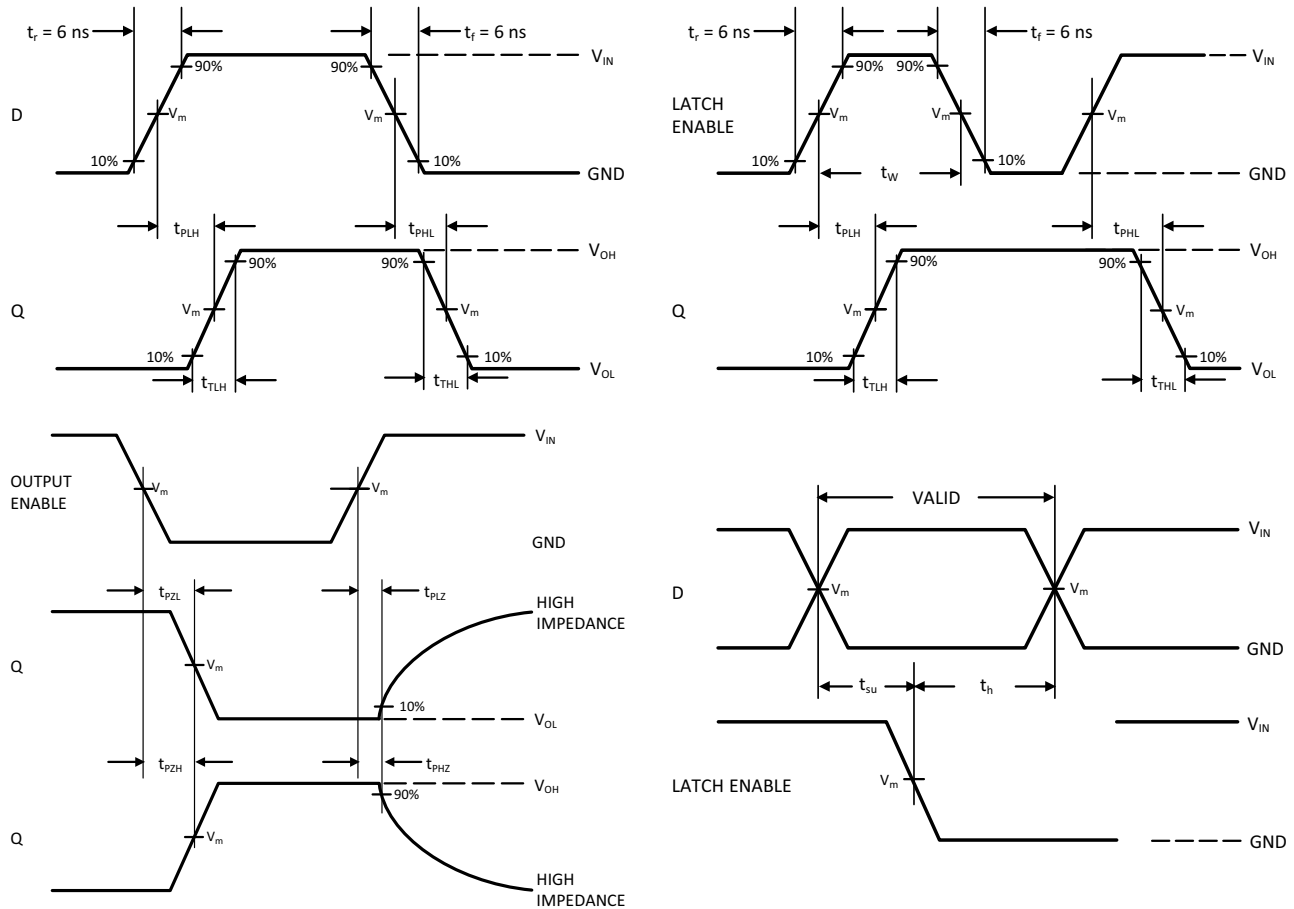
MC74HC573A, MC74HCT573A



*C_L Includes probe and jig capacitance

Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	50 pF	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 2. Test Circuit



Device	V _{IN} , V	V _m , V
MC74HC573A	V _{CC}	50% x V _{CC}
MC74HCT573A	3 V	1.3 V

Figure 3. Switching Waveforms

MC74HC573A, MC74HCT573A

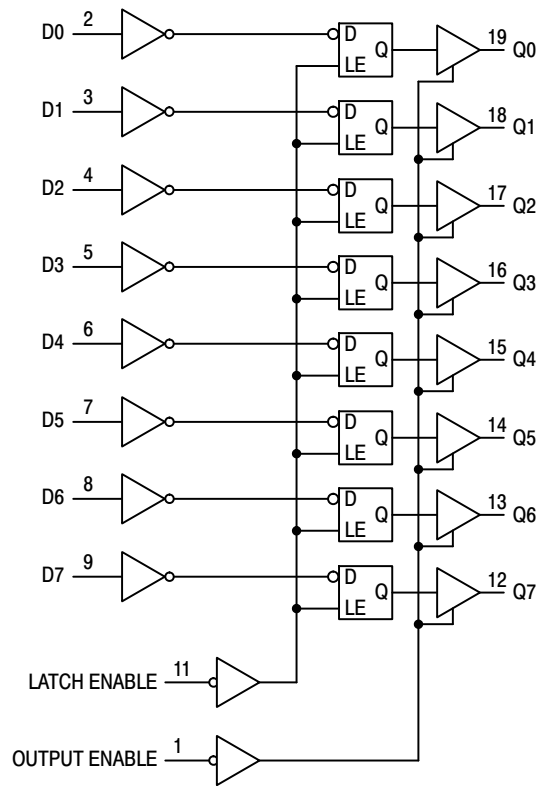


Figure 4. Expanded Logic Diagram

MC74HC573A, MC74HCT573A

ORDERING INFORMATION

Device	Package	Marking	Shipping†
MC74HC573ADWG	SOIC-20 Wide	HC573A	38 Units / Rail
MC74HC573ADWR2G	SOIC-20 Wide	HC573A	1000 / Tape & Reel
MC74HC573ADTG	TSSOP-20	HC 573A	75 Units / Rail
MC74HC573ADTR2G	TSSOP-20	HC 573A	2500 / Tape & Reel
MC74HC573ADTR2G-Q*	TSSOP-20	HC 573A	2500 Units / Tape & Reel
MC74HCT573ADWG	SOIC-20 Wide	HCT573A	38 Units / Rail
MC74HCT573ADWR2G	SOIC-20 Wide	HCT573A	1000 / Tape & Reel
MC74HCT573ADWR2G-Q*	SOIC-20 Wide	HCT573A	1000 / Tape & Reel
MC74HCT573ADTR2G	TSSOP-20	HCT 573A	2500 / Tape & Reel
MC74HCT573ADTR2G-Q*	TSSOP-20	HCT 573A	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

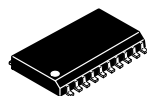
* -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

REVISION HISTORY

Revision	Description of Changes	Date
20	Added one new automotive OPN.	2/19/2026

* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

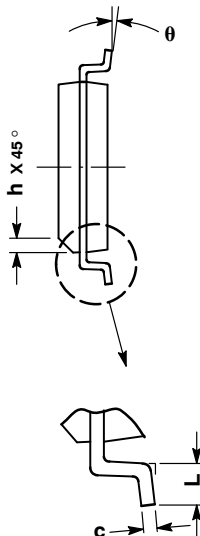
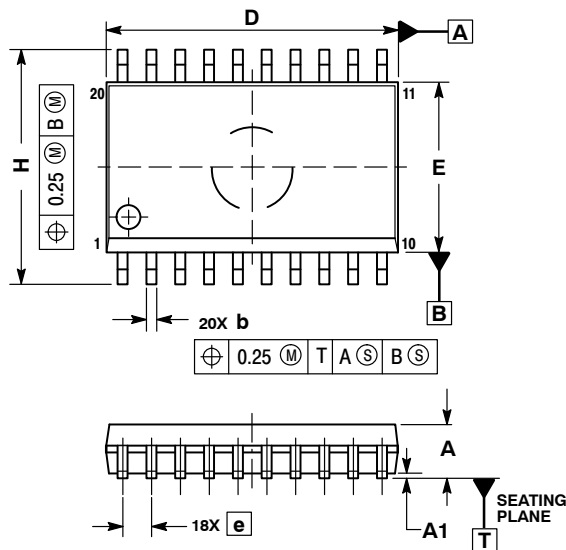




SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

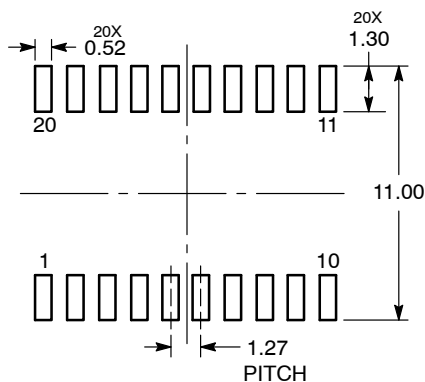


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

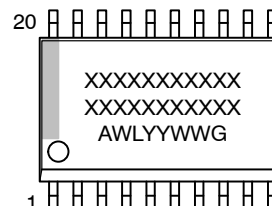
RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

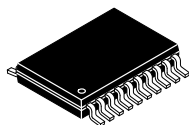


XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

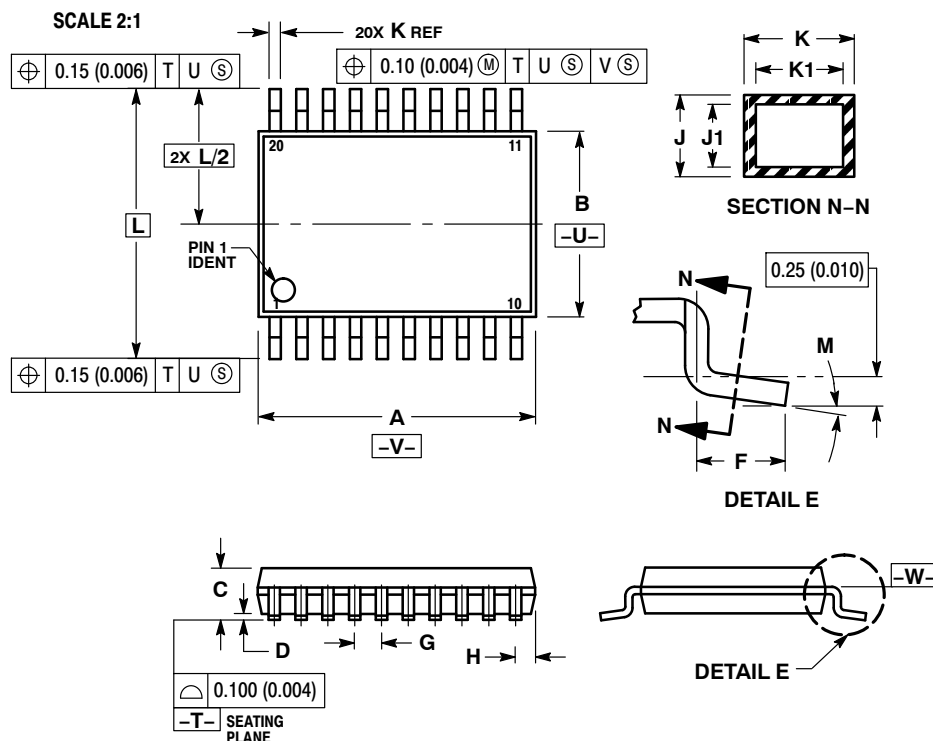
DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



TSSOP-20 WB
CASE 948E
ISSUE D

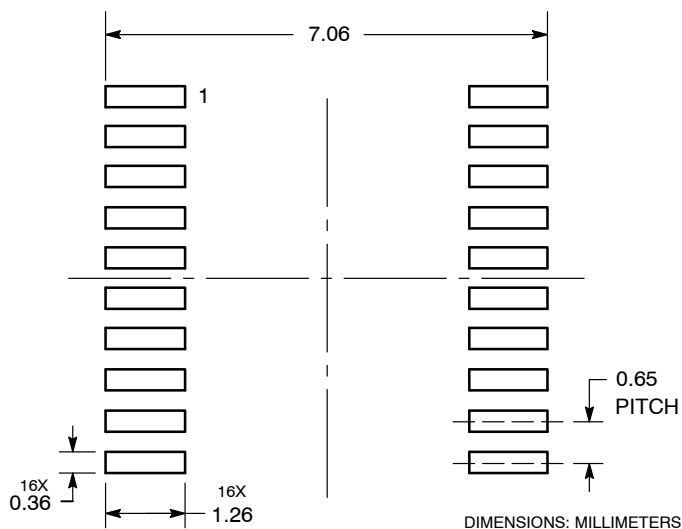
DATE 17 FEB 2016



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

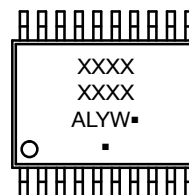
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual. SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-20 WB	PAGE 1 OF 1

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales