MC33907_08 safe system basis chip hardware design and product guidelines

Contents

1 Introduction

This application note provides design guidelines for integrating the MC33907_08 system basis chip (SBC) into automotive and industrial electronic systems. It shows how to optimize PCB layout and gives recommendations regarding external components.

To minimize the EMC impact from embedded DC/DC converters, pay attention to PCB component routing when designing with the MC33907_08.

2 Overview

The MC33907 and MC33908 are multi-output power supply integrated circuits dedicated to the automotive market. The MC33907_08 simplifies system implementation by providing ISO 26262 system solutions, documentation, and an optimized MCU interface, enabling customers to minimize the cost and complexity of their designs. The MCC33907_08's integral EMC and ESD protection also facilitates less complex system designs with increased functional reliability.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow integrating precision analog, power functions, and dense CMOS logic together on a single cost-effective die.

This application note applies to all MC33907_08 part numbers. Exceptions are specifically indicated.

2.1 Typical block diagram

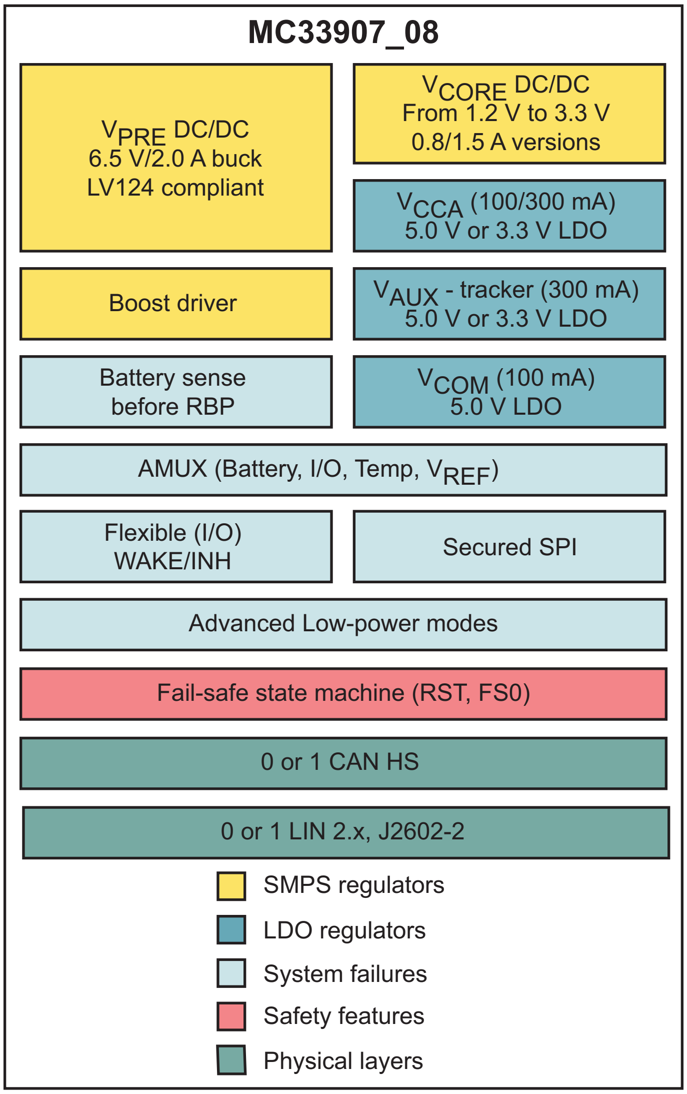


Figure 1. MC33907_08 block diagram

2.1.1 Key features

- Flexible DC/DC buck pre-regulator with optional boost to fit with LV124
- Efficient dual DC/DC converter topology
- Multiple supplies up to 1.5 A
- Ultra low-voltage operation down to 2.7 V
- Scalable family of products supporting a wide range of MCU and power segmentation architectures
- Analog multiplexer and battery sensing
- Low-power mode 32 μA
- Multiple wake-up sources in Low-power mode: CAN, LIN, IOs
- Secured SPI interface
- Robust High Speed CAN and LIN physical layers with superior EMI/ESD performance
- Independent fail-safe state machine monitoring safety critical parameters and supporting functional safety standards
- Fit for ASIL D safety requirements

2.1.2 Typical applications (automotive and industrial)

- Electrical power steering, engine/battery management
- Active suspension, gear box, transmission
- EV, HEV, inverter, ADAS
- Automation (PLC, robotics), medical (infusion pump, and stairs)
- Building control (lift), transportation (military, mobile machine)

2.2 Voltage regulators

2.2.1 V_{PRE} voltage pre-regulator (SMPS)

V_{PRE} is a flexible switched-mode power supply working in PWM at a fixed 440 kHz frequency. V_{PRE} is a current mode controlled SMPS, with a fully integrated compensation network. V_{PRE} can be configured in two topologies: non-inverting buck-boost or standard buck configuration. The output voltage is regulated at 6.5 V with 2.0 A current capability. V_{PRE} keeps power dissipation down and eliminates the need for bulky heat sinks compared to linear regulators for a wide input supply range from 2.7 V to 40 V.

2.2.2 V_{CORE} voltage regulator (SMPS)

V_{CORE} is a step-down switched-mode converter working in PWM at a fixed 2.4 MHz frequency. V_{CORE} is a voltage mode controlled SMPS, with an external compensation network.The output voltage can be configured from a 1.2 V to 3.3 V range, with an external resistor bridge (a maximum of 1% accuracy resistors are recommended) connected between V_{CORE} and the FB_CORE pin. The V_{CORE} output voltage accuracy is ±2.0% with a 0.8 A current capability for the MC33907 and 1.5 A for the MC33908.

2.2.3 V_{CCA} voltage regulator (LDO)

V_{CCA} is a linear voltage regulator mainly dedicated to supplying the MCU I/Os, especially the ADC reference voltage. The output voltage is selectable at 5.0 V or 3.3 V due to the resistor value connected to the SELECT pin. The V_{CCA} output voltage accuracy is ±1.0% for a 5.0 V configuration and ±1.5% for a 3.3 V configuration, with an output current capability of 100 mA. An external PNP transistor can be used to boost the current capability up to 300 mA with a ±3.0% output voltage accuracy.

2.2.4 V_{AUX} voltage regulator (LDO)

V_{AUX} is an auxiliary voltage regulator mainly dedicated to suppling additional devices in the ECU, additional MCU I/Os, or sensors outside the ECU. The external PNP is mandatory. V_{AUX} is protected against short to battery for up to 40 V. The output voltage is selectable at 5.0 V or 3.3 V due to the resistor value connected to the SELECT pin. V_{AUX} output voltage accuracy is ±3.0% with an output current capability of 300 mA. V_{AUX} can be configured as a tracker of V_{CCA} with a ±15 mV accuracy, when V_{AUX} is supplying a sensor and V_{CCA} the reference of the ADC, converting the sensor data to do ratio metric conversions.

If V_{AUX} is shorted to GND or the battery during the automatic built in self test (ABIST), either an undervoltage or an overvoltage condition is detected and the test fails. A failed ABIST inhibits the release of the RSTB pin. After eight seconds, the device goes to deep fail-safe state.

2.2.5 CAN_5V voltage regulator

CAN_5V is a linear voltage regulator dedicated to the embedded HSCAN interface. If the internal CAN transceiver is not used in the application, the CAN_5V regulator can be used to supply an external standalone CAN or FLEX-RAY transceiver.

2.2.6 Regulators restart condition after LPOFF

Conditions:

- Regulator shutdown by the SPI before entering into LPOFF (valid for all regulators)
- Regulator shutdown by ILIM detection (valid for V_{AUX} and V_{CCA} with PNP, because they are shutdown after T_ILIM to protect external PNP)

MC33097AE, MC33908AE behavior:

- If the device goes to LPOFF with a regulator shutdown from the previous condition, the regulator does not restart automatically after a wake-up from LPOFF, ABIST fails, Reset remains asserted low and the device moves to deep fail-safe state after 8.0 s.

MC33907NAE, MC33907LAE, MC33908NAE, MC33908LAE behavior:

- If the device goes to LPOFF with a regulator shutdown from the previous condition, the regulator restarts automatically after a wake-up from LPOFF, ABIST passes and reset is released.

2.3 Built-in CAN transceiver

Available on all MC33907_08 part numbers, the built-in high-speed CAN interface meets the ISO11898-2 and -5 standards. Local and bus failure diagnostics, protection, and fail-safe operation modes are provided. The high speed CAN exhibits wake-up capability with a very low-current consumption. The CAN transceiver integrated inside the MC33907 and MC33908 is compliant with the various OEM EMC requirements available in automotive market (see Section 9. Physical layers certifications, page 41).

2.4 Built-in LIN transceiver

Available on MC33907LAE and MC33908LAE part numbers only, the built-in LIN interface is compatible with the LIN protocol specification 1.3, 2.0, 2.1, 2.2, and SAEJ2602-2. Local and bus failure diagnostics, protection, and fail-safe operation modes are provided. The LIN exhibits wake-up capability with a very low current consumption.

2.5 Analog multiplexer

The analog multiplexer allows multiplexing of the following voltages to be output from the MC33907_08 and connected to one of the MCU ADC channels. The MCU can use the information for monitoring purposes (refer to the device datasheet for more details):

- 2.5 V internal reference voltage with a ±1.0% accuracy
- Battery sense
- Analog inputs IO_0 and IO_1
- Die temperature T(°C) = (V_{AMUX} - V_{AMUX_TP}) / $V_{AMUX\_TP\_CO}$ + 165

A serial resistor can be added to filter the MUX_out pin before the MCU ADC input. This resistor is not mandatory, and depends on the application need and PCB layout performances. If a resistor is added, the MUX_out time constant is longer.

2.6 Configurable I/Os

The MC33907_08 includes six multi-purpose I/Os. IO_0/1/4/5 are global pins and can be connected outside the ECU. They are load dump proof and robust against ISO7637 pulses with a serial resistor to limit the current during the high transient pulse on the line. IO_2/3 are local pins and must be connected inside the ECU.

2.7 Safety outputs

The MC33907_08 has two safety outputs RSTB and FS0B. The RSTB pin is intended to be connected to the MCU reset pin. The FS0B pin is intended to take remedial action (i.e disable actuators) after any critical fault detection within the system fault interval time (FTTI). Both safety outputs are active low. (Refer to MC33907_8NLSMUG “Safety Manual for MC33907 and MC33908”, see Section 10. References, page 44).

2.8 Fail-safe machine

To fulfill the safety-critical applications, a dedicated fail-safe machine (FSM) is provided. The FSM is composed of three main sub-blocks:

- Voltage supervisors
- Fail-safe output driver (FSO)
- Built-in self test (BIST)

The FSM is independent from the rest of the circuitry to avoid common cause failure. The FSM has its own voltage regulators (analog and digital), dedicated bandgap, and oscillator. This block is physically independent from the rest of the circuitry by doing dedicated layout placement and trench isolation.

2.9 Low-power mode OFF

In Low-power mode OFF (LPOFF), all the voltage regulators are turned off. Only V_{PRE} is turned ON when $V_{SUP} < V_{SUP\_UV\_7}$ for availability reasons. The MCU connected to V_{CORE} is not supplied. The MC33907_08 configuration monitors external events to wake-up and leave the LPOFF mode. Wake-up events can be generated via the CAN interface, LIN interface or I/O inputs. A wake-up event triggers the regulators to turn on.

After wake-up from LPOFF, it is recommended to read the reset error counter and decrement it to an appropriate value by several consecutive good watchdog refreshes before a reset request by the SPI. The number of watchdog refreshes needed (N) depends on the reset error counter value (RSTB_err_2:0) and the WD refresh counter (WD_refresh_2:0) setup during INIT phase.
N = RSTB_err_2:0 x (WD_refresh_2:0 + 1) to decrement the counter to “0”.

2.10 Watchdog

The Watchdog is managed by the fail-safe part of the device. Consequently the watchdog timings are derived from the fail-safe clock, running at 450 kHz, with ±10% accuracy.

2.11 Simplified internal power tree

Figure 2 describes a simplified internal power tree to help understand basic concept between the main and the Fail-safe part of the device.

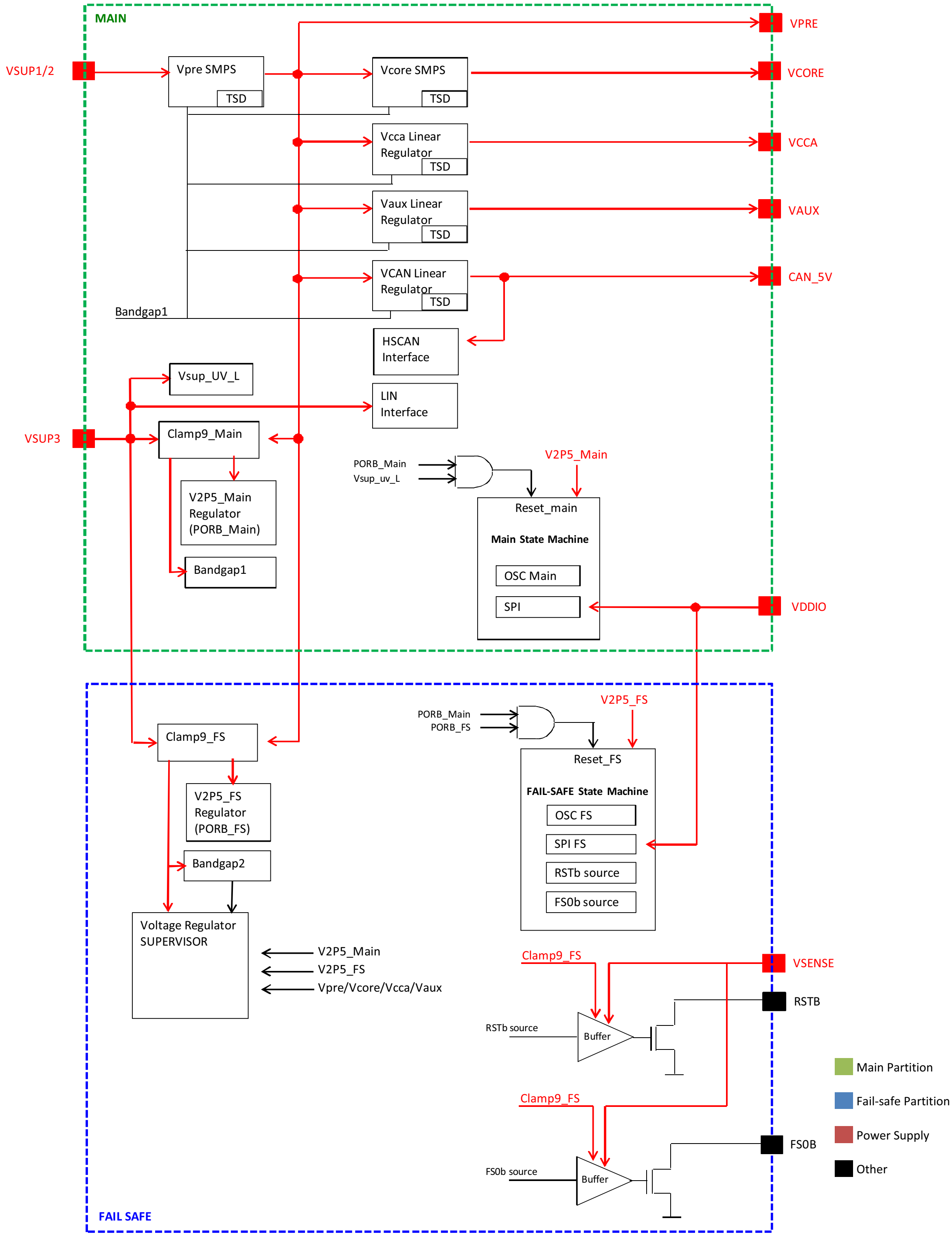


Figure 2. Simplified internal power tree

3 Application schematic

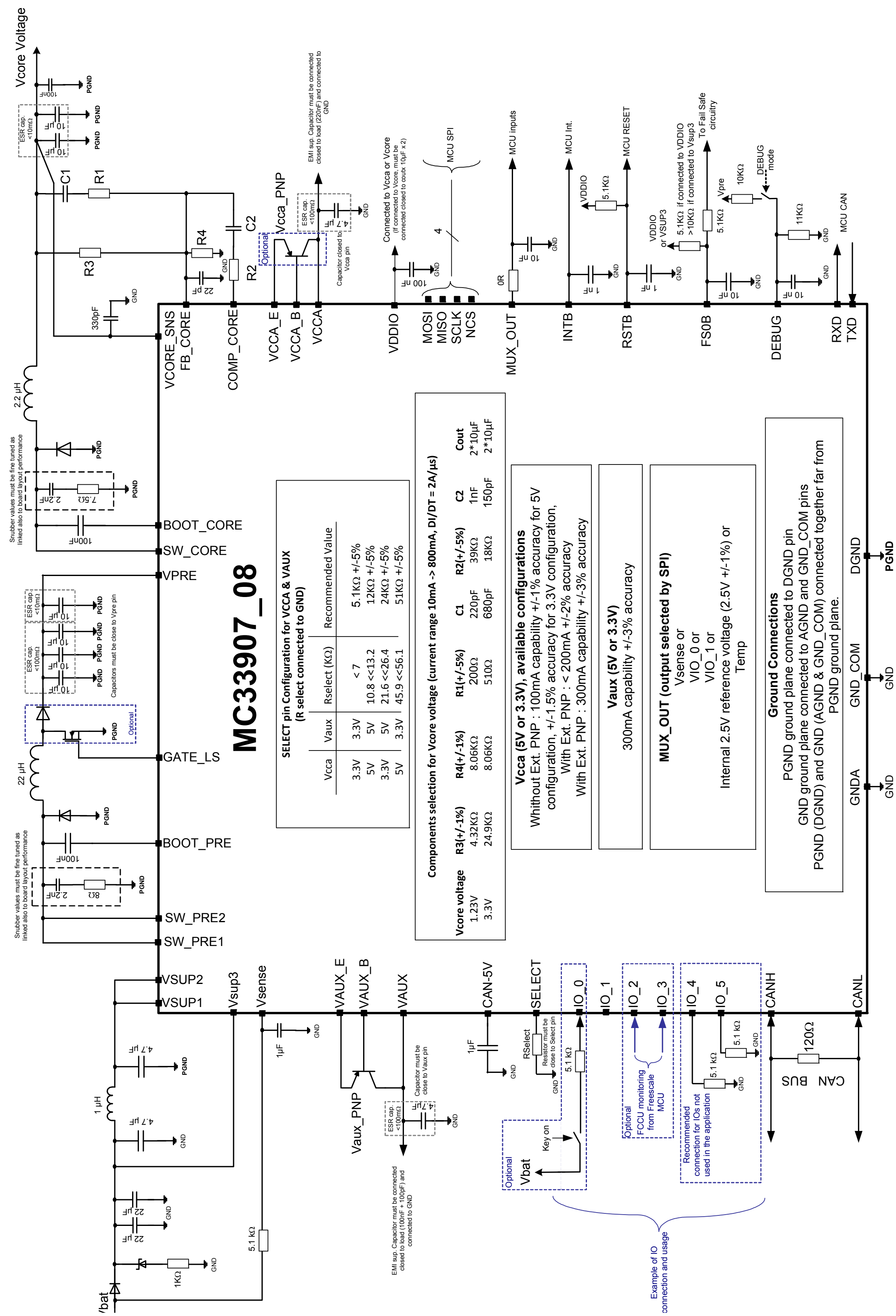


Figure 3. Application schematic

4 Optional configurations

According to customer application needs, optional configurations for the MC33907_08 are described by the following sections.

4.1 Pre-regulator, buck or buck-boost configuration

Two topologies are available on the MC33907_08 for the V_{PRE} pre-regulator. The MC33907_08 can be configured in buck only or buck-boost converter mode according to the GATE_LS pin connection. The detection is done automatically during the startup sequence, from power on reset or after each wake-up from LPOFF.

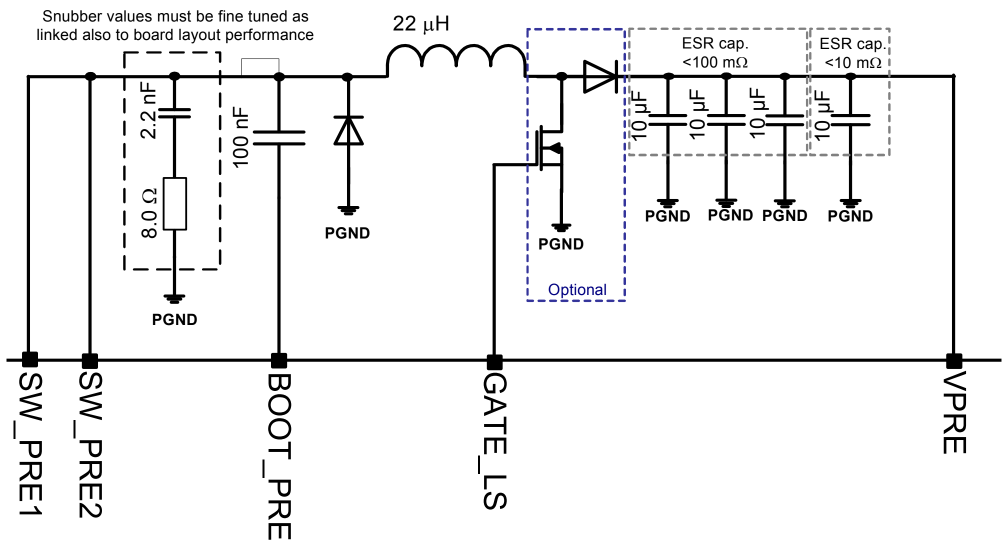


Figure 4. Buck-boost configuration

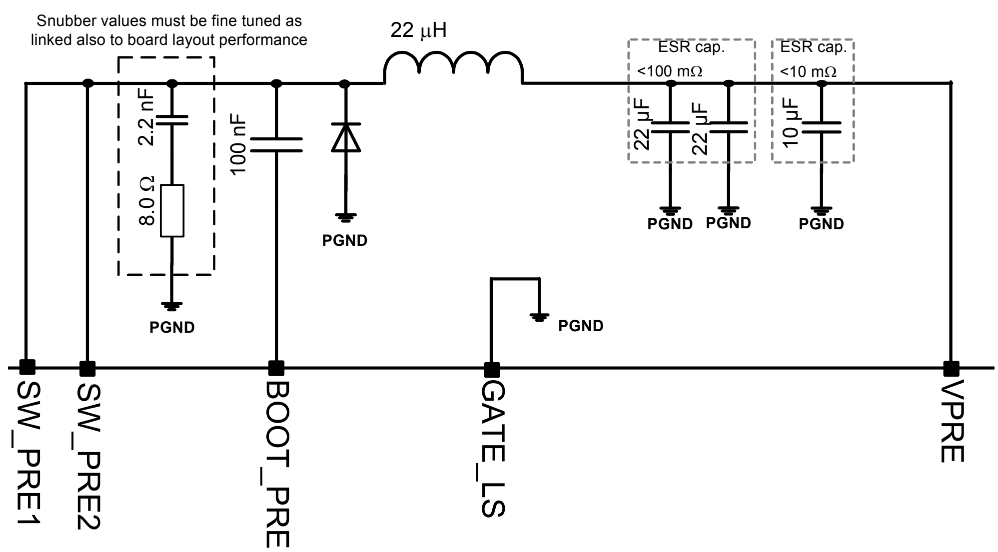


Figure 5. Buck configuration

In buck only configuration, the external low-side MOS and the diode are removed, and the Gate_LS pin must be connected to ground (PGND or GND).

4.2 V_{CCA}, current capability

To increase the current capability from 100 mA to 300 mA on the V_{CCA} linear regulator, an external PNP transistor must be connected. Using an external PNP increases the current capability and reduces the accuracy from ±1.0% at 100 mA to ±3.0% at 300 mA.

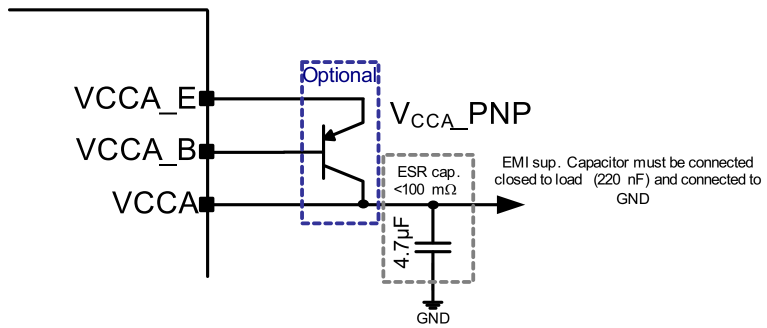


Figure 6. V_{CCA} current capability 300 mA, ±3.0% accuracy

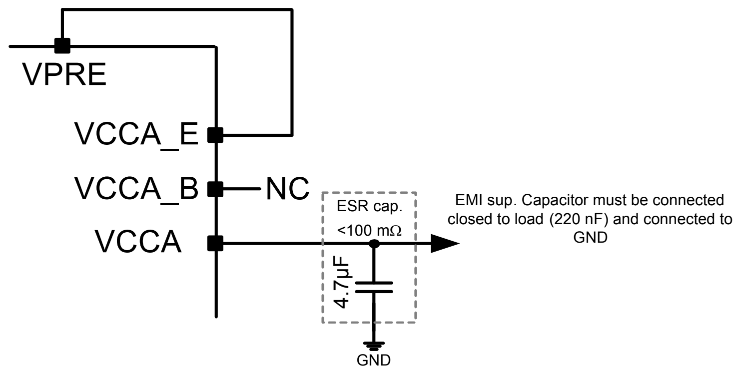


Figure 7. V_{CCA} current capability 100 mA, ±1.5% (3.3 V), ±1.0% (5.0 V)

When no external PNP is connected to V_{CCA}, the VCCA_E pin must be connected to the VPRE pin.

4.3 V_{AUX}

Depending on application needs, the auxiliary regulator can be used. The following figures show the correct connections of V_{AUX} in both cases. The external PNP is mandatory.

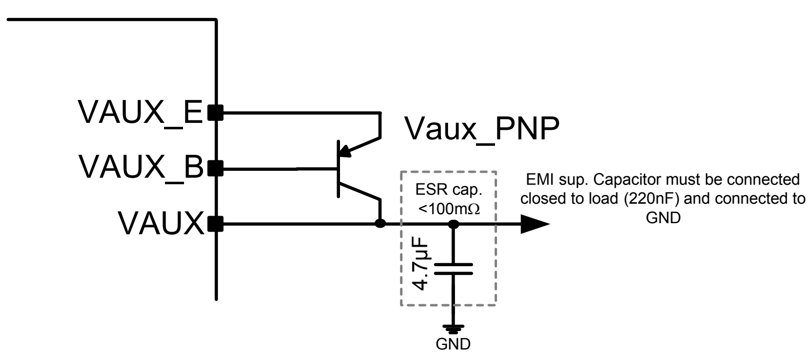


Figure 8. V_{AUX} current capability 300 mA, ±3.0% accuracy

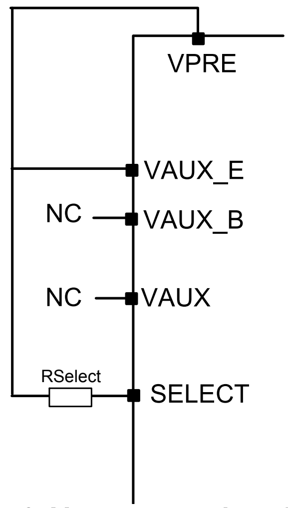


Figure 9. V_{AUX} connections if not used

When V_{AUX} is not used, the VAUX_E and SELECT pins must be connected to the VPRE pin.

4.4 IO_0 ignition connection

In automotive applications, it is recommended to connect IO_0 to ignition to be able to recover from deep fail-safe state by a key OFF, Key ON action.

4.5 IO_1 FB_CORE monitoring

When the application targets the ISO26262 ASIL D safety level, it is recommended to monitor the V_{CORE} output voltage through IO_1. In this case, a second resistor bridge is needed, which is a duplication of the R3/R4 external resistor bridge used to create V_{CORE} from FB_CORE. Available on MC33907NAE, MC33907LAE, MC33908NAE, and MC33908LAE part numbers only, refer to the MC33907_8NLSMUG safety manual for more information.

4.6 IO_2 and IO_3, FCCU monitoring

IO_2 and IO_3 can be configured as safety inputs to allow monitoring of the NXP microcontroller FCCU output pins FCCU_E[0] and FCCU_E[1].

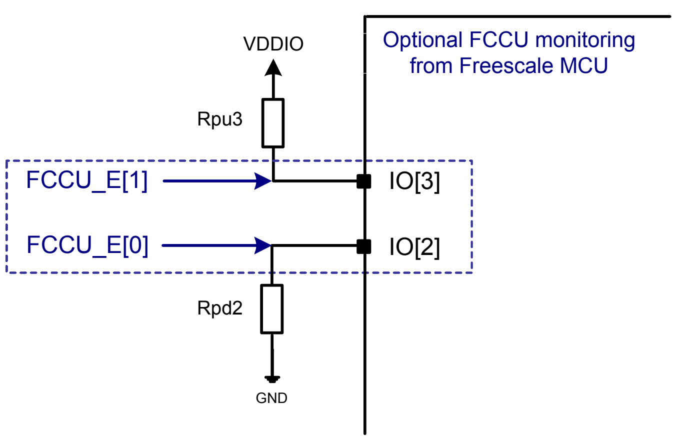


Figure 10. IO_2 and IO_3 configured as safety inputs

IO_2 should be connected to FCCU_EF[0] and IO_3 to FCCU_E[1]. A pull-up resistor must be connected to IO_3/FCCU_E[1] and a pull-down resistor to IO_2/FCCU_E[0]. Bi-stable protocol only from MCU is supported. (Refer to MC33907_8NLSMUG “Safety Manual for MC33907 and MC33908”, see Section 10. References, page 44). If not used, IO_2 and IO_3 can be left open or pulled down to GND.

5 MC33907_08 external components

This section is based on Figure 3, and details how to select the external components. It also proposes some references and tolerances needed to ensure optimal performance of the system. All the recommended components are based on NXP use case validations.

5.1 MC33907_08 power supply

Power to the MC33907_08 is provided by the VSUP1, VSUP2, and VSUP3 supply pins. An external reverse battery protection diode must be connected between the VBAT external battery input and the capacitor input filter.

A PI filter is implemented to avoid current switching noises coming from DC/DC converters to be propagated to VBAT and VSUP3 supplies. For that reason, VSUP3 must be connected before the PI filter to deliver a clean supply to the MC33907_08, de-correlated from the VSUP1 and VSUP2 dedicated to VPRE SMPS pre-regulator.

The total capacitor (C_{BAT1} + C_{BAT2}) between the VBAT and VSUP pins must be greater than 44 µF, to limit the slew rate on VSUP pins in case of a high transient. The resistor connected to VSENSE is mandatory to limit the current at the pin, in case of a high transient (positive and negative).

If the application has to sustain ISO pulses on VBAT in LPOFF mode, the connection of a an external zener diode (D_{IP}) and a serial resistor to the ground (R_{IP}) is needed to discharge the C_{BAT} capacitors.

If the application has to pass J2962 certification for the American automotive market, a ferrite bead (FB) on the V_{BAT} line is recommended to pass the radiated emission test.

The MC33907_08 power connection is shown in Figure 11.

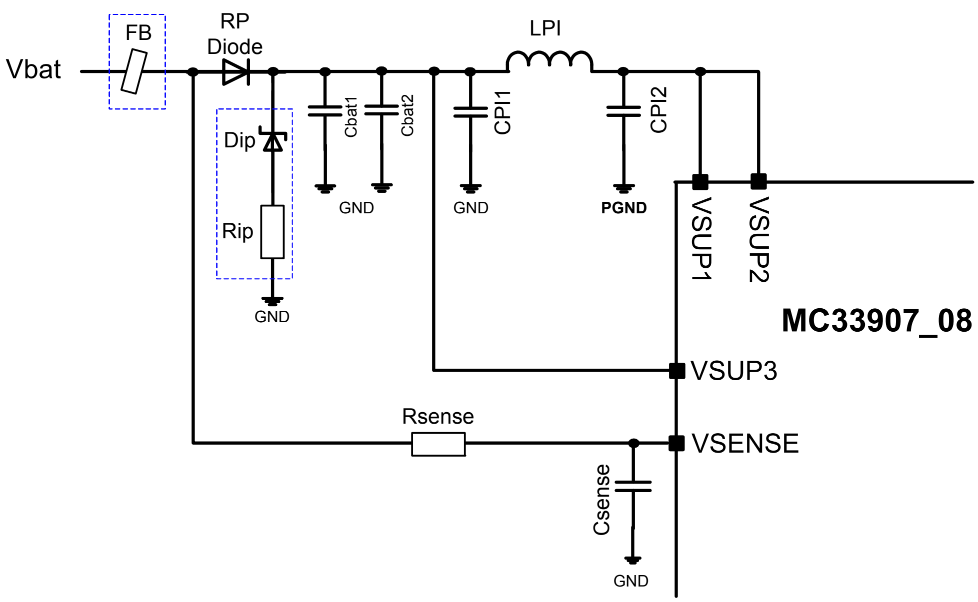


Figure 11. Power supply connection

The PI filter has a resonance frequency at $f\_res = \frac{1}{2\pi \times \sqrt{LPI \cdot CPI}}$ with a filtering slope at -40 dB per decade.

The pre-regulator V_{PRE} is the main contributor to the noise reported to V_{BAT}. The resonance frequency of the PI filter must be f_res < V_{PRE} switching frequency (f_res < F_{SWPRE} < 440 kHz). All MC33907_08 validations and EMC certifications have been successfully passed with LPI = 1.0 µH and CPI = 4.7 µF, giving a resonance frequency f_res = 73 kHz. The resonance frequency of the PI filter can be adjusted at the application level to improve EMC performances.

Table 1. Power supply component list

Component	Value	Reference/manufacturer proposal	Ground connection
FB		MPZ1608S101ATAH0/TDK	
RP Diode		MBR5H100MFS/On Semiconductor (I_F=5A, V_R=100V) PMEG10030ELP/NXP (I_F=3A, V_R=100V) PMEG10020ELP/NXP (I_F=2A, V_R=100V) PMEG10010ELR/NXP (I_F=1A, V_R=100V) SBRS81100T3G/On Semiconductor (I_F=2A, V_R=100V)	
Dip	Zener 30 V	BZX384C/NXP	
Rip	1.0 kΩ		GND
Cbat1	22 µF		GND
Cbat2	22 µF		GND
CPI1	4.7 µF	GCM32ER71H475K/Murata	GND
LPI	1.0 µH	B82472G6102M000/TDK-EPCOS	
CPI2	4.7 µF	GCM32ER71H475K/Murata	PGND
Rsense	5.1 kΩ		
Csense	1.0 µF	CGA5L3X7R1H105K/Murata	GND

5.2 MC33907_08 V_{PRE} pre-regulator

The pre-regulator V_{PRE} delivers a 6.5 V typical output voltage.

- In buck only configuration, the Gate_LS pin must be tied to PGND or GND.
- In buck-boost configuration, an external logic level MOSFET (N-type) must be connected to the Gate_LS pin and an additional diode is needed, as shown in Figure 4.

The three capacitors in parallel (C_{OUT_VPRE1}, C_{OUT_VPRE2}, and C_{OUT_VPRE3}) can be replaced by two 22 µF in parallel, or even one 47 µF capacitor, but with always ESR < 100 mΩ. The pre-regulator connections are shown in Figure 12.

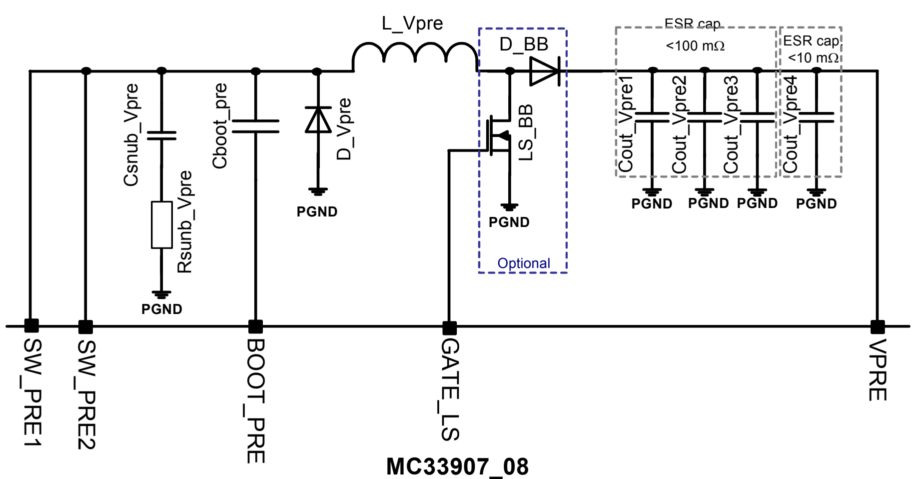


Figure 12. V_{PRE} connections

5.2.1 V_{PRE} main characteristics

- V_{SUPMAX} = 40 V
- V_{SUPMIN} = 2.7 V
- V_{PRE} = 6.5 V
- $V_{PRE\_MAXRATING}$ = 8.0 V
- I_{PREMAX} = 2.0 A
- I_{PREMIN} = 0.3 A (in boost mode when V_{SUP} < 4.0 V)
- F_{SWPRE} = 440 kHz

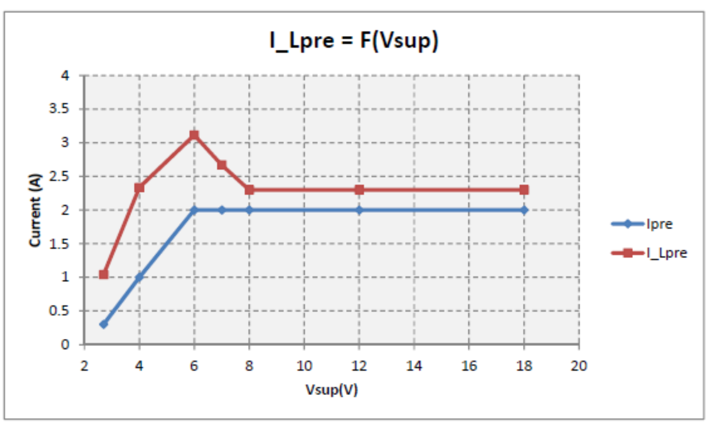
5.2.2 L_V_{PRE} calculation

- Inductor current ripple: I_{RIP} = K x I_{PREMAX} = 0.6 A with K = 0.3 (30% of I_{PRE})
- Buck configuration: $LVpre = \dfrac{(Vpre \times (Vsupmax - Vpre))}{K \times Vsupmax \times Ipremax \times Fswpre}$
- Boost configuration: $LVpre = \dfrac{(Vsupmin^2 \times (Vpre - Vsupmin))}{K \times Vpre^2 \times Ipremin \times Fswpre}$
- From calculation, L_V_{PRE} = 20.6 µH in buck mode and L_V_{PRE} = 16.6 µH in boost mode
- From normalized value, recommended L_V_{PRE} = 22 µH
- The current discharge slope in the inductor is $\dfrac{-Vpre}{LVpre}$. With V_{PRE} = 6.5 V and L_V_{PRE} = 22 µH, I_{SLOPE} = -300 mA/µs.
- V_{PRE} is a current mode controlled SMPS with a -500 mA/µs internal slope compensation to avoid sub-harmonic oscillations when the duty cycle is >50%. A minimum L_V_{PRE} must be chosen to maintain the current discharge slope in the inductor lower than the internal slope compensation.

5.2.3 L_V_{PRE} selection

- Must be shielded inductor
- Inductor value: 22 µH

Boost mode



Buck mode only

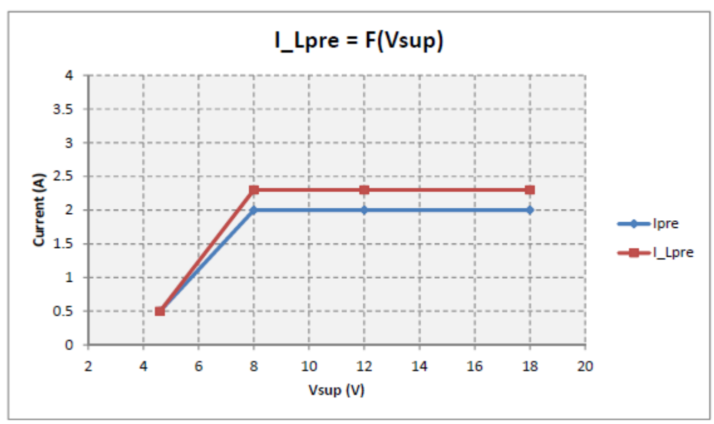


Figure 13. Peak current in the inductor

- Buck mode only:
  - — rated current: $I_R > I_{PREMAX} > 2.0$ A
  - — saturation current: $I_{SAT} > I_R + (I_{RIP}/2) > 2.3$ A
- Buck/boost mode (80% efficiency considered in boost mode):
  - — rated current: $I_R > I_{SUP} > 2.7$ A
  - — saturation current: $I_{SAT} > I_{SUP} + (I_{RIP}/2) > 3.1$ A
- Serial resistance: DCR < 100 mΩ

5.2.4 D_V_{PRE} selection:

- Schottky diode is recommended
  - – lower forward voltage drop (V_F) reduces power dissipation
  - – lower parasitic capacitor improves EMC performance
- Reverse voltage: $V_R \geq V_{SUPMAX} \geq 40$ V
- Average rectified forward current: $I_F > I_{PREMAX} + (I_{RIP}/2) > 2.3$ A
- Power dissipation: $P_D = V_F \times I_F$

5.2.5 LS_BB selection:

- Must be logic level N-type MOSFET
- Low $R_{DS(on)}$ reduces conduction losses
- Drain source voltage: $V_{DS} > V_{PRE\_MAXRATING} + V_{F(D\_BB)} > \sim 9.0$ V
- Drain current: $I_{DS} > I_{PREMAX} + (I_{RIP}/2) > 2.3$ A
- Gate source capacitance: $Cgs = \frac{(Iboost \times Trise)}{Vpre}$. With I_{BOOST} = 300 mA and T_{RISE} = 30 ns, C_{GS} = 1.5 nF

5.2.6 D_BB selection

- Schottky diode is recommended
  - – lower forward voltage drop (V_F) reduces power dissipation
  - – lower parasitic capacitor improves EMC performance
- Reverse voltage: $V_R \geq V_{PRE\_MAXRATING} \geq 8.0$ V
- Average rectified forward current: $I_F > I_{PREMAX} + (I_{RIP}/2) > 2.3$A
- Power dissipation: $P_D = V_F \times I_F$

5.2.7 Output capacitors

- 40 µF ceramic capacitor(s) with low ESR << 100 mΩ is recommended
- The ESR of the output capacitor is one of the main contributor to the output voltage ripple. The ripple generated by the ESR is proportional to its value (ESR * I_{RIP}). A high ripple can disturb the regulation loop.
- Low ESR capacitors reduces the ripple, avoid instability and lower EMI.

5.2.8 Snubber

In asynchronous SMPS, a freewheeling diode is used to discharge the inductor (during recirculation phase). When this diode is turned OFF (corresponding to when the MOS is turned ON), some oscillations happen due to the leakage inductance and output capacitance of the diode plus the PCB layout parasitics. A RC snubber in parallel to the diode dampens these oscillations and lower EMI (see the damping effect of a well designed snubber in Figure 14).

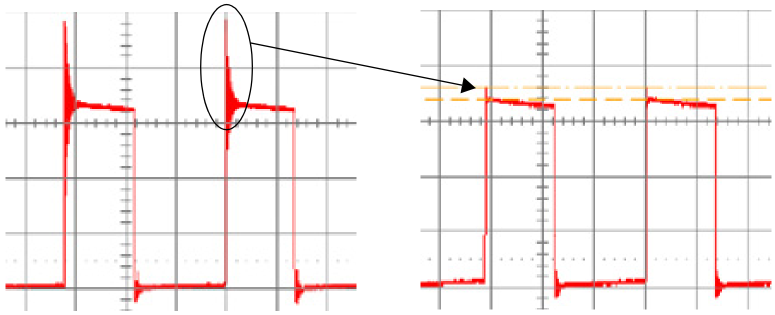


Figure 14. Snubber effect

- $\text{Fring} = \dfrac{1}{2\pi \times \sqrt{Lp \times Cp}}$ is the oscillation frequency where L_P and C_P are the parasitic inductor/capacitor mainly depending on the diode and the PCB layout.
- A good starting point to design the snubber is to take:
  - — C_P = diode output capacitance from diode datasheet
  - — C_{SNUB} = 5 x C_P
  - — Calculate L_P from Fring measured by oscilloscope
  - — $\text{Rsnub} = 1/2 \times \sqrt{(Lp)/(Cp)}$
- Try the snubber calculated values or try the values provided for V_{PRE} and V_{CORE} in this application note
- And adjust them experimentally to compensate the PCB layout parasitics.

5.2.9 V_{PRE} RC snubber

- RC snubber in parallel to the freewheeling diode D_V_{PRE} is recommended to dampen the voltage ringing at the SW_PRE pin and reduce high frequency emissions.
- C_{SNUB_VPRE} and R_{SNUB_VPRE} values must be tuned according to board and layout performance to take into account parasitic inductance/capacitance.
- The current pike in R_{SNUB_VPRE} at each V_{PRE} cycle is important. R_{SNUB_VPRE} resistor must be at least a 1/4 W resistor type for V_{SUPMAX} = 18 V. P(R_{SNUB_VPRE}) = 1/2 * C_{SNUB_VPRE} * ($V_P^2 + V_N^2$) * F_{SW} where V_P and V_N are the voltage levels (positive and negative) measured at the resistor R_{SNUB_VPRE} (see Figure 12).
- From Figure 15, P(R_{SNUB_VPRE}) = 1/2 * 4.7 nF * (14.7² + 3.6²) * 440 kHz = 0.237 W.

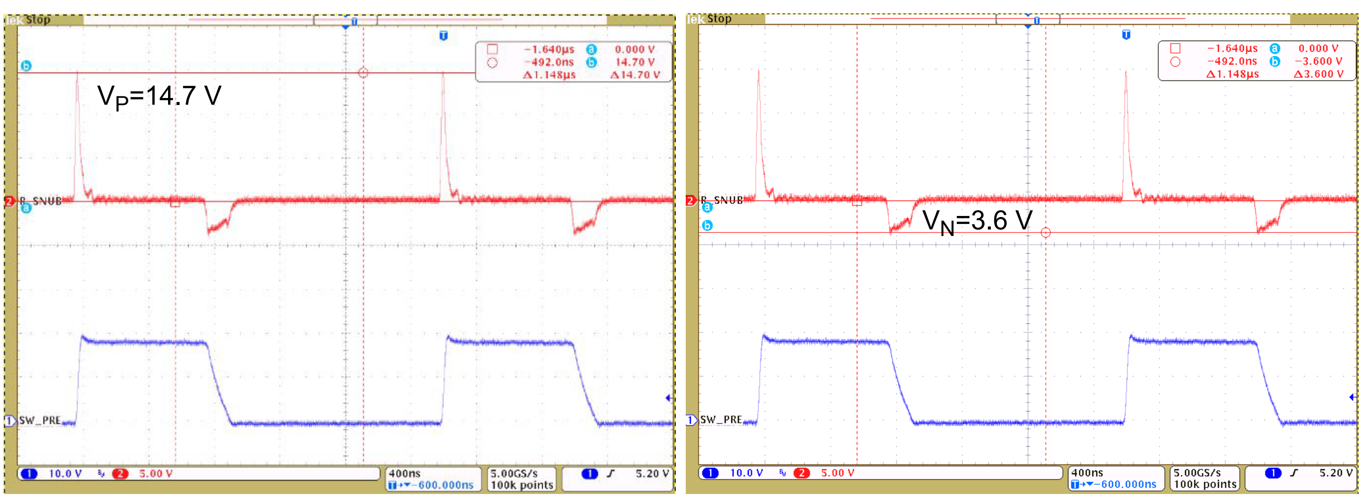


Figure 15. V_{PRE} R_{SNUB} V_P and V_N measurement at V_{SUP} = 18 V (on KIT33908AEEVBE)

5.2.10 Continuous mode

- V_{PRE} must work in continuous mode (current in the inductor always > 0) for a good stability and good EMC performances
- V_{PRE} is in continuous when I_{PRE} > 180 mA (for a 22 μH inductor)
- $I_{PRE} = I_{CCA} + I_{AUX} + I_{CAN} + (I_{CORE} * V_{CORE} / V_{PRE} / V_{CORE\_EFF})$ where V_{CORE_EFF} is V_{CORE} efficiency (~85% at 3.3 V and ~70% at 1.2 V)

5.2.11 V_{SUP} slow ramp up

The V_{PRE} pre-regulator is connected to V_{SUP}. Very slow V_{SUP} ramp up could influence the start-up of the pre-regulator in buck mode only. During the start-up phase in buck mode only, V_{PRE} follows V_{SUP} when $V_{SUP\_UV\_5} < V_{SUP} < 6.5$ V.

When $V_{PRE} > V_{PRE\_UV}$, all the regulators start (VCORE, VCCA, VAUX, and CAN_5V) and sink current from V_{SUP}, creating a voltage drop thru the reverse battery diode and the input filter.

V_{PRE} may decrease below V_{PRE_UV}, depending on application components and layout, and may take more than 8.0 s to recover, sending the device into deep fail-safe due to reset stuck during the > 8.0 s recovery.

In case the application must start with a very slow V_{SUP} ramp up down to 0.5 V/min, it is recommended to implement the boost mode of the pre-regulator V_{PRE}. In this case, V_{PRE} starts in boost mode when $V_{SUP} > V_{SUP\_UV\_5}$ and gives more room to V_{PRE_UV} when the regulators starts.

5.2.12 Component list proposal

Table 2. V_{PRE} supply component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{SNUB_VPRE}	2.2 nF		
R_{SNUB_VPRE}	8.0 Ω		PGND
C_{BOOT_PRE}	100 nF		
D_V_{PRE}		- MBRS340T3/ON Semiconductor (I_F = 3.0 A, V_R = 40 V) - SS24T3G/On Semiconductor (I_F = 2.0 A, V_R = 40 V) - PMEG4030EP/NXP (I_F = 3.0 A, V_R = 40 V) - PMEG4020EP/NXP (I_F = 2.0 A, V_R = 40 V)	PGND
L_V_{PRE}	22 μH	- B82479G1223M/TDK-EPCOS (I_R = 3.1 A, I_{SAT} = 6.0 A) - B82464G4223M/TDK-EPCOS (I_R = 2.25 A, I_{SAT} = 2.5 A) - MSS1278-223MLB/COILCRAFT (I_R = 4.0 A, I_{SAT} = 6.0 A)	(1)
LS_BB		- BUK9832-55A/NXP - BUK9M26-60E/NXP	PGND
D_BB		- MBRS340T3/ON Semiconductor (I_F = 3.0 A, V_R = 40 V) - SS24T3G/On Semiconductor (I_F = 2.0 A, V_R = 40 V) - PMEG4030EP/NXP (I_F = 3.0 A, V_R = 40 V) - PMEG4020EP/NXP (I_F = 2.0 A, V_R = 40 V)	
C_{OUT_VPRE1}	10 μF	Ceramic capacitor ESR<100 mΩ CGA6M3X7R1C106K/TDK	PGND
C_{OUT_VPRE2}	10 μF	Ceramic capacitor ESR<100 mΩ CGA6M3X7R1C106K/TDK	PGND
C_{OUT_VPRE3}	10 μF	Ceramic capacitor ESR < 100 mΩ CGA6M3X7R1C106K/TDK	PGND
C_{OUT_VPRE4}	10 μF	Ceramic capacitor ESR < 10 mΩ CGA6M3X7R1C106K/TDK	PGND

Notes:
1. In buck mode only configuration

5.3 MC33907_08 V_{CORE} supply regulator

The core supply regulator is configurable from 1.2 V to 3.3 V range and adjustable around these voltages with an external resistor bridge (R3 and R4). An external compensation network made of R1, C1, R2, and C2 is connected between VCORE_SNS, FB_CORE, and COMP_CORE to ensure a good stability of the closed loop. The core supply connections are shown in Figure 16.

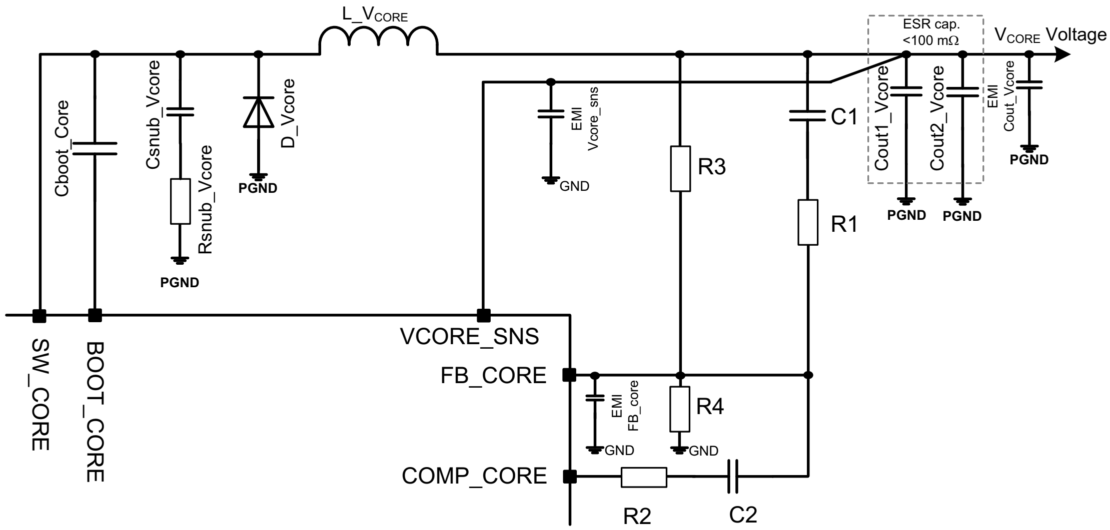


Figure 16. V_{CORE} connections

5.3.1 V_{CORE} main characteristics

- V_{PREMAX} = 7.0 V
- $V_{PRE\_MAXRATING}$ = 8.0 V
- $V_{COREMAX}$ = 3.3 V
- $I_{COREMAX}$ = 1.5 A for MC33908, $I_{COREMAX}$ = 0.8 A for MC33907
- F_{SWCORE} = 2.4 MHz

5.3.2 L_V_{CORE} calculation

- Inductor current ripple: I_{RIP} = K x $I_{COREMAX}$ = 0.45 A with K = 0.3 (30% of I_{CORE})
- Buck configuration: $LVcore = \frac{(Vcore \times (Vpremax - Vcore))}{K \times Vpremax \times Icoremax \times Fswcore}$
- From calculation, for V_{CORE} = 3.3 V/1.5 A, L_V_{CORE} = 1.62 µH
- From normalized value, recommended L_V_{CORE} = 2.2 µH

5.3.3 L_V_{CORE} selection

- Must be shielded inductor
- Inductor value: 2.2 µH
- Rated current: $I_R > I_{COREMAX}$ > 1.5 A
- Saturation current: $I_{SAT} > I_R + (I_{RIP}/2)$ > 1.73 A
- Serial resistance: DCR < 50 mΩ

5.3.4 D_V_{CORE} selection

- Schottky diode is recommended
  - lower forward voltage drop (V_F) reduces power dissipation
  - lower parasitic capacitor improves EMC performance
- Reverse voltage: $V_R \geq V_{PRE\_MAXRATING} \geq 8.0$ V
- Average rectified forward current: $I_F > I_{COREMAX} + (I_{RIP}/2) > 1.73$ A
- Power dissipation: $P_D = V_F \times I_F$

5.3.5 Output capacitors

- 20 µF ceramic capacitor(s) with low ESR << 100 mΩ is recommended for the MC33907.
- 40 µF ceramic capacitor(s) with low ESR << 100 mΩ is recommended for the MC33908.
- The ESR of the output capacitor is one of the main contributor to the output voltage ripple. The ripple generated by the ESR is proportional to its value (ESR * I_{RIP}). A high ripple can disturb the regulation loop.
- Low ESR capacitors reduces the ripple, avoid instability and lower EMI.

5.3.6 V_{CORE} RC snubber

- An RC snubber in parallel to the freewheeling diode D_V_{CORE} is recommended to dampen the voltage ringing at SW_CORE pin and reduce high frequency emissions.
- C_{SNUB_VCORE} and R_{SNUB_VCORE} values must be tuned according to board and layout performance to take parasitic inductance/capacitance into account.
- The current pike in R_{SNUB_VCORE} at each V_{CORE} cycle is important. The R_{SNUB_VCORE} resistor type must be at least 1/4 W. $P(R_{SNUB\_VCORE}) = 1/2 * C_{SNUB\_VCORE} * (V_P^2 + V_N^2) * F_{SW}$ where V_P and V_N are the voltage levels (positive and negative) measured at the resistor R_{SNUB_VCORE} (see Figure 16).

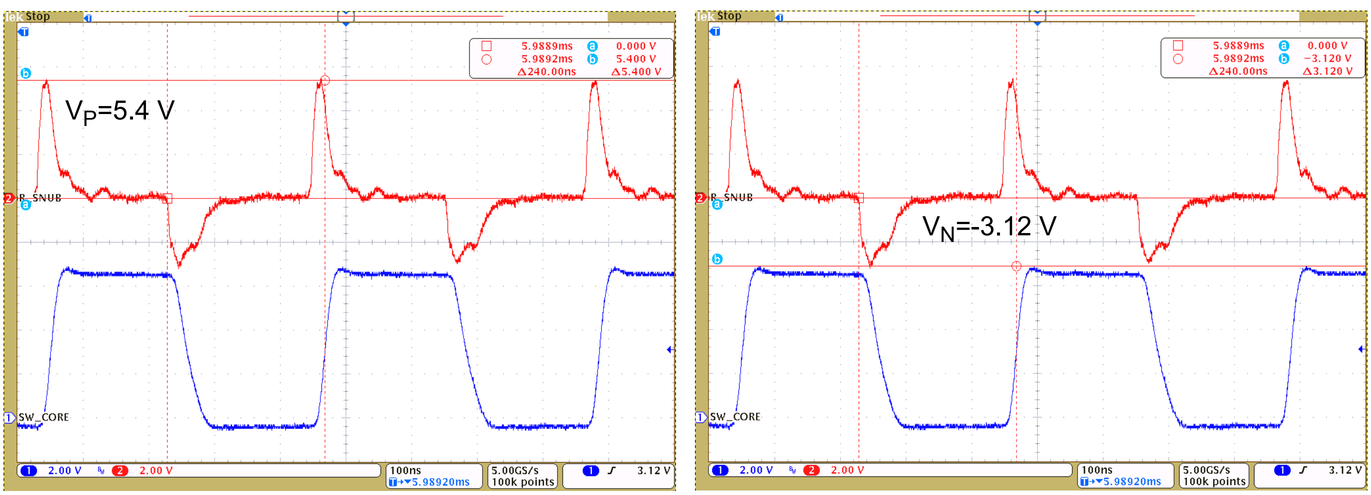


Figure 17. V_{CORE} R_{SNUB} V_P and V_N measurement (on KIT33908AEEVBE)

- From Figure 17, $P(R_{SNUB\_VPRE}) = 1/2 * 4.7\text{ nF} * (5.4^2 + 3.12^2) * 2.4\text{ MHz} = 0.219$ W.

5.3.7 Continuous mode

- V_{CORE} must work in continuous mode (current in the inductor always > 0) for a good stability and good EMC performances
- For V_{CORE} = 3.3 V configuration, V_{CORE} is in continuous when I_{CORE} > 160 mA (for a 2.2 µH inductor)
- For V_{CORE} = 1.2 V configuration, V_{CORE} is in continuous when I_{CORE} > 120 mA (for a 2.2 µH inductor)

5.3.8 Compensation network

V_{CORE} is a voltage mode buck converter with two poles and needs a compensation network which creates a large phase boost. Such amplifier circuit is called “type 3 amplifier compensation”. It gives a very good transient response to the circuit.

The compensation network connection is shown Figure 18 and the “AN4661: Designing the V_{CORE} compensation network” covers this subject in detail. In addition, a simulation tool is available to optimize IC performance for specific use cases.

The compensation network R1, C1, R2, and C2 is external to be flexible. It can be tuned to attach the MC33907_8 to a different MCU. Only C3, which is a very small capacitor value, is internal. A simulation tool, based on Matlab model, can be provided on demand to support optimized compensation network design.

Component values for VCORE 3.3 V and 1.2 V configurations are provided in the datasheet and in the Figure 3 application schematic.

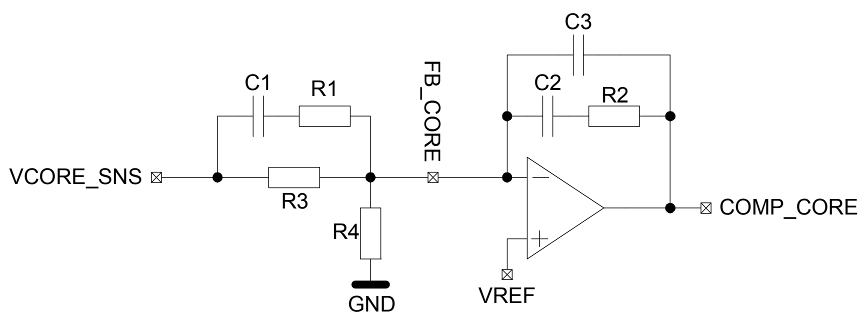


Figure 18. V_{CORE} compensation network

5.3.9 Component list proposal

Table 3. V_{CORE} supply component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{BOOT_CORE}	100 nF		
C_{SNUB_VCORE}	2.2 nF		
R_{SNUB_VCORE}	7.5 Ω		PGND
D_V_{CORE}		- SS22T3G/ON Semiconductor (I_F = 2.0 A, V_R = 20 V) - PMEG3020EH/NXP (I_F = 2.0 A, V_R = 30 V) - PMEG3020EP/NXP (I_F = 2.0 A, V_R = 30 V) - PMEG3020ER/NXP (I_F = 2.0 A, V_R = 30 V)	PGND
L_V_{CORE}	2.2 µH	B82472G6222M000/TDK-EPCOS	
R3	4.32 kΩ ±1%	Configuration for V_{CORE} = 1.23 V	
R4	8.06 kΩ ±1%		GND
R1	200 Ω ±5%	Current up to 800 mA	
C1	220 pF ±10%		
R2	39K Ω ±5%		
C2	1.0 nF ±10%		
R3	24.9 kΩ ±1%	Configuration for V_{CORE} = 3.3 V	
R4	8.06 kΩ ±1%		GND

Table 3. V_{CORE} supply component list (continued)

Component	Value	Reference/manufacturer proposal	Ground connection
R1	510 Ω	Current up to 800 mA	
C1	680 pF		
R2	18 kΩ		
C2	150 pF		
C_{OUT1_VCORE}	10 µF	Ceramic capacitor ESR < 100 mΩ GCM32ER71E106K/Murata	PGND
C_{OUT2_VCORE}	10 µF	Ceramic capacitor ESR < 100 mΩ GCM32ER71E106K/Murata	PGND [(2)]
EMI C_{OUT_VCORE}	100 nF		PGND
EMI V_{CORE_SNS}	330 pF		GND
EMI FB_C_{ORE}	22 pF		GND

Notes:
2. To improve emission performance, this output capacitor can be connected to GND, in case the V_{CORE} emission level is measured between VCORE and GND (global GND) and not PGND.

5.4 MC33907_08 linear regulators, V_{CCA} and V_{AUX}

The V_{CCA} and V_{AUX} regulators can deliver 3.3 V or 5.0 V independently, according to the resistor value connected on the SELECT pin. The detection of this resistor value is done during the start-up sequence and the regulators output voltage is automatically settle to their selected voltage value.

5.4.1 V_{CCA} with external PNP and V_{AUX} used

An external PNP can be connected to VCCA to increase its current capability from 100 mA (configuration with internal PMOS) to 300 mA (configuration with external PNP).

The VCCA with external PNP and VAUX connections are shown in Figure 19.

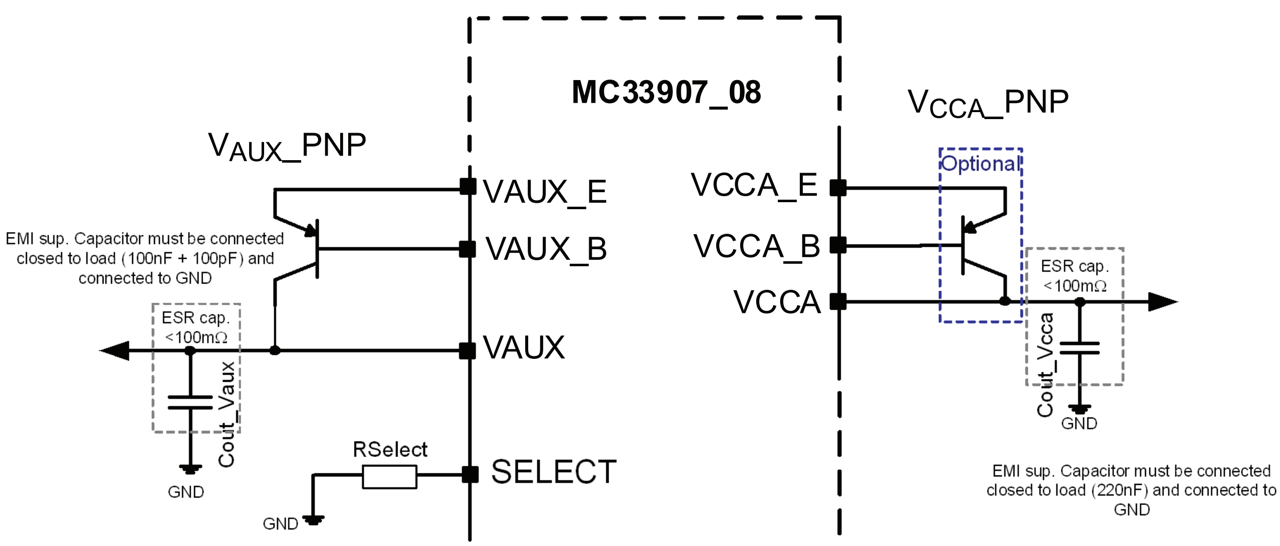


Figure 19. Linear regulator connection

5.4.2 PNP selection

- V_{CCA} PNP
  - Collector-Emitter voltage: VCE $\geq V_{PRE\_MAXRATING} \geq$ 8.0 V
  - Collector-Baser voltage: VCB $\geq V_{PRE\_MAXRATING} \geq$ 8.0 V
  - Collector current: IC $\geq I_{CCA\_LIM} \geq$ 675 mA
  - Current gain: 150 < HFE < 450
  - Power dissipation: Pd = $(V_{PRE} - V_{CCA}) * I_{CCA}$ = 1.0 W for V_{CCA} = 3.3 V/300 mA
- V_{AUX} PNP
  - Collector-Emitter voltage: VCE $\geq V_{SUPMAX} \geq$ 40 V
  - Collector-Baser voltage: VCB $\geq V_{SUPMAX} \geq$ 40 V
  - Collector current: IC $\geq I_{AUX\_LIM} \geq$ 700 mA
  - Current gain: 100< HFE < 450
  - Power dissipation: $P_D = (V_{PRE} - V_{AUX}) * I_{AUX}$ = 1.0 W for V_{AUX} = 3.3 V/300 mA

5.4.3 Reduce Vaux_PNP power dissipation

When V_{AUX} is used at 3.3 V and high current, the power dissipation in the external PNP can be reduced by adding a resistance in serial with the PNP collector, as shown in Figure 20. R_{AUX} reduces the drop in V_{AUX_PNP} and its power dissipation.

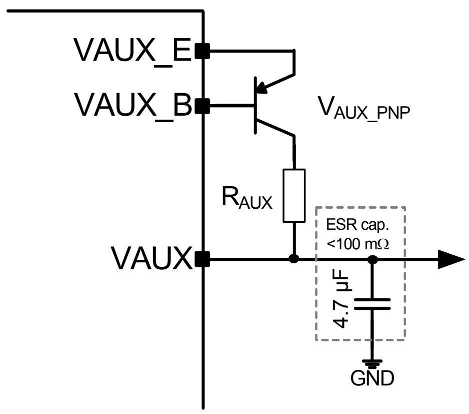


Figure 20. Reduce V_{AUX_PNP} power dissipation

V_{AUX_PNP} voltage drop must be > 1.5 V so R_{AUX} voltage drop must be less than $V_{PRE} - V_{AUX}$ - 1.5 V < 1.7 V. R_{AUX} must be < 4.0 Ω.

R_{AUX} value depends on I_{AUX} and P_{DIS_RAUX} to be balanced with $P_{DIS\_VAUX\_PNP}$.

- Without R_{AUX}:
  - $P_{DIS\_VAUX\_PNP} = (V_{PRE} - V_{AUX}) \times I_{AUX}$ = (6.5 V - 3.3 V) x 0.4 A = 1.3 W
- With R_{AUX} = 3.0 Ω:
  - $P_{DIS\_MAX} = (V_{PRE} - V_{AUX} - (R_{AUX} \times I_{AUX})) \times I_{AUX}$ = (6.5 V - 3.3 V - (3 x 0.4)) x 0.4 A = 0.8 W
  - $P_{DIS\_RAUX} = R_{AUX} \times I_{AUX}^2$ = 0.5 W

5.4.4 V_{AUX} supplying a sensor

When V_{AUX} is used to supply a sensor outside the ECU, this regulator can be shorted to GND or shorted to battery at start-up, in case of a sensor failure. During the start-up phase of the MC33907_08, a V_{AUX_UV} or V_{AUX_OV} is detected during the ABIST verification and the device does not release its RSTB pin, preventing the MCU to start and diagnose the failure. Moreover, if the failure is permanent, the MC33907_08 moves to deep fail safe state after 8 s and shuts down all the regulators, awaiting for IO_0 transition to recover.

To avoid this behavior, a switch controlled by the MCU can be inserted between V_{AUX} regulator and the Sensor input supply. This switch isolates V_{AUX} from the Sensor, allowing the MC33907_08 to pass the ABIST verification and release its RSTB pin even in the case of Sensor failure during the start up phase. The MCU starts and then closes the switch M1 before starting the application.

Figure 21 illustrates a generic switch connection to isolate V_{AUX} from the sensor input supply. Additional application specific components may be required. M1 can be replaced by a low VCEsat PNP transistor when MCU GPIO drives 3.3 V.

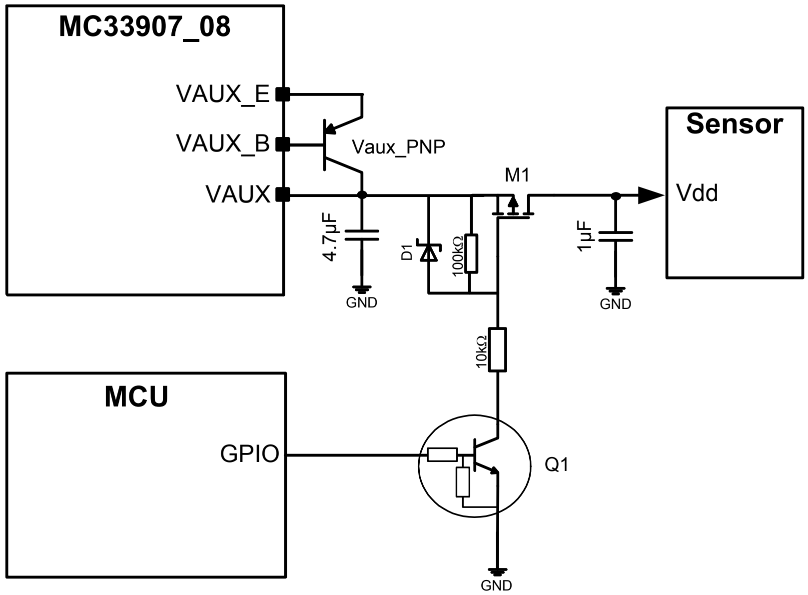


Figure 21. V_{AUX} sensor supply with switch isolation

5.4.5 Component list proposal

Table 4. Linear Regulator Component List

Component	Value	Reference/manufacturer proposal	Ground connection
V_{AUX_PNP}		- NJT4030P/ON Semiconductor - PBSS5350Z/NXP - PHPT60603PY/NXP	
C_{OUT_VAUX}	4.7 µF ±10%	Ceramic capacitor ESR < 100 mΩ GCM31CR71C475KA37 / Murata	GND
D1		BZX84-C10/NXP	
M1		- PMOS: PMV250EPEA/NXP - PNP: PBSS5260QA/NXP	
Q1		PBRN113ZT/NXP	GND
V_{CCA_PNP}		- NJT4030P/ON Semiconductor - PBSS5350Z/NXP - PHPT60603PY/NXP	
C_{OUT_VCCA}	4.7 µF ±10%	Ceramic capacitor ESR < 100 mΩ GCM31CR71C475KA37 / Murata	GND
Component	**Value**	**V_{AUX}/V_{CCA} voltage configuration**	
R_{SELECT}	5.1 kΩ ±5.0%	V_{CCA} = 3.3 V, V_{AUX} = 3.3 V	GND
R_{SELECT}	12 kΩ ±5.0%	V_{CCA} = 5.0 V, V_{AUX} = 5.0 V	GND
R_{SELECT}	24 kΩ ±5.0%	V_{CCA} = 3.3 V, V_{AUX} = 5.0 V	GND
R_{SELECT}	51 kΩ ±5.0%	V_{CCA} = 5 V, V_{AUX} = 3.3 V	GND
R_{SELECT}	Open	V_{CCA} = 3.3 V, V_{AUX} = 3.3 V	

5.4.6 V_{CCA} without external PNP and V_{AUX} not used

If V_{AUX} is not used in the application, the VAUX_E and RSELECT pins must be connected to the VPRE pin. The VAUX_B and VAUX pins can be left open. If V_{CCA} is used without the external PNP, the VCCA_E pin must be connected to the VPRE pin. VCCA_B pin can be left open. The V_{CCA} without an external PNP and V_{AUX} unused connections are shown in Figure 22.

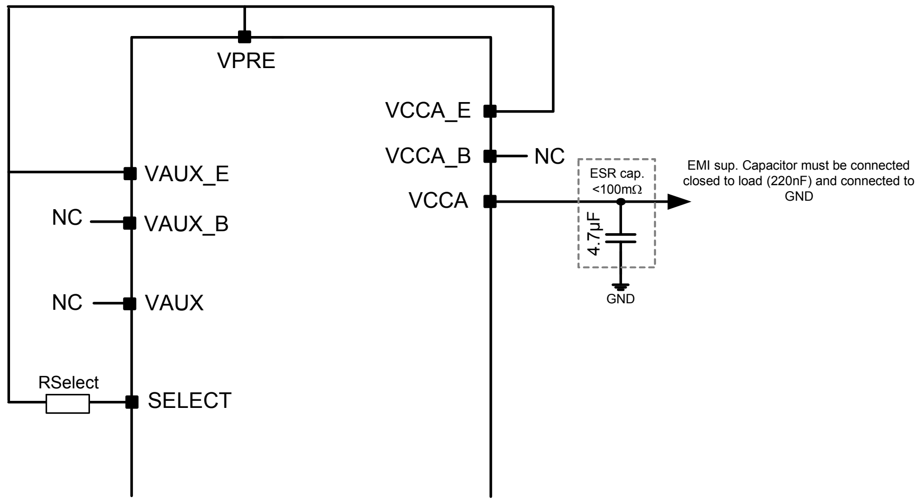


Figure 22. VAUX not used and VCCA w/o PNP

Table 5. RSelect component list

Component	Value	V_{CCA} voltage configuration	Ground connection
R_{SELECT}	5.1 kΩ ±1.0%	V_{CCA} = 3.3 V	GND
R_{SELECT}	12.1 kΩ ±1.0%	V_{CCA} = 5.0 V	GND
R_{SELECT}	24.9 kΩ ±1.0%	V_{CCA} = 5.0 V	GND
R_{SELECT}	51.1 kΩ ±1.0%	V_{CCA} = 5.0 V	GND
R_{SELECT}	Open	V_{CCA} = 3.3 V	

5.5 CAN_5V

CAN_5V is a regulator dedicated to the internal physical layer. An external capacitor is needed for filtering purposes, as shown in Figure 23

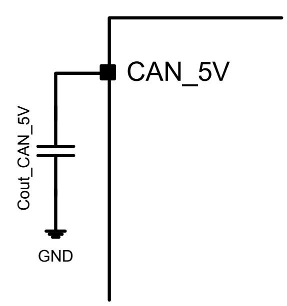


Figure 23. CAN_5V connection

Table 6. CAN_5V component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{OUT_VCAN}	1.0 µF	CGA4J2X7R1C105K / TDK	GND

5.6 Reset and fail-safe output, RSTB and FS0B

The RESET pin must be connected to the MCU reset pin. The MC33907_08 asserts RSTB low if a fault is reported. Refer to the datasheet for more information.

The FS0B pin is a safety output pin. In case of a major fault in the system, the MC33907_08 asserts FS0B low, disconnecting the critical functions in the application. FS0B is a global pin and can be connected outside the ECU. FS0B is load dump proof and robust against ISO7637 pulses with a serial resistor to limit the current during the high transient pulse on the line. RSTB and FS0B connections are shown in Figure 24.

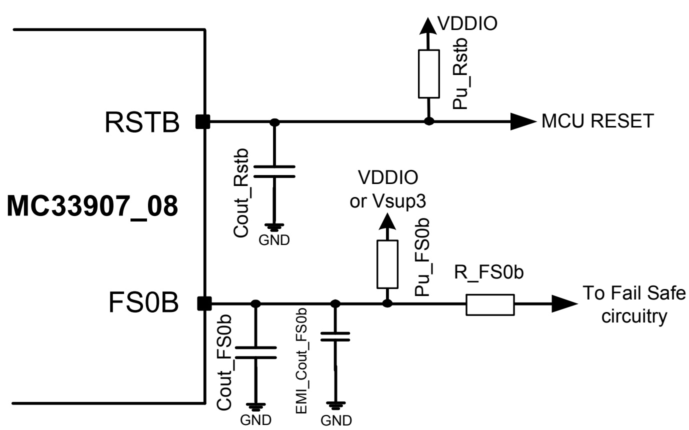


Figure 24. Reset and fail-safe output connections

If FS0B is not used in the application, it is recommended to pull down this pin to GND with an external 10 K resistor, to avoid unexpected FS0B failure detection during ABIST or when an application is running.

In LPOFF mode, RSTB and FS0B are asserted low. If the FS0B pull-up is connected to V_{SUP3}, expect some current through the pull-up resistor (V_{SUP3} / P_{U_FS0B}) in addition to the MC33907_8 LPOFF current (32 µA). This can be avoided by connecting the FS0B pull-up to V_{DDIO} which is OFF in LPOFF mode.

Table 7. Reset and fail-safe output component list

Component	Value	Ground connection
C_{OUT_RSTB}	1.0 nF	GND
P_{U_RSTB}	5.1 kΩ	
C_{OUT_FS0B}	10 nF	GND
R_{FS0B}	5.1 kΩ	
P_{U_FS0B} (if connected to VDDIO)	5.1 kΩ	
P_{U_FS0B} (if connected to VSUP3)	10 kΩ	

5.7 MC33907_08 debug pin

The connections shown in Figure 25 can be used to enter into debug mode on the MC33907_08. Debug mode allows the user to debug software with the MCU. The deep fail-safe (regulator OFF, RSTB, and FS0B asserted low) and the WD timeout are disabled (fail-safe state machine). The CAN and the LIN are in normal mode by default (main state machine).

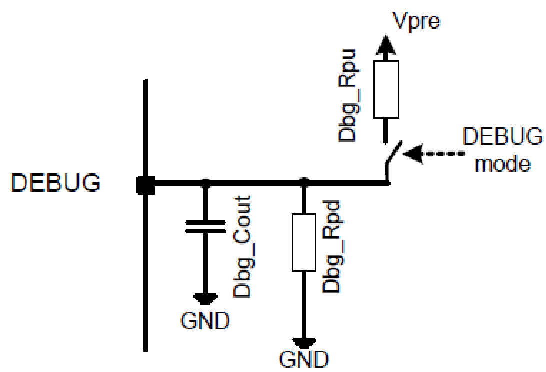


Figure 25. Debug mode entry connection

The Debug mode pin is scanned by the main and the fail-safe state machines at each power on reset. In the application, the main state machine is always powered by the battery while the fail-safe state machine is OFF in LPOFF mode. If the debug mode entry is done after release from LPOFF, only the fail-safe state machine is in debug mode with deep fail-safe and WD timeout disabled, not the main state machine. The CAN and LIN mode have to be configured to normal mode by the SPI.

Table 8. Debug mode component list

Component	Value	Ground connection
D_{BG_COUT}	10 nF	GND
D_{BG_RPD}	11 kΩ	GND
D_{BG_RPU}	10 kΩ	

5.8 MC33907_08 fail-safe start-up sequence

After a POR or a wake-up from LPOFF, the fail-safe state machine must be configured during the INIT_FS phase. Figure 26 illustrates the initialization process.

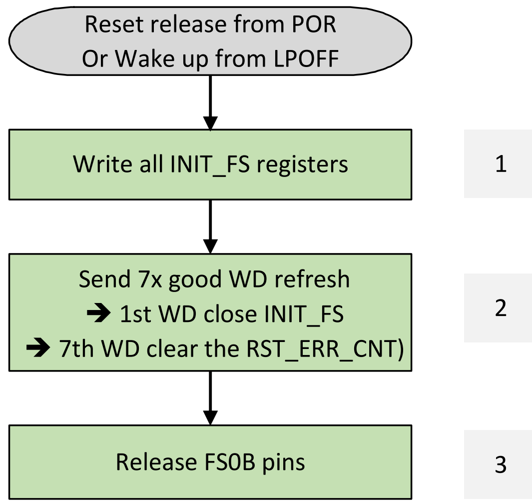


Figure 26. Fail-safe state machine initialization

1. Configure all the INIT_FS registers in regards to safety behavior expected on RSTB and FS0B at application level. Do not forget to disable IO_23_FS monitoring in INIT_FSSM2 register when IO_23 pins are not connected to FCCU pins of the MC, otherwise a reset generates when INIT_FS is closed by the first WD refresh.The INIT_FS phase is time limited to 256 ms maximum.

2. Refer to datasheet chapter 6.5.2.1 (see Section 10. References, page 44) for the watchdog answer calculation method. The first LFSR after POR or wake-up from LPOFF is always 0xB2. Consequently, the first seven good WD refresh required to close the INIT_FS phase and clear the reset error counter pin are: 0xD04D, 0xD19B, 0xD137, 0xD16E, 0xD1DC, 0xD1B9, and 0xD072. These WD_Answer SPI words are for reference and debug only. They must not be hard coded. The calculation method described in the datasheet must be followed to achieve the watchdog safety diagnostic coverage.

3. Refer to datasheet chapter 6.5.6 (see Section 10. References, page 44) for the FS_OUT register calculation based on WD_LFSR value to release the FS0B pin. Following the 7 WD refresh from step 2 (above), the FS_OUT register value to release FS0B pin is: 0xD327. This FS_OUT SPI word is for reference and debug only. It must not be hard coded. The calculation method described in the datasheet must be followed.

After step 2 (above), the watchdog must be periodically refreshed within the open window. Otherwise, a reset generates when the watchdog error counter reaches its final value (after 3 WD errors in default configuration, WD_ERR_CNT = 6).

The INIT phase of the main state machine is not time limited and can be handled when it is appropriate from an application standpoint. However, the INIT phase of the main state machine must be closed to allow CAN and LIN communications, MUX_OUT output selection, and transition to LPOFF by SPI command from the MCU.

6 MC33907_08 extended use cases

6.1 V_{SENSE} accuracy

V_{SENSE} voltage, image of the battery voltage, can be monitored through the MUX_OUT pin with 5% accuracy out of the NXP production line (as specified in the datasheet). As described in Figure 27, this accuracy depends on the V_{SENSE} resistor bridge and MUX_OUT amplifier offset, both varying with temperature, voltage, and process.

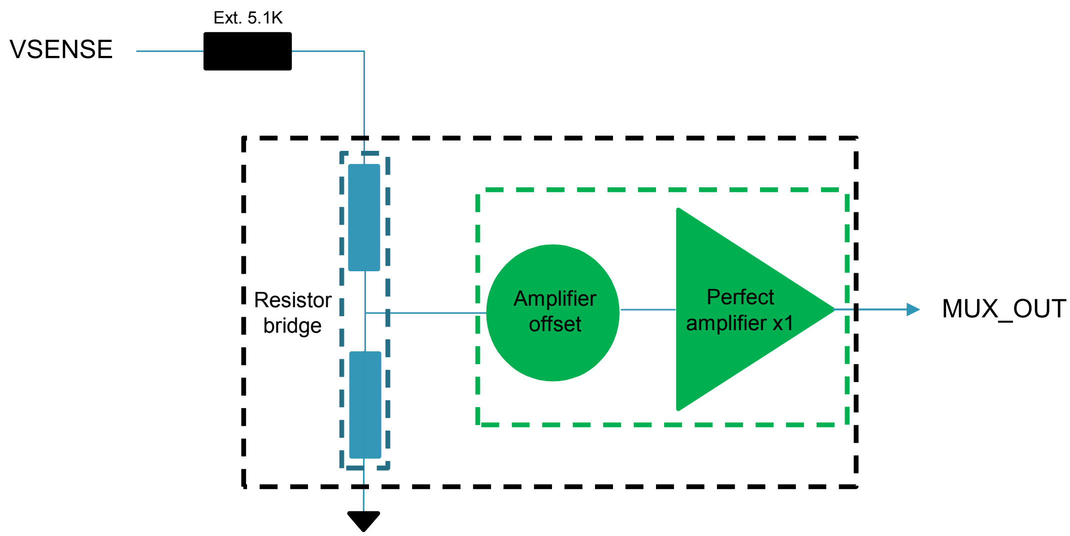


Figure 27. Simplified V_{SENSE} to MUX_OUT block diagram

Statistical analysis shows the main contributor to the accuracy is the process variation which can be removed with a part to part calibration at customer production line test. The calibration can be done at room temperature, and static V_{SENSE} between 9.0 V and 19 V (ideally 12 V or 14 V).

After calibration, the V_{SENSE} monitoring accuracy can achieve ±1%, for both V_{DDIO} = 3.3 V and 5.0 V, in wide range resistor bridge configuration (without taking into account the V_{SENSE} supply accuracy used for the calibration).

6.2 Wake-up by IO

The wake-up by IO is detected when a rising or a falling edge event happens at the IO pin and the device is in LPOFF mode. It means a transition from low to high or high to low must happen when the device is in LPOFF mode to validate the wake-up event.

If the IO wake-up event (rising or falling edge) arrives after the SPI LPOFF command and before the device entry to LPOFF, the wake-up event is not detected and the device does not wake-up. The device waits for the next IO transition to wake-up. See Figure 28 illustrating the IO_0 wake-up edge detection scenario.

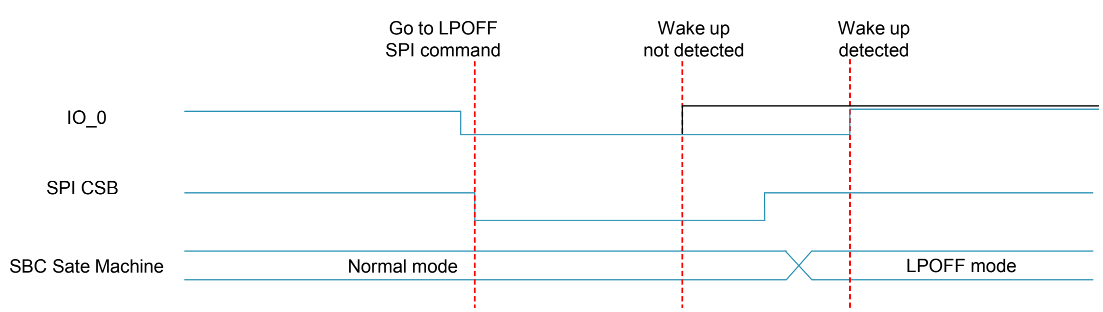


Figure 28. Wake-up by the IO_0 edge

At a 2.0 MHz SPI clock, the window where this could happen is less than 10 µs. A work around is proposed in Figure 29 to avoid missing an IO wake-up event, as previously described.

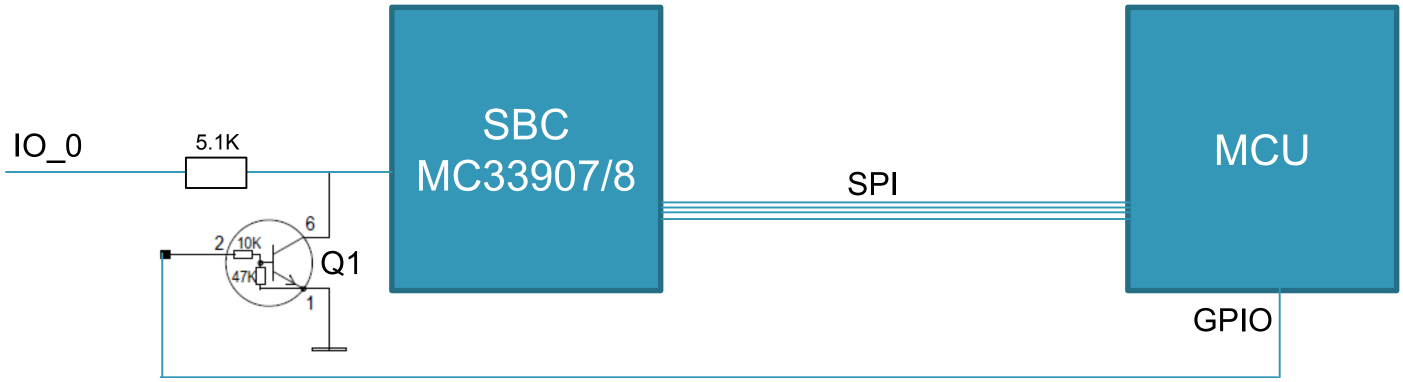


Figure 29. Work around to wake-up by a IO_0 level

When IO_0 goes low, the MCU is informed through the IO_0 bit from IO_Input register. Before sending the LPOFF SPI command, the MCU activates the Q1 transistor to maintain IO_0 low during the SPI transmission and the device entry to the LPOFF process. When the MC33907_08 goes to LPOFF, all the regulators are shutdown. Q1 is released when the MCU is unpowered. If IO_0 moves to high during this short period, it is released and the IO_0 transition from low to high wakes up the device. This work around is applicable for all IOs.

6.3 MC33907 attach to Infineon Aurix MCU

MC33907 can be attach to the Aurix MCU from Infineon. It has been validated with TC275 and TC277 versions and it is running in production. Figure 30 is a power tree proposal to show a possible connection between these two devices. This is not the only power tree possible, and can be adjusted depending on application need.

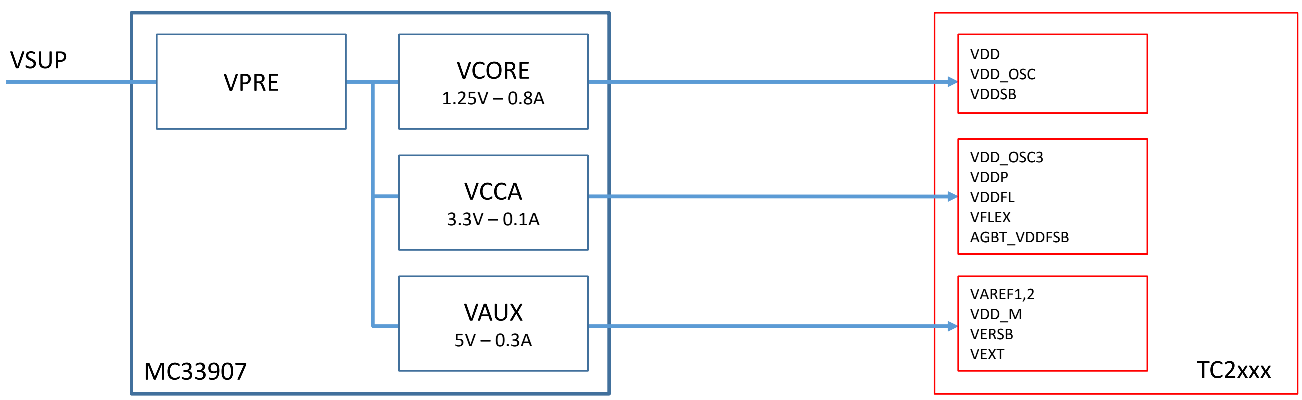


Figure 30. Power tree proposal

6.4 MC34FS6407_08 derivatives from MC33907_08

Industrial MC34FS6407NAE and MC34FS6408NAE devices are derivatives from automotive MC33907NAE and MC33908NAE devices, qualified for 24 V DC input voltage up to a 36 V maximum operating voltage. All the hardware designs and product guidelines in this application note also apply to these industrial devices.The max. rating voltage is 40 V and an additional input protection is required to sustain a 60 V load dump in 24 V transportation applications.

Figure 31 is a companionship proposal for the MC34FS6407_08 to sustain this load dump requirement. The MAX6495 limits the input voltage at V_{OV} (set here at 37.7 V) in order to not exceed the max. rating of the MC34FS6507_08 and keep the application running during the load dump condition.

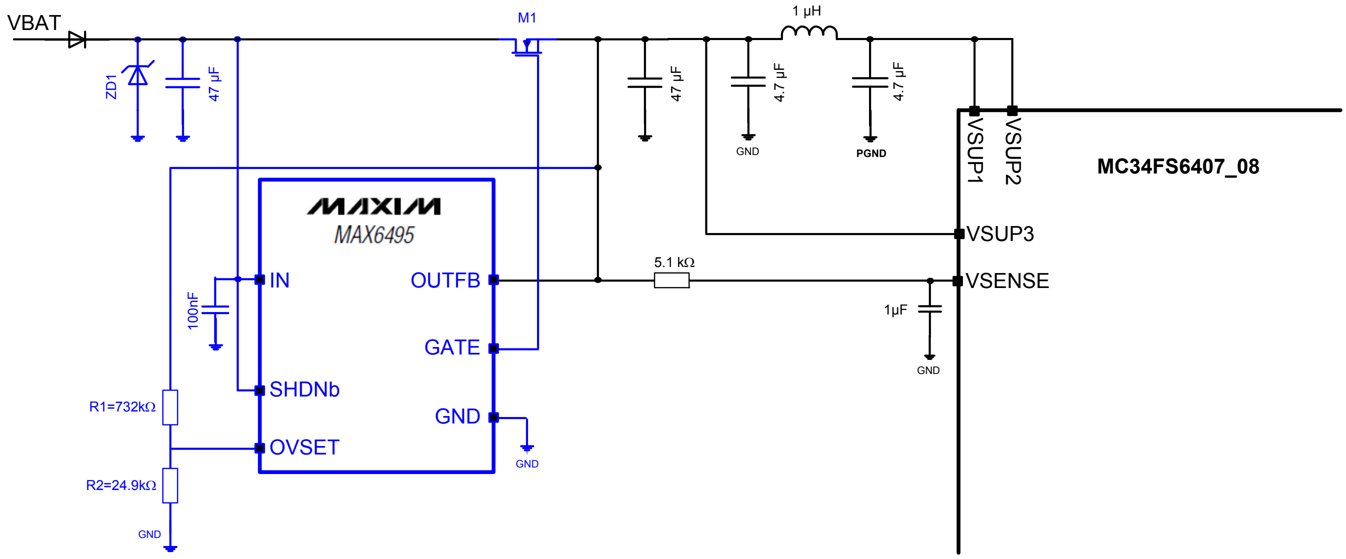


Figure 31. Battery connection proposal to sustain 60 V load dump

Table 9. MAX6495 external component list

Component	Value	Reference/manufacturer proposal	Ground connection
ZD1		- SMBJ54A/Fairchild - PTVS54VP1UP/NXP	GND
M1		- BUK7275-100A/NXP - BUK7Y65-100E/NXP	

7 PCB layout recommendations

To minimize the effects of switching noise on the embedded DC/DC converters, special attention must be paid to the layout of the power components when designing a printed circuit board (PCB) using the MC33907_08.

Component locations and ground connections on the PCB are important to consider when successfully optimizing overall performance with regards to high transient current loops, as shown in Figure 32.

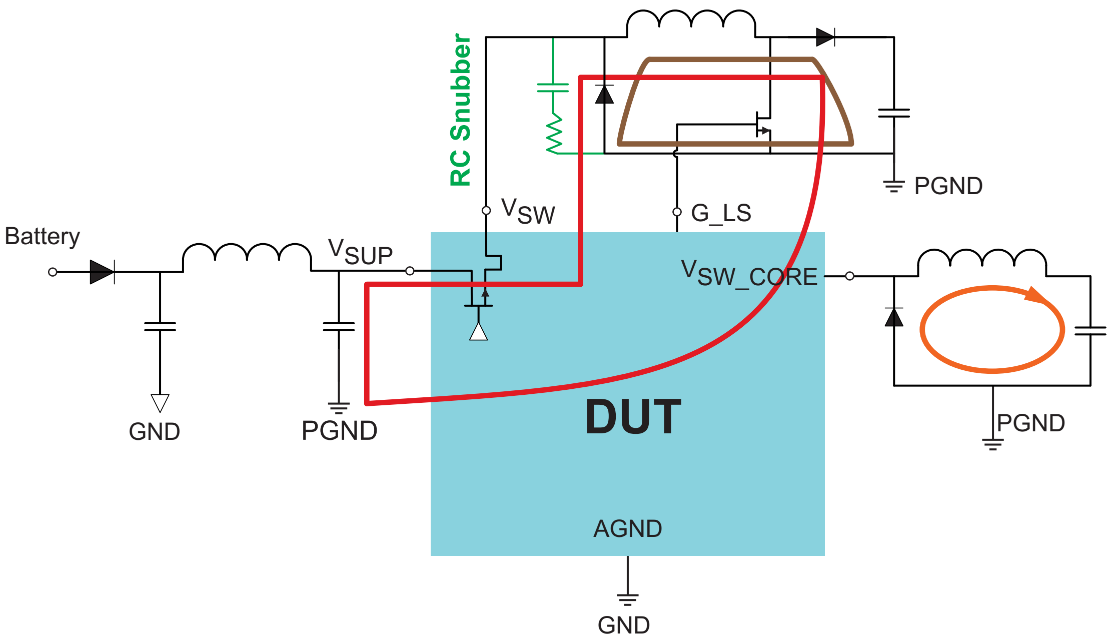


Figure 32. Current loops

7.1 Ground connections

Three grounds are available on the MC33907_08:

- AGND (analog ground),
- GND_COM (physical layer ground), and
- DGND (logic ground).

On the PCB, two grounds must be clearly separated:

- Local PGND for power components involved in the high transient current loops
- GND for other components connected to ground.

The star connection between PGND and GND must be done as far as possible from the local PGND ground on the PCB. The exposed pad is not electrically connected to ground, but this connection to the ground plane serves the power dissipation. The MCU digital ground should be connected to PGND to avoid any perturbation to GND. Each of the MC33907_08's external component connections to adequate ground are listed in MC33907_08 external components. Connections from MC33907_08 grounds and PCB grounds are shown in Figure 33.

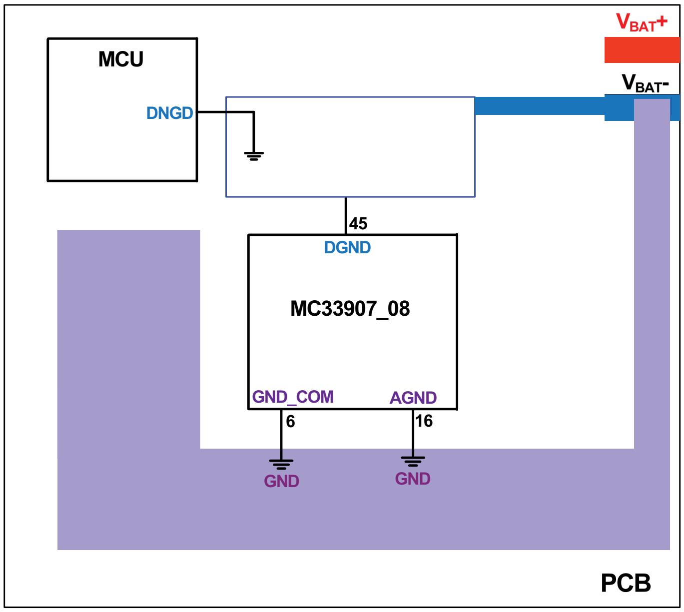


Figure 33. Ground connections between MC33907_08 and PCB ground

7.2 Routing external components

It is important to minimize the current loop on the PCB as much as possible. One way to do this is to place the power stage components involved in the high transient current loop as close as possible to the device. Avoid placing any power stage components close to other components which need to drive low current levels. Such components could easily be perturbed by switching noise.

7.2.1 The V_{PRE} Pre-regulator

Based on Figure 12, the PGND line of D_V_{PRE} is connected close to the PGND line near the C_{OUT_VPRE}(n) capacitors. C_{OUT_VPRE}(n) is kept close to the VPRE pin. The snubber (C_{SNUB_VPRE}, R_{SNUB_VPRE}) is kept close to D_V_{PRE}.

7.2.2 The V_{CORE} supply regulator

Based on Figure 16, the PGND line of D_V_{CORE} is connected close to the PGND line of the C_{OUT_VCORE}(n) capacitors. The snubber (C_{SNUB_VCORE}, R_{SNUB_VCORE}) is kept close to D_V_{CORE}. MC33907_08 V_{CORE} output must be connected close to the MCU core supply input to avoid DC voltage drop in the PCB track.

7.2.3 V_{AUX}, V_{CCA} linear regulators

Based on Figure 19, Cout _Vaux is kept close to the VAUX pin. C_{OUT_VCCA} is kept close to the VCCA pin.

7.2.4 VCAN

Based on Figure 23, keep $C_{OUT\_CAN\_5V}$ close to the CAN_5V pin.

7.2.5 R_{SELECT}

Based on Figure 19, R_{SELECT} must be placed close to the SELECT pin. Avoid power stage components close to the RSELECT pin so as not disturb the current in the resistor during startup. (This is the resistor used for V_{CCA} and V_{AUX} voltage configuration).

7.2.6 Best practice

- If a high current loop is going thru multiple PCB layers, multiple vias are recommended to limit the parasitic (R and L) in the high current path.
- Avoid AGND plane/signal below SMPS power components
- Avoid low level signal below SMPS power components
- Connect components with high-impedance signals close to the device pin to avoid noise injection

7.2.7 Placement example

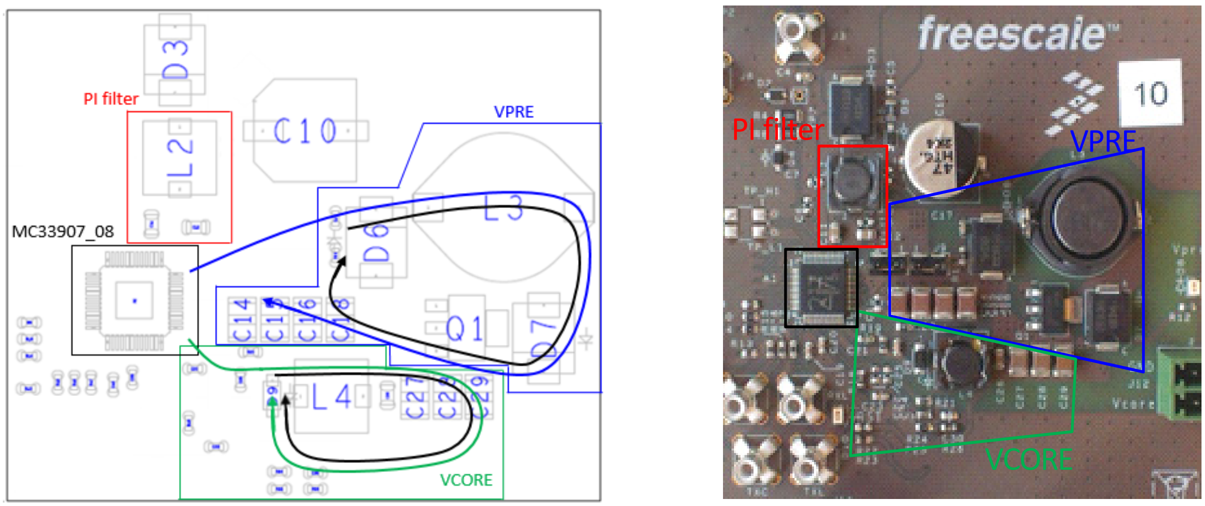


Figure 34. Placement example

- D3 is the reverse battery diode
- C10 is the V_{SUP} input capacitor which must be > 44 μF
- The input capacitor of the PI filter (in red) close to VSUP3 pin and output capacitor close to VSUP1/2 pin
- V_{PRE} in buck-boost configuration (with Q1, D7)
- V_{PRE} and V_{CORE} are located close together to facilitate the PGND local ground (SMPS ground)
- V_{CORE} external resistor bridge and compensation network components close to the device pin
- In blue and green, V_{PRE} and V_{CORE} current loops during inductor charging phase
- In black, current loops during inductor discharging phase

7.2.8 Ground connection example

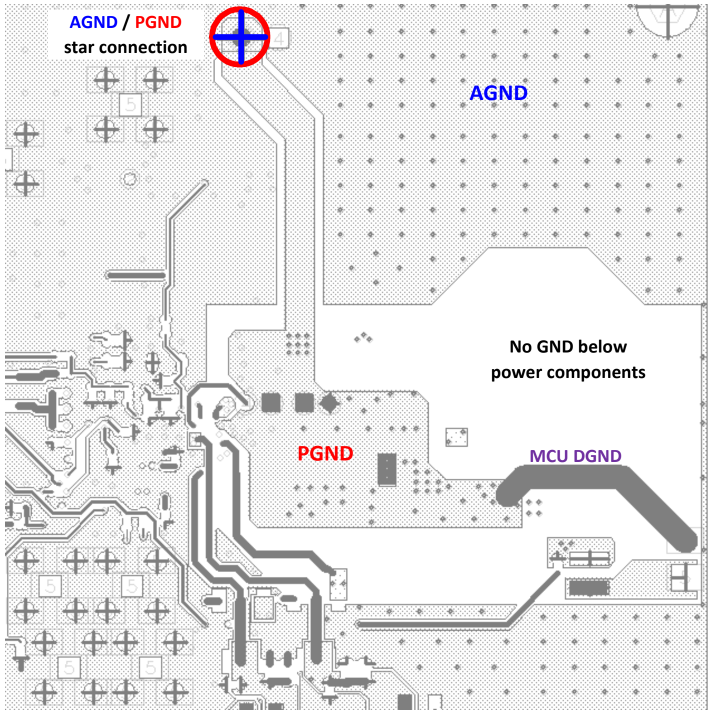


Figure 35. Ground connection example

- PGND is the SMPS power local ground
- AGND is a ground plane
- Star connection between PGND and AGND far from the local PGND (at the input power connector)
- No AGND plane below the V_{PRE}/V_{CORE} SMPS power components
- MCU DGND connected to PGND

8 ISO pulses

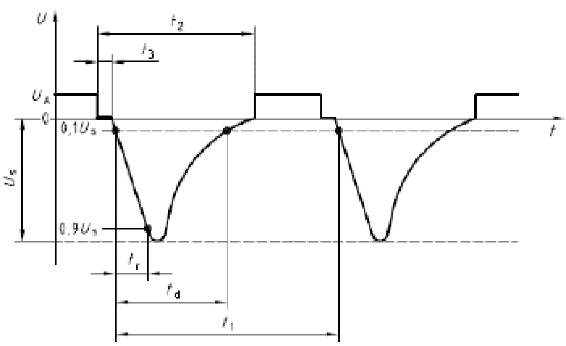
8.1 Reference documents

- German Car OEMs requirements: “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”. File: “OEM_HW_Requirements_For_CAN_LIN_FR_Interfaces_V1.2_20110325.pdf”
- ISO 7637-1: 2001, Road vehicles – Electrical disturbances from conduction and coupling
  Part1: Definitions and general considerations
- ISO 7637-2: 2008, Road vehicles – Electrical disturbances from conduction and coupling
  Part2: Electrical transient conduction along supply lines only
- ISO 7637-3: 2007, Road vehicles – Electrical disturbances from conduction and coupling
  Part3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

8.2 Test pulses description

Test pulse 1:

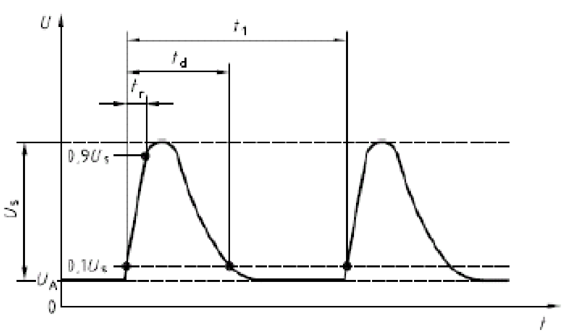
Ri = 10Ω



Test pulse description
Transient Test Pulse 1:
Us = -100V, tr = 1µs, td = 2ms, t1 = 5s, t2 = 0.2s, t3 = 100µs, Ri = 10O
Transient Test Pulse 2a:
Us = +100V, tr = 10µs, td = 50µs, t1 = 0.2s, Ri = 2O
Transient Test Pulse 2a:
Us = -30V, tr = 10µs, td = 50µs, t1 = 0.5s, Ri = 2O
Transient Test Pulse 2a:
Us = +30V, tr = 10µs, td = 50µs, t1 = 0.5s, Ri = 2O

Test pulse 2a (for positive Us):

Ri = 2Ω



Test pulse 2a (for negative Us):

Ri = 2Ω

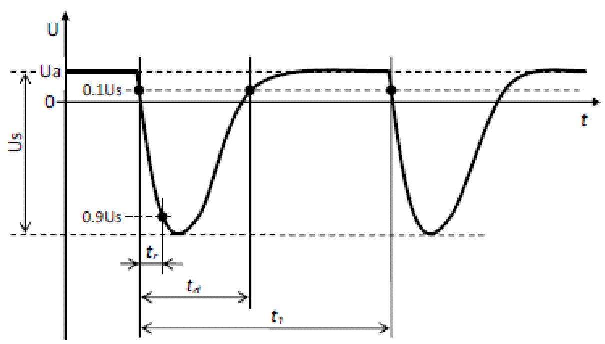
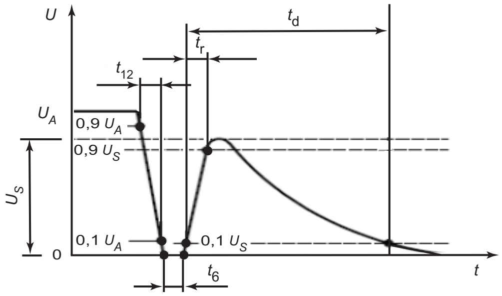


Figure 36. ISO test pulses description (1 of 3)

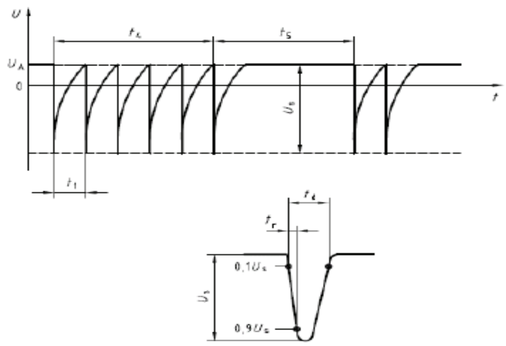
Test Pulse 2b:
Ri - 0.05Ω



Test pulse description
Transient Test Pulse 2b:
Us = +10V, tr = 1ms, td = 0.2s, t6 = 1ms, t12 = 1ms, Ri = 0.05Ω
Transient Test Pulse 3a:
Us = -150V, tr ≤ 5ns, td = 100ns, t1 = 100µs, t4 = 10ms, t5 = 90ms, Ri = 50Ω
Transient Test Pulse 3b:
Us = +100V, tr ≤ 5ns, td = 100ns, t1 = 100µs, t4 = 10ms, t5 = 90ms, Ri = 50Ω

Test pulse 3a:

Ri = 50Ω



Test pulse 3b:

Ri = 50Ω

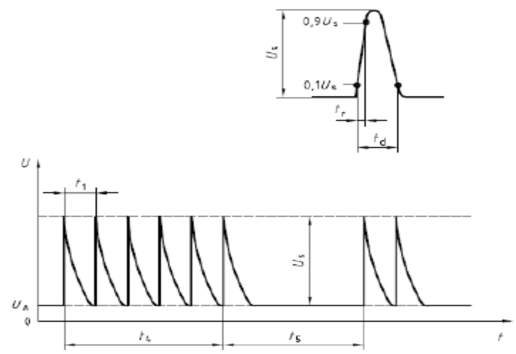
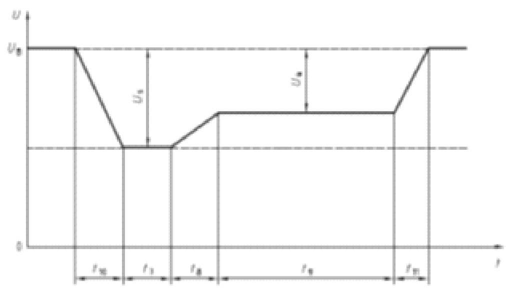


Figure 37. ISO test pulses description (2 of 3)

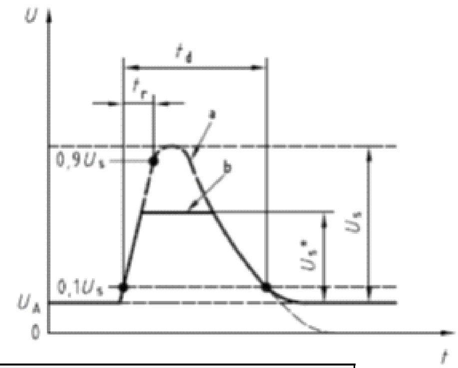
Test pulse 4 (Cranking):

Ri = 0.01Ω



Test pulse 5b (Load-dump):

Ri = 0.5Ω (clamped to ≤ 40V during test)



Test pulse description
Transient Test Pulse 4 (crank):
VBAT= U_B = 12V, Us = 6.9V, Ua = 5V, t10 = 5ms, t7 = 40ms,
t8 = 50ms, t9 = 20s, t11 = 5ms … 100ms, Ri = 0.01O
Transient Test Pulse 4 (crank):
VBAT= U_B = 12V, Us = 8.8V, Ua = 7V, t10 = 5ms, t7 = 40ms,
t8 = 50ms, t9 = 20s, t11 = 5ms … 100ms, Ri = 0.01O
Transient Test Pulse 5b (load dump):
Us = 87V (ext. Clamp = 40V), tr = 5ms … 10ms, td = 400ms, Ri = 0.5O

Figure 38. ISO test pulses description (3 of 3)

8.3 ISO pulse schematic

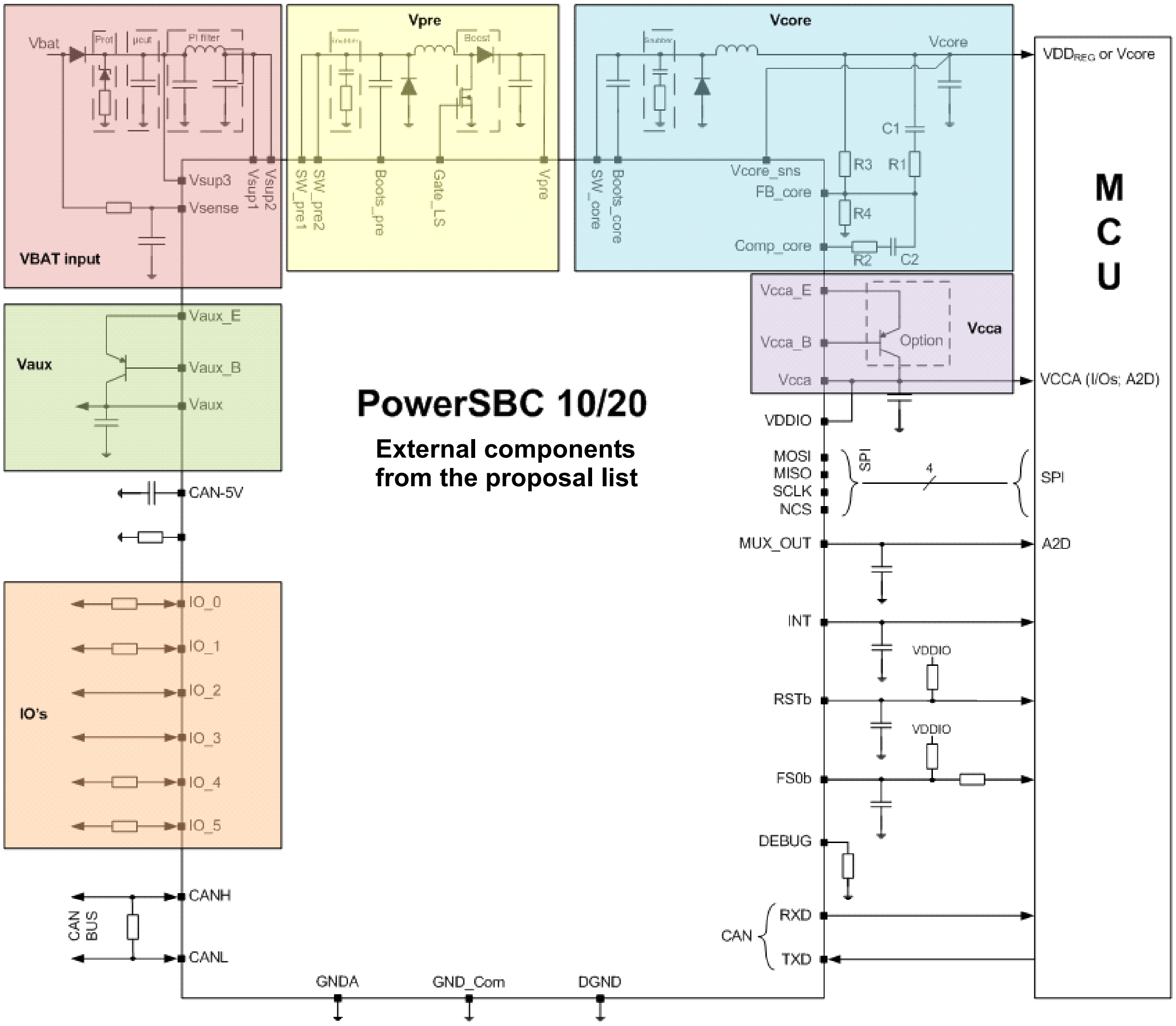


Figure 39. ISO pulse schematic

8.4 Product setup

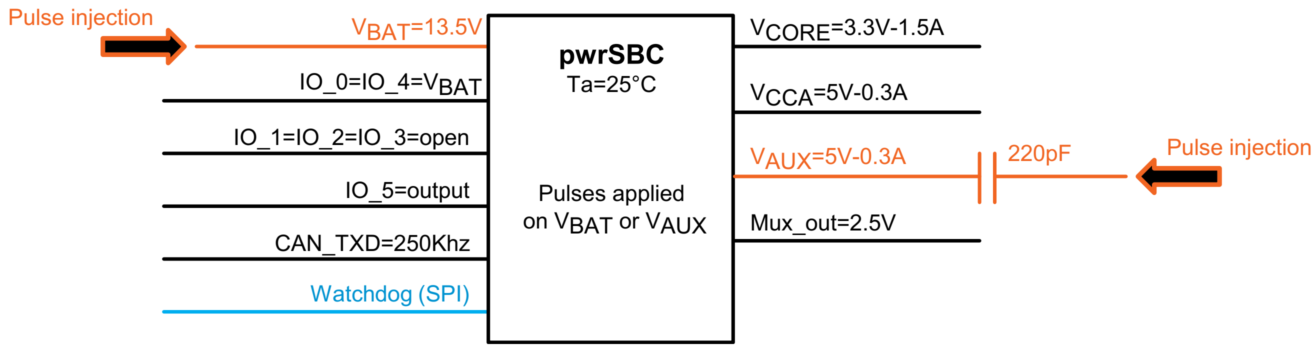


Figure 40. Product setup

Product setup in normal mode, **without** Fault (RSTB = 1, **FS0B = 1**) and **with** Fault (RSTB = 1, **FS0B = 0**):

- V_{BAT} = 13.5 V (unless otherwise noted), T_A = 25 °C
- V_{CORE} = 3.3 V at 1.5 A, V_{CCA} = V_{AUX} = 5.0 V at 0.3 A (with external ballast)
- Fault: No watchdog refresh asserts FS0B low when Reset Error Counter = 3
- IO_1, IO_2, and IO_3 not connected
- IO_0, IO_4 connected to VBAT with external resistor in series (5.1k)
- IO_5 configured as an output.
- Only IO_0 configured as wake-up input
- MUX_OUT configured by default to send internal reference voltage (2.5 V).
- Wake-up by CAN enabled on single dominant pulse (CAN_WU_conf = 1).
- CAN: TXD (pin 20) = 250 kHz, 5.0 V square wave signal, DC = 50%

8.5 Results

Applied on	Pulse type	Nb of pulse or test time	Pulse description and product setup	Class
Vbat	Pulse 1	5000	Transient Test Pulse 1 - buck boost	C
			Transient Test Pulse 1 - buck only	C
	Pulse 2a	5000	Transient Test Pulse 2a (+100 V) - buck boost	B
			Transient Test Pulse 2a (+100 V) - buck only	B
		500	Transient Test Pulse 2a (+30 V) - buck boost	A
			Transient Test Pulse 2a (+30 V) - buck only	A
			Transient Test Pulse 2a (-30 V) - buck boost	A
			Transient Test Pulse 2a (-30 V) - buck only	A
	Pulse 2b	5000	Transient Test Pulse 2b - buck boost	C
			Transient Test Pulse 2b - buck only	C
	Pulse 3a	10 mn	Transient Test Pulse 3a - buck boost	A
			Transient Test Pulse 3a - buck only	A
	Pulse 3b	10 mn	Transient Test Pulse 3b - buck boost	A
			Transient Test Pulse 3b - buck only	A
	Pulse 4	10	Transient Test Pulse 4 (Vmin=2.7 V) - buck boost	C*
			Transient Test Pulse 4 (Vmin=2.7 V) - buck only	C
			Transient Test Pulse 4 (Vmin=4.6 V) - buck boost	A
			Transient Test Pulse 4 (Vmin=4.6 V) - buck only	C**
	Pulse 5	5	Transient Test Pulse 5 - buck boost	B
			Transient Test Pulse 5 - buck only	B
Vaux	Pulse 3a	10 mn	Transient Test Pulse 3a - buck boost	A
			Transient Test Pulse 3a - buck only	A
	Pulse 3b	10 mn	Transient Test Pulse 3b - buck boost	A
			Transient Test Pulse 3b - buck only	A

* full load condition on all regulators as detailed in the setup slide

** VCCA and VAUX configured at 5.0 V

8.6 Failing criteria

8.6.1 Class A without fault (RSTB = 1, FS0B = 1)

- Monitoring of supply voltages: V_{CORE} (3.3 V) ±3%, V_{CCA} (5.0 V) ±3%, V_{AUX} (5.0 V) ±3%, V_{CAN} (5.0 V) ±5%
- Monitoring of internal reference voltage (on MUX_OUT pin): 2.5 V ±1%
- RXD (CAN) follows TXD (pin 20) with amplitude within 5.0 V ±0.9 V, and jitter ±10%
- No active reset means no RSTB latched during 10 ms (default init FSSM1 register configuration)
- No activation of FS0B
- No SPI configuration change (init. registers)
- No diag and status register change

8.6.2 Class A with fault (RSTB = 1, FS0B = 0)

- Monitoring of supply voltages: V_{CORE} (3.3 V) ±3%, V_{CCA} (5.0 V) ±3%, V_{AUX} (5.0 V) ±3%, V_{CAN} (5.0 V) ±5%
- Monitoring of internal reference voltage (on MUX_OUT pin): 2.5 V ±1%
- RXD (CAN) follows TXD (pin 20) with amplitude within 5.0 V ±0.9 V, and jitter ±10%
- Fault still reported (FS0B = 0)
- No Diag and status register change

8.6.3 Class B without fault (RSTB = 1, FS0B = 1)

- All functions return automatically to within normal limits after exposure is removed
- One or more of the supply or reference voltages can go beyond specified tolerances
- RXD (CAN) pin can go beyond specified tolerances
- No active reset means no RSTB latched during 10 ms (default init FSSM1 register configuration)
- No activation of FS0B
- No SPI configuration change (init. registers)
- No Diag and status register change

8.6.4 Class B with fault (RSTB = 1, FS0B = 0)

- All functions return automatically to within normal limits after exposure is removed
- One or more of the supply or reference voltages can go beyond specified tolerances
- RXD (CAN) pin can go beyond specified tolerances
- Fault still reported (FS0B = 0)
- No Diag and status register change

8.6.5 Class C without fault (RSTB = 1, FS0B = 1)

- All functions return automatically to within normal limits after exposure is removed
- Reset RSTB occurs with or without activation of FS0b

8.6.6 Class C with fault (RSTB = 1, FS0B = 0)

- All functions return automatically to within normal limits after exposure is removed
- One or more of fault outputs have changed (RSTB = 0 or FS0B = 1)

9 Physical layers certifications

9.1 Reference documents

- ISO 11898-2:2003, Road vehicles - Controller area network (CAN)
- Part 2: High-speed medium access unit
- ISO 11898-5:2007, Road vehicles - Controller area network (CAN)
- Part 5: High-speed medium access unit with low-power mode
- C&S: CAN High Speed Transceiver Conformance Test according to “GIFT ICT group - Conformance test specification V1.0”
- IBEE: IEC TS 62228, Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Application – AUDI, BMW, Daimler, Porsche, Volkswagen – Revision 1.3 / 2012
- J2962-2: Latest draft version from 2014 (official release under voting).

9.2 Results

MC33907_08 has several part number derivatives depending on CAN and LIN physical layers embedded. The certification results for the different part numbers are summarized in Table 10.

Table 10. Certification results summary

	MC33907_08AE	MC33097_08NAE	MC33907_08LAE
CAN	1	1	1
LIN	0	0	1
C&S Conformance	PASS	PASS	PASS
IBEE (Zwickau)	PASS	PASS	PASS
SAE J2962-1	NA	NA	PASS
SAE J2962-2	NA	PASS	PASS
VELIO	PASS	PASS	PASS

Note:
3. ESD protection option 2 is recommended

9.2.1 Conducted emission

Typical spectrum on VBAT, CAN, and LIN during IBEE certification (MC33908LAE), valid for other part numbers.

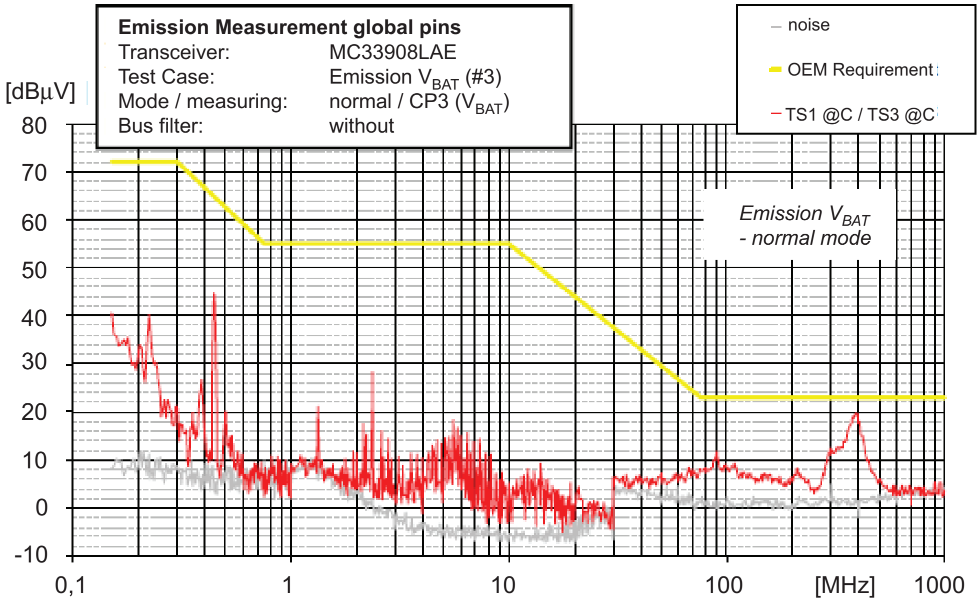


Figure 41. Conducted emission on V_{BAT}

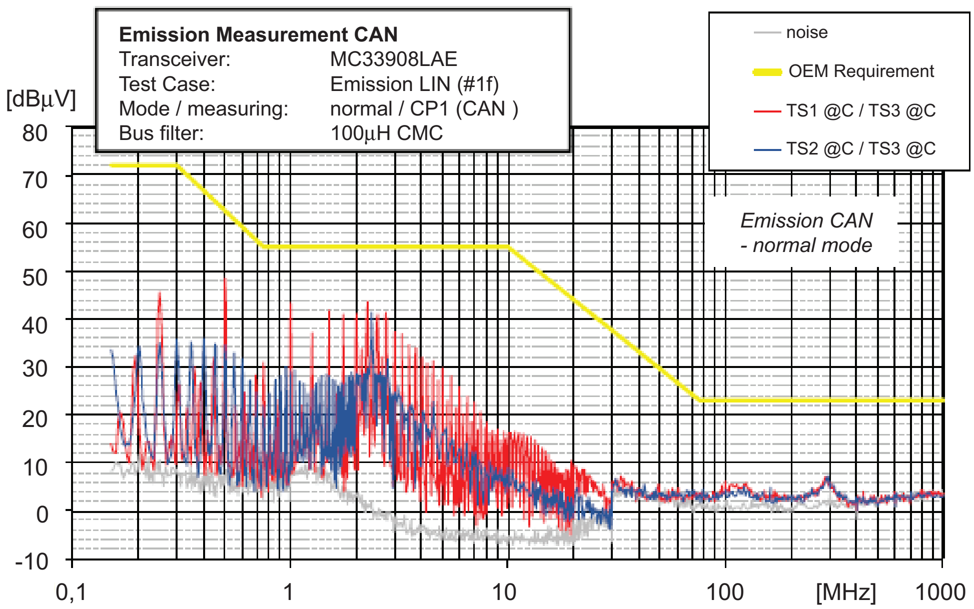


Figure 42. Conducted emission on the CAN Bus

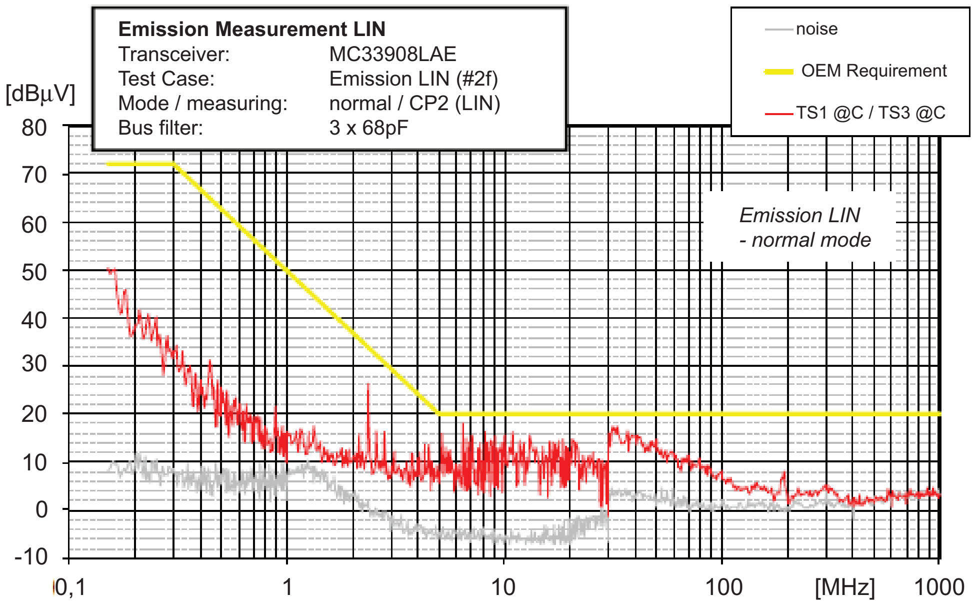


Figure 43. Conducted emission on LIN Bus

9.2.2 SAE J2962-2 option 2 description

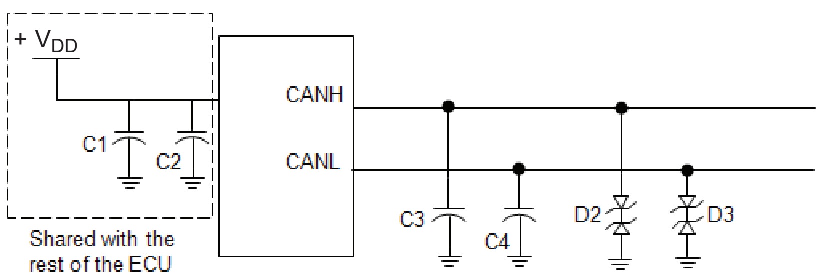


Figure 44. CAN ESD protection - option 2

Table 11. CAN ESD protection component list

Option No.	Component name	Label	Value
2	Capacitor	C3, C4	82 pF, 100 V ±5% (1)
	Zener	D2, D3	NXP PESD1CAN, (in same SOT23 package)

Note
1. Over entire voltage and temperature operating range

10 References

The following are URLs where you can obtain information on related NXP products and application solutions:

NXP.com Support Pages	Description	URL
MC33907_8	Power System Basis Chip with High Speed CAN Transceiver	http://www.nxp.com/files/analog/doc/data_sheet/MC33907_8.pdf
MC33907-MC33908D2	Power System Basis Chip with High Speed CAN and LIN Transceivers	http://www.nxp.com/files/analog/doc/data_sheet/MC33907-MC33908D2.pdf
MC34FS6407-08	Power System Basis Chip with High Speed CAN Transceiver	http://www.nxp.com/files/analog/doc/data_sheet/MC34FS6407-08.pdf
AN4661	Designing the VCORE Compensation Network For The MC33907/MC33908 System Basis Chips	http://www.nxp.com/files/analog/doc/app_note/AN4661.pdf
AN4442	Integrating the MPC5643L and MC33907/08 for Safety Applications	http://www.nxp.com/files/32bit/doc/app_note/AN4442.pdf
AN4388	Quad Flat Package (QFP)	http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf
AN4843	Low-Power Wireless Charging Using the NXP WCT1001A Controller	http://www.nxp.com/files/microcontrollers/doc/app_note/AN4843.pdf
AN5099	Integrating the MPC5744P and MC33907/08 for Safety Applications	http://www.nxp.com/files/microcontrollers/doc/app_note/AN5099.pdf
MC33907-MC33908PD TCALC	MC33907/8 Power Dissipation Tool	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33908&tab=Design_Tools_Tab
Vcore compensation network simulation tool		Upon demand
Non ISO pulses report		Upon demand
FMEDA	MC33907/8 FMEDA	Upon demand
MC33907_8SMUG	MC33907/8AE Safety Manual	https://www.nxp.com/webapp/Download?colCode=MC33907_8SMUG
MC33907_8NLSMUG	MC33907/8NAE, MC33907/8LAE Safety Manual	https://www.nxp.com/webapp/Download?colCode=MC33907NL-MC33908NLSMUG
KIT33908AEEVB	Evaluation Board	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33908AEEVB
KIT33908LAEEVB	Evaluation Board	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33908LAEEVB
KIT33908MBEVBE	Evaluation Mother Board (EVM)	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33908MBEVBE
KITMPC5643DBEVM	Evaluation Daughter Board (Qorivva MPC5643L)	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KITMPC5643DBEVM
KITMPC5744DBEVM	Evaluation Daughter Board (Qorivva MPC5744P)	http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KITMPC5744DBEVM
MC33907 Product Summary Page		http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33907
MC33908 Product Summary Page		http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33908
Analog Home Page		http://www.nxp.com/analog

11 Revision history

Revision	Date	Description
1.0	1/2014	• Initial release
2.0	3/2015	• Major updates • Added MC33907_8NL supported part numbers • Added CAN and LIN physical layers certification results • Added SMPS components calculation/selection method • Added Layout example • Added ISO pulses • Improved overall descriptions • Updated graphics to conform with NXP standards
3.0	8/2015	• Updated J2962 certification results • Updated V_{BAT} input filter requirement for J2962 • Added Simplified Internal Power Tree • Added V_{SENSE} accuracy improvement chapter • Added IO wake-up chapter • Added **Section 6.3, MC33907 attach to Infineon Aurix MCU**, page 28 • Added **Section 6.4, MC34FS6407_08 derivatives from MC33907_08**, page 28
4.0	3/2016	• Updated Figure 1 • Updated with NXP external components references • Corrected Debug Mode Entry Figure 25 (Dbg_Rpd resistor was not visible) • Added chapter 5.4.3 Reduce Vaux_PNP Power Dissipation • Added chapter 5.4.4 V_{AUX} Supplying a Sensor • Added chapter 5.8 MC33907_08 Basic Start up Sequence • Updated form and style

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Document Number: AN4766
Rev. 4.0
3/2016