

PIN DESCRIPTIONS

POWER SUPPLY

VDD

Positive Power Supply (Pin 6)

This is the most positive power supply and is typically connected to +3 V. This pin should be decoupled to VSS with a 0.1 μ F ceramic capacitor.

VSS

Negative Power Supply (Pin 15)

This is the most negative power supply and is typically connected to 0 V.

VAG

Analog Ground Output (Pin 20)

This output pin provides a mid-supply analog ground. This pin should be decoupled to VSS with a 0.01 μ F ceramic capacitor. All analog signal processing within this device is referenced to this pin. If the audio signals to be processed are referenced to VSS, then special precautions must be utilized to avoid noise between VSS and the VAG pin. Refer to the applications information in this document for more information. The VAG pin becomes high impedance when this device is in the powered-down mode.

VAG Ref

Analog Ground Reference Bypass (Pin 1)

This pin is used to capacitively bypass the on-chip circuitry that generates the mid-supply voltage for the VAG output pin. This pin should be bypassed to VSS with a 0.1 μ F ceramic capacitor using short, low inductance traces. The VAG Ref pin is only used for generating the reference voltage for the VAG pin. Nothing is to be connected to this pin in addition to the bypass capacitor. All analog signal processing within this device is referenced to the VAG pin. If the audio signals to be processed are referenced to VSS, then special precautions must be utilized to avoid noise between VSS and the VAG pin. Refer to the applications information in this document for more information. When this device is in the powered-down mode, the VAG Ref pin is pulled to the VDD power supply with a non-linear, high-impedance circuit.

CONTROL

HB

Transmit High-Pass Filter Bypass (Pin 16)

This pin selects whether the transmit high-pass filter will be used or bypassed, which allows frequencies below 200 Hz to appear at the input of the ADC to be digitized. This high-pass filter is a third order filter for attenuating power line frequencies, typically 50/60 Hz. A logic low selects this filter. A logic high deselects or bypasses this filter. When the filter is bypassed, the transmit frequency response extends down to dc.

PDI

Power-Down Input (Pin 10)

This pin puts the device into a low power dissipation mode when a logic 0 is applied. When this device is powered down, all of the clocks are gated off and all bias currents are turned off, which causes RO-, PO-, PO+, TG, VAG, and DT to become high impedance. The device will operate normally

when a logic 1 is applied to this pin. The device goes through a power-up sequence when this pin is taken to a logic 1 state, which prevents the DT PCM output from going low impedance for at least two FST cycles. The VAG and VAG Ref circuits and the signal processing filters must settle out before the DT PCM output or the RO- receive analog output will represent a valid analog signal.

ANALOG INTERFACE

TI+

Transmit Analog Input (Non-Inverting) (Pin 19)

This is the non-inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single-ended circuit for the input gain setting op amp. This allows input signals that are referenced to the VSS pin to be level shifted to the VAG pin with minimum noise. This pin may be connected to the VAG pin for an inverting amplifier configuration if the input signal is already referenced to the VAG pin. The common mode range of the TI+ and TI- pins is from 1.2 V, to VDD minus 1.2 V. This is an FET gate input.

The TI+ pin also serves as a digital input control for the transmit input multiplexer. Connecting the TI+ pin to VDD will place this amplifier's output (TG) into a high-impedance state, and selects the TG pin to serve as a high-impedance input to the transmit filter. Connecting the TI+ pin to VSS will also place this amplifier's output (TG) into a high-impedance state, and selects the TI- pin to serve as a high-impedance input to the transmit filter.

TI-

Transmit Analog Input (Inverting) (Pin 18)

This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI- pins is from 1.2 V to VDD - 1.2 V. This is an FET gate input.

The TI- pin also serves as one of the transmit input multiplexer pins when the TI+ pin is connected to VSS. When TI+ is connected to VDD, this pin is ignored. See the pin descriptions for the TI+ and the TG pins for more information.

TG

Transmit Gain (Pin 17)

This is the output of the transmit gain setting operational amplifier and the input to the transmit band-pass filter. This op amp is capable of driving a 2 k Ω load. Connecting the TI+ pin to VDD will place the TG pin into a high-impedance state, and selects the TG pin to serve as a high-impedance input to the transmit filter. All signals at this pin are referenced to the VAG pin. When TI+ is connected to VSS, this pin is ignored. See the pin descriptions for TI+ and TI- pins for more information. This pin is high impedance when the device is in the powered-down mode.

RO-

Receive Analog Output (Inverting) (Pin 2)

This is the inverting output of the receive smoothing filter from the digital-to-analog converter. This output is capable of driving a 2 k Ω load to 0.886 V peak referenced to the VAG pin. If the device is operated half-channel with the FST pin clocking and FSR pin held low, the receive filter input will be

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FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of this device includes a low-noise, three-terminal op amp capable of driving a 2 k Ω load. This op amp has inputs of TI+ (Pin 19) and TI- (Pin 18) and its output is TG (Pin 17). This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down by connecting the TI+ input to the V_{DD} power supply. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a 3-pole anti-aliasing pre-filter. This pre-filter incorporates a 2-pole Butterworth active low-pass filter, followed by a single passive pole. This pre-filter is followed by a single-ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully-differential circuitry. The next section is a fully-differential, 5-pole switched-capacitor low-pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3-pole switched-capacitor high-pass filter having a cutoff frequency of about 200 Hz. This high-pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. The high-pass filter may be bypassed or removed from the signal path by the HB pin. When the high-pass filter is bypassed, the frequency response extends down to include dc. The last stage of the high-pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital-to-analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched-capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A capacitor array (CDAC) is combined with a resistor string (RDAC) to implement the 13-bit linear DAC structure. The encode process uses the DAC, the voltage reference, and a frame-by-frame autozeroed comparator to implement a successive approximation conversion algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a 5-pole, 3400 Hz switched capacitor low-pass filter with sinX/X correction, and a 2-pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is buffered by an amplifier, which is output at the RO- pin. This output is capable of driving a 2 k Ω load to the V_{AG} pin. The MC145483 also has a pair of power amplifiers that are connected in a push-pull configuration. The PI pin is the inverting input to the PO- power amplifier. The non-inverting input is internally tied to the V_{AG} pin. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of minus one, and is internally connected to the PO- output. This complete power amplifier circuit is a differential (push-pull) amplifier with adjustable gain. The power amplifier may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD}.

The calibration level for both ADC and DAC of this 13-bit linear PCM Codec-Filter is referenced to Mu-Law with the

same bit voltage weighting about the zero crossing. This results in the 0 dBm0 calibration level being 3.20 dB below the peak sinusoidal level before clipping. Based on the reference voltage of 0.886 V, the calibration level is 0.436 V_{rms} or -5 dBm at 600 Ω .

The MC145483 has the ability to attenuate the receive analog output when used in the receive gain adjust mode. This mode is accessed by applying a logic high to the BCLKR pin while the rest of the clock pins are clocked normally. This allows three additional bits that will be used to control the gain of the analog output to be clocked into the DR pin following the 13 bits of voice data. Table 1 shows the attenuation values and the corresponding digital codes.

Table 1. Receive Gain Adjust Mode Coefficients and Attenuation Weightings

Coefficient	Attenuation in dB
000	0
001	-3
010	-6
011	-9
100	-12
101	-15
110	-18
111	-21

POWER-DOWN

There are two methods of putting this device into a low power consumption mode, which makes the device nonfunctional and consumes virtually no power. $\overline{\text{PDI}}$ is the power-down input pin which, when taken low, powers down the device. Another way to power the device down is to hold both the FST and FSR pins low while the BCLKT and MCLK pins are clocked. When the chip is powered down, the V_{AG}, TG, RO-, PO+, PO-, and DT outputs are high impedance and the V_{AG} Ref pin is pulled to the V_{DD} power supply with a non-linear, high-impedance circuit. To return the chip to the power-up state, $\overline{\text{PDI}}$ must be high and the FST frame sync pulse must be present while the BCLKT and MCLK pins are clocked. The DT output will remain in a high-impedance state for at least two 8 kHz FST pulses after power-up.

MASTER CLOCK

Since this codec-filter design has a single DAC architecture, the MCLK pin is used as the master clock for all analog signal processing including analog-to-digital conversion, digital-to-analog conversion, and for transmit and receive filtering functions of this device. The clock frequency applied to the MCLK pin may be 256 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 2.56 MHz, or 4.096 MHz. This device has a prescaler that automatically determines the proper divide ratio to use for the MCLK input, which achieves the required 256 kHz internal sequencing clock. The clocking requirements of the MCLK input are independent of the PCM data transfer mode (i.e., Long Frame Sync, Short Frame Sync, whether the device is used in the synchronous modes or not).

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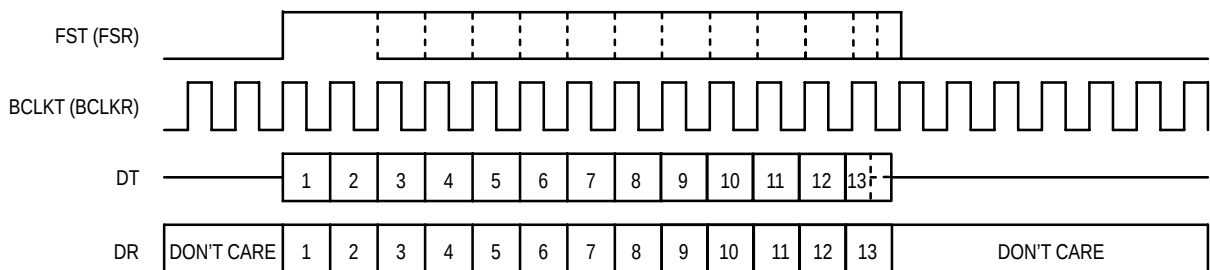


Figure 2a. Long Frame Sync (Transmit and Receive Have Individual Clocking)

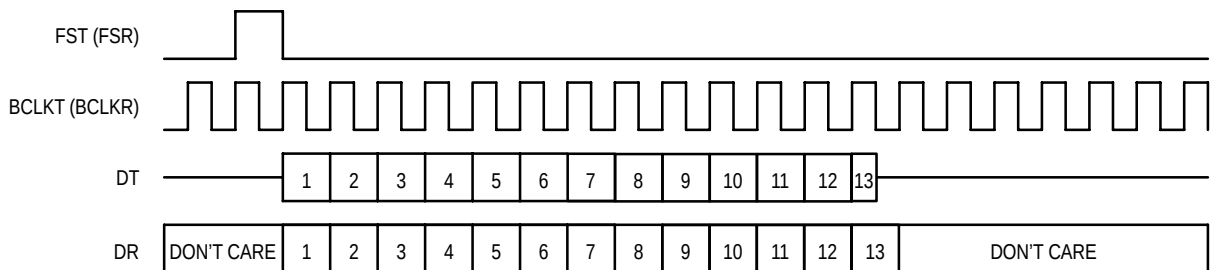


Figure 2b. Short Frame Sync (Transmit and Receive Have Individual Clocking)

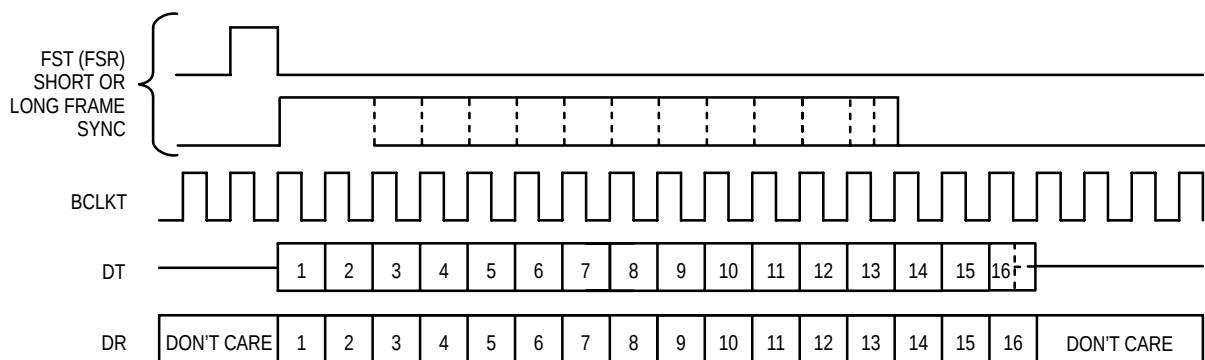


Figure 2c. Sign-Extended (BCLKR = 0)

Transmit and receive both use BCLKT, and the first four data bits are the sign bit. FST may occur at a different time than FSR.

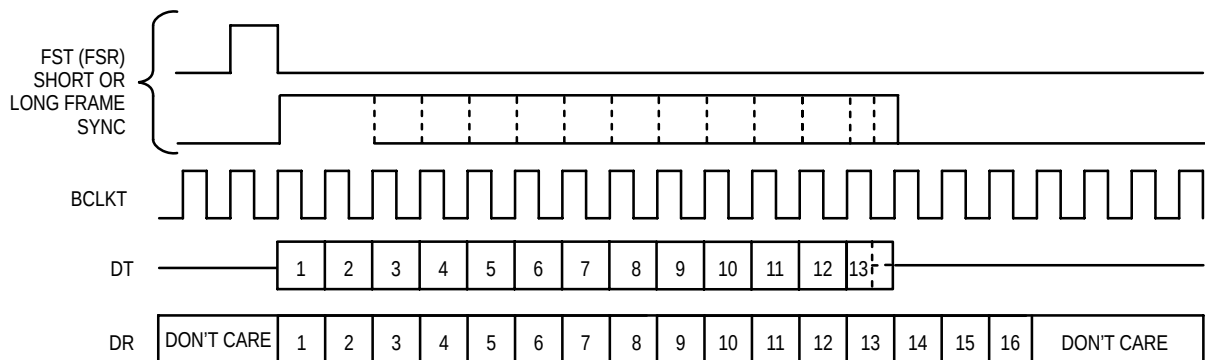


Figure 2d. Receive Gain Adjust (BCLKR = 1)

Transmit and receive both use BCLKT. FST may occur at a different time than FSR. Bits 14, 15, and 16, clocked into DR, are used for attenuation control for the receive analog output.

Figure 2. Digital Timing Modes for the PCM Data Interface

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If possible, reference audio signals to the V_{AG} pin instead of to the V_{SS} pin. Handset receivers and telephone line interface circuits using transformers may be audio signal referenced completely to the V_{AG} pin. Re-

fer to the application schematics for examples of this circuitry. The V_{AG} pin cannot be used for ESD or line protection.

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ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} = 2.7$ to 3.6 V, $V_{SS} = 0$ V, $T_A = -40$ to $+85^\circ\text{C}$)

Characteristics		Min	Typ	Max	Unit
Input Current	TI+, TI–	—	± 0.1	± 1.0	μA
Input Resistance to V_{AG} ($V_{AG} - 0.3 \text{ V} \leq V_{in} \leq V_{AG} + 0.3 \text{ V}$)	TI+, TI–	10	—	—	$\text{M}\Omega$
Input Capacitance	TI+, TI–	—	—	10	pF
Input Offset Voltage of TG Op Amp	TI+, TI–	—	—	± 5	mV
Input Common Mode Voltage Range	TI+, TI–	1.2	—	$V_{DD} - 1.2$	V
Input Common Mode Rejection Ratio	TI+, TI–	—	60	—	dB
Gain Bandwidth Product (10 kHz) of TG Op Amp ($R_L \geq 10 \text{ k}\Omega$)	—	—	2000	—	kHz
DC Open Loop Gain of TG Op Amp ($R_L \geq 10 \text{ k}\Omega$)	—	—	95	—	dB
Equivalent Input Noise (C–Message) Between TI+ and TI– at TG	—	—	– 28	—	dBrnC
Output Load Capacitance for TG Op Amp	—	0	—	100	pF
Output Voltage Range for TG ($R_L = 2 \text{ k}\Omega$ to V_{AG})	—	0.4	—	$V_{DD} - 0.4$	V
Output Current ($0.5 \text{ V} \leq V_{out} \leq V_{DD} - 0.5 \text{ V}$)	TG, RO–	± 1.0	—	—	mA
Output Load Resistance to V_{AG}	TG, RO–	2	—	—	$\text{k}\Omega$
Output Impedance	RO–	—	1	—	Ω
Output Load Capacitance	RO–	0	—	200	pF
DC Output Offset Voltage of RO– Referenced to V_{AG}	—	—	—	± 25	mV
V_{AG} Output Voltage Referenced to V_{SS} (No Load)	—	$V_{DD}/2 - 0.05$	$V_{DD}/2$	$V_{DD}/2 + 0.05$	V
V_{AG} Output Current with ± 25 mV Change in Output Voltage	—	± 1.0	± 2	—	mA
Power Supply Rejection Ratio (0 to 100 kHz @100 mVrms Applied to V_{DD} , C–Message Weighting, All Analog Signals Referenced to V_{AG} Pin)	Transmit Receive	40 40	60 60	— —	dB
Power Drivers PI, PO+, PO–					
Input Current ($V_{AG} - 0.3 \text{ V} \leq PI \leq V_{AG} + 0.3 \text{ V}$)	PI	—	± 0.05	± 1.0	μA
Input Resistance ($V_{AG} - 0.3 \text{ V} \leq PI \leq V_{AG} + 0.3 \text{ V}$)	PI	10	—	—	$\text{M}\Omega$
Input Offset Voltage	PI	—	—	± 20	mV
Output Offset Voltage of PO+ Relative to PO– (Inverted Unity Gain for PO–)	—	—	—	± 50	mV
Output Current ($V_{SS} + 0.4 \text{ V} \leq PO+ \text{ or } PO- \leq V_{DD} - 0.4 \text{ V}$)	—	± 10	—	—	mA
PO+ or PO– Output Resistance (Inverted Unity Gain for PO–)	—	—	1	—	Ω
Gain Bandwidth Product (10 kHz, Open Loop for PO–)	—	—	1000	—	kHz
Load Capacitance (PO+ or PO– to V_{AG} , or PO+ to PO–)	—	0	—	1000	pF
Gain of PO+ Relative to PO– ($R_L = 300 \Omega$, + 3 dBm0, 1 kHz)	—	– 0.2	0	+ 0.2	dB
Total Signal to Distortion at PO+ and PO– with a Differential Load of: 300 Ω 100 nF in series with $\geq 20 \Omega$ Current Limitation $\pm 10 \text{ mA} \geq 100 \Omega$	—	45 — —	60 40 40	— — —	dB
Power Supply Rejection Ratio (0 to 25 kHz @ 50 mVrms Applied to V_{DD} , PO– Connected to PI. Differential or Measured Referenced to V_{AG} Pin.)	0 to 4 kHz 4 to 25 kHz	40 —	55 40	— —	dB

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DIGITAL SWITCHING CHARACTERISTICS, LONG FRAME SYNC AND SHORT FRAME SYNC

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, All Digital Signals Referenced to V_{SS}, T_A = - 40 to + 85°C, C_L = 150 pF, Unless Otherwise Noted)

Ref. No.	Characteristics	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK	— — — — — — —	256 512 1536 1544 2048 2560 4096	— — — — — — —	kHz
1	MCLK Duty Cycle for 256 kHz Operation	45	—	55	%
2	Minimum Pulse Width High for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
3	Minimum Pulse Width Low for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
4	Rise Time for All Digital Signals	—	—	50	ns
5	Fall Time for All Digital Signals	—	—	50	ns
6	Setup Time from MCLK Low to FST High	50	—	—	ns
7	Setup Time from FST High to MCLK Low	50	—	—	ns
8	Bit Clock Data Rate for BCLKT or BCLKR	256	—	4096	kHz
9	Minimum Pulse Width High for BCLKT or BCLKR	50	—	—	ns
10	Minimum Pulse Width Low for BCLKT or BCLKR	50	—	—	ns
11	Hold Time from BCLKT (BCLKR) Low to FST (FSR) High	20	—	—	ns
12	Setup Time for FST (FSR) High to BCLKT (BCLKR) Low	80	—	—	ns
13	Setup Time from DR Valid to BCLKR Low	0	—	—	ns
14	Hold Time from BCLKR Low to DR Invalid	50	—	—	ns
LONG FRAME SPECIFIC TIMING					
15	Hold Time from 2nd Period of BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
16	Delay Time from FST or BCLKT, Whichever is Later, to DT for Valid MSB Data	—	—	60	ns
17	Delay Time from BCLKT High to DT for Valid Data	—	—	60	ns
18	Delay Time from the Later of the 13th (16th for Sign-Extended Mode) BCLKT Falling Edge, or the Falling Edge of FST to DT Output High Impedance	10	—	60	ns
19	Minimum Pulse Width Low for FST or FSR	50	—	—	ns
SHORT FRAME SPECIFIC TIMING					
20	Hold Time from BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
21	Setup Time from FST (FSR) Low to MSB Period of BCLKT (BCLKR) Low	50	—	—	ns
22	Delay Time from BCLKT High to DT Data Valid	10	—	60	ns
23	Delay Time from the 13th (16th for Sign-Extended Mode) BCLKT Low to DT Output High Impedance	10	—	60	ns

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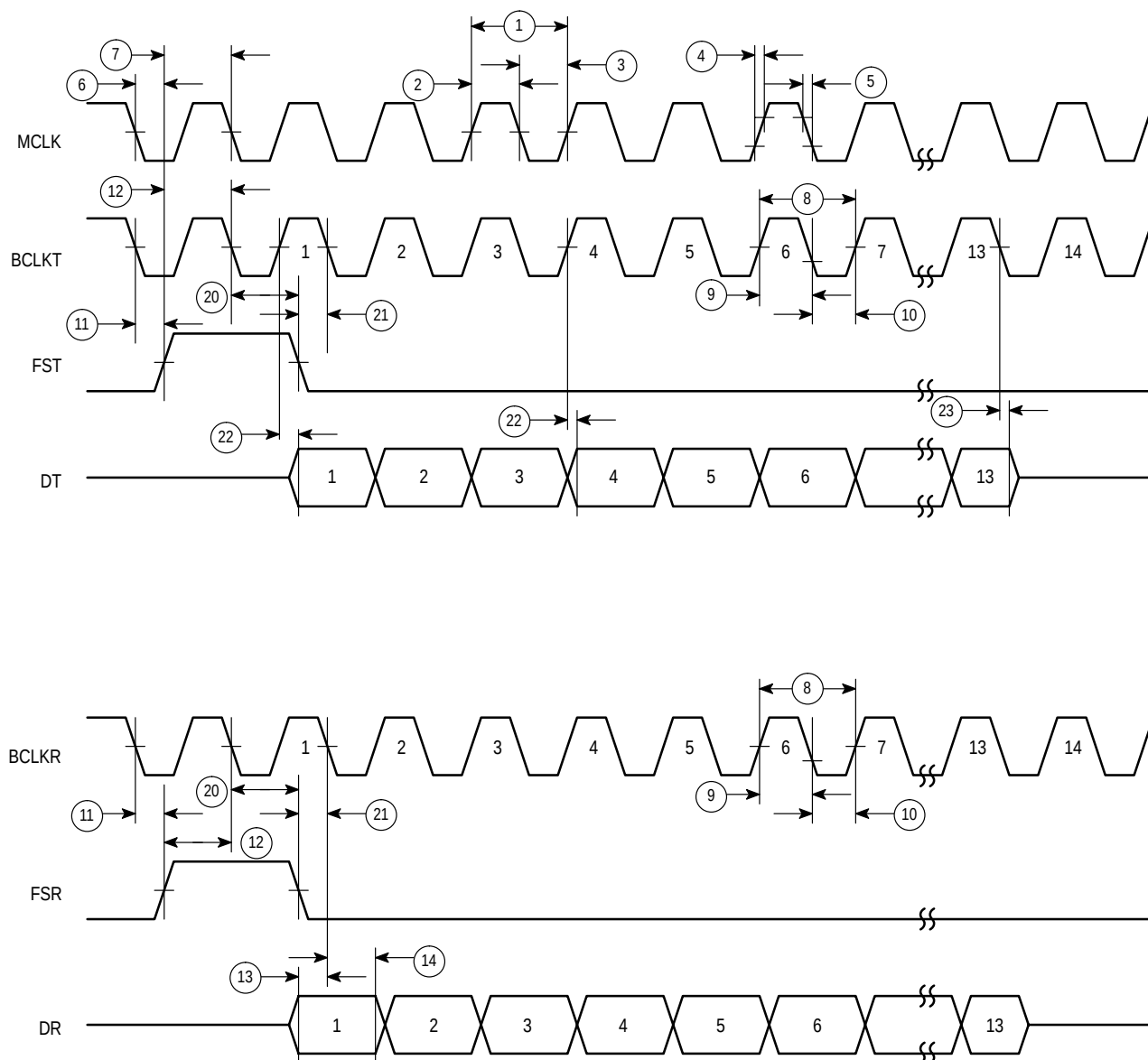


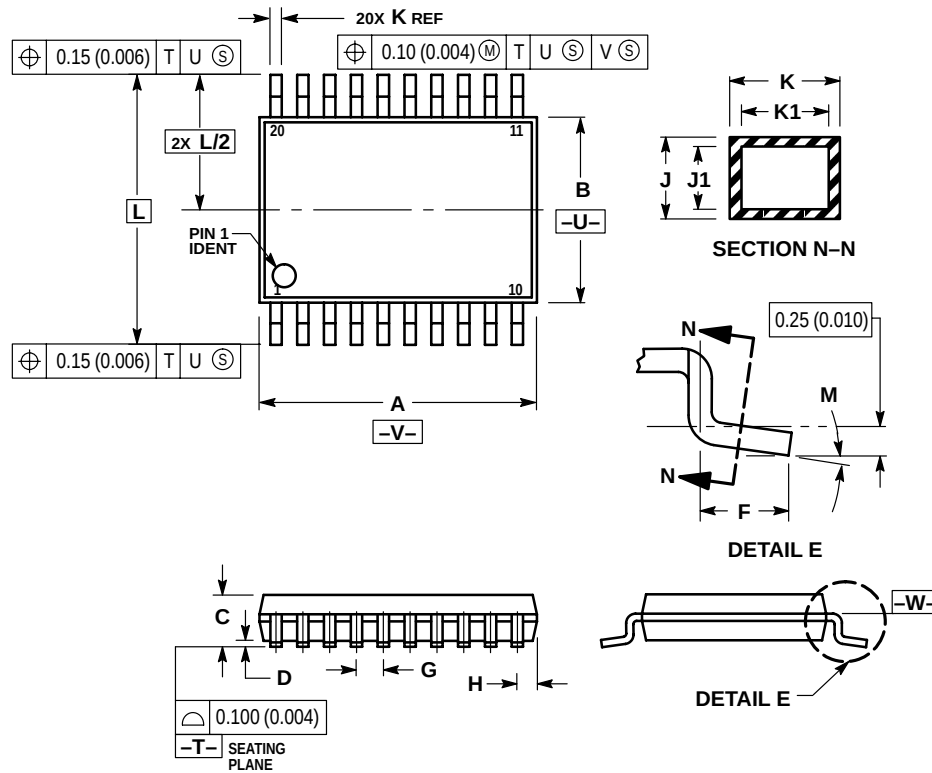
Figure 4. Short Frame Sync Timing



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DT SUFFIX
TSSOP
CASE 948E-02



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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