

## 3.3 V ECL Programmable Delay Chip with FTUNE

### MC100EP196

The MC100EP196 is a programmable delay chip (PDC) designed primarily for clock deskewing and timing adjustment. It provides variable delay of a differential NECL/PECL input transition. It has similar architecture to the EP195 with the added feature of further tuneability in delay using the FTUNE pin. The FTUNE input takes an analog voltage from  $V_{CC}$  to  $V_{EE}$  to fine tune the output delay from 0 to 60 ps.

The delay section consists of a programmable matrix of gates and multiplexers as shown in the logic diagram, Figure 2. The delay increment of the EP196 has a digitally selectable resolution of about 10 ps and a net range of up to 10.2 ns. The required delay is selected by the 10 data select inputs D[9:0] values and controlled by the LEN (pin 10). A LOW level on LEN allows a transparent LOAD mode of real time delay values by D[9:0]. A LOW to HIGH transition on LEN will LOCK and HOLD current values present against any subsequent changes in D[10:0]. The approximate delay values for varying tap numbers correlating to D0 (LSB) through D9 (MSB) are shown in Table 5.

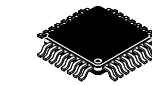
Because the EP196 is designed using a chain of multiplexers, it has a fixed minimum delay of 2.4 ns. An additional pin, D10, is provided for controlling Pins 14 and 15, CASCADE and  $\overline{\text{CASCADE}}$ , also latched by LEN, in cascading multiple PDCs for increased programmable range. The cascade logic allows full control of multiple PDCs. Switching devices from all "1" states on D[0:9] with SETMAX LOW to all "0" states on D[0:9] with SETMAX HIGH will increase the delay equivalent to "D0", the minimum increment.

Select input pins, D[10:0], may be threshold controlled by combinations of interconnects between  $V_{EF}$  (pin 7) and  $V_{CF}$  (pin 8) for LVCMOS, ECL, or LVTTL level signals. LVTTL and LVCMOS operation is available in PECL mode only. For LVCMOS input levels, leave  $V_{CF}$  and  $V_{EF}$  open. For ECL operation, short  $V_{CF}$  and  $V_{EF}$  (pins 7 and 8). For LVTTL level operation, connect a 1.5 V supply reference to  $V_{CF}$  and leave open  $V_{EF}$  pin. The 1.5 V reference voltage to  $V_{CF}$  pin can be accomplished by placing a 2.2 k $\Omega$  resistor between  $V_{CF}$  and  $V_{EE}$  for 3.3 V power supply.

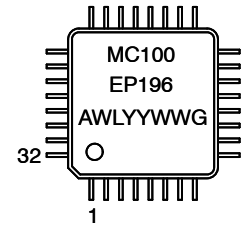
The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series contains temperature compensation.

#### MARKING DIAGRAM\*



LQFP-32, 7 x 7  
FA SUFFIX  
CASE 561AB-01



|    |                     |
|----|---------------------|
| A  | = Assembly Location |
| WL | = Wafer Lot         |
| YY | = Year              |
| WW | = Work Week         |
| G  | = Pb-Free Package   |

\*For additional marking information, refer to Application Note [AND8002/D](#).

- Maximum Frequency > 1.2 GHz Typical
- Programmable Range: 0 ns to 10 ns
- Delay Range: 2.4 ns to 12.4 ns
- 10 ps Increments
- PECL Mode Operating Range:  
 $V_{CC} = 3.0 \text{ V}$  to  $3.6 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -3.0 \text{ V}$  to  $-3.6 \text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- A Logic High on the  $\overline{\text{EN}}$  Pin Will Force Q to Logic Low
- D[10:0] Can Accept Either ECL, LVCMOS, or LVTTL Inputs
- $V_{BB}$  Output Reference Voltage
- These are Pb-Free Devices\*

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

MC100EP196

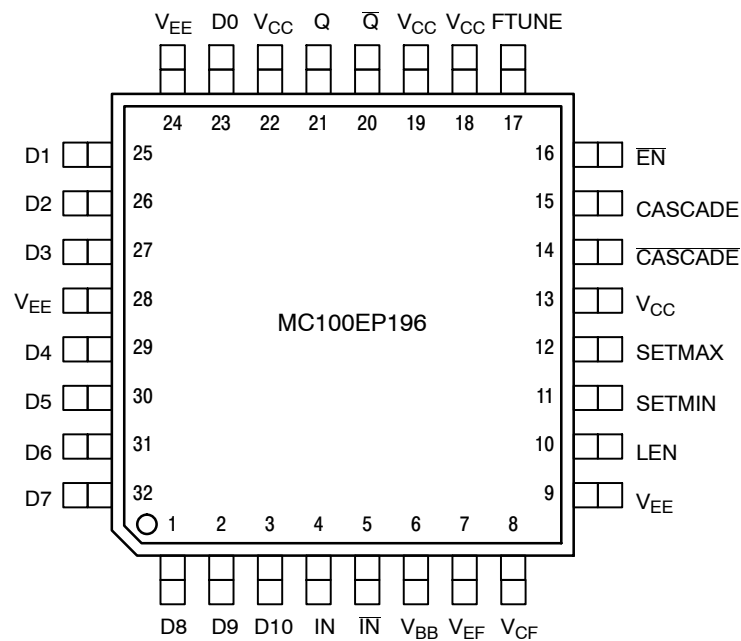


Figure 1. 32-Lead LQFP Pinout (Top View)

Table 1. PIN DESCRIPTION

| Pin                                        | Name                 | I/O                           | Default State | Description                                                                                                                     |
|--------------------------------------------|----------------------|-------------------------------|---------------|---------------------------------------------------------------------------------------------------------------------------------|
| 23, 25, 26, 27,<br>29, 30, 31, 32,<br>1, 2 | D[0:9]               | LVC MOS, LV TTL,<br>ECL Input | LOW           | Single-ended Parallel Data Inputs [0:9]. Internal 75 k $\Omega$ to $V_{EE}$ . (Note 1)                                          |
| 3                                          | D[10]                | LVC MOS, LV TTL,<br>ECL Input | LOW           | Single-ended CASCADE/CASCADE Control Input. Internal 75 k $\Omega$ to $V_{EE}$ . (Note 1)                                       |
| 4                                          | IN                   | ECL Input                     | LOW           | Noninverted Differential Input. Internal 75 k $\Omega$ to $V_{EE}$ .                                                            |
| 5                                          | $\overline{IN}$      | ECL Input                     | HIGH          | Inverted Differential Input. Internal 75 k $\Omega$ to $V_{EE}$ .                                                               |
| 6                                          | $V_{BB}$             | –                             | –             | ECL Reference Voltage Output                                                                                                    |
| 7                                          | $V_{EF}$             | –                             | –             | Reference Voltage for ECL Mode Connection                                                                                       |
| 8                                          | $V_{CF}$             | –                             | –             | LVC MOS, ECL, OR LV TTL Input Mode Select                                                                                       |
| 9, 28                                      | $V_{EE}$             | –                             | –             | Negative Supply Voltage. All $V_{EE}$ Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 13, 18, 19, 22                             | $V_{CC}$             | –                             | –             | Positive Supply Voltage. All $V_{CC}$ Pins must be externally Connected to Power Supply to Guarantee Proper Operation. (Note 2) |
| 10                                         | LEN                  | ECL Input                     | LOW           | Single-ended D pins LOAD / HOLD input. Internal 75 k $\Omega$ to $V_{EE}$ .                                                     |
| 11                                         | SETMIN               | ECL Input                     | LOW           | Single-ended Minimum Delay Set Logic Input. Internal 75 k $\Omega$ to $V_{EE}$ . (Note 1)                                       |
| 12                                         | SETMAX               | ECL Input                     | LOW           | Single-ended Maximum Delay Set Logic Input. Internal 75 k $\Omega$ to $V_{EE}$ . (Note 1)                                       |
| 14                                         | $\overline{CASCADE}$ | ECL Output                    | –             | Inverted Differential Cascade Output for D[10] Input. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2 V$ .        |
| 15                                         | CASCADE              | ECL Output                    | –             | Noninverted Differential Cascade Output for D[10] Input. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2 V$ .     |
| 16                                         | $\overline{EN}$      | ECL Input                     | LOW           | Single-ended Output Enable Pin. Internal 75 k $\Omega$ to $V_{EE}$ .                                                            |
| 17                                         | FTUNE                | Analog Input                  | –             | Fine Tuning Input.                                                                                                              |
| 21                                         | Q                    | ECL Output                    | –             | Noninverted Differential Output. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2 V$ .                             |
| 20                                         | $\overline{Q}$       | ECL Output                    | –             | Inverted Differential Output. Typically Terminated with 50 $\Omega$ to $V_{TT} = V_{CC} - 2 V$ .                                |

1. SETMIN will override SETMAX if both are high. SETMAX and SETMIN will override all D[0:10] inputs.
2. All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.



Table 2. CONTROL PIN

| Pin    | State        | Function                                                                                                               |
|--------|--------------|------------------------------------------------------------------------------------------------------------------------|
| EN     | LOW (Note 3) | Input Signal is Propagated to the Output                                                                               |
|        | HIGH         | Output Holds Logic Low State                                                                                           |
| LEN    | LOW (Note 3) | Transparent or LOAD mode for real time delay values present on D[0:10].                                                |
|        | HIGH         | LOCK and HOLD mode for delay values on D[0:10]; further changes on D[0:10] are not recognized and do not affect delay. |
| SETMIN | LOW (Note 3) | Output Delay set by D[0:10]                                                                                            |
|        | HIGH         | Set Minimum Output Delay                                                                                               |
| SETMAX | LOW (Note 3) | Output Delay set by D[0:10]                                                                                            |
|        | HIGH         | Set Maximum Output Delay                                                                                               |
| D10    | LOW          | CASCADE Output LOW, $\overline{\text{CASCADE}}$ Output HIGH                                                            |
|        | HIGH         | $\overline{\text{CASCADE}}$ Output LOW, CASCADE Output High                                                            |

3. Internal pulldown resistor will provide a logic LOW if pin is left unconnected.

Table 3. CONTROL D[0:10] INTERFACE

| Pin      | State                 | Function            |
|----------|-----------------------|---------------------|
| $V_{CF}$ | $V_{EF}$ Pin (Note 4) | ECL Mode            |
| $V_{CF}$ | No Connect            | LVC MOS Mode        |
| $V_{CF}$ | 1.5 V $\pm$ 100 mV    | LVTTL Mode (Note 5) |

4. Short  $V_{CF}$  (pin 8) and  $V_{EF}$  (pin 7).

5. When Operating in LVTTL Mode, the reference voltage can be provided by connecting an external resistor,  $R_{CF}$  (suggested resistor value is 2.2 k $\Omega$   $\pm$  5%), between  $V_{CF}$  and  $V_{EE}$  pins.

Table 4. DATA INPUT ALLOWED OPERATING VOLTAGE MODE TABLE

| POWER SUPPLY              | CONTROL DATA SELECT INPUTS PINS (D [0:10]) |       |        |        |
|---------------------------|--------------------------------------------|-------|--------|--------|
|                           | LVC MOS                                    | LVTTL | LVPECL | LVNECL |
| PECL Mode Operating Range | YES                                        | YES   | YES    | N/A    |
| NECL Mode Operating Range | N/A                                        | N/A   | N/A    | YES    |



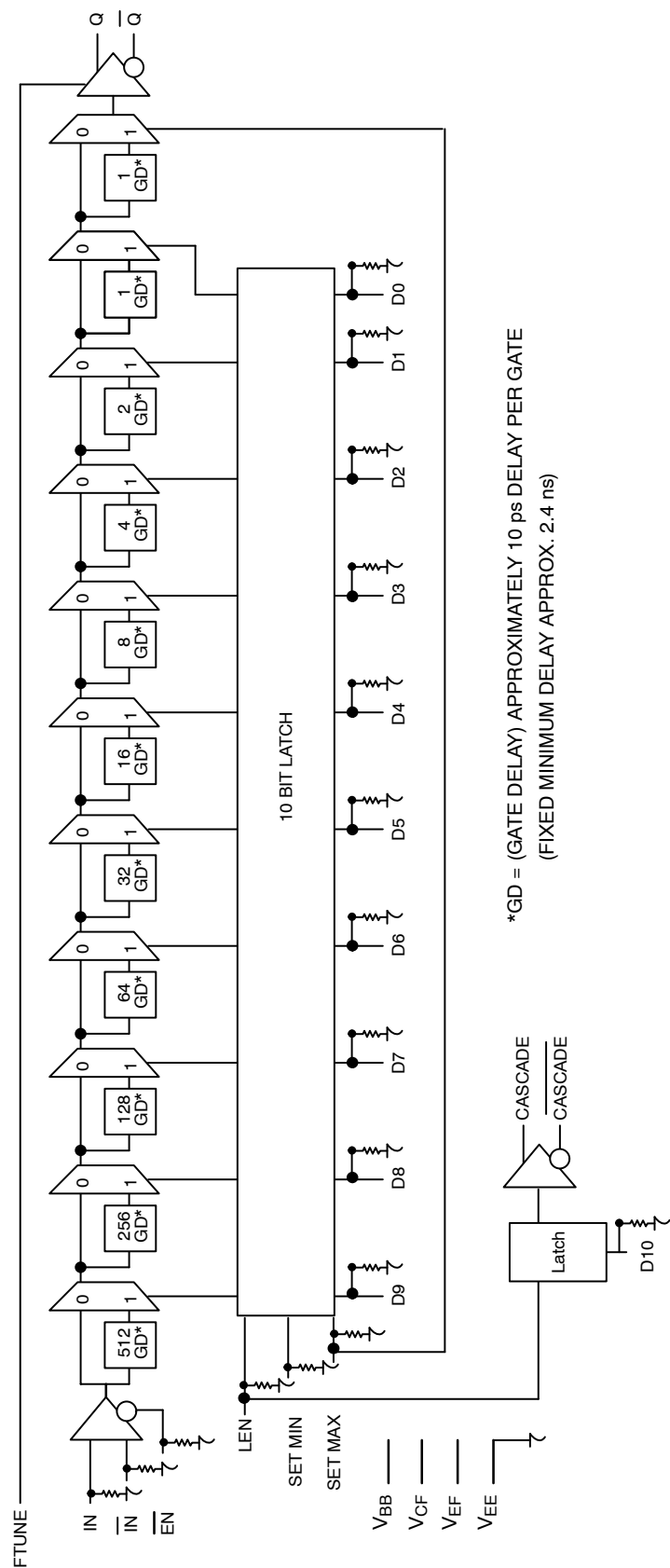


Figure 2. Logic Diagram

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**Table 5. THEORETICAL DELTA DELAY VALUES**

| D(9:0) Value | SETMIN | SETMAX | Programmable Delay* |
|--------------|--------|--------|---------------------|
| XXXXXXXXXX   | H      | L      | 0 ps                |
| 0000000000   | L      | L      | 0 ps                |
| 0000000001   | L      | L      | 10 ps               |
| 0000000010   | L      | L      | 20 ps               |
| 0000000011   | L      | L      | 30 ps               |
| 0000000100   | L      | L      | 40 ps               |
| 0000000101   | L      | L      | 50 ps               |
| 0000000110   | L      | L      | 60 ps               |
| 0000000111   | L      | L      | 70 ps               |
| 0000001000   | L      | L      | 80 ps               |
| 0000010000   | L      | L      | 160 ps              |
| 0000100000   | L      | L      | 320 ps              |
| 0001000000   | L      | L      | 640 ps              |
| 0010000000   | L      | L      | 1280 ps             |
| 0100000000   | L      | L      | 2560 ps             |
| 1000000000   | L      | L      | 5120 ps             |
| 1111111111   | L      | L      | 10230 ps            |
| XXXXXXXXXX   | L      | H      | 10240 ps            |

\*Fixed minimum delay not included.

**Table 6. TYPICAL FTUNE DELAY PIN**

| Input Range         | Output Range |
|---------------------|--------------|
| $V_{CC}-V_{EE}$ (V) | 0 – 60 (ps)  |

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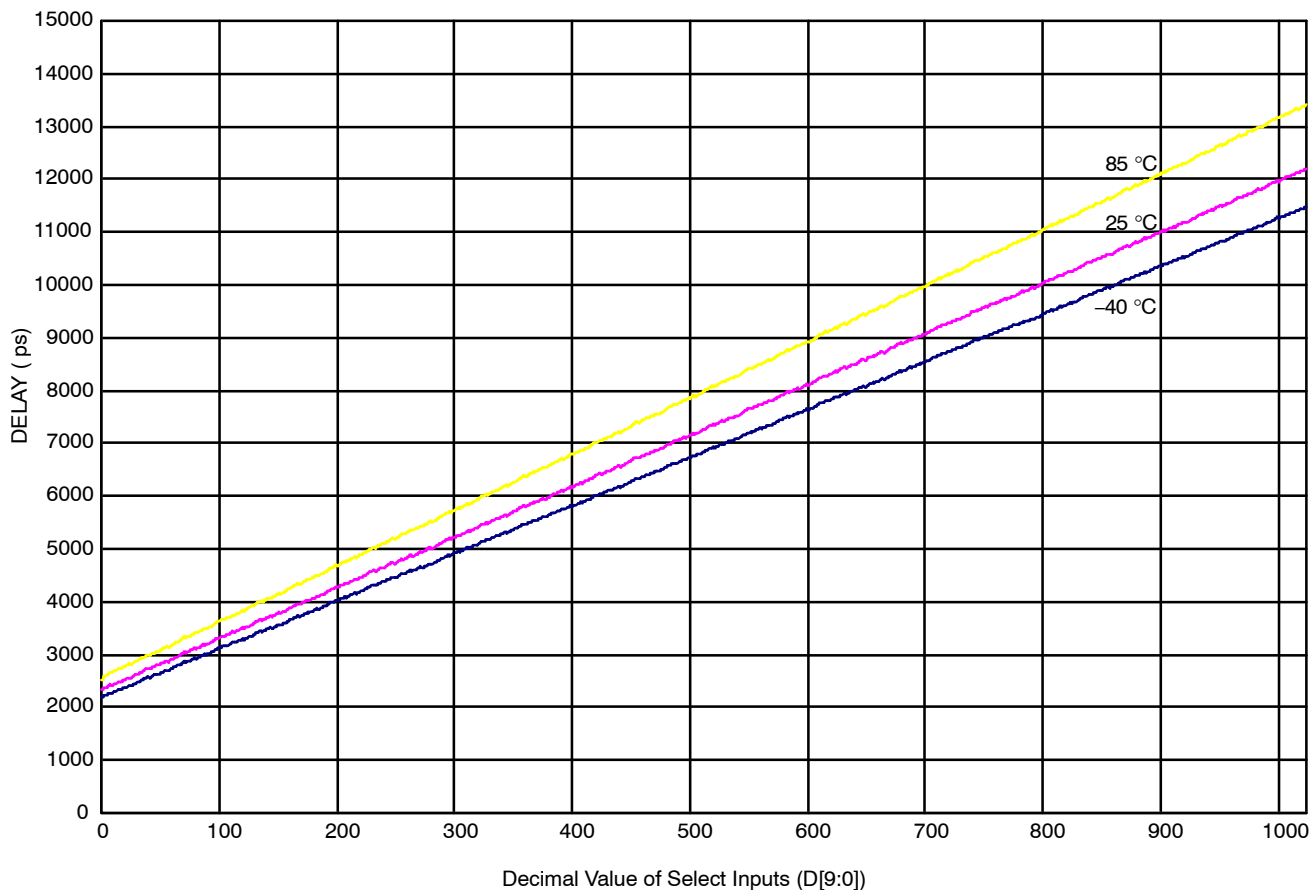


**Figure 3. Measured Delay vs. Select Inputs**

**Table 7. ATTRIBUTES**

| Characteristics                                               |                      | Value                |
|---------------------------------------------------------------|----------------------|----------------------|
| Internal Input Pulldown Resistor                              |                      | 75 kΩ                |
| Internal Input Pullup Resistor                                |                      | N/A                  |
| ESD Protection                                                | Human Body Model     | > 2 kV               |
|                                                               | Machine Model        | > 100 V              |
|                                                               | Charged Device Model | > 2 kV               |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) |                      | Pb-Free Pkg          |
| LQFP-32                                                       |                      | Level 2              |
| Flammability Rating Oxygen Index: 28 to 34                    |                      | UL 94 V-0 @ 0.125 in |
| Transistor Count                                              |                      | 1237 Devices         |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                      |                      |

1. For additional information, see Application Note AND8003/D.

Table 8. MAXIMUM RATINGS

| Symbol        | Parameter                                | Condition 1           | Condition 2       | Rating      | Units |
|---------------|------------------------------------------|-----------------------|-------------------|-------------|-------|
| $V_{CC}$      | PECL Mode Power Supply                   | $V_{EE} = 0\text{ V}$ |                   | 6           | V     |
| $V_{EE}$      | NECL Mode Power Supply                   | $V_{CC} = 0\text{ V}$ |                   | -6          | V     |
| $V_I$         | PECL Mode Input Voltage                  | $V_{EE} = 0\text{ V}$ | $V_I \leq V_{CC}$ | 6           | V     |
|               | NECL Mode Input Voltage                  | $V_{CC} = 0\text{ V}$ | $V_I \geq V_{EE}$ | -6          | V     |
| $I_{out}$     | Output Current                           | Continuous<br>Surge   |                   | 50          | mA    |
|               |                                          |                       |                   | 100         | mA    |
| $I_{BB}$      | $V_{BB}$ Sink/Source                     |                       |                   | $\pm 0.5$   | mA    |
| $T_A$         | Operating Temperature Range              |                       |                   | -40 to +85  | °C    |
| $T_{stg}$     | Storage Temperature Range                |                       |                   | -65 to +150 | °C    |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm                | LQFP-32           | 80          | °C/W  |
|               |                                          | 500 lfpm              | LQFP-32           | 55          | °C/W  |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case)    | Standard Board        | LQFP-32           | 12 to 17    | °C/W  |
| $T_{sol}$     | Wave Solder                      Pb-Free |                       |                   | 265         | °C    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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**Table 9. DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)

| Symbol      | Characteristic                                                                                    | -40°C                |      |                      | 25°C                 |      |                      | 85°C                 |      |                      | Unit          |
|-------------|---------------------------------------------------------------------------------------------------|----------------------|------|----------------------|----------------------|------|----------------------|----------------------|------|----------------------|---------------|
|             |                                                                                                   | Min                  | Typ  | Max                  | Min                  | Typ  | Max                  | Min                  | Typ  | Max                  |               |
| $I_{EE}$    | Power Supply Current                                                                              | 100                  | 125  | 160                  | 110                  | 130  | 170                  | 110                  | 135  | 175                  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)                                                                      | 2155                 | 2300 | 2405                 | 2155                 | 2300 | 2405                 | 2155                 | 2300 | 2405                 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)                                                                       | 1305                 | 1520 | 1605                 | 1305                 | 1500 | 1605                 | 1305                 | 1485 | 1605                 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)<br>LVPECL<br>LVCMOS<br>LVTTL                                    | 2075<br>2000<br>2000 |      | 2420<br>3300<br>3300 | 2075<br>2000<br>2000 |      | 2420<br>3300<br>3300 | 2075<br>2000<br>2000 |      | 2420<br>3300<br>3300 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)<br>LVPECL<br>LVCMOS<br>LVTTL                                     | 1305<br>0<br>0       |      | 1675<br>800<br>800   | 1305<br>0<br>0       |      | 1675<br>800<br>800   | 1305<br>0<br>0       |      | 1675<br>800<br>800   | mV            |
| $V_{BB}$    | Output Voltage Reference                                                                          | 1775                 | 1875 | 1975                 | 1775                 | 1875 | 1975                 | 1775                 | 1875 | 1975                 | mV            |
| $V_{CF}$    | LVTTL Mode Input Detect Voltage<br>@ $I_{V_{CF}} = 700\text{ }\mu\text{A}$                        | 1.4                  | 1.5  | 1.6                  | 1.4                  | 1.5  | 1.6                  | 1.4                  | 1.5  | 1.6                  | V             |
| $V_{EF}$    | Reference Voltage for<br>ECL Mode Connection                                                      | 1900                 | 1960 | 2050                 | 1875                 | 1953 | 2050                 | 1850                 | 1945 | 2050                 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode<br>Range (Differential Configuration)<br>(Note 4)                  | 2.0                  |      | 3.3                  | 2.0                  |      | 3.3                  | 2.0                  |      | 3.3                  | V             |
| $I_{IH}$    | Input HIGH Current (PECL)<br>$I_N, \bar{I}_N, \bar{E}_N, \bar{L}_N, \text{SETMIN}, \text{SETMAX}$ |                      |      | 150                  |                      |      | 150                  |                      |      | 150                  | $\mu\text{A}$ |
| $I_{IHH}$   | FTUNE Input High Current @ $V_{CC}$                                                               | 50                   | 87   | 150                  | 50                   | 84   | 150                  | 50                   | 82   | 150                  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current (PECL)<br>$I_N, \bar{I}_N, \bar{E}_N, \bar{L}_N, \text{SETMIN}, \text{SETMAX}$  | 0.5                  |      |                      | 0.5                  |      |                      | 0.5                  |      |                      | $\mu\text{A}$ |
| $I_{ILL}$   | FTUNE Input LOW Current @ $V_{EE}$                                                                | -10                  | 0    | 10                   | -10                  | 0    | 10                   | -10                  | 0    | 10                   | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -0.3 V.

3. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

4.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 10. DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -3.3\text{ V}$  (Note 5)

| Symbol      | Characteristic                                                                    | -40°C        |       |       | 25°C         |       |       | 85°C         |       |       | Unit          |
|-------------|-----------------------------------------------------------------------------------|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
|             |                                                                                   | Min          | Typ   | Max   | Min          | Typ   | Max   | Min          | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                                              | 100          | 125   | 160   | 110          | 130   | 170   | 110          | 135   | 175   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)                                                      | -1145        | -1000 | -895  | -1145        | -1000 | -895  | -1145        | -1000 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)                                                       | -1995        | -1780 | -1695 | -1995        | -1800 | -1695 | -1995        | -1815 | -1695 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)<br>LVNECL                                       | -1225        |       | -880  | -1225        |       | -880  | -1225        |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)<br>LVNECL                                        | -1995        |       | -1625 | -1995        |       | -1625 | -1995        |       | -1625 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                          | -1525        | -1425 | -1325 | -1525        | -1425 | -1325 | -1525        | -1425 | -1325 | mV            |
| $V_{EF}$    | Reference Voltage for ECL Mode<br>Connection                                      | -1400        | -1340 | -1250 | -1425        | -1347 | -1250 | -1450        | -1355 | -1250 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode<br>Range (Differential Configuration)<br>(Note 7)  | $V_{EE}+2.0$ |       | 0     | $V_{EE}+2.0$ |       | 0     | $V_{EE}+2.0$ |       | 0     | V             |
| $I_{IH}$    | Input HIGH Current<br>IN, $\overline{IN}$ , $\overline{EN}$ , LEN, SETMIN, SETMAX |              |       | 150   |              |       | 150   |              |       | 150   | $\mu\text{A}$ |
| $I_{IHH}$   | FTUNE Input High Current @ $V_{CC}$                                               | 50           | 87    | 150   | 50           | 84    | 150   | 50           | 82    | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current<br>IN, $\overline{IN}$ , $\overline{EN}$ , LEN, SETMIN, SETMAX  | 0.5          |       |       | 0.5          |       |       | 0.5          |       |       | $\mu\text{A}$ |
| $I_{ILL}$   | FTUNE Input LOW Current @ $V_{EE}$                                                | -10          | 0     | 10    | -10          | 0     | 10    | -10          | 0     | 10    | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -0.3 V.

6. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 11. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-3.6\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 8)

| Symbol                 | Characteristic                                                                                                                    | -40°C                       |                                                                  |                              | 25°C                         |                                                                   |                              | 85°C                         |                                                                   |                              | Unit |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------------------------------------------------------------------|------------------------------|------------------------------|-------------------------------------------------------------------|------------------------------|------------------------------|-------------------------------------------------------------------|------------------------------|------|
|                        |                                                                                                                                   | Min                         | Typ                                                              | Max                          | Min                          | Typ                                                               | Max                          | Min                          | Typ                                                               | Max                          |      |
| $f_{\max}$             | Maximum Frequency                                                                                                                 |                             | 1.2                                                              |                              |                              | 1.2                                                               |                              |                              | 1.2                                                               |                              | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>IN to Q; D(0-9) = 0<br>IN to Q; D(0-9) = 1023<br>$\overline{EN}$ to Q; D(0-9) = 0<br>D10 to CASCADE          | 1810<br>9500<br>1780<br>350 | 2210<br>11496<br>2277<br>450                                     | 2610<br>13500<br>2780<br>550 | 1960<br>10000<br>1930<br>380 | 2360<br>12258<br>2430<br>477                                      | 2760<br>14000<br>2930<br>580 | 2180<br>10955<br>2150<br>420 | 2580<br>13454<br>2650<br>520                                      | 2980<br>15955<br>3150<br>620 | ps   |
| $t_{\text{RANGE}}$     | Programmable Range<br>{D(0-9) = HI} - {D(0-9) = LO}                                                                               | 8600                        | 9285                                                             | 10000                        | 9200                         | 9897                                                              | 10700                        | 9900                         | 10875                                                             | 12000                        | ps   |
| $\Delta t$             | Step Delay (Note 9)<br>D0 High<br>D1 High<br>D2 High<br>D3 High<br>D4 High<br>D5 High<br>D6 High<br>D7 High<br>D8 High<br>D9 High |                             | 7<br>23<br>39<br>58<br>137<br>293<br>590<br>1158<br>2317<br>4647 |                              |                              | 11<br>30<br>48<br>67<br>149<br>313<br>629<br>1237<br>2472<br>4955 |                              |                              | 13<br>32<br>53<br>73<br>154<br>337<br>681<br>1353<br>2712<br>5440 |                              | ps   |
| Mono                   | Monotonicity (Note 10)                                                                                                            |                             |                                                                  |                              |                              |                                                                   |                              |                              |                                                                   |                              | ps   |
| $t_{\text{SKEW}}$      | Duty Cycle Skew (Note 11)<br>$ t_{PHL} - t_{PLH} $                                                                                |                             | 20                                                               |                              |                              | 22                                                                |                              |                              | 27                                                                |                              | ps   |
| $t_s$                  | Setup Time<br>D to LEN<br>D to IN (Note 12)<br>EN to IN (Note 13)                                                                 | 150<br>100<br>150           | -10<br>-130<br>-105                                              |                              | 150<br>100<br>150            | -70<br>-150<br>-120                                               |                              | 150<br>100<br>150            | -70<br>-165<br>-140                                               |                              | ps   |
| $t_h$                  | Hold Time<br>LEN to D<br>IN to $\overline{EN}$ (Note 14)                                                                          | 225<br>450                  | 170<br>275                                                       |                              | 200<br>450                   | 70<br>305                                                         |                              | 200<br>450                   | 60<br>325                                                         |                              | ps   |
| $t_R$                  | Release Time<br>EN to IN (Note 15)<br>SET MAX to LEN<br>SET MIN to LEN                                                            | 150<br>400<br>300           | -105<br>70<br>165                                                |                              | 150<br>400<br>350            | -120<br>110<br>180                                                |                              | 150<br>400<br>350            | -140<br>160<br>205                                                |                              | ps   |
| $t_{jit}$              | Random Clock Jitter<br>@ 1.2 GHz, SETMAX Delay                                                                                    |                             | 3                                                                |                              |                              | 3                                                                 |                              |                              | 3                                                                 |                              | ps   |
| $V_{PP}$               | Input Voltage Swing<br>(Differential Configuration)                                                                               | 150                         | 800                                                              | 1200                         | 150                          | 800                                                               | 1200                         | 150                          | 800                                                               | 1200                         | mV   |
| $t_r$<br>$t_f$         | Output Rise/Fall Time<br>20-80% (Q)<br>20-80% (CASCADE)                                                                           | 85<br>100                   | 110<br>150                                                       | 130<br>200                   | 95<br>110                    | 120<br>160                                                        | 145<br>210                   | 110<br>125                   | 135<br>175                                                        | 160<br>225                   | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

9. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.

10. The monotonicity indicates the increased delay value for each binary count increment on the control inputs D(0-9).

11. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.

12. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.

13. This setup time is the minimum time that EN must be asserted prior to the next transition of IN/ $\overline{IN}$  to prevent an output response greater than  $V_{CC} - 1425\text{ mV}$  to that IN/ $\overline{IN}$  transition.

14. This hold time is the minimum time that  $\overline{EN}$  must remain asserted after a negative going IN or positive going  $\overline{IN}$  to prevent an output response greater than  $V_{CC} - 1425\text{ mV}$  to that IN/ $\overline{IN}$  transition.

15. This release time is the minimum time that EN must be deasserted prior to the next IN/ $\overline{IN}$  transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.

## MC100EP196

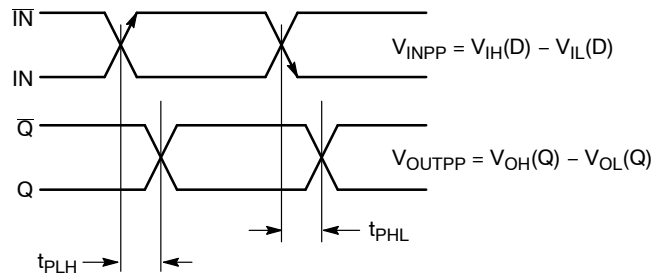


Figure 4. AC Reference Measurement

### USING THE FTUNE ANALOG INPUT

The analog FTUNE pin on the EP196 device is intended to add more delay in a tunable gate to enhance the 10 ps resolution capabilities of the fully digital EP196. The level of resolution obtained is dependent on the voltage applied to the FTUNE pin.

To provide this further level of resolution, the FTUNE pin must be capable of adjusting the additional delay finer than the 10 ps digital resolution (See Logic Diagram). This requirement is easily achieved because a 60 ps additional delay can be obtained over the entire FTUNE voltage range (See Figure 5). This extra analog range ensures that the

FTUNE pin will be capable even under worst case conditions of covering a digital resolution. Typically, the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, Figure 5 should be used. There are numerous voltage ranges which can be used to cover a given delay range; users are given the flexibility to determine which one best fits their designs.

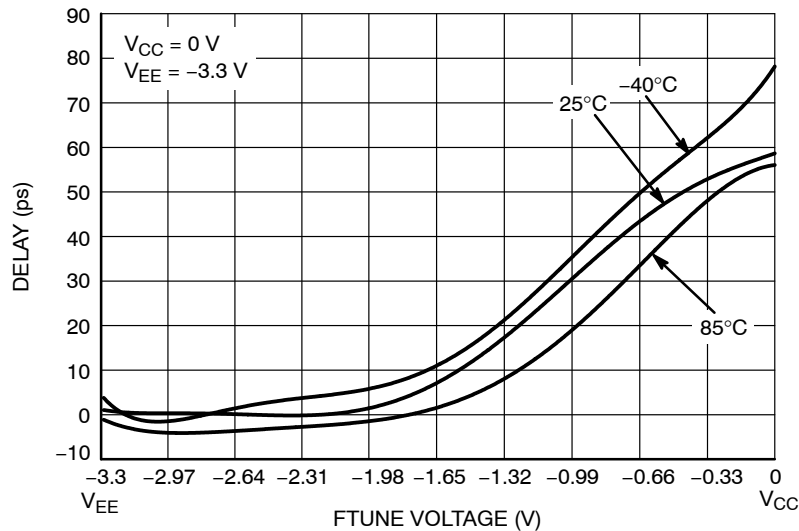


Figure 5. Typical EP196 Delay versus FTUNE Voltage

### CASCADING MULTIPLE EP196S

To increase the programmable range of the EP196, internal cascade circuitry has been included. This circuitry allows for the cascading of multiple EP196s without the need for any external gating. Furthermore, this capability requires only one more address line per added EP196. Obviously, cascading multiple programmable delay chips will result in a larger programmable range; however, this increase is at the expense of a longer minimum delay.

Figure 6 illustrates the interconnect scheme for cascading two EP196s. As can be seen, this scheme can easily be

expanded for larger EP196 chains. The D10 input of the EP196 is the cascade control pin and when assert **HIGH** switches output pin **CASCADE** to **HIGH** and pin **CASCADE** to **LOW**. With the interconnect scheme of Figure 6 when D10 is asserted, it signals the need for a larger programmable range than is achievable with a single device. The A11 address can be added to generate a cascade output for the next EP196. For a 2-device configuration, A11 is not required.

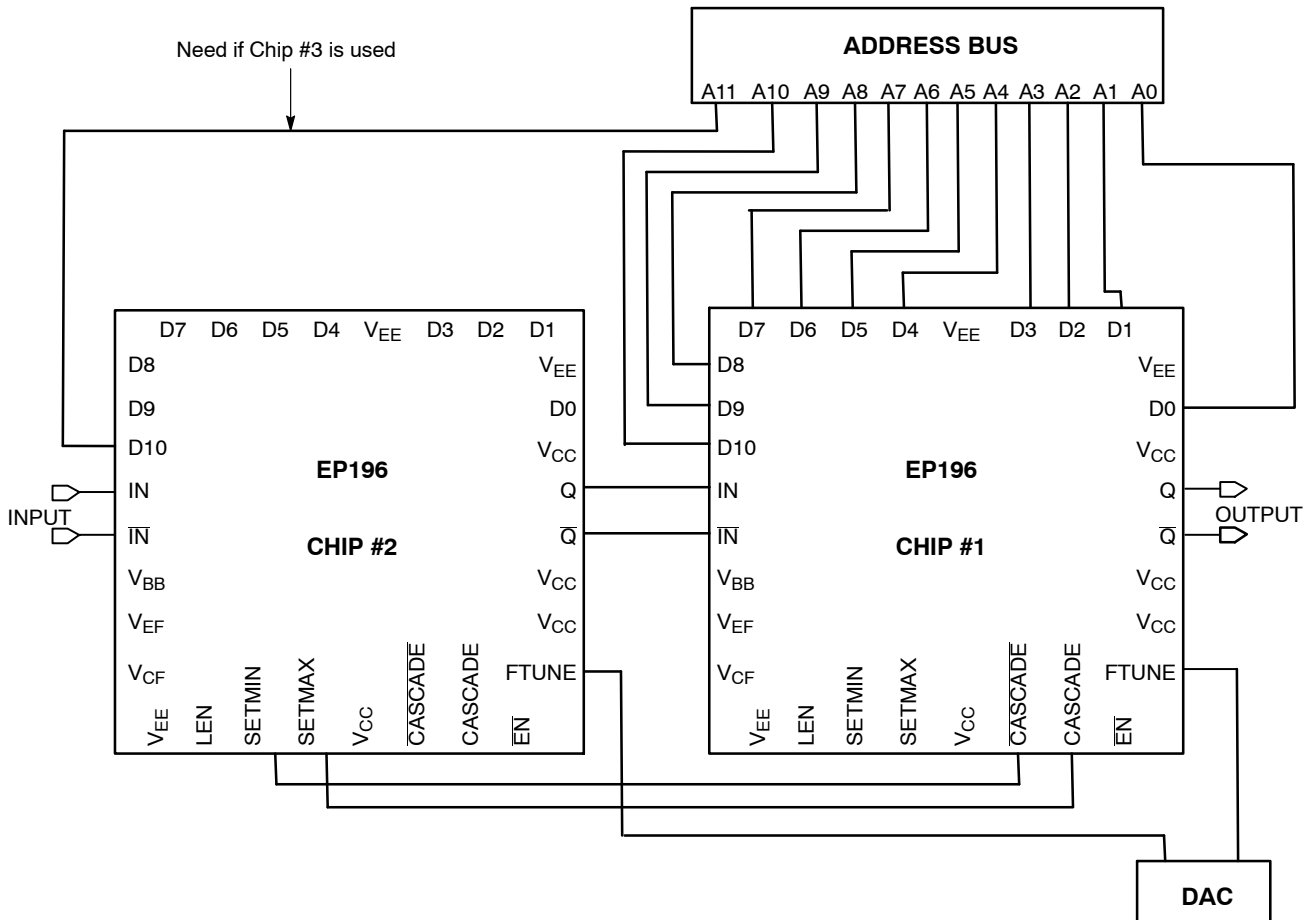


Figure 6. Cascading Interconnect Architecture

## MC100EP196

An expansion of the latch section of the block diagram is pictured in Figure 7. Use of this diagram will simplify the explanation of how the SETMIN and SETMAX circuitry works in cascade. When D10 of chip #1 in Figure 5 is LOW, this device's cascade output will also be LOW while the CASCADE output will be HIGH. In this condition, the SETMIN pin of chip #2 will be asserted HIGH and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay.

Chip #1, on the other hand, will have both SETMIN and SETMAX deasserted so that its delay will be controlled entirely by the address bus A0–A9. If the delay needed is greater than can be achieved with 1023 gate delays (111111111 on the A0–A9 address bus), D10 will be asserted to signal the need to cascade the delay to the next EP196 device. When D10 is asserted, the SETMIN pin of

chip #2 will be deasserted and the SETMAX pin asserted, resulting in the device delay to be the maximum delay. Table 12 shows the delay time of two EP196 chips in cascade.

To expand this cascading scheme to more devices, one simply needs to connect the D10 pin from the next chip to the address bus and CASCADE outputs to the next chip in the same manner as pictured in Figure 6. The only addition to the logic is the increase of one line to the address bus for cascade control of the second programmable delay chip.

Furthermore, to fully utilize EP196, the FTUNE pin can be used for additional delay and for finer resolution than 10 ps. As shown in Figure 5, an analog voltage input from DAC can adjust the FTUNE pin with an extra 60 ps of delay for each chip.

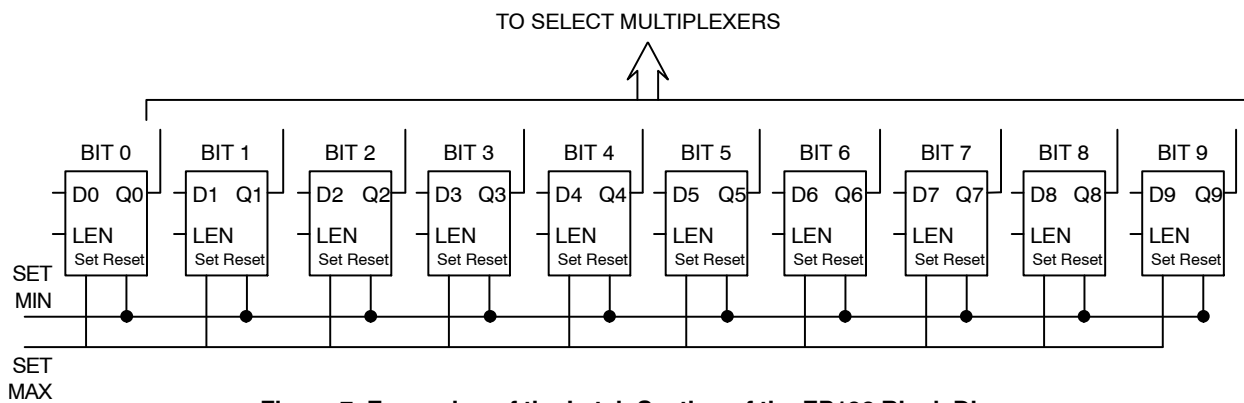


Figure 7. Expansion of the Latch Section of the EP196 Block Diagram

# MC100EP196

Table 12. CASCADED DELAY VALUE OF TWO EP196S

| VARIABLE INPUT TO CHIP #1 AND SETMIN FOR CHIP #2 |    |    |    |    |    |    |    |    |    |    |             |             |
|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|-------------|-------------|
| INPUT FOR CHIP #1                                |    |    |    |    |    |    |    |    |    |    | Total       |             |
| D10                                              | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Delay Value | Delay Value |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 ps        | 4400 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 10 ps       | 4410 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 20 ps       | 4420 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 30 ps       | 4430 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 40 ps       | 4440 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 50 ps       | 4450 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 60 ps       | 4460 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 70 ps       | 4470 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 80 ps       | 4480 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 160 ps      | 4560 ps     |
| 0                                                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 320 ps      | 4720 ps     |
| 0                                                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 640 ps      | 5040 ps     |
| 0                                                | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1280 ps     | 5680 ps     |
| 0                                                | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 2560 ps     | 6960 ps     |
| 0                                                | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 5120 ps     | 9520 ps     |
| 0                                                | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 10230 ps    | 14630 ps    |

| VARIABLE INPUT TO CHIP #1 AND SETMAX FOR CHIP #2 |    |    |    |    |    |    |    |    |    |    |             |             |
|--------------------------------------------------|----|----|----|----|----|----|----|----|----|----|-------------|-------------|
| INPUT FOR CHIP #1                                |    |    |    |    |    |    |    |    |    |    | Total       |             |
| D10                                              | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Delay Value | Delay Value |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 10240 ps    | 14640 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 10250 ps    | 14650 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 10260 ps    | 14660 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 10270 ps    | 14670 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 10280 ps    | 14680 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 10290 ps    | 14690 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 10300 ps    | 14700 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 10310 ps    | 14710 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 10320 ps    | 14720 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 10400 ps    | 14800 ps    |
| 1                                                | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 10560 ps    | 14960 ps    |
| 1                                                | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 10880 ps    | 15280 ps    |
| 1                                                | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 11520 ps    | 15920 ps    |
| 1                                                | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 12800 ps    | 17200 ps    |
| 1                                                | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 15360 ps    | 19760 ps    |
| 1                                                | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 20470 ps    | 24870 ps    |



## MULTI-CHANNEL DESKEWING

The most practical application for EP196 is in multiple channel delay matching. Slight differences in impedance and cable length can create large timing skews within a high-speed system. To deskew multiple signal channels, each channel can be sent through each EP196 as shown in

Figure 8. One signal channel can be used as reference and the other EP196s can be used to adjust the delay to eliminate the timing skews. Nearly any high-speed system can be fine tuned (as small as 10 ps) to reduce the skew to extremely tight tolerances using the available FTUNE pin.

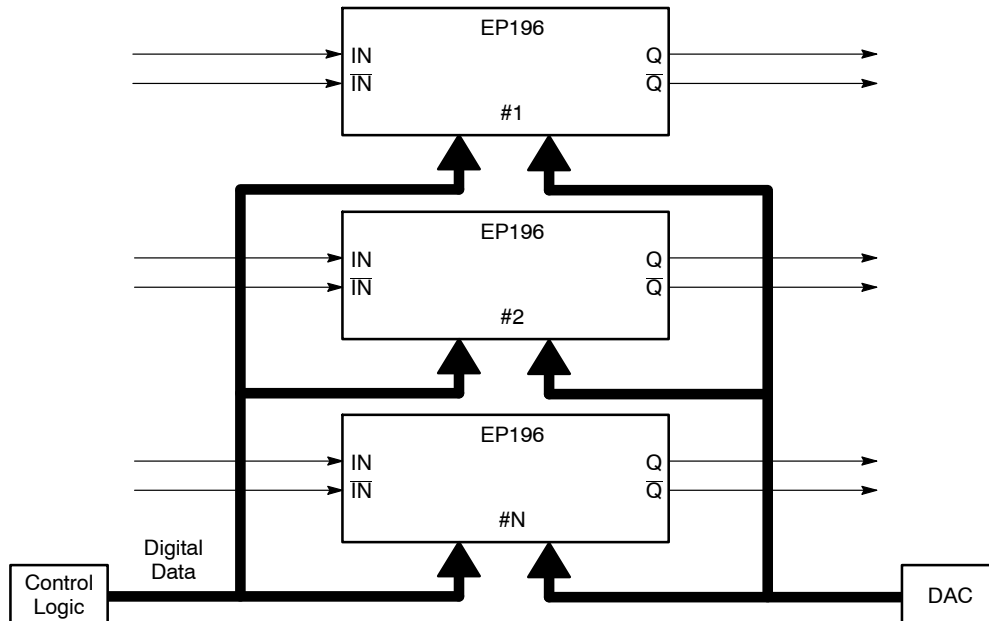


Figure 8. Multiple Channel Deskewing Diagram

## MC100EP196

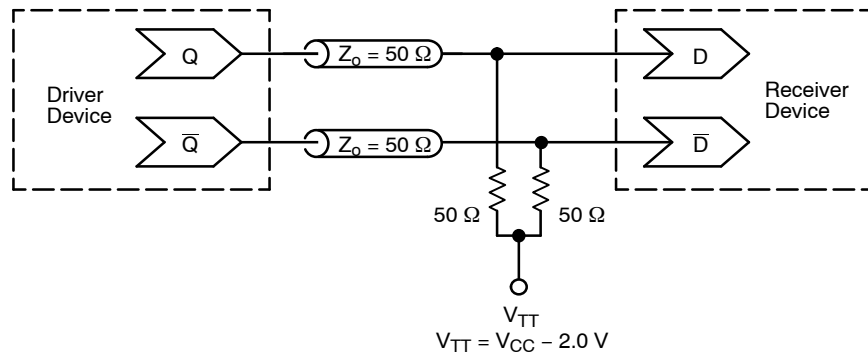


**Figure 9. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

| Device          | Package              | Shipping <sup>†</sup> |
|-----------------|----------------------|-----------------------|
| MC100EP196FAG   | LQFP-32<br>(Pb-Free) | 250 Units / Tray      |
| MC100EP196FAR2G | LQFP-32<br>(Pb-Free) | 2000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

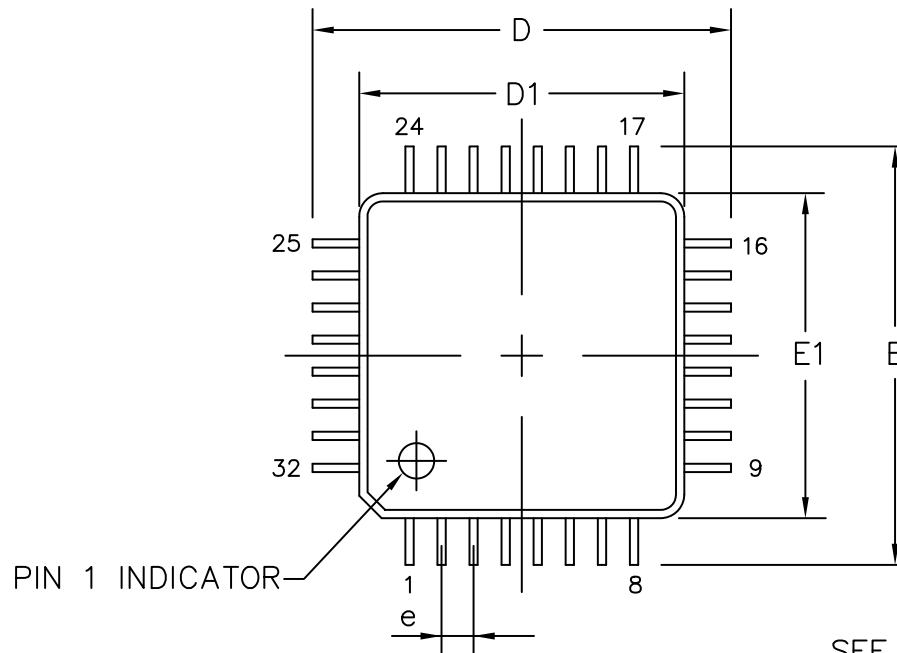
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

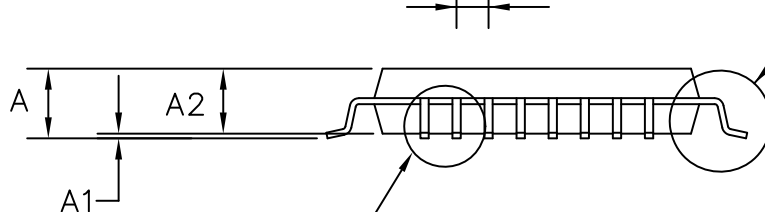
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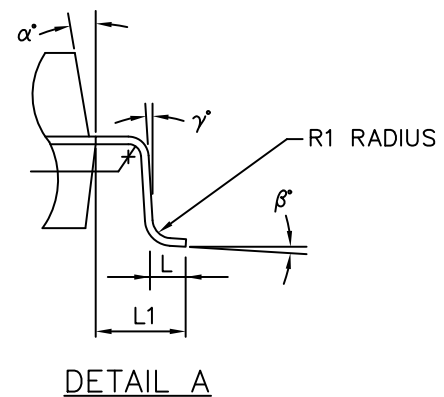
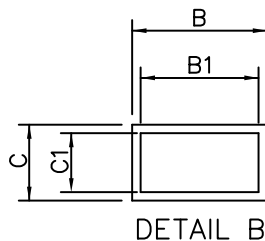


| SYMBOL         | MIN       | NOM  | MAX  |
|----------------|-----------|------|------|
| A              | —         | —    | 1.60 |
| A1             | 0.05      | —    | 0.15 |
| A2             | 1.35      | 1.40 | 1.45 |
| B              | 0.30      | 0.37 | 0.45 |
| B1             | 0.30      | 0.35 | 0.40 |
| C              | 0.09      | —    | 0.20 |
| C1             | 0.09      | —    | 0.16 |
| D              | 9.00 BSC  |      |      |
| D1             | 7.00 BSC  |      |      |
| E              | 9.00 BSC  |      |      |
| E1             | 7.00 BSC  |      |      |
| e              | 0.80 BSC. |      |      |
| L              | 0.45      | 0.60 | 0.75 |
| L1             | 1.00      |      |      |
| R1             | 0.08      | —    | 0.20 |
| $\alpha^\circ$ | 11        | —    | 13   |
| $\beta^\circ$  | 0         | —    | 7    |
| $\gamma^\circ$ | 0         | —    | —    |



SEE DETAIL A

SEE DETAIL B



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