

## 3.3 V/5 V Hex Differential Line Receiver/Driver

### MC100EP116

#### Description

The MC100EP116 is a 6-bit differential line receiver based on the EP16 device. The 3.0 GHz bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below  $V_{CC}$ .

The 100 Series contains temperature compensation.

#### Features

- 260 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 5.5 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to -5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- $V_{BB}$  Output
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



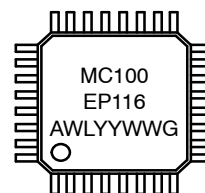
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LQFP-32  
FA SUFFIX  
CASE 561AB

#### MARKING DIAGRAM\*



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

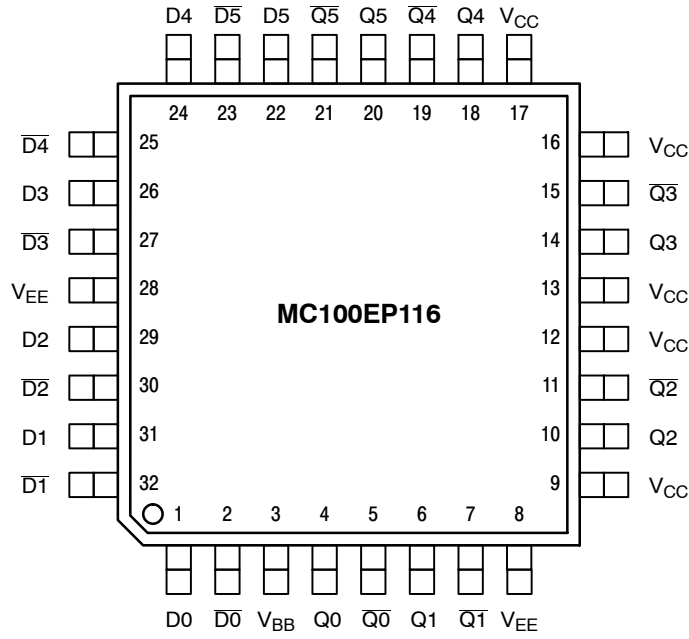
\*For additional marking information, refer to Application Note [AND8002/D](#).

#### ORDERING INFORMATION

| Device        | Package              | Shipping†        |
|---------------|----------------------|------------------|
| MC100EP116FAG | LQFP-32<br>(Pb-Free) | 250 Units / Tray |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

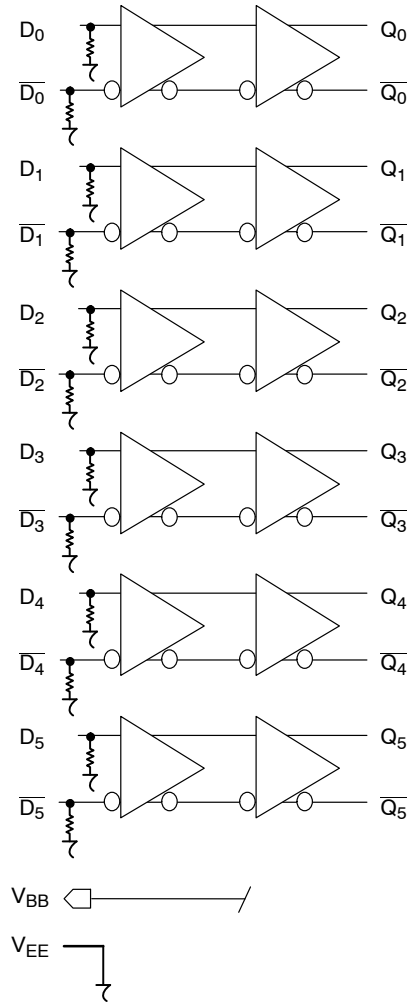


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

| PIN                            | FUNCTION                      |
|--------------------------------|-------------------------------|
| D[0:5]*, $\overline{D}$ [0:5]* | ECL Differential Data Inputs  |
| Q[0:5], $\overline{Q}$ [0:5]   | ECL Differential Data Outputs |
| $V_{BB}$                       | Reference Voltage Output      |
| $V_{CC}$                       | Positive Supply               |
| $V_{EE}$                       | Negative Supply               |

\* Pins will default LOW when left open.

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**Table 2. ATTRIBUTES**

| Characteristics                                                             | Value                       |             |
|-----------------------------------------------------------------------------|-----------------------------|-------------|
| Internal Input Pulldown Resistor                                            | 75 kΩ                       |             |
| Internal Input Pullup Resistor                                              | N/A                         |             |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 100 V<br>> 2 kV |             |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)               |                             | Pb-Free Pkg |
| LQFP-32                                                                     |                             | Level 2     |
| Flammability Rating<br>Oxygen Index: 28 to 34                               | UL-94 V-0 @ 0.125 in        |             |
| Transistor Count                                                            | 729 Devices                 |             |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                      |                             |             |

1. For additional information, see Application Note [AND8003/D](#).

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                          | Condition 1                                    | Condition 2                                                          | Rating      | Units |
|------------------|----------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|-------------|-------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |                                                                      | 6           | V     |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |                                                                      | -6          | V     |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6     | V     |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |                                                                      | 50<br>100   | mA    |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |                                                |                                                                      | ±0.5        | mA    |
| T <sub>A</sub>   | Operating Temperature Range                        |                                                |                                                                      | -40 to +85  | °C    |
| T <sub>stg</sub> | Storage Temperature Range                          |                                                |                                                                      | -65 to +150 | °C    |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | 32 LQFP<br>32 LQFP                                                   | 80<br>55    | °C/W  |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | 32 LQFP                                                              | 12 to 17    | °C/W  |
| T <sub>sol</sub> | Wave Solder<br>Pb-Free                             |                                                |                                                                      | 265         | °C    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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**Table 4. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)

| Symbol      | Characteristic                                                             | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                            | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                       | 60    | 75   | 90   | 60   | 80   | 95   | 60   | 85   | 95   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)                                               | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)                                                | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | 1355  |      | 1675 | 1490 |      | 1675 | 1490 |      | 1675 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                   | 1775  | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

3. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

4.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 5. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 5)

| Symbol      | Characteristic                                                             | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|----------------------------------------------------------------------------|-------|------|------|------|------|------|------|------|------|---------------|
|             |                                                                            | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current                                                       | 60    | 75   | 90   | 60   | 80   | 95   | 60   | 85   | 95   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)                                               | 3855  | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)                                                | 3055  | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                          | 3775  |      | 4120 | 3775 |      | 4120 | 3775 |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                           | 3790  |      | 3375 | 3190 |      | 3375 | 3190 |      | 3375 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                   | 3475  | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current                                                         |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                          | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

6. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 6. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 8)

| Symbol      | Characteristic                                                              | -40°C        |       |       | 25°C         |       |       | 85°C         |       |       | Unit          |
|-------------|-----------------------------------------------------------------------------|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
|             |                                                                             | Min          | Typ   | Max   | Min          | Typ   | Max   | Min          | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current                                                        | 60           | 75    | 90    | 60           | 80    | 95    | 60           | 85    | 95    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 9)                                                | -1145        | -1020 | -895  | -1145        | -1020 | -895  | -1145        | -1020 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 9)                                                 | -1945        | -1820 | -1695 | -1945        | -1820 | -1695 | -1945        | -1820 | -1695 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)                                           | -1225        |       | -880  | -1225        |       | -880  | -1225        |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)                                            | -1945        |       | -1625 | -1945        |       | -1625 | -1945        |       | -1625 | mV            |
| $V_{BB}$    | Output Voltage Reference                                                    | -1525        | -1425 | -1325 | -1525        | -1425 | -1325 | -1525        | -1425 | -1325 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10) | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current                                                          |              |       | 150   |              |       | 150   |              |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current                                                           | 0.5          |       |       | 0.5          |       |       | 0.5          |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .

9. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

10.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 7. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 11)

| Symbol                   | Characteristic                                                       | -40°C |     |            | 25°C |     |            | 85°C |     |            | Unit |
|--------------------------|----------------------------------------------------------------------|-------|-----|------------|------|-----|------------|------|-----|------------|------|
|                          |                                                                      | Min   | Typ | Max        | Min  | Typ | Max        | Min  | Typ | Max        |      |
| $f_{\text{max}}$         | Maximum Frequency (See Figure 3 $F_{\text{max}}/\text{JITTER}$ )     |       | > 3 |            |      | > 3 |            |      | > 3 |            | GHz  |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay to Output Differential                             | 160   | 250 | 340        | 160  | 260 | 340        | 190  | 300 | 380        | ps   |
| $t_{\text{SKEW}}$        | Duty Cycle Skew (Note 12)                                            |       | 5.0 | 20         |      | 5.0 | 20         |      | 5.0 | 20         | ps   |
| $t_{\text{SKEW}}$        | Within Device Skew<br>Device to Device Skew (Note 12)                |       |     | 100<br>180 |      |     | 100<br>180 |      |     | 100<br>190 | ps   |
| $t_{\text{JITTER}}$      | Cycle-to-Cycle Jitter (See Figure 3 $F_{\text{max}}/\text{JITTER}$ ) |       | 0.2 | < 1        |      | 0.2 | < 1        |      | 0.2 | < 1        | ps   |
| $V_{PP}$                 | Input Voltage Swing (Differential Configuration)                     | 150   | 800 | 1200       | 150  | 800 | 1200       | 150  | 800 | 1200       | mV   |
| $t_r$ ,<br>$t_f$         | Output Rise/Fall Times<br>(20% - 80%) $Q, \bar{Q}$                   | 90    | 150 | 220        | 90   | 160 | 240        | 90   | 160 | 250        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

11. Measured using a 750 mV source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

12. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

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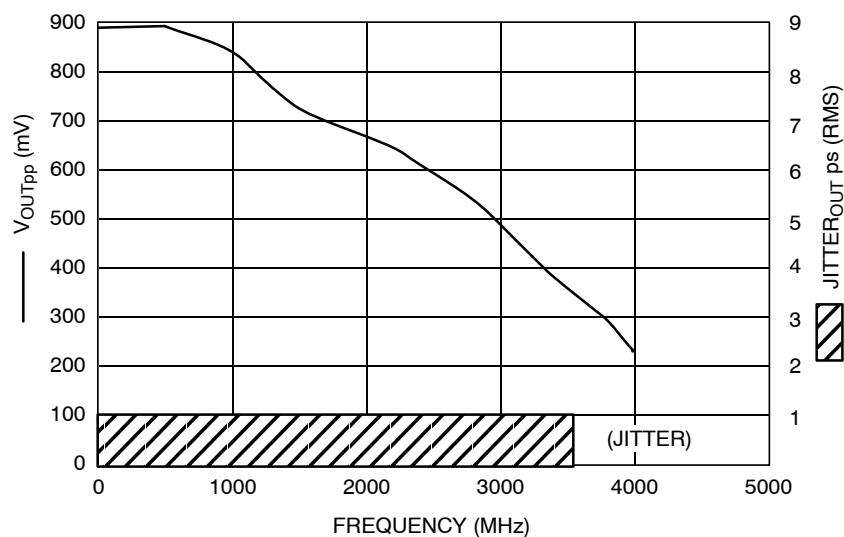


Figure 3.  $F_{max}$ /Jitter

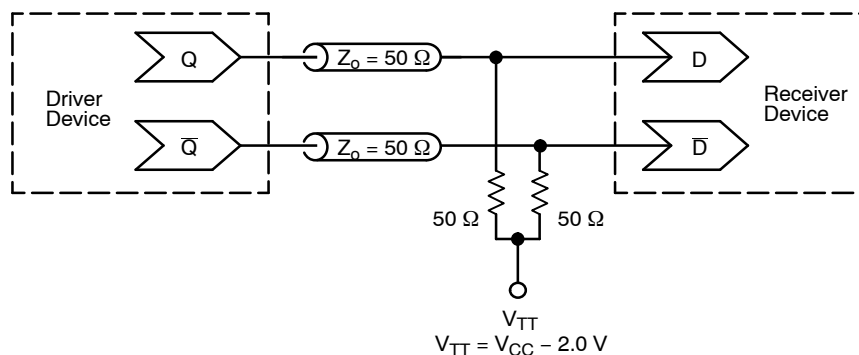


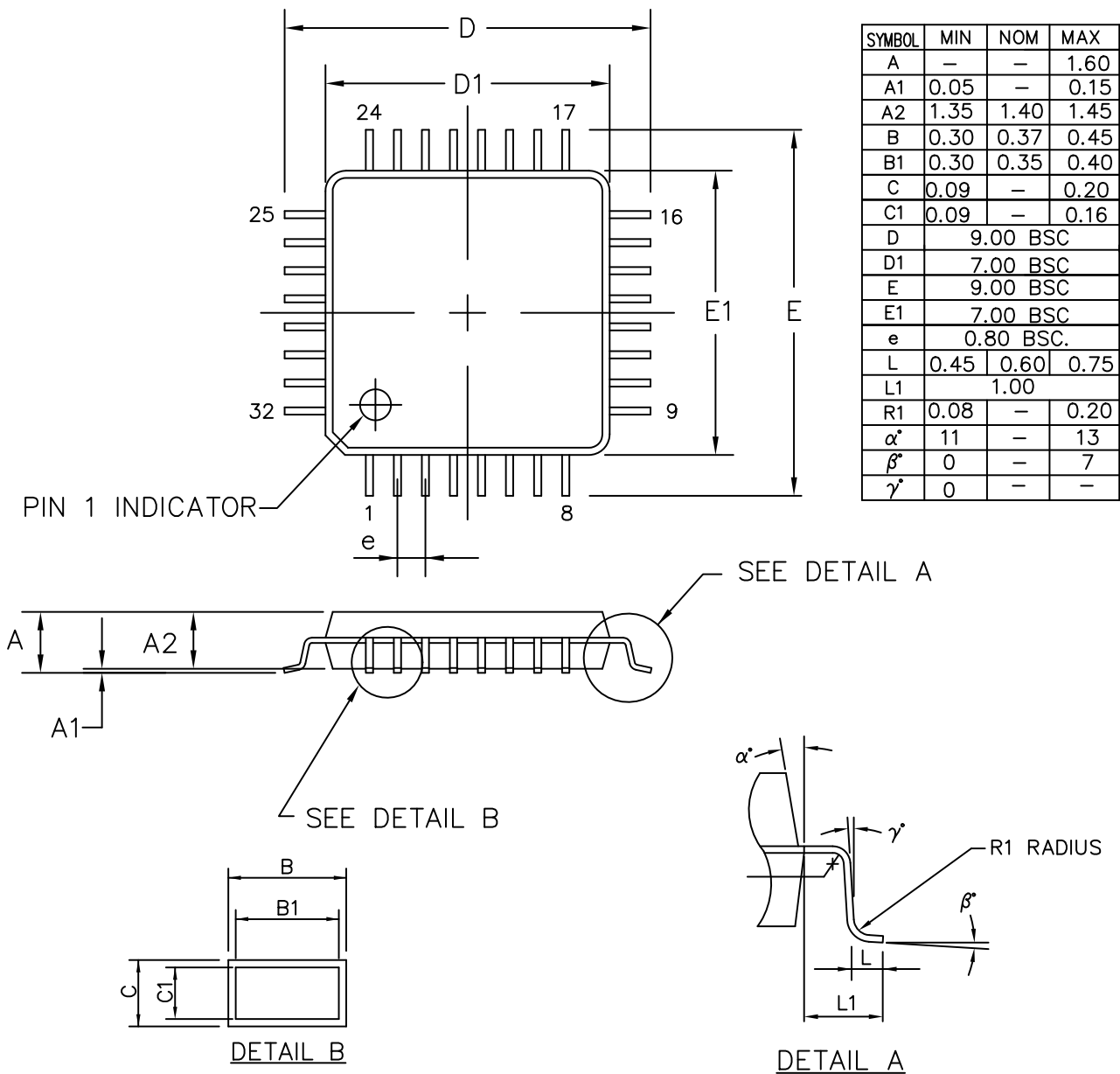
Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

### Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D – Metastability and the ECLinPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1672/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLinPS
- AND8090/D – AC Characteristics of ECL Devices

**LQFP-32, 7x7**  
CASE 561AB  
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