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March 2013

µSerDes™ FIN212AC
12-Bit Serializer / Deserializer Supporting Cameras and Small Displays

Features

Data & Control Bits	12-Bit
Frequency	40MHz
Capability	Camera or LCD
Interface	Microcontroller, RGB, YUV
µController Usage	m68 & i86
Selectable Edge Rates	Yes
Standby Current	<10 µA
Core Voltage ($V_{DDA/S}$)	2.5 to 3.6V
I/O Voltage (V_{DDP})	1.65 to 3.6V
ESD (I/O to GND)	14kV
Package	32-Terminal MLP 42-Ball USS-BGA
Ordering Information	FIN212ACMLX FIN212ACGFX

Description

The FIN212AC µSerDes™ is a low-power serializer / deserializer optimized for use in cell phone displays and camera paths. The device reduces a 12-bit data path to four wires. For camera applications, an additional master clock can be passed in the opposite direction of data flow. The device utilizes Fairchild's proprietary ultra-low power, low-EMI technology.

Applications

- Slider, Folder, & Clamshell Mobile Handsets
- Printers
- Security Cameras

Related Resources

- For samples and questions, please contact: Interface@fairchildsemi.com.

Typical Application

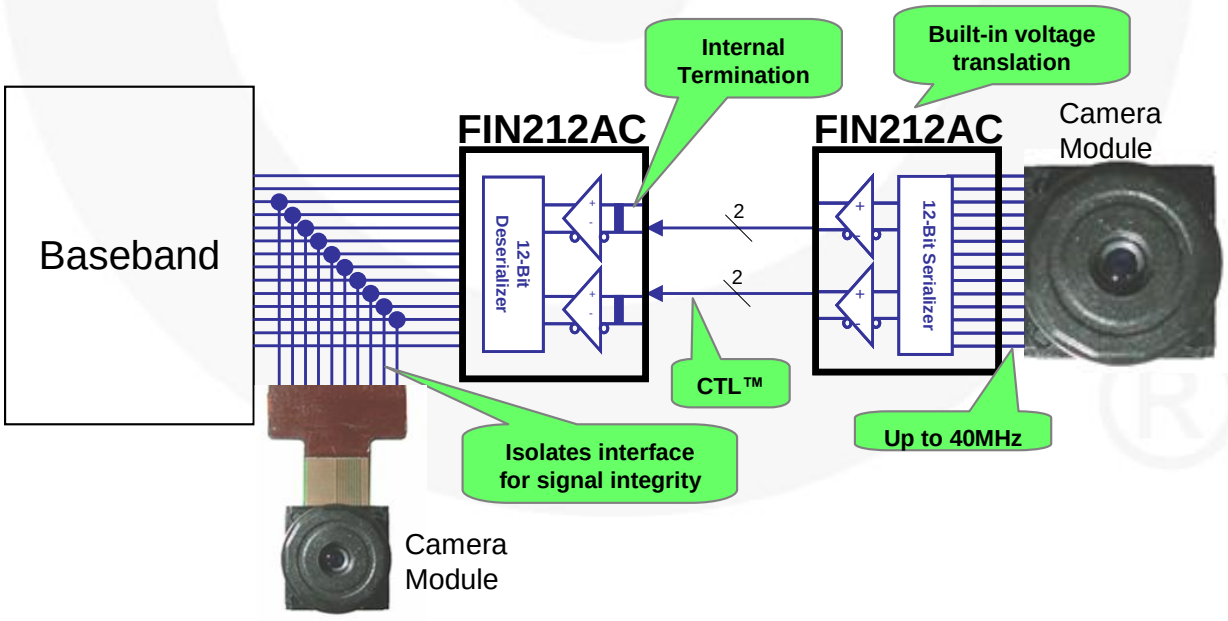

Figure 1. Mobile Phone Example

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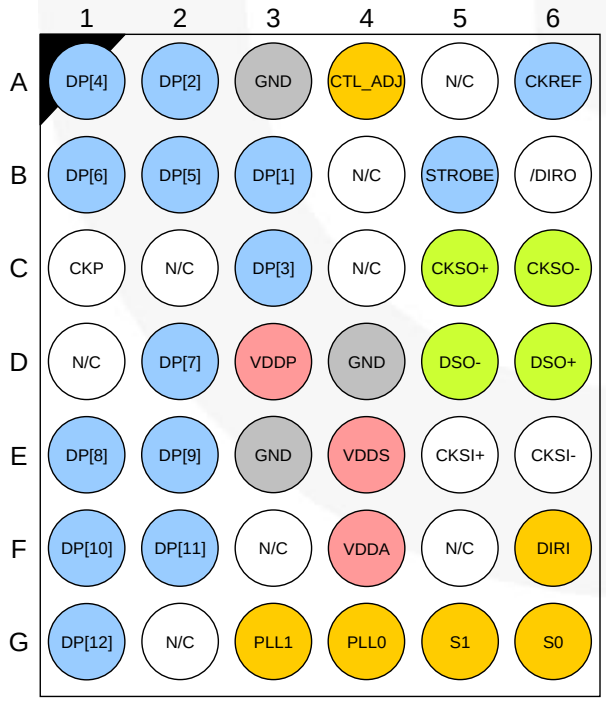
FIN212AC (Serializer DIRI=1) Pin Descriptions

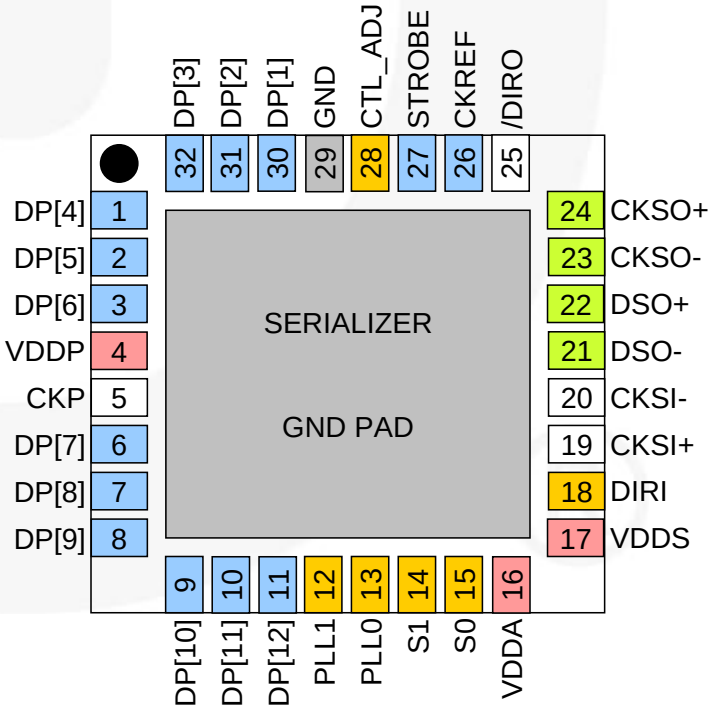
Pin Name	Description		
DIRI	Control to determine serializer or deserializer configuration.	0	Deserializer
		1	Serializer
CTL_ADJ	Adjusts CTL drive to compensate for environmental conditions and length.	0	Low drive (low power)
		1	High drive (high power)
S0	Configure frequency range for the PLL.	See Table 1 Serializer (DIRI=1) Control Pin.	
S1	Configure frequency range for the PLL.	See Table 1 Serializer (DIRI=1) Control Pin.	
PLL0	Divide or adjust the serial frequency.	See Table 1 Serializer (DIRI=1) Control Pin.	
PLL1	Divide or adjust the serial frequency.	See Table 1 Serializer (DIRI=1) Control Pin.	
CKREF	LV-CMOS clock input and PLL reference.		
STROBE	LV-CMOS strobe input for latching data (DP [1:12]) into the serializer on the rising edge.		
DP[1:12]	LV-CMOS parallel data input. (GND input if not used)		
CKSO+ CKSO-	CTL Differential serializer output bit clock. CKSO+: Positive signal; CKSO-: Negative signal.		
DSO+ DSO-	CTL Differential serial output data signals. DSO+: Positive signal; DSO-: Negative signal.		
CKSI+ CKSI-	CTL Differential deserializer input bit clock. CKSI+: Positive signal; CKSI-: Negative signal.	No connect unless in “clock pass-through” mode.	
CKP	LV-CMOS word clock output or Pixel clock output.	No connect unless in “clock pass-through” mode.	
/DIRO	LV-CMOS output, Inversion of DIRI in normal operation. Can be used to drive the DIRI signal of the deserializer where the interface needs to be turned around.	No connect if not used.	
VDDP	Power supply for parallel I/O. (All VDDP pins must be connected to VDDP)		
VDDS	Power supply for serial I/O.		
VDDA	Power supply for core.		
GND	All GND pins must be connected to ground. BGA: all GND pads. MLP: Pin 29 & GND PAD must be grounded.		
N/C	No connect. (Do not connect to GND or VDD)		

Note:
1. 0=GND; 1=VDDP

FIN212AC (Serializer DIRI=1) Pin Configurations



42-Ball BGA, 3.5 x 4.5mm, .5mm pitch (Top View)



32-pin MLP, 5 x 5mm, .5mm pitch (Top View)

Figure 2. FIN212AC (Serializer DIRI=1) Pin Assignments (Top View)

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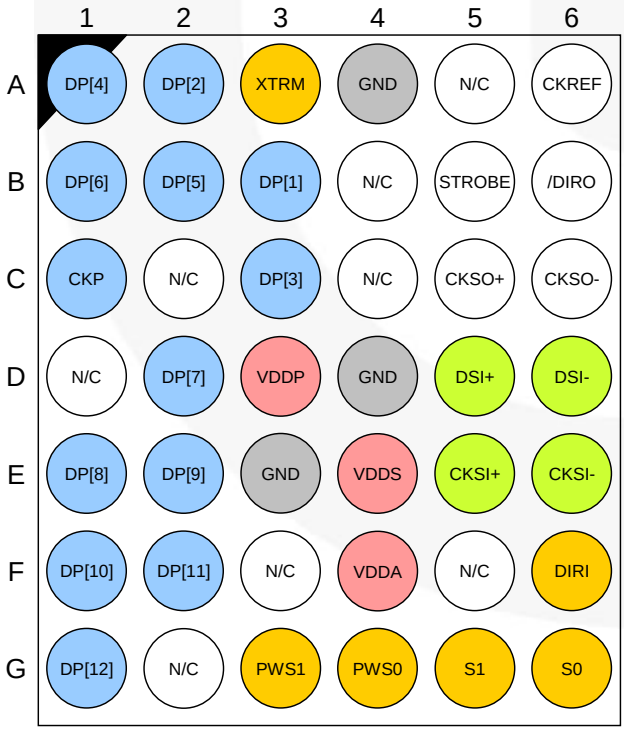
FIN212AC (Deserializer DIRI=0) Pin Descriptions

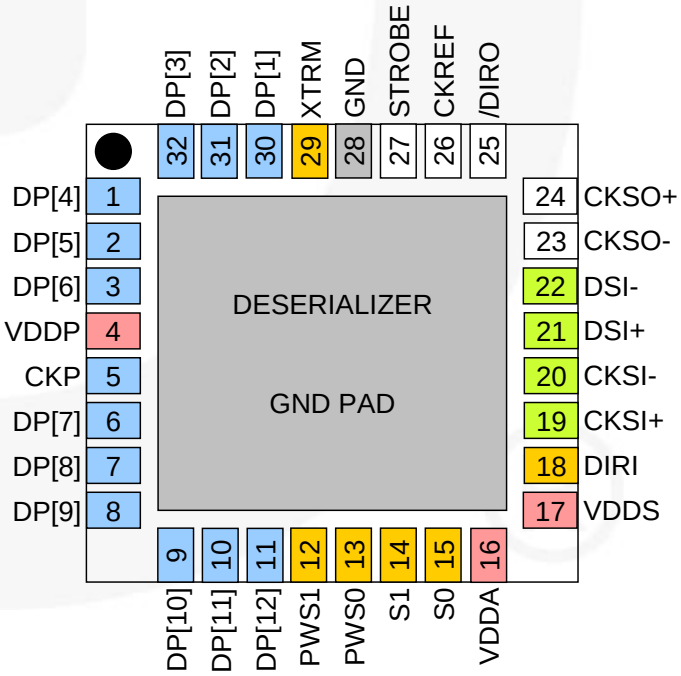
Pin Name	Description		
DIRI	Control to determine serializer or deserializer configuration.	0	Deserializer
		1	Serializer
XTERM	Control to determine if using internal or external termination	0	Internal termination used
		1	External termination required on CKSI & DSI
S0	Signals used to define the edge rate of parallel I/O.	*See Table 2 Deserializer (DIRI=0) Control Pin.*	
S1	Signals used to define the edge rate of parallel I/O.	*See Table 2 Deserializer (DIRI=0) Control Pin.*	
PWS0	Configure CKP pulse width.	*See Table 2 Deserializer (DIRI=0) Control Pin.*	
PWS1	Configure CKP pulse width.	*See Table 2 Deserializer (DIRI=0) Control Pin.*	
DP[1:12]	LV-CMOS parallel data output. (N/C if not used)		
CKP	LV-CMOS word clock output or Pixel clock output.		
DSI+ DSI-	CTL Differential serial input data signals. DSI+: Positive signal; DSI-: Negative signal.		
CKSI+ CKSI-	CTL Differential deserializer input bit clock. CKSI+: Positive signal; CKSI-: Negative signal.		
CKSO+ CKSO-	CTL Differential serializer output bit clock. CKSO+: Positive signal; CKSO-: Negative signal.	No connect unless in “clock pass-through” mode.	
CKREF	LV-CMOS clock input and PLL reference.	No connect unless in “clock pass-through” mode.	
STROBE	LV-CMOS strobe input for latching data into the serializer.	No connect unless in “clock pass-through” mode.	
/DIRO	LV-CMOS Output. Inversion of DIRI in normal operation.	No connect if not used.	
VDDP	Power supply for parallel I/O. (All VDDP pins must be connected to VDDP)		
VDDS	Power supply for serial I/O.		
VDDA	Power supply for core.		
GND	All GND pins must be connected to ground. BGA: all GND pads. MLP: Pin 28, 29, GND PAD must be grounded.		
N/C	No connect. BGA: G1, F2; MLP: 10, 11; (Do not connect to GND or VDD)		

Note:
2. 0=GND; 1=VDDP

FIN212AC (Deserializer DIRI=0) Pin Configurations



42-Ball BGA, 3.5 x 4.5mm, .5mm pitch (Top View)



32-pin MLP, 5mm x 5mm, .5mm pitch (Top View)

Figure 3. FIN212AC (Deserializer DIRI=0) Pin Assignments (Top View)

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System Control Pin

Conditions	Function			Control Pin			
	CKREF	STROBE	PLL Multiplier	PLL0	PLL1	S0	S1
Slow Frequencies							
Normal operation	5MHz to 14MHz	≤ CKREF (Up to 14MHz)	1	1	0	0	1
Supports spread spectrum on CKREF	4.7MHz to 13.3MHz	≤ CKREF (Up to 13.3MHz)	0.954	0	0	0	1
With a fixed CKREF input; STROBE can be 1/2 the speed	5MHz to 14MHz	≤ CKREF / 2 (Up to 7MHz)	2	0	1	0	1
With a fixed CKREF input; STROBE can be 1/3 the speed	5MHz to 14MHz	≤ CKREF / 3 (Up to 4.67MHz)	3	1	1	0	1
Medium Frequencies							
Normal operation	8MHz to 28MHz	≤ CKREF (Up to 28MHz)	1	1	0	1	1
Supports spread spectrum on CKREF	9.5MHz to 26.7MHz	≤ CKREF (Up to 26.7MHz)	0.954	0	0	1	1
With a fixed CKREF input; STROBE can be 1/2 the speed	8MHz to 28MHz	≤ CKREF / 2 (Up to 14MHz)	2	0	1	1	1
With a fixed CKREF input; STROBE can be 1/3 the speed	8MHz to 28MHz	≤ CKREF / 3 (Up to 9.3MHz)	3	1	1	1	1
Fast Frequencies							
Normal operation	20MHz to 40MHz	≤ CKREF (Up to 40MHz)	1	1	0	1	0
Supports spread spectrum on CKREF	19MHz to 38.2MHz	≤ CKREF (Up to 38.2MHz)	0.954	0	0	1	0
With a fixed CKREF input; STROBE can be 1/2 the speed	20MHz to 40MHz	≤ CKREF / 2 (Up to 20MHz)	2	0	1	1	0
With a fixed CKREF input; STROBE can be 1/3 the speed	20MHz to 40MHz	≤ CKREF / 3 (Up to 13.3MHz)	3	1	1	1	0
Power-Down				X	X	0	0

Table 1: Serializer (DIRI=1) Control Pin

LVCMOS Output Edge Rates	CKP to STROBE	CKP Pulse Width Low Time		Reference		Control Pin			
		CKREF=19.2 MHz	CKREF=26 MHz	PLL Multiplier (Serializer)	Pwidth Multiplier	PWS0	PWS1	S0	S1
Slow Frequencies									
~7 – 8ns (C_L=8pF) [Typically for 5MHz to 14MHz signals]	Non-Inverted	52.1ns	38.5ns	2	7	0	0	0	1
	Inverted	52.1ns	38.5ns	2	7	1	0	0	1
	Non-Inverted	96.7ns	71.4ns	2	13	0	1	0	1
	Non-Inverted	126.5ns	93.4ns	2	17	1	1	0	1
Medium Frequencies									
~4 – 5ns (C_L=8pF) [Typically for 8MHz to 28MHz signals]	Non-Inverted	78.1ns	57.7ns	3	7	0	0	1	1
	Inverted	78.1ns	57.7ns	3	7	1	0	1	1
	Non-Inverted	145.1ns	107.1ns	3	13	0	1	1	1
	Non-Inverted	189.7ns	140.1ns	3	17	1	1	1	1
Fast Frequencies									
~2 – 3ns (C_L=8pF) [Typically for 20MHz to 40MHz signals]	Non-Inverted	26ns	19.2ns	1	7	0	0	1	0
	Inverted	26ns	19.2ns	1	7	1	0	1	0
	Non-Inverted	48.4ns	35.7ns	1	13	0	1	1	0
	Non-Inverted	63.2ns	46.7ns	1	17	1	1	1	0
Power-Down						X	X	0	0

Table 2: Deserializer (DIRI=0) Control Pin

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Pulse Width Calculations

CKP Pulse Width Low Time=(PLL Multiplier * Pwidth Multiplier) / (CKREF*14) (1)

Example: CKREF=26MHz; PLL Multiplier=2; Pwidth Multiplier=13

CKP Pulse width=(2 * 13) / (26MHz * 14)=71.4ns (2)

Power-Down States

When both S1 and S0 signals are 0, regardless of the state of the DIRI signal, the FIN212AC resets and powers down. The power-down mode shuts down all internal analog circuitry, disables the serial input and output of the device, and resets all internal digital logic. Table 3: Power-Down indicates the state of the input states and output buffers in Power-Down mode.

Signal Pins	DIRI=1 (Serializer)	DIRI=0 (Deserializer)
DP[12:1]	Inputs Disabled	High-Z
CKP	HIGH	High-Z
STROBE	Input Disabled	Input Disabled
CKREF	Input Disabled	Input Disabled
/DIRO	0	1

Table 3: Power-Down

Clock Pass-Through Mode

Clock pass-through mode allows a harmonic rich clock source to be sent to the serializer in a CTL format to reduce the overall harmonic content of the phone, and can reduce the need for EMI filters. The Master Clock Pass through mode performs a translation to the clock in the CTL link, and does not serialize this signal. The following describes how to enable this functionality for an image sensor *(See Figure 6)*.

Deserializer Configuration (DIRI=0)

1. Connect CKREF(BGA pin A6) to GROUND
2. Connect master clock to STROBE (BGA pin B5)

Serializer Configuration (DIRI=1)

1. CKSI passes master clock to CKP output (BGA pin C1)

CKREF and STROBE Signals

Please note that there is a setup and hold time between STROBE and data that must be met as seen on the electrical characteristics section. The relationship between CKREF and STROBE can be synchronous or asynchronous depending on what is available in the system. It is suggested that if the signals are synchronous and in normal operation that CKREF is tied to STROBE as close to the chip as possible. If you are running an asynchronous or spread spectrum setup, please be aware this may result on cycle jitter on the CKP signal. They cycle jitter does not effect the output data and clock relationship, the display or end application should continue to work as normal.

PLL Note

Please note that the PLL ranges can overlap, power consumption can be reduced by selecting the operation in the lower end of the higher speed PLL range.

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Application Diagrams

The following application diagrams illustrate the most typical applications for the FIN212 device. Specific configurations of the control pins may vary based on the needs of a given system. The following recommendations are valid for all of the applications shown.

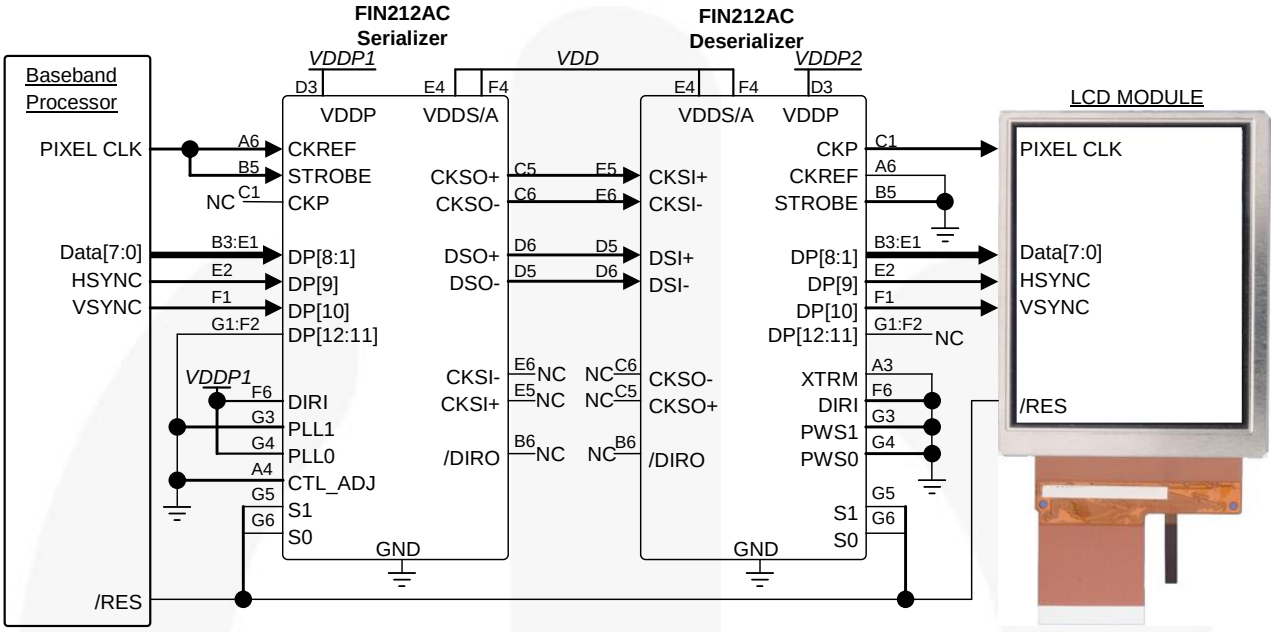

Figure 4. 8-Bit RGB Application (Example Shows BGA 42-Pin Package)

Serializer Configuration:

8MHz to 28MHz Frequency Range (S1=S0=1)

Normal Mode (PLL1=0; PLL0=1)

Deserializer Configuration:

~4 – 5ns output edge rates (S1=S0=1)

~50% CKP PW,(PWS1=PWS0=0)

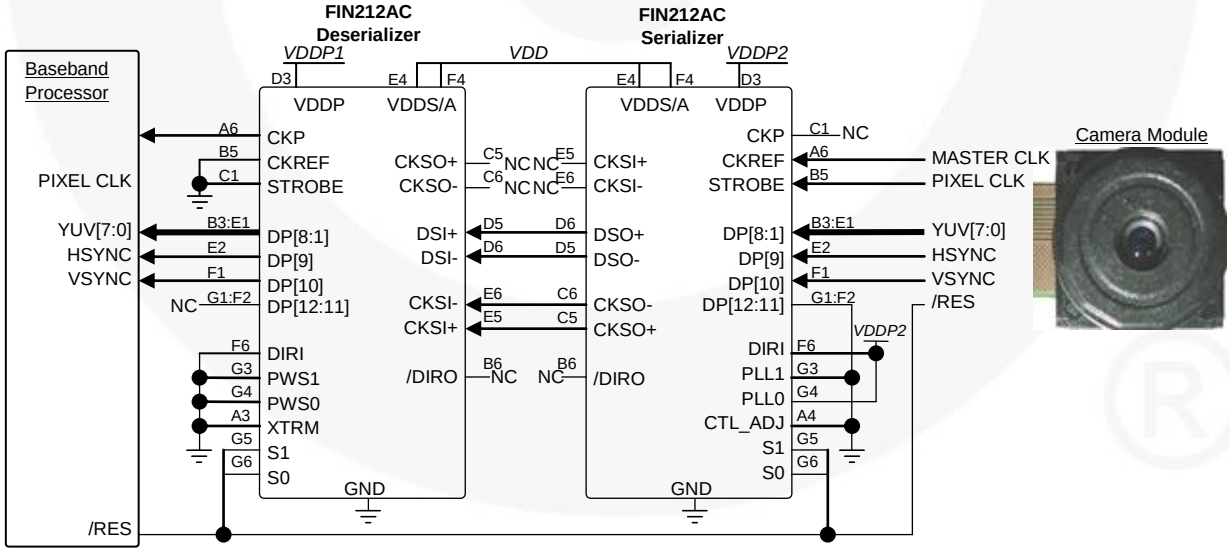

Figure 5. 8-Bit YUV 1.3MPixel CMOS Imager (Example Shows BGA 42-Pin Package)

Deserializer Configuration:

~2 – 3ns output edge rates (S1=0, S0=1)

~50% CKP PW,(PWS1=PWS0=0)

Serializer Configuration:

20MHz to 40MHz Frequency Range (S1=0, S0=1)

Normal Mode (PLL1=0, PLL0=1)

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Application Diagrams (Continued)

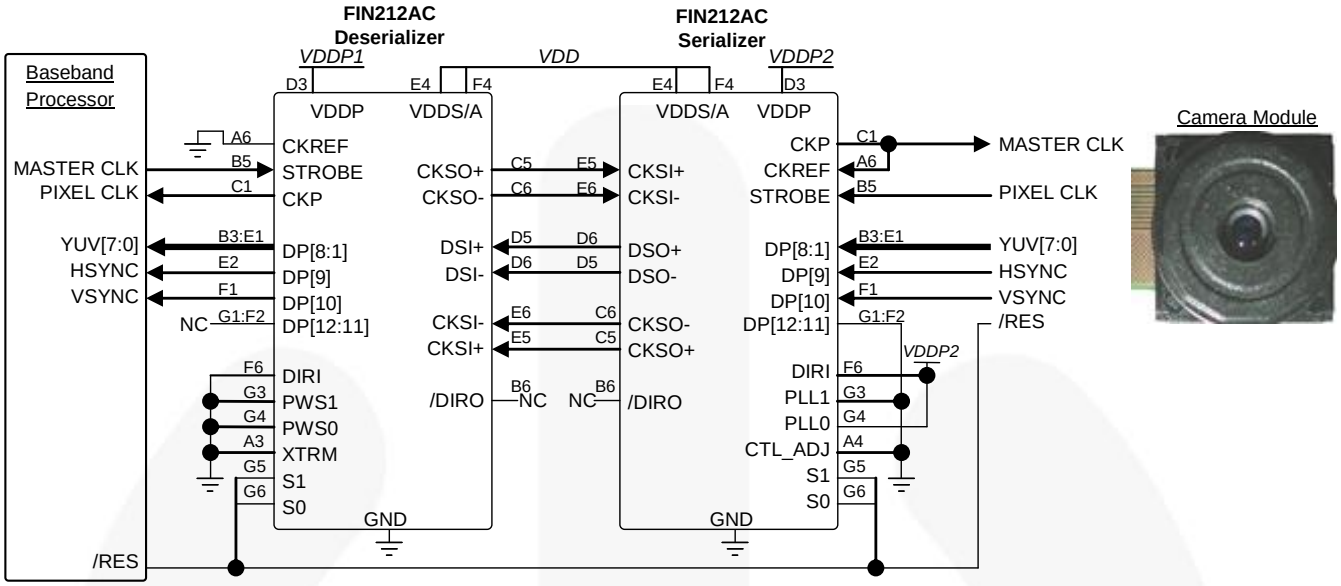

Figure 6. 8-Bit YUV 1.3MPixel CMOS Imager In Clock Pass-Through Mode

Serializer Configuration:

20MHz to 40MHz Frequency Range (S1=0, S0=1)

Normal Mode (PLL1=0; PLL0=1)

Master clock bypass mode.

Deserializer Configuration:

~2 – 3ns output edge rates (S1=0, S0=1)

~50% CKP PW,(PWS1=PWS0=0)

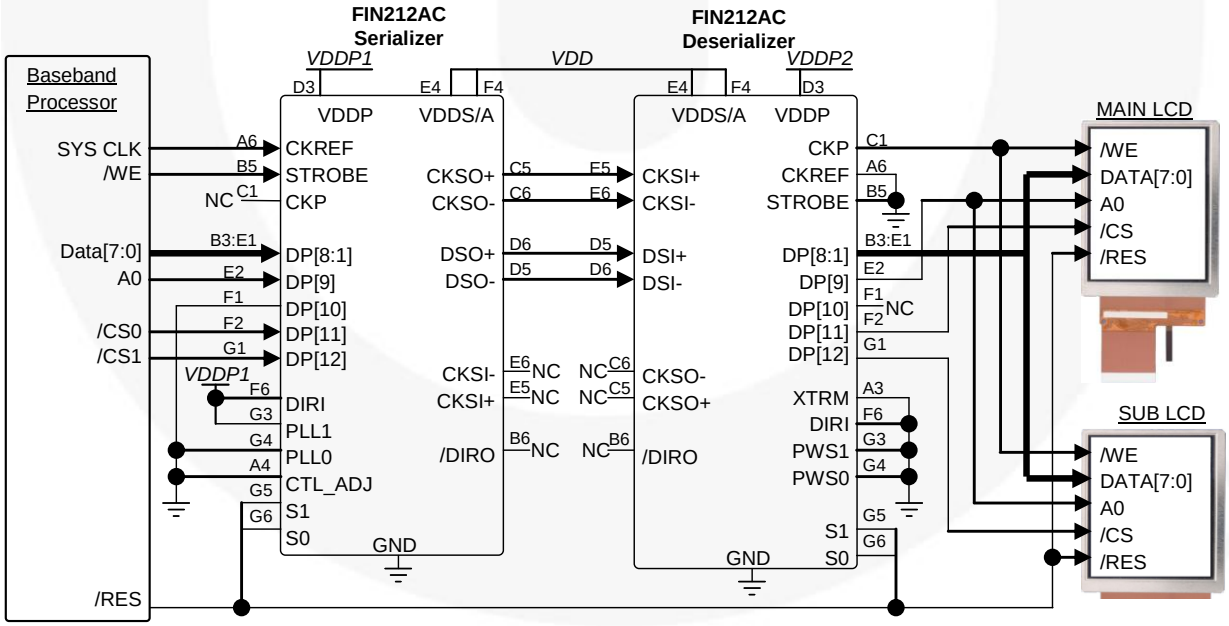

Figure 7. 8-Bit WRITE-Only Microcontroller Interface (Example Shows BGA 42-Pin Package)

Serializer Configuration:

20MHz to 40MHz Frequency Range (S1=0, S0=1)

CKREF is twice as fast STROBE (PLL1=1; PLL0=0)

CKREF=26MHz & STROBE Frequency=10 MHz

Deserializer Configuration:

~7 – 8ns output edge rates (S1=1, S0=0)

~50% CKP PW,(PWS1=PWS0=0)

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Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

- Keep all four differential Serial Wires the same length.
- Do not allow noisy signals over or near differential serial wires.
  Example: No LVCMOS traces over differential serial wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Design goal of 100Ω differential characteristic impedance.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.
- For additional applications notes or flex guidelines see your sales representative or contact Fairchild directly.
- For samples and questions, please contact: Interface@fairchildsemi.com.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		-0.5V	+4.6	V
	All Input/Output Voltage		-0.5	V_{DD}+0.5	V
	CTL Output Short-Circuit Duration		Continuous		
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature		+150		°C
T_L	Lead Temperature (Soldering, four seconds)		+260		°C
ESD	Human Body Model JESD22-A114	Serial I/O Pins to GND		14	kV
		All Pins		8	kV
	Charged Device Model, JESD22-C101			2	kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	3.6	V
V_{DDP}	Supply Voltage	1.65	3.60	V
T_A	Operating Temperature	-30	+70	ºC
V_{DDA-PP}	Supply Noise Voltage	100		mV_{PP}

DC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.[3]	Max.	Unit
LVCMOS I/O						
V_{IH}	Input High Voltage		0.65xV_{DDP}		V_{DDP}	
V_{IL}	Input Low Voltage		GND		0.35xV_{DDP}	V

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DC Electrical Characteristics (Continued)

V_{OH}	Output High Voltage		I_{OH}=-2.0mA, S1=0,S0=1	0.75xV_{DDP}		V_{DDP}	V
			I_{OH}=-0.4mA, S1=1,S0=0				
			I_{OH}=-1.0mA, S1=1,S0=1				
V_{OL}	Output Low Voltage		I_{OL}=2.0mA, S1=0,S0=1	0		0.25xV_{DDP}	V
			I_{OL}=0.4mA, S1=1,S0=0				
			I_{OL}=1.0mA, S1=1,S0=1				
I_{IN}	Input Current		V_{IN}= 0V to 3.6V	-5.0		5.0	µA
DIFFERENTIAL I/O							
I_{ODH}	Output HIGH Source Current	V_{OS}=1.0V	CTL_ADJ=0		-2		mA
			CTL_ADJ=1		-3.4		
I_{ODL}	Output LOW Sink Current	V_{OS}=1.0V	CTL_ADJ=0		1.2		mA
			CTL_ADJ=1		2		
V_{GO}	Input Voltage Ground Offset[4]				0		V
R_{TRM}	CKS Internal Receiver Termination Resistor		V_{ID}=50mV, V_{IC}=925mV,	80	100	120	Ω
			DIRI=0				
	DS Internal Receiver Termination Resistor		V_{ID}=50mV, V_{IC}=925mV,	80	100	120	Ω
			DIRI=0				

Notes:

3. Typical values are given for V_{DD}=2.775V and T_A=25°C. Positive current values refer to the current flowing into the device and negative values refer to the current flowing out of pins. Voltages are referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).
4. V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

Power Supply Currents

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
I_{DD_PD}	V_{DD} Power-Down Supply Current	S1=S0=0, All Inputs at GND or VDD				0.1		µA
I_{DD_SER1}	Dynamic Serializer Power Supply Current	f_{CKREF}=f_{STRB}, PLL1=0,PLL0=1; CTL_ADJ=0; C_L=0pF	S1=L S0=H	20MHz		13		mA
				40MHz		19		mA
			S1=H S0=L	5MHz		9.5		mA
				14MHz		17		mA
			S1=H S0=H	8MHz		11		mA
				28MHz		20		mA
I_{DD_DES1}	Dynamic Deserializer Power Supply Current	f_{CKREF}=$f_{STRB,}$ PLL1=0,PLL0=1; CTL_ADJ=0; C_L=0pF	S1=L S0=H	20MHz		10		mA
				40MHz		14		mA
			S1=H S0=L	5MHz		8		mA
				14MHz		9		mA
			S1=H S0=H	8MHz		9		mA
				28MHz		12		mA

Pin Capacitance Tables

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}, C_{IO}, $C_{IO\text{-}DIFF}$	Capacitance of Input Only Signals; Parallel Port Pins DP[1:10]; Differential I/O	DIRI=1, S1=0, S0=0, V_{DD}=2.5V		2		pF

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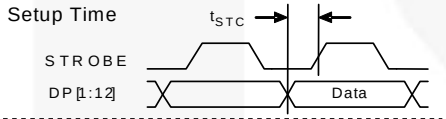
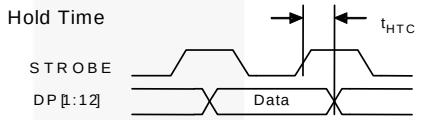
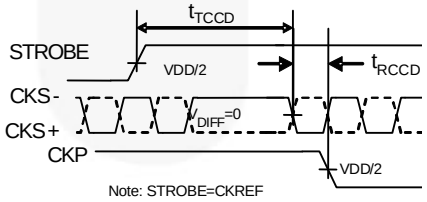
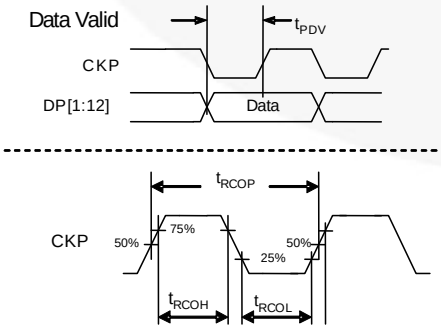
AC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Serializer Input Operating Conditions							
f_{CKREF}	CKREF Clock Frequency (5MHz - >40MHz);	$f_{CKREF}=f_{STRB}$	S1=0, S0=1	18		40	MHz
			S1=1, S0=0	5		14	
			S1=1, S0=1	10		28	
f_{STRB}	Strobe Frequency Relative to CKREF Frequency	$f_{CKREF} \neq f_{STRB}$	PLL1=0, PLL0=0			100	% of f_{CKREF}
			PLL1=0, PLL0=1			100	
			PLL1=1, PLL0=0			50	
			PLL1=1, PLL0=1			$33^1/_3$	
t_{CPWH}	CKREF DC	$T=1/f_{CKREF}$		0.2	0.5	0.8	T
t_{CPWL}	CKREF DC	$T=1/f_{CKREF}$		0.2	0.5	0.8	T
t_{CLKT}	LVCMOS Input Transition Time(5)	10-90%				20	ns
$t_{SPWH/L}$	STROBE Pulse Width HIGH/LOW	$T=1/f_{CKREF}$		T x $^4/_{14}$		T x $^{10}/_{14}$	ns
t_{STC}	$DP_{(n)}$ Setup to STROBE (DIRI=1, f=5MHz)	Setup Time 		2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE (DIRI=1, f=5MHz)	Hold Time 		2.0			ns
Serializer AC Electrical Characteristics							
t_{TCCD}	Transmitter Clock Input to Clock Output Delay(6)	 DIRI=1, $f_{CKREF}=f_{STRB}$		21a+1.5		23a+6.5	ns
Phase Lock Loop (PLL) AC Electrical Characteristics							
t_{TPLLS0}	Serializer PLL Stabilization Time	CKREF toggling and stable		200		600	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock					30.0	µs
t_{TPLLD1}	PLL Power-Down Time					20.0	ns

Deserializer AC Electrical Characteristics

Symbol	Parameter	Test Conditions	PWS1	PWS0	Min.	Typ.	Max.	Unit
t_{RCOL}	 Setup: DIRI= 0, CKSI and DS are valid signals.							
		$f_{STRB}=f_{CKREF}$	0	0	7a-3		7a+3	ns
		$f_{STRB}=f_{CKREF}$	0	1	7a-3		7a+3	
		$f_{STRB}=.5x\ f_{CKREF}$	1	0	13a-3		13a+3	
		$f_{STRB}=.5x\ f_{CKREF}$	1	1	17a-3		17a+3	
t_{PDV}		Data Valid to CKP HIGH (Rising Edge STROBE), C_L=5pF			8a-3		8a+3	ns

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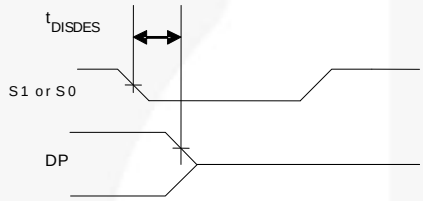
AC Electrical Characteristics (Continued)

t_{RFD}	Output Rise/Fall Time Data (20% to 80%)	C_L=8pF	S1=0,S0=1		3		ns
			S1=1,S0=0		8		
			S1=1,S0=1		5		
t_{RFC}	Output Rise/Fall Time CKP (20% to 80%)	C_L=8pF	S1=0,S0=1		2		ns
			S1=1,S0=0		7		
			S1=1,S0=1		4		

Notes:

5. Parameter is characterized, but not production tested.
6. The average bit time "a" is a function of the serializer CKREF frequency; a=(1/f)/14.

Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI to /DIRO	DIRI L->H or H->L			17	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI to DP	DIRI L->H or H->L			25	ns
t_{DISDES}	Deserializer Disable Time: S0 or S1 LOW to DPTri-State; DIRI=0,  Note: If S0(2) is transitioning, S1(1) must =0 for test to be valid.				25	ns
t_{DISSER}	Serializer Disable Time: S0 or S1 LOW to CKP HIGH	DIRI=1; S1(0) and S0(1)=H->L			25	ns

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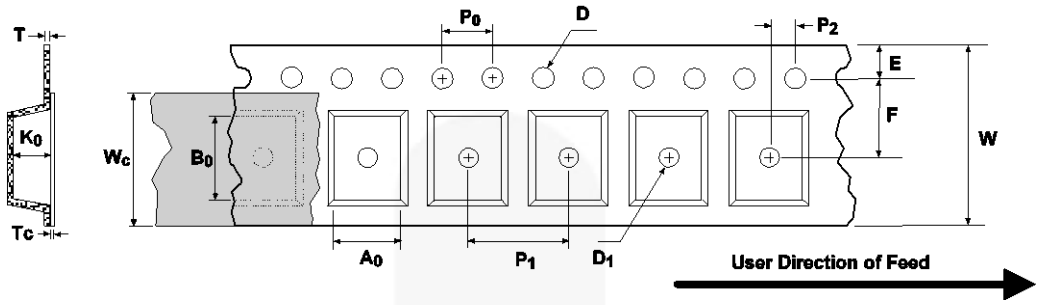
Tape and Reel Specifications

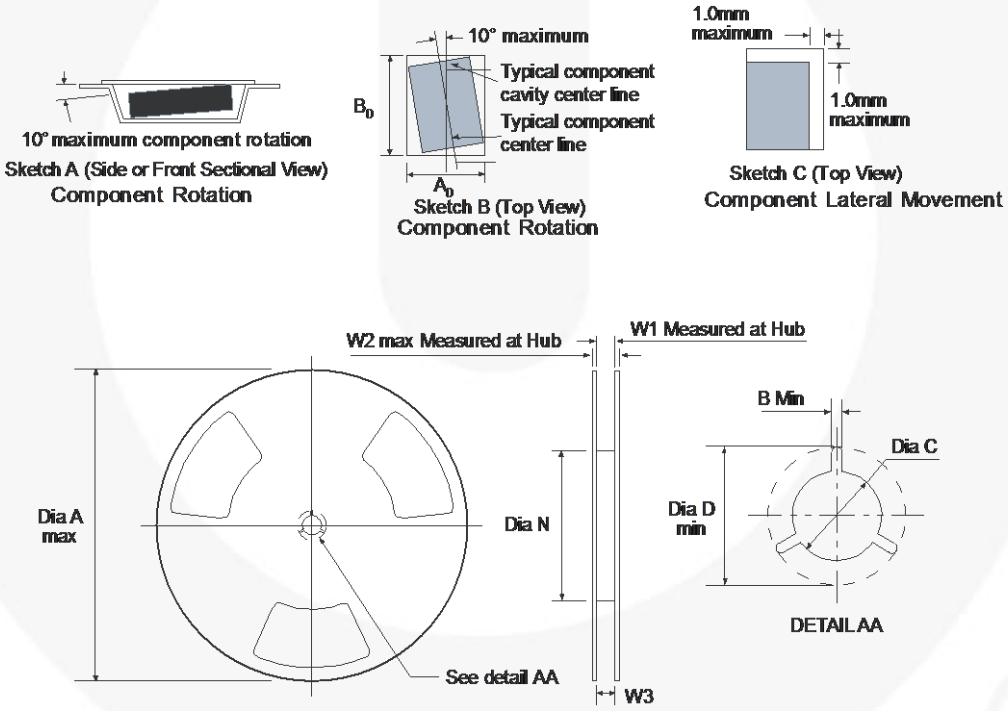
MLP Embossed Tape Dimensions



Package	A_0 ±0.1	B_0 ±0.1	D ±0.5	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0.5	T Typ.	T_C ±0/05	W ±0.3	W_C Typ.
5 x 5	5.35	5.35	1.55	1.50	1.75	5.50	1.40	8.00	4.00	2.00	0.30	0.07	12.00	9.30
6 x 6	5.35	5.35	1.55	1.50	1.75	5.50	1.40	8.00	4.00	2.00	0.30	0.07	12.00	9.30

Notes:
A_0, B_0, and K_0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

MLP Shipping Reel Dimensions



Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/-0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/-0	Dim W2	Dim W3 (LSL-USL)
8	330.0	1.5	13.0	20.2	178.0.	8.4	14.4	7.9 ~ 10.4
12	330.0	1.5	13.0	20.2	178.0.	12.4	18.4	11.9 ~ 15.4
16	330.0	1.5	13.0	20.2	178.0.	16.4	22.4	15.9 ~ 19.4

Figure 8. MLP Tape and Reel

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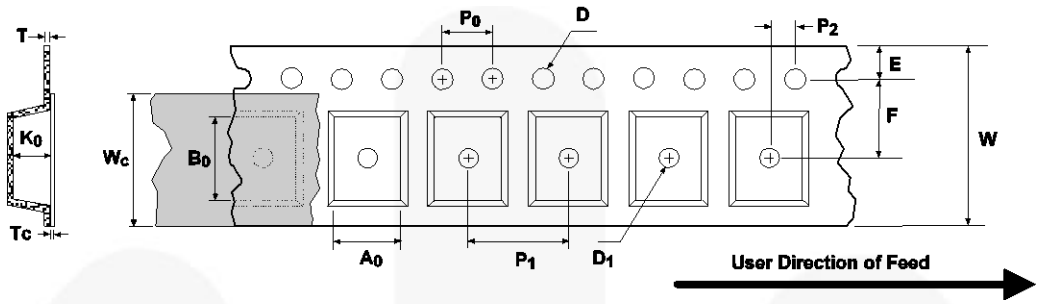
Tape and Reel Specifications (Continued)

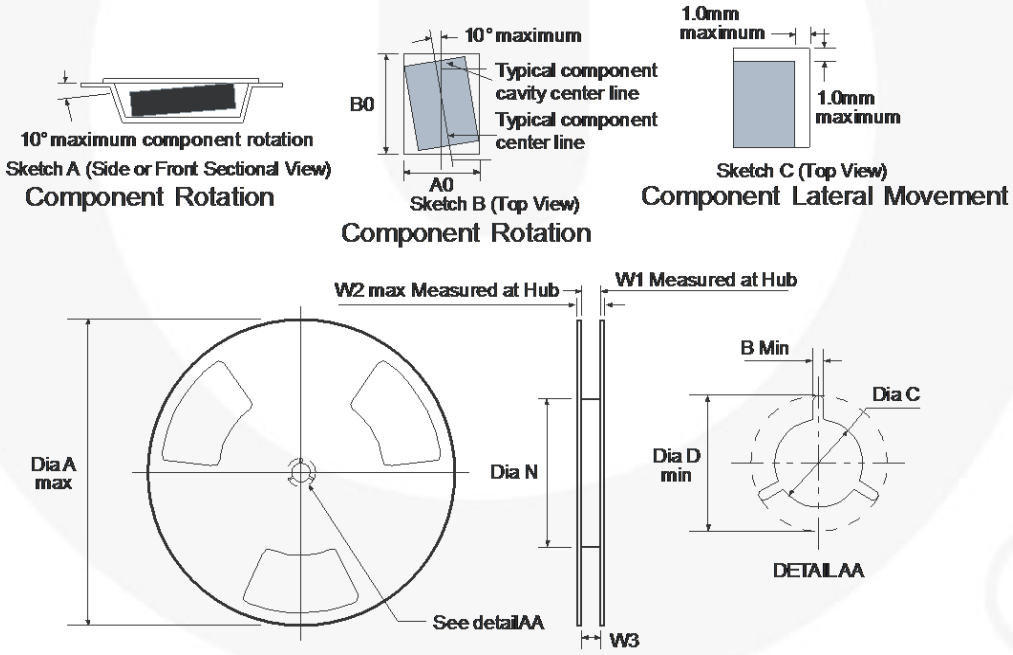
BGA Embossed Tape Dimensions



Package	A_0 ±0.1	B_0 ±0.1	D ±0.5	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0.5	T Typ.	T_C ±0/05	W ±0.3	W_C Typ.
3.5 x 4.5	3.85	4.80	1.55	1.50	1.75	5.50	1.10	8.00	4.00	2.00	0.30	0.07	12.00	9.3

Notes:
A_0, B_0, and K_0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

BGA Shipping Reel Dimensions



Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/-0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/-0	Dim W2	Dim W3 (LSL-USL)
8	330.0	1.5	13.0	20.2	178.0.	8.4	14.4	7.9 ~ 10.4
12	330.0	1.5	13.0	20.2	178.0.	12.4	18.4	11.9 ~ 15.4
16	330.0	1.5	13.0	20.2	178.0.	16.4	22.4	15.9 ~ 19.4

Figure 9. BGA Tape and Reel

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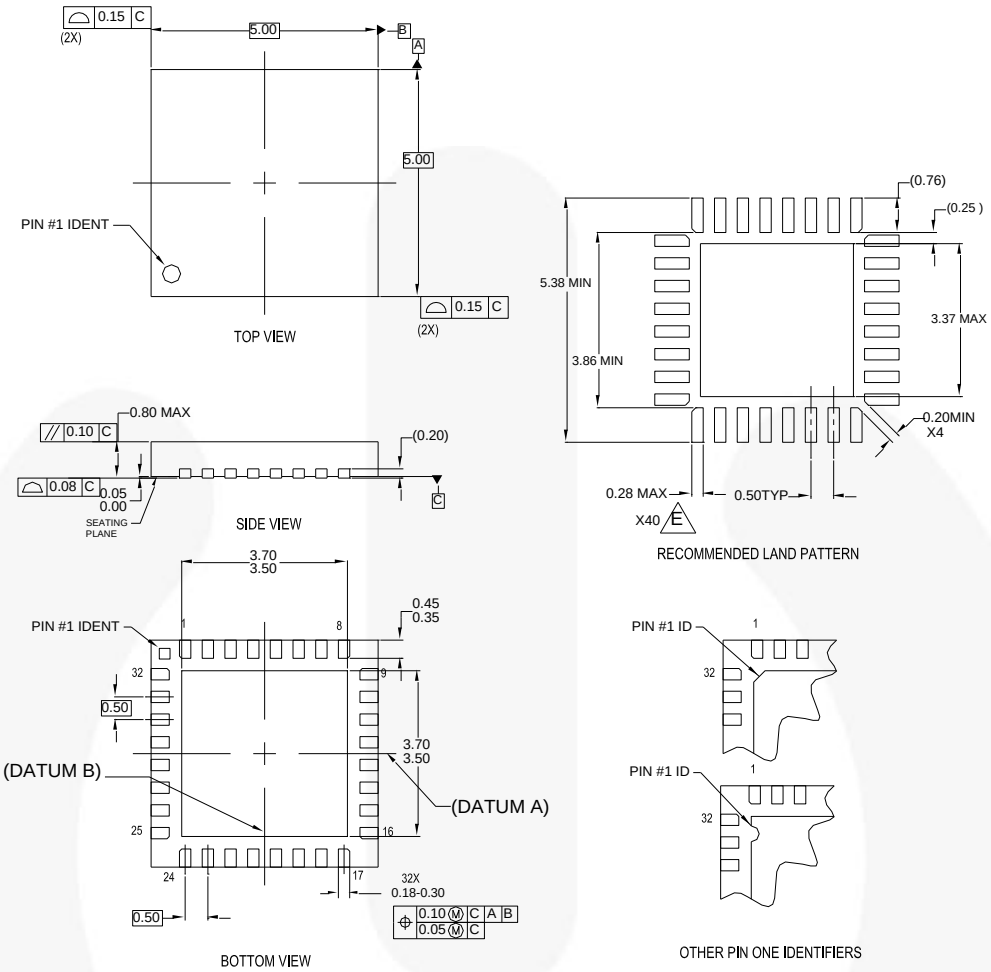
Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-4. THIS PACKAGE IS ALSO FOOTPRINT COMPATIBLE WITH WHHD-5.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

D. LAND PATTERN PER IPC SM-782.

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

F. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, OR TIE BAR PROTRUSIONS.

G. DRAWING FILENAME: MKT-MLP32Arev3.

Figure 10. 32-Lead, Molded Leadless Package (MLP)

Order Number	Operating Temperature Range	Package Description	Packing Method
FIN212ACMLX	-30 to 70°C	32-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 5mm Square	Tape & Reel

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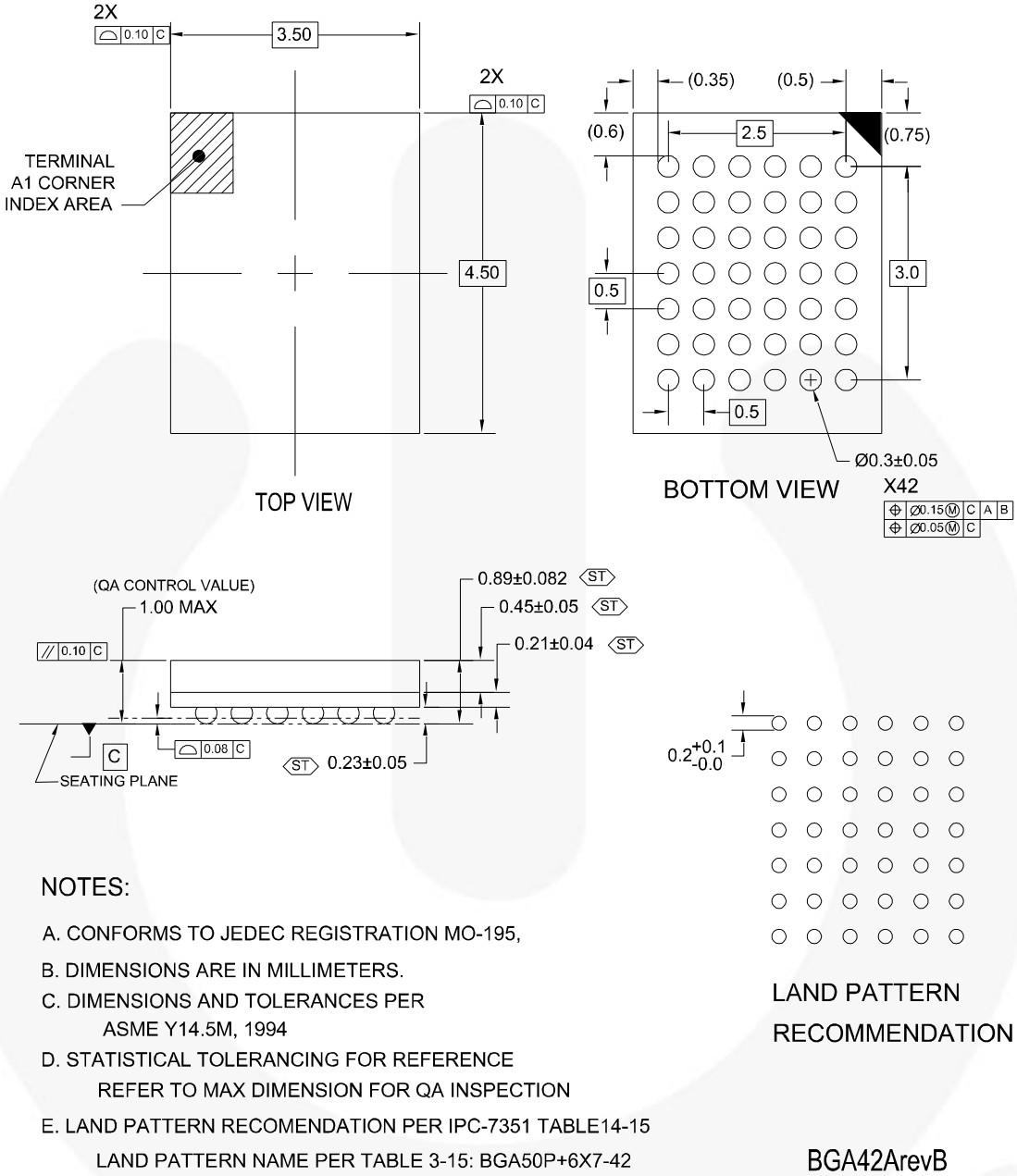
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE
REFER TO MAX DIMENSION FOR QA INSPECTION

E. LAND PATTERN RECOMENDATION PER IPC-7351 TABLE14-15
LAND PATTERN NAME PER TABLE 3-15: BGA50P+6X7-42

Figure 11. 42-Ball, Ball Grid Array (BGA) Package

Order Number	Operating Temperature Range	Package Description	Packing Method
FIN212ACGFX	-30 to 70°C	42-Ball Ultra Small-Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5 x 4.5mm Wide, 0.5mm Ball Pitch	Tape & Reel

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