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FDZ1040L Integrated Load Switch

Features

- Optimized for Low-Voltage Core ICs in Portable Systems
- Very Small Package Dimension: WLCSP
0.8 X 0.8 X 0.5 mm³
- Current = 1.2 A, V_{IN} max = 4 V
- Current = 2 A, V_{IN} max = 4 V (Pulsed)
- R_{DS(on)} = 80 mΩ at V_{ON} = V_{IN} = 4 V
- R_{DS(on)} = 85 mΩ at V_{ON} = V_{IN} = 3.6 V
- R_{DS(on)} = 90 mΩ at V_{ON} = V_{IN} = 3 V
- R_{DS(on)} = 110 mΩ at V_{ON} = 0.7 V, V_{IN} = 1.6 V
- R_{DS(on)} = 309 mΩ at V_{ON} = 0.7 V, V_{IN} = 1 V
- RoHS Compliant

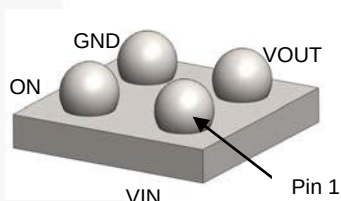


Figure 1. Bottom View

Description

This device is particularly suited for compact power management in portable applications needing 1 V to 4 V input and 1.2 A output current capability. This load switch integrated a level-shifting function that drives a P-channel power MOSFET in a very small 0.8 X 0.8 X 0.5 mm³ WLCSP package.

Applications

- Load Switch
- Power Management in Portable Applications

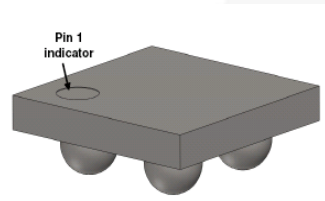


Figure 2. Top View

Ordering Information

Part Number	Device Mark	Ball Pitch	Operating Temperature Range	Switch	Package	Packing Method
FDZ1040L	ZL	0.4 mm	-40 to 85°C	80 m, P-Channel MOSFET	0.8 x 0.8 x 0.5 mm ³ WLCSP	Tape & Reel

Typical Application

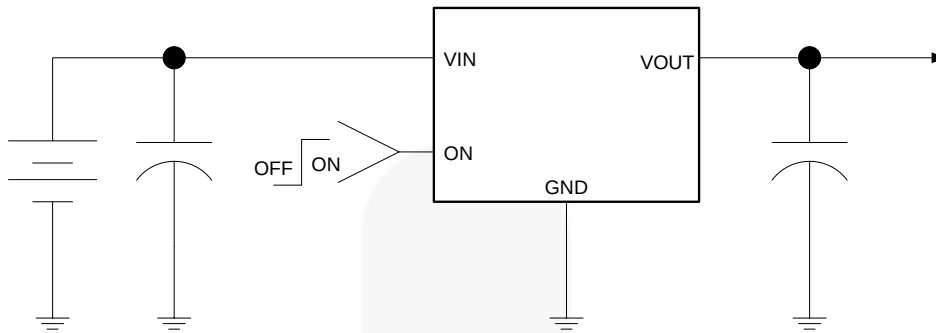


Figure 3. Typical Application

Block Diagram

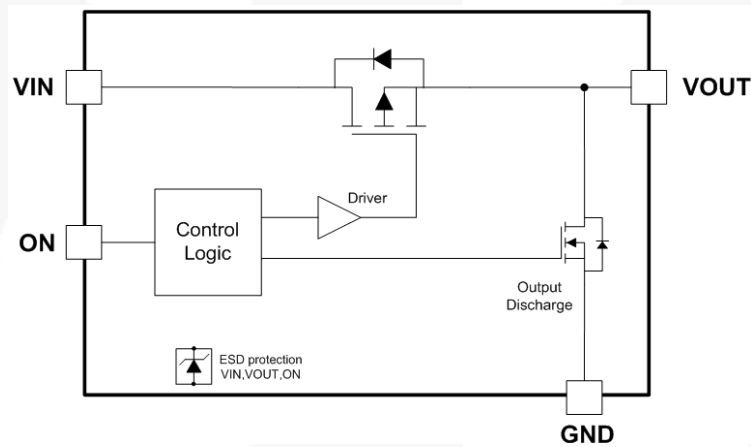


Figure 4. Internal Block Diagram

Pin Configuration

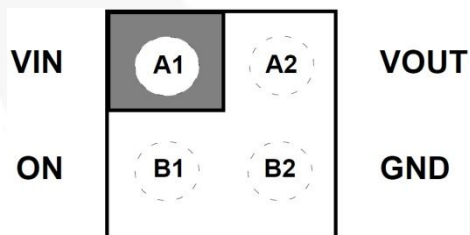


Figure 5. Top View (Bumps Down)

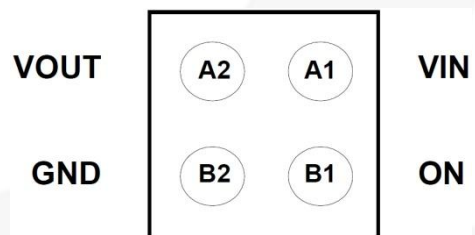


Figure 6. Bottom View (Bumps Up)

Pin Descriptions

Pin #	Name	Description
A1	VIN	Supply Input: Input to the load switch
A2	VOUT	Switch Output: Output of the load switch
B1	ON	ON/OFF Control Input, Active High
B2	GND	Ground

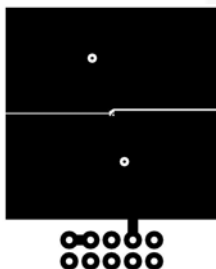
Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Voltage on VIN, VOUT, ON to GND	-0.3	4.2	V
I_{OUT_C}	I_{OUT} -Load Current (Continuous) ^(1a)		1.2	A
I_{OUT_P}	I_{OUT} -Load Current (Pulsed)		2	A
P_D	Power Dissipation at $T_A = 25^{\circ}\text{C}$ ^(1a)		0.9	W
T_A	Operating Temperature Range	-40	85	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-65	150	$^{\circ}\text{C}$
$R\theta_{JA}$	Thermal Resistance, Junction to Ambient ^(1a)		135	$^{\circ}\text{C/W}$
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8	kV
		Charged Device Model, JESD22-C101	2	

Notes:

- $R\theta_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R\theta_{JC}$ is guaranteed by design, while $R\theta_{JA}$ is determined by the board design.



a. 117°C/W when mounted on a 1-inch square pad of 2-oz copper.



b. 277°C/W when mounted on a minimum pad of 2-oz copper.

- Pulse test: pulse width $< 300\ \mu\text{s}$; duty cycle $< 2.0\%$.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Voltage on VIN Pin	1	4	V
V_{ON}	Voltage on ON Pin	0.7	4.0	V
T_A	Operating Temperature Range	-40	85	$^{\circ}\text{C}$

Electrical Characteristics

$T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage		1		4	V
V_{IL}	ON Input Logic Low Voltage	$1.6\text{ V} \leq V_{IN} \leq 4\text{ V}$			0.35	V
		$1\text{ V} \leq V_{IN} \leq 1.6\text{ V}$			0.25	
V_{IH}	ON Input Logic High Voltage	$1.6\text{ V} \leq V_{IN} \leq 4\text{ V}$	1.0			V
		$1\text{ V} \leq V_{IN} \leq 1.6\text{ V}$	0.7			
I_Q	Quiescent Current	$V_{IN} = V_{ON} = 1.8\text{ V}$, $V_{OUT} = \text{Float}$			1	μA
$I_{Q(\text{off})}$	Off Supply Current	$V_{IN} = 1.8\text{ V}$, $V_{ON} = \text{GND}$, $V_{OUT} = \text{Float}$			1	μA
$I_{SD(\text{off})}$	Off Switch Leakage Current	$V_{IN} = 1.8\text{ V}$, $V_{ON} = \text{GND}$, $V_{OUT} = 0\text{ V}$			100	nA
R_{PD}	Output Discharge Pull-Down Resistance			200		Ω
I_{ON}	ON Input Leakage	$V_{ON} = V_{IN}$ or GND			1	μA
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{ON} = V_{IN} = 4\text{ V}$, $I_{OUT} = 300\text{ mA}$		48	80	m Ω
		$V_{ON} = V_{IN} = 3.6\text{ V}$, $I_{OUT} = 300\text{ mA}$		49	85	
		$V_{ON} = V_{IN} = 3\text{ V}$, $I_{OUT} = 300\text{ mA}$		51	90	
		$V_{ON} = 0.7\text{ V}$, $V_{IN} = 1.6\text{ V}$, $I_{OUT} = 300\text{ mA}$		70	110	
		$V_{ON} = 0.7\text{ V}$, $V_{IN} = 1\text{ V}$, $I_{OUT} = 300\text{ mA}$		142	309	
		$V_{IN} = 3.6\text{ V}$, $I_{OUT} = 300\text{ mA}$, $T_J = 85^\circ\text{C}$		59	120	

Switching Characteristics

Symbol	Parameter	Test Conditions	Typical	Unit
$t_{d(\text{on})}$	Turn-On Delay	$V_{IN} = 1.6\text{ V}$, $V_{ON} = 0.7\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 500\text{ }\Omega$	22	μs
t_r	Turn-On Rise Time		23	μs
$t_{d(\text{off})}$	Turn-Off Delay		127	μs
t_f	Turn-Off Fall Time		298	μs
$t_{d(\text{on})}$	Turn-On Delay	$V_{IN} = 1\text{ V}$, $V_{ON} = 1.8\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 500\text{ }\Omega$	37	μs
t_r	Turn-On Rise Time		35	μs
$t_{d(\text{off})}$	Turn-Off Delay		161	μs
t_f	Turn-Off Fall Time		544	μs
$t_{d(\text{on})}$	Turn-On Delay	$V_{IN} = 1.8\text{ V}$, $V_{ON} = 1.8\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 500\text{ }\Omega$	20	μs
t_r	Turn-On Rise Time		22	μs
$t_{d(\text{off})}$	Turn-Off Delay		136	μs
t_f	Turn-Off Fall Time		272	μs
$t_{d(\text{on})}$	Turn-On Delay	$V_{IN} = 2.5\text{ V}$, $V_{ON} = 1.8\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 500\text{ }\Omega$	15	μs
t_r	Turn-On Rise Time		20	μs
$t_{d(\text{off})}$	Turn-Off Delay		168	μs
t_f	Turn-Off Fall Time		229	μs
$t_{d(\text{on})}$	Turn-On Delay	$V_{IN} = 3.3\text{ V}$, $V_{ON} = 1.8\text{ V}$, $C_L = 1\text{ }\mu\text{F}$, $R_L = 500\text{ }\Omega$	13	μs
t_r	Turn-On Rise Time		19	μs
$t_{d(\text{off})}$	Turn-Off Delay		202	μs
t_f	Turn-Off Fall Time		214	μs

Typical Performance Characteristics

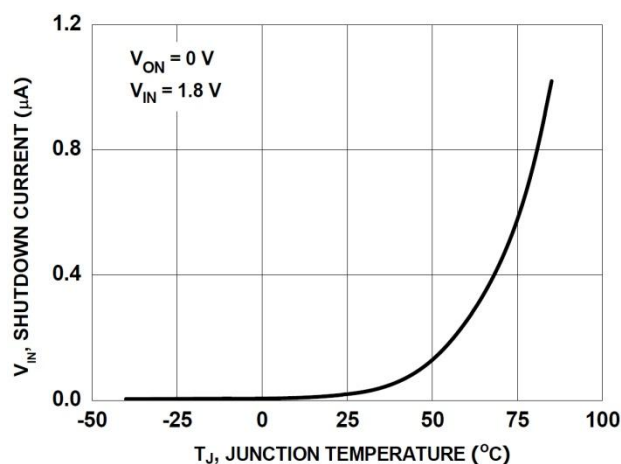


Figure 7. Shutdown Current vs. Temperature

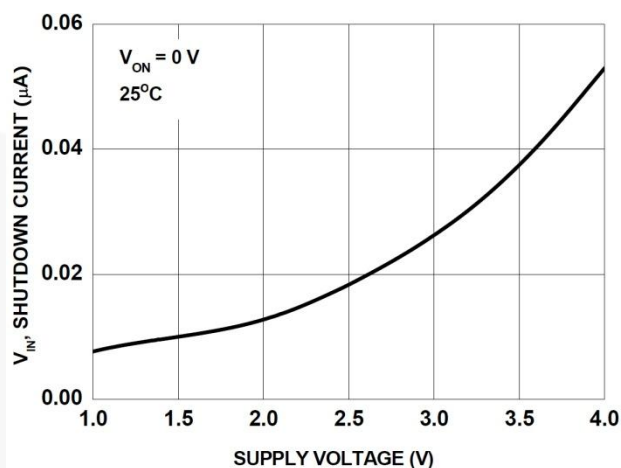


Figure 8. Shutdown Current vs. Supply Voltage

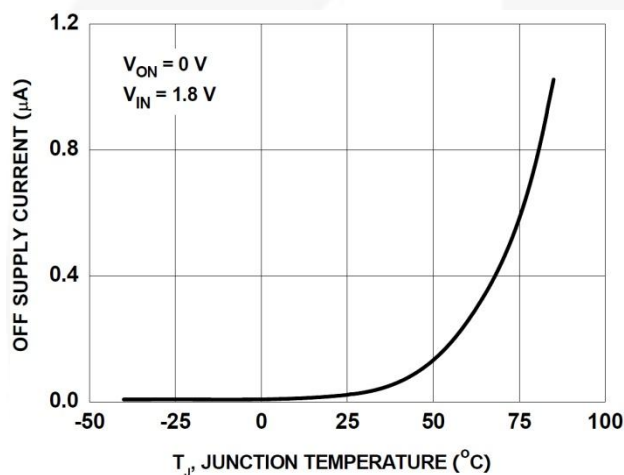


Figure 9. Off Supply Current vs. Temperature

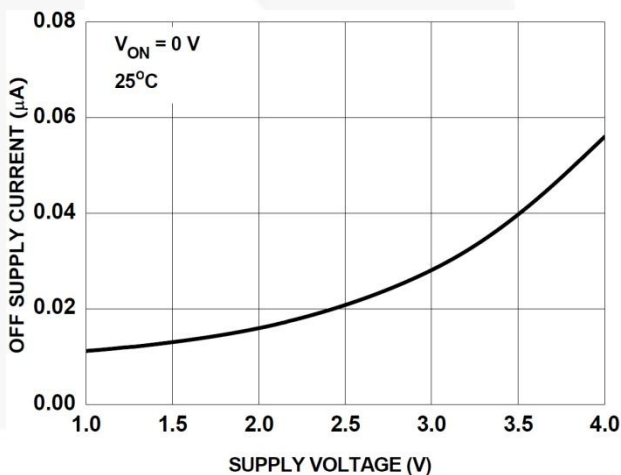


Figure 10. Off Supply Current vs. Supply Voltage

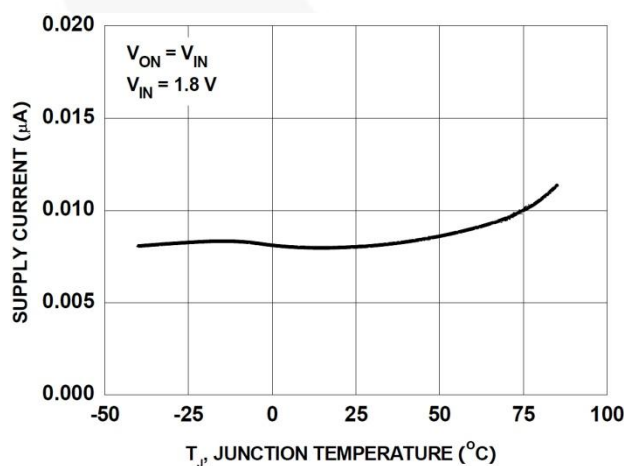


Figure 11. Quiescent Current vs. Temperature

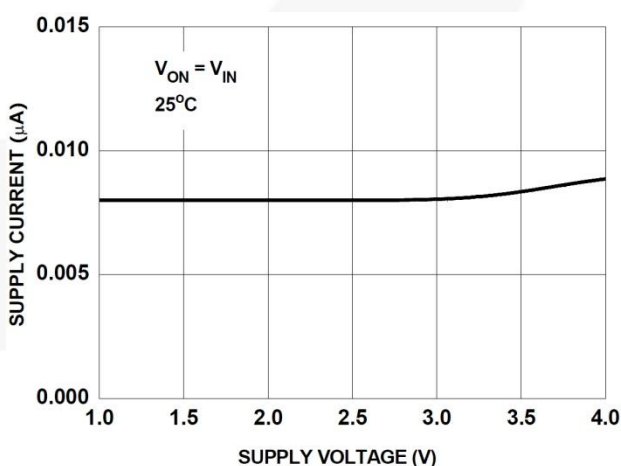


Figure 12. Quiescent Current vs. Supply Voltage

Typical Performance Characteristics

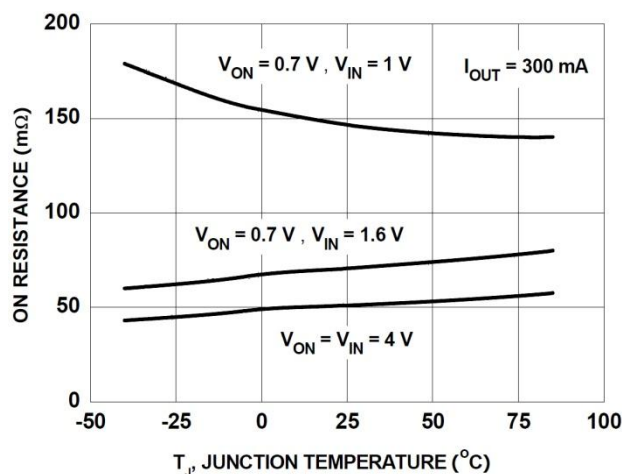
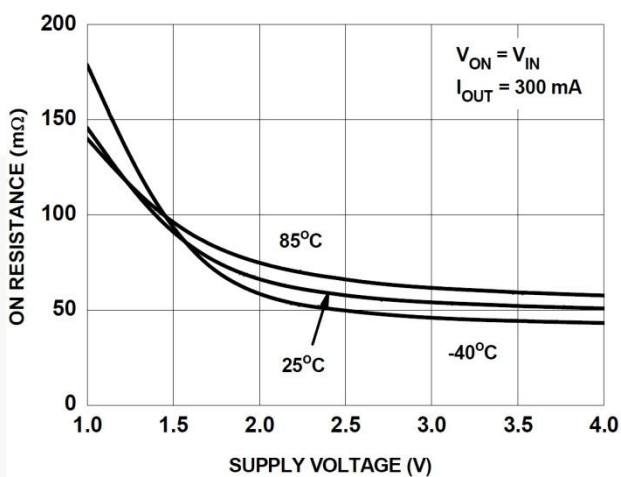
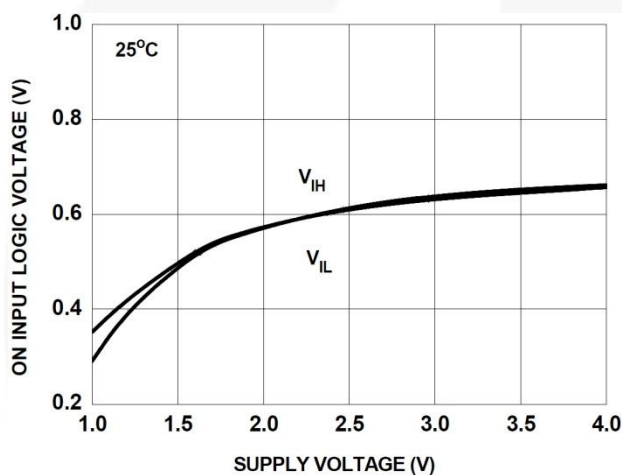
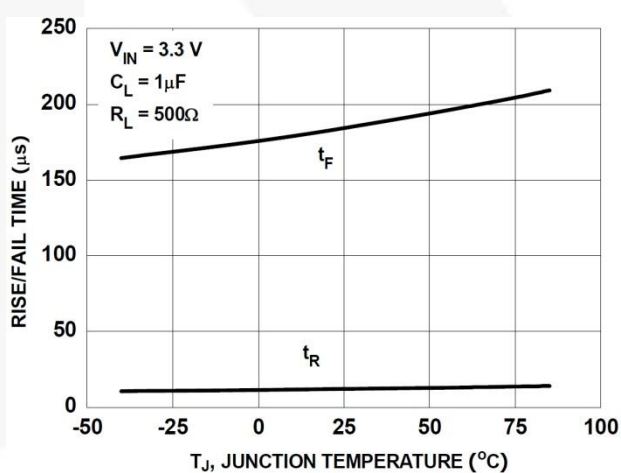
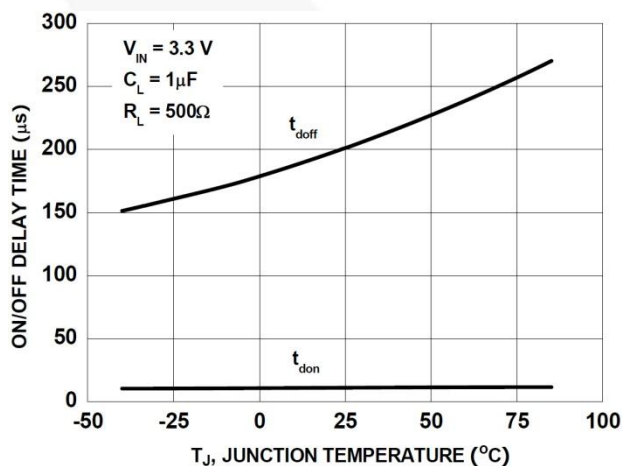
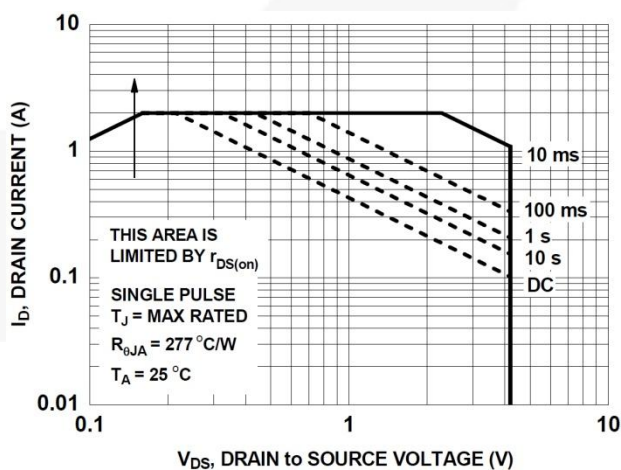
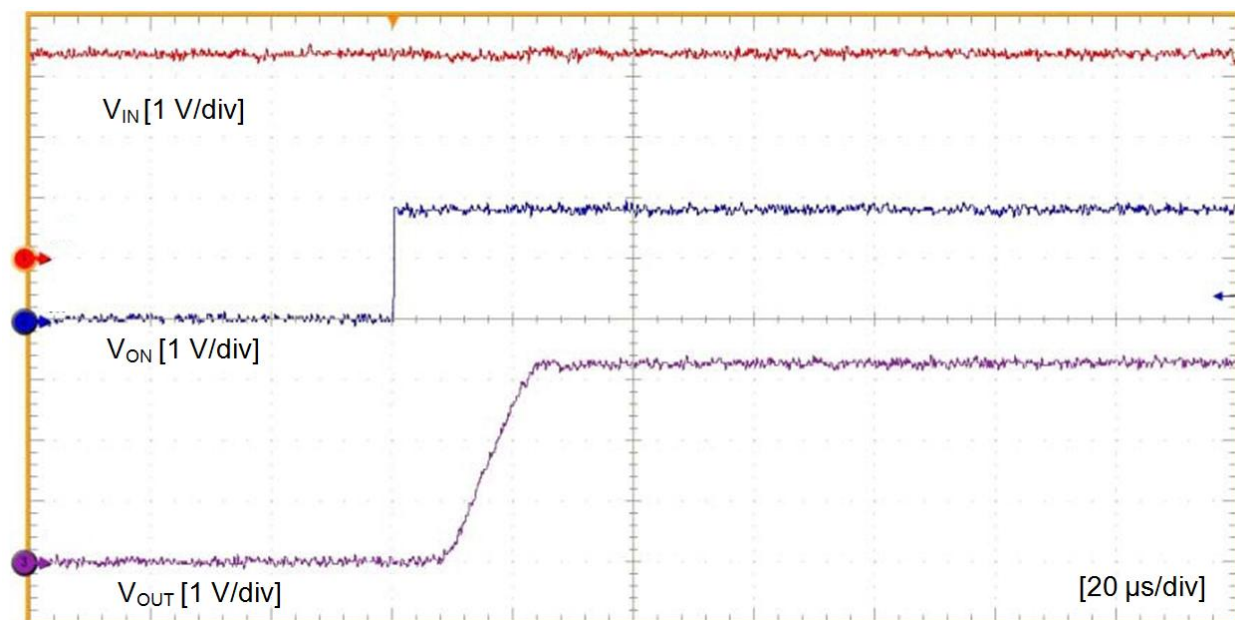
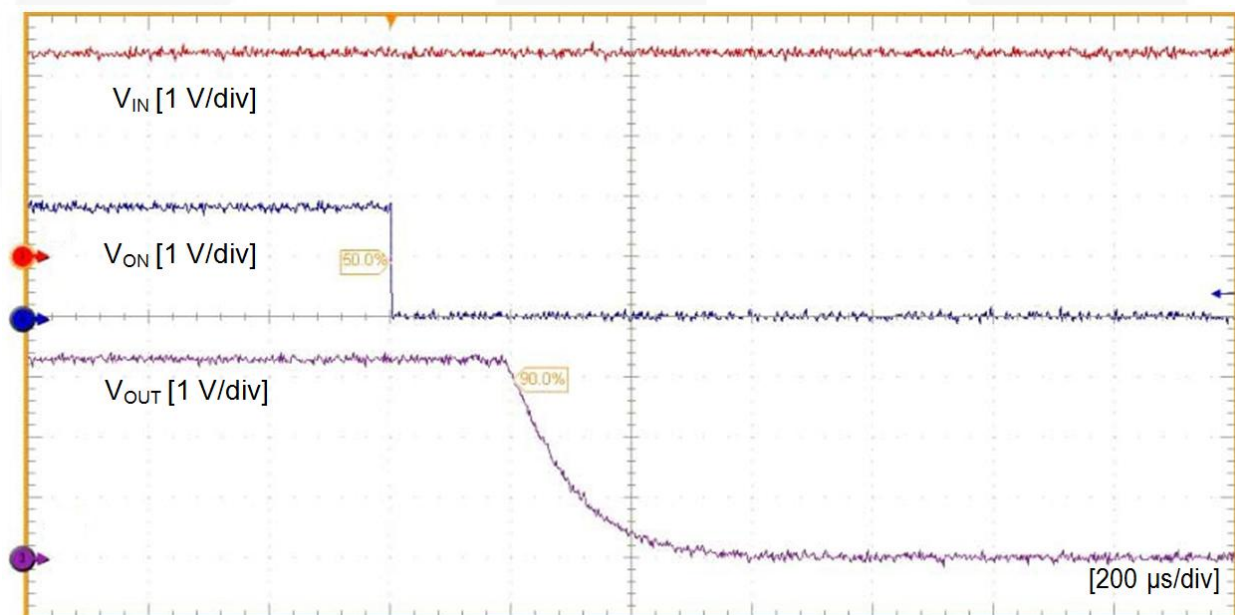
Figure 13. R_{ON} vs. TemperatureFigure 14. R_{ON} vs. Supply VoltageFigure 15. ON-Pin Threshold vs. V_{IN} Figure 16. V_{OUT} Rise and Fall Time vs. Temperature at $R_L=500\ \Omega$ Figure 17. V_{OUT} Turn-On and Turn-Off Delay vs. Temperature at $R_L=500\ \Omega$ 

Figure 18. Forward Bias Safe Operation Area

Typical Performance Characteristics

Figure 19. Turn-On Response ($V_{IN} = 3.3$ V, $C_{OUT}=1$ μ F, $R_L=500$ Ω)Figure 20. Turn-Off Response ($V_{IN} = 3.3$ V, $C_{OUT}=1$ μ F, $R_L=500$ Ω)

Functional Description

The FDZ1040L is a low- $R_{DS(ON)}$ P-channel load switch packaged in space-saving 0.8x0.8 WLCSP.

The core of the device is a 80 m Ω P-channel MOSFET capable of functioning over a wide input operating range

of 1-4 V. The ON pin, an active HIGH TTL-compatible input that supports input as low as 0.7 V, controls the state of the switch.

Applications Information

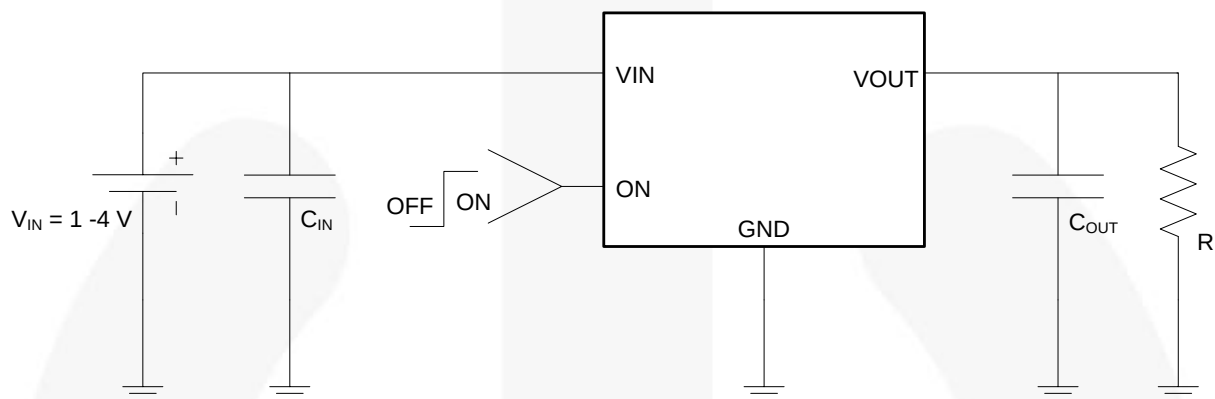


Figure 21. Typical Application

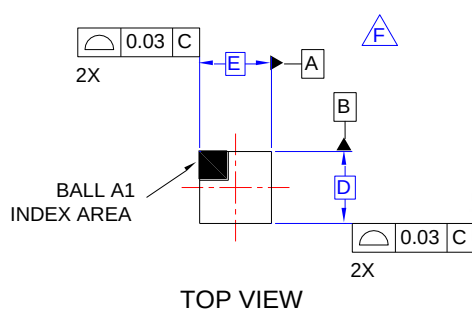
Input Capacitor

To reduce device inrush current effect, a 0.1 μ F ceramic capacitor, C_{IN} , is recommended close to the VIN pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

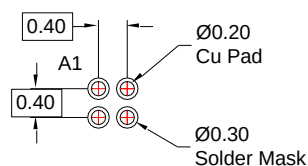
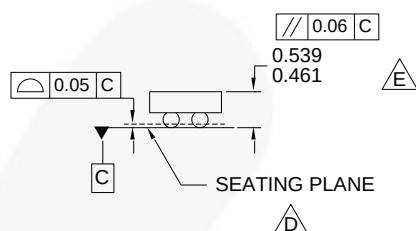
Output Capacitor

FDZ1040L works without an output capacitor. However, if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1 μ F capacitor, C_{OUT} , should be placed between the VOUT and GND pins.

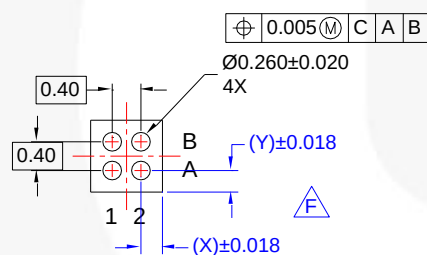
Physical Dimensions



TOP VIEW

RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)

SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ± 39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004ARev1.

Figure 22. 4-Ball, WLCSP, 2 X 2 Array, 0.4 mm Pitch, 250 μ m Ball

Product-Specific Dimensions

Product	D	E	X	Y
FDZ1040L	0.8 $\pm$ 0.03 mm	0.8 $\pm$ 0.03 mm	0.21 mm	0.21 mm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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