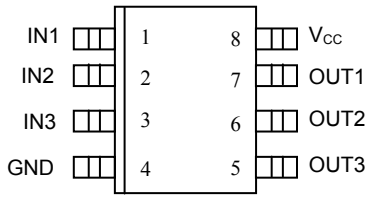
DS1135
3-in-1 High-Speed Silicon Delay Line

FEATURES

- **All-Silicon Timing Circuit**
- **Three Independent Buffered Delays**
- **Stable and Precise Over Temperature and Voltage**
- **Leading and Trailing Edge Precision Preserves the Input Symmetry**
- **Vapor Phasing, IR, and Wave Solderable**
- **Available in Tape and Reel**
- **Commercial and Industrial Temperature Ranges Available**
- **5V Operation (Refer to DS1135L for 3V Operation)**
- **Recommended Replacement for DS1013 and DS1035**

PIN ASSIGNMENT



DS1135Z 8-Pin SO (150 mils)

PIN DESCRIPTION

IN1-IN3	- Input Signals
OUT1-OUT3	- Output Signals
V_{CC}	- +5V Supply
GND	- Ground

DESCRIPTION

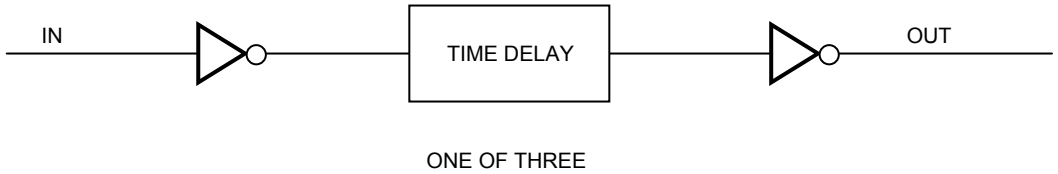
The DS1135 series is a low-power, +5V high-speed version of the popular DS1013 and DS1035.

The DS1135 series of delay lines have three independent logic buffered delays in a single package. The device is our fastest 3-in-1 delay line. It is available in a standard 8-pin 150-mil SO.

The device features precise leading and trailing edge accuracy. It has the inherent reliability of an all-silicon delay line solution. Each output is capable of driving up to 10 LS loads.

Standard delay values are indicated in Table 1.

LOGIC DIAGRAM Figure 1



PART NUMBER DELAY TABLE (t_{PLH}, t_{PHL}) Table 1

PART NUMBER	DELAY PER OUTPUT (ns)	INITIAL TOLERANCE (Note 1)	TOLERANCE OVER TEMP AND VOLTAGE (Note 2)	
			0°C to +70°C	-40°C to +85°C
DS1135Z-6+	6/6/6	±1.0ns	±1.0ns	±1.5ns
DS1135Z-8+	8/8/8	±1.0ns	±1.0ns	±1.5ns
DS1135Z-10+	10/10/10	±1.0ns	±1.0ns	±1.5ns
DS1135Z-12+	12/12/12	±1.0ns	±1.0ns	±1.5ns
DS1135Z-15+	15/15/15	±1.0ns	±1.5ns	±2ns
DS1135Z-20+	20/20/20	±1.0ns	±1.5ns	±2ns
DS1135Z-25+	25/25/25	±1.5ns	±1.5ns	±2ns
DS1135Z-30+	30/30/30	±1.5ns	±1.5ns	±2ns

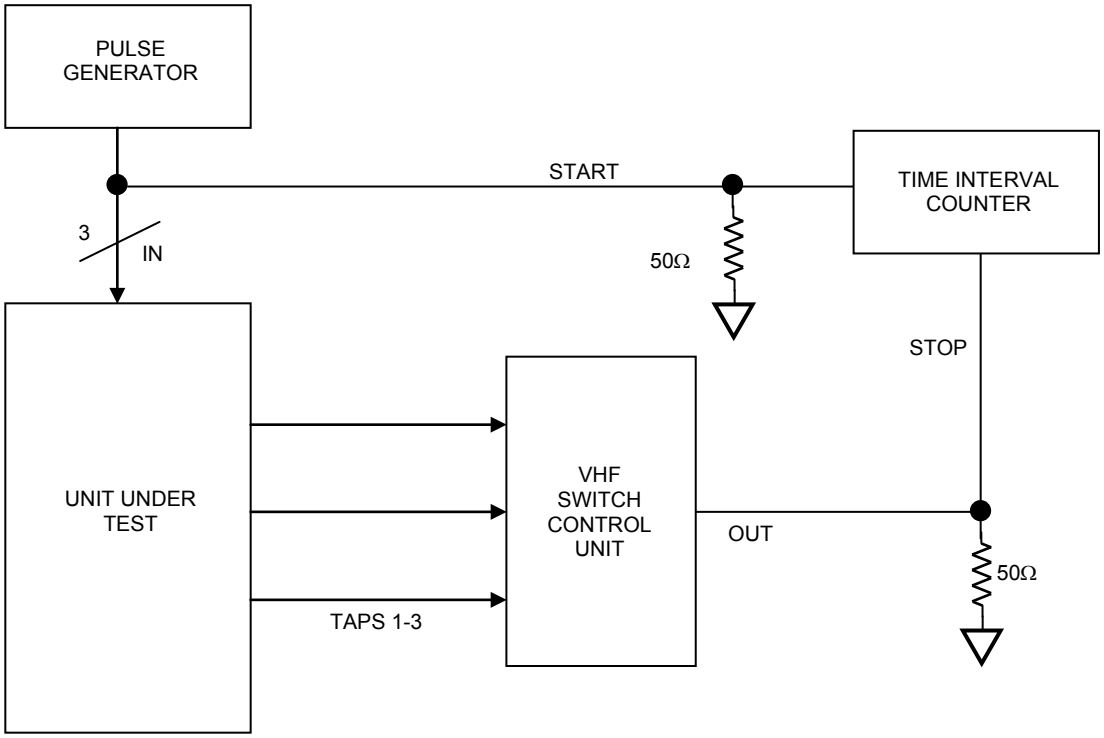
NOTES:

1. Nominal conditions are +25°C and V_{CC} =+5.0V.
2. Voltage range of 4.75V to 5.25V.
3. Delay accuracies are for both leading and trailing edges.

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1135. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20ps resolution) connected to the output. The DS1135 output taps are selected and connected to the interval counter by a VHF switch control unit. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

DS1135 TEST CIRCUIT Figure 2



ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-1.0V to +6.0V
Short Circuit Output Current	50mA for 1 second
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Soldering Temperature (reflow)	+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.00	5.25	V	1
Active Current	I_{CC}	V_{CC} = 5.25V, period = 1µs			35	mA	
High Level Input Voltage	V_{IH}		2.2		V_{CC} +0.5	V	1
Low Level Input Voltage	V_{IL}		-0.5		0.8	V	1
Input Leakage	I_L	$0V \leq V_I \leq V_{CC}$	-1.0		+1.0	µA	
High Level Output Current	I_{CC}	V_{CC} = 4.75V, V_{OH} = 4V			-1.0	mA	1
Low Level Output Current	I_{CC}	V_{CC} = 4.75V, V_{OL} = 0.5V	12			mA	1

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	2 (t_{WI})			ns	2
Input Pulse Width	t_{WI}	100% of Tap Delay			ns	2
Input-to-Output Delay	t_{PLH}, t_{PHL}	See Table 1		ns		
Output Rise or Fall Time	t_{OF}, t_{OR}		2.0	2.5	ns	
Power-up Time	t_{PU}			100	ms	3

CAPACITANCE

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

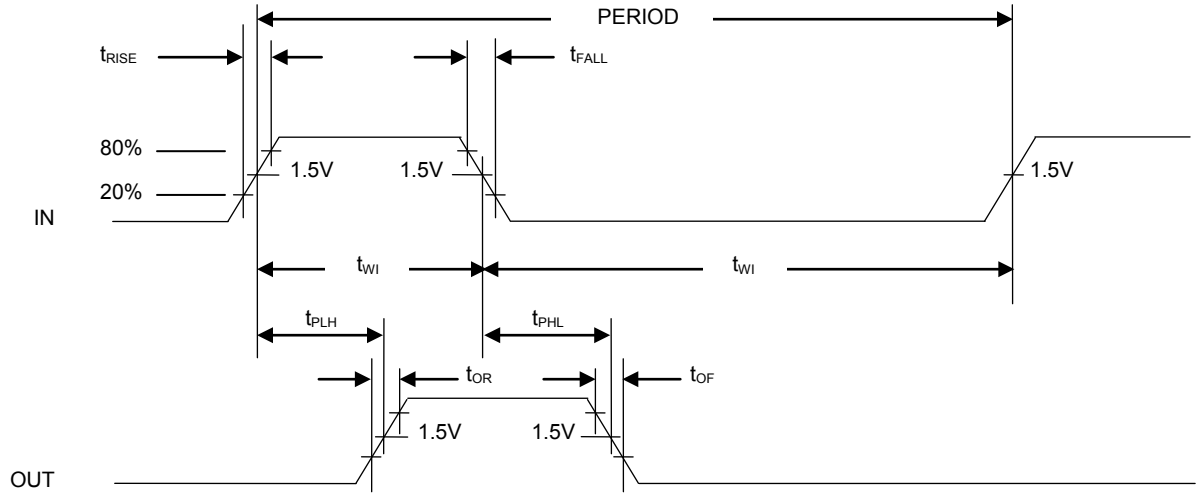
Ambient Temperature: 25°C ± 3°C
Supply Voltage (V_{CC}): 5.0V ± 0.1V
Input Pulse:
High: 3.0V ± 0.1V
Low: 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise and Fall Time: 3.0ns Max. - Measured between 0.6V and 2.4V.
Pulse Width: 500ns
Pulse Period: 1µs
Output Load Capacitance: 15pF
Output: Each output is loaded with the equivalent of one 74F04 input gate.
Data is measured at the 1.5V level on the rising and falling edges.

Note: The above conditions are for test only and do not restrict the devices under other data sheet conditions.

NOTES:

1. All voltages are referenced to ground.
2. Pulse width and duty cycle specifications may be exceeded; however, accuracy will be application sensitive with respect to decoupling, layout, etc.
3. Power-up time is the time from the application of power to the time stable delays are being produced at the output.

TIMING DIAGRAM



TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5-volt point on the leading edge and the 1.5-volt point on the trailing edge or the 1.5-volt point on the trailing edge and the 1.5-volt point on the leading edge.

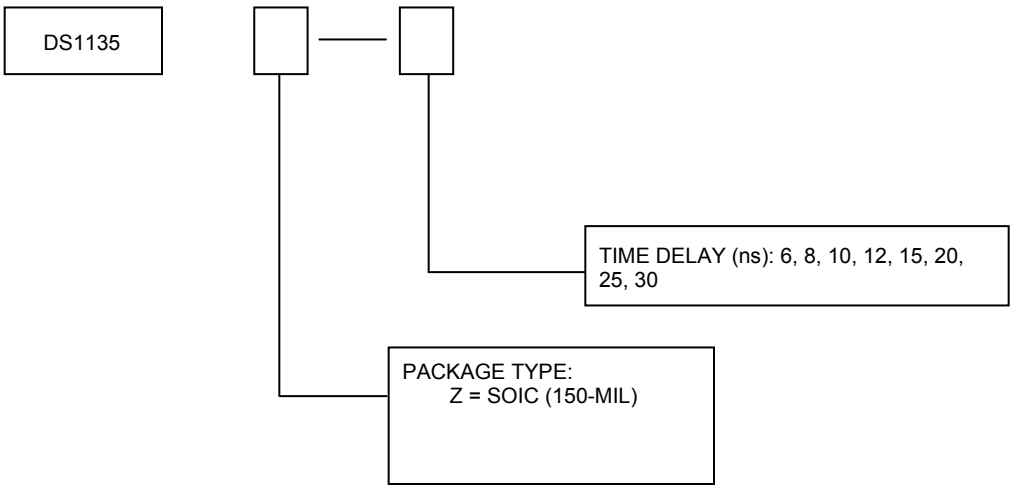
t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge on the input pulse.

t_{PLH} (Time Delay, Rising): The elapsed time between the 1.5-volt point on the leading edge of the input pulse and the 1.5-volt point on the leading edge of the output pulse.

t_{PHL} (Time Delay, Falling): The elapsed time between the 1.5-volt point on the falling edge of the input pulse and the 1.5-volt point on the falling edge of the output pulse.

ORDERING INFORMATION



PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+2	21-0041	90-0096

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
8/12	Removed the DIP and µSOP packages; updated the *Absolute Maximum Ratings section*; added the *Package Information* section	1, 2, 4, 6

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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