Low Voltage, Dual SPDT Analog Switch with Charge Pump

DESCRIPTION

The DG2616, DG2617, DG2618 are monolithic CMOS analog switching products designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2616, DG2617, DG2618 are ideal for portable and battery powered applications.

The DG2616, DG2617, DG2618 have built-in charge-pump circuitry which lowers the minimum supply voltage to + 1.5 V while maintaining low on-resistance. The Control circuitry allows the DG2616, DG2617, DG2618 to operate in different configurations.

Built on Vishay Siliconix's low voltage process, the DG2616, DG2617, DG2618 has an epitaxial layer that prevents latch-up. Break-before-make is guaranteed.

The DG2616, DG2617, DG2618 are manufactured in space saving DFN-10 (3.0 x 3.0 mm). And as a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations and is 100 % RoHS compliant.

FEATURES

- Low voltage operation (1.5 V to 3.6 V)
- Low on-resistance - R_{ON}: 4.2 Ω typ. at 2.7 V
- Fast switching: t_{ON} = 39 ns
  t_{OFF} = 8 ns
- DFN-10 package

Pb-free
RoHS COMPLIANT

BENEFITS

- Reduced power consumption
- High accuracy
- Reduce board space
- TTL/1.8 V logic compatible
- High bandwidth

APPLICATIONS

- Cellular phones
- Audio and video signal routing
- PCMCIA cards
- Battery operated systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TRUTH TABLE DG2616

Logic	NC1, 2	NO1, 2
0	ON	OFF
1	OFF	ON

TRUTH TABLE DG2617

SHDN/$\overline{EN}$ Logic	IN Logic	NC1, 2	NO1, 2	Charge Pump
0	0	ON	OFF	ON
0	1	OFF	ON	ON
1	0	ON	OFF	OFF
1	1	OFF	ON	OFF

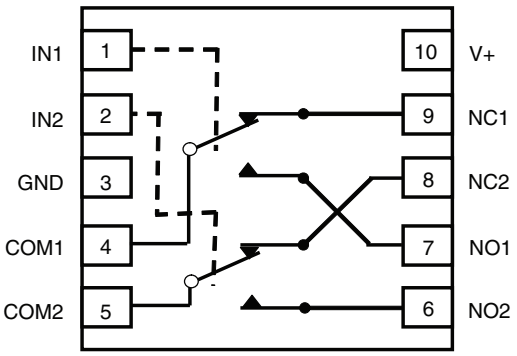
TRUTH TABLE DG2618

SHDN/$\overline{EN}$ Logic	IN Logic	NC1, 2	NO1, 2	Charge Pump
0	0	ON	OFF	ON
0	1	OFF	ON	ON
1	x	OFF	OFF	OFF

ORDERING INFORMATION

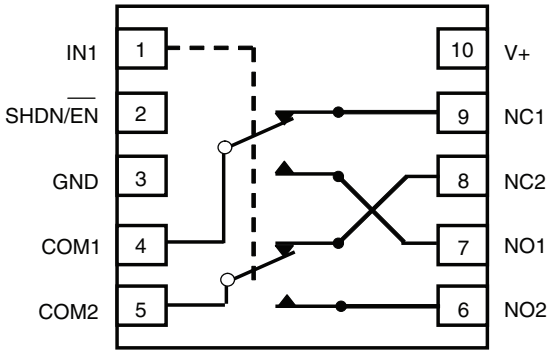
Temp. Range	Package	Part Number
- 40 °C to 85 °C	DFN-10	DG2616DN-T1-E4 DG2617DN-T1-E4 DG2618DN-T1-E4

DG2616



Top View

DG2617/DG2618



Top View

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted			
Parameter		**Limit**	**Unit**
Reference to GND	V+	- 0.3 to 6.0	V
	IN, COM, NC, NO[a]	- 0.3 to (V+ + 0.3)	
Current (Any terminal except NO, NC or COM)		30	mA
Continuous Current (NO, NC, or COM)		± 150	
Peak Current (Pulsed at 1 ms, 10 % Duty Cycle)		± 300	
Storage Temperature (D-Suffix)		- 65 to 150	°C
Package Solder Reflow Conditions[d]			
Power Dissipation (Packages)[b]	DFN-10[c]	1191	mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 14.9 mW/°C above 70 °C

d. Manual soldering with iron is not recommended for leadless components. The DFN-10 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

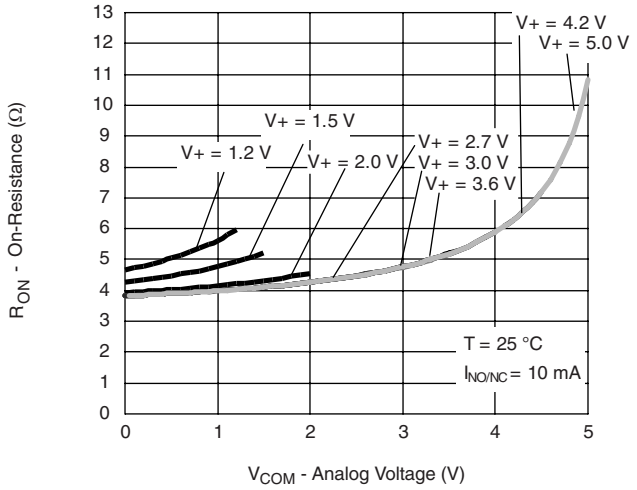
SPECIFICATIONS V+ = 3 V							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.5 or 1.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 1.5 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		5.3	7.0 8.0	Ω
		V+ = 2.7 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 10 mA	Room		4.2	7.0	
		V+ = 2.7 V, V_{COM} = 2.7 V, I_{NO}, I_{NC} = 10 mA			4.7		
			Full			8.0	
		V+ = 3.6 V, V_{COM} = 3.6 V, I_{NO}, I_{NC} = 10 mA	Room Full		5.5	7.0 8.0	
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 1.5 V, 2.7 V, I_{NO}, I_{NC} = 10 mA	Room		0.6	2.0	
R_{ON} Match[d]	ΔR_{ON}		Room		0.1		
On Resistance (Shutdown)	R_{SHDN}	V+ = 3.6 V, V_{COM} = 1.7 V, I_{NO}, I_{NC} = 10 mA	Room Full		15	20 21	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.6 V, V_{NO}, V_{NC} = 0.3 V/3.3 V, V_{COM} = 3.3 V/0.3 V	Room Full	- 2 - 10		2 10	nA
	$I_{COM(off)}$		Room Full	- 2 - 10		2 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.6 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3.3 V	Room Full	- 2 - 10		2 10	
Digital Control							
Input High Voltage	V_{INH}	V+ = 1.5 V	Full	1.0			V
		V+ = 2.7 V to 3.6 V		1.4			
Input Low Voltage	V_{INL}	V+ = 1.5 V				0.4	
		V+ = 2.7 V to 3.6 V				0.5	
Input Capacitance	C_{in}		Full		3.2		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V+ = 2.7 or 3.6 V, V_{NO} or V_{NC} = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room Full		39	69 76	ns
Turn-Off Time	t_{OFF}		Room Full		9	39 41	
Break-Before-Make Time	t_d		Full	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		7		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 77		dB
		R_L = 50 Ω, C_L = 5 pF, f = 100 MHz			- 32		
Crosstalk[d, f]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz			- 80		
		R_L = 50 Ω, C_L = 5 pF, f = 100 MHz			- 32		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	f = 1 MHz	Room		9		pF
	$C_{NC(off)}$		Room		7		
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		21		
	$C_{NC(on)}$		Room		19		

SPECIFICATIONS V+ = 3 V							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.5 or 1.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Power Supply							
Power Supply Range	V+			1.5		3.6	V
Power Supply Current	I+	V+ = 3.6 V, V_{IN} = 0 or V+, SHDN/$\overline{EN}$ = 0 V	Full		104	300	µA
		V+ = 3.6 V, V_{IN} = 0 or V+, SHDN/$\overline{EN}$ = V+			0.1	2	

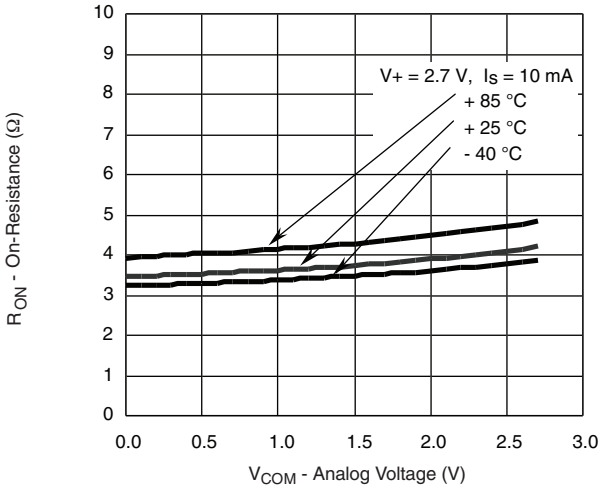
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Crosstalk measured between channels.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

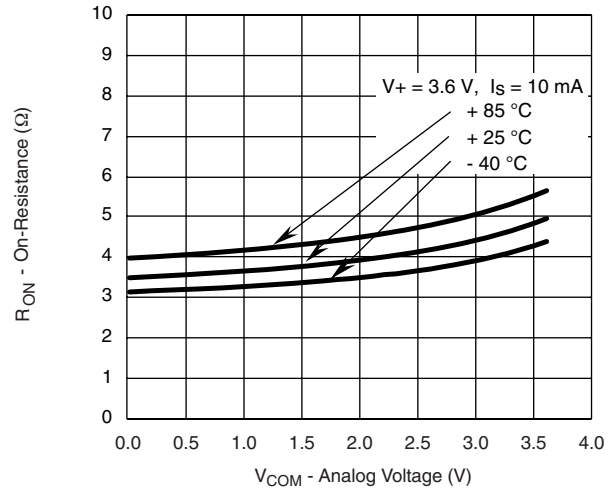
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



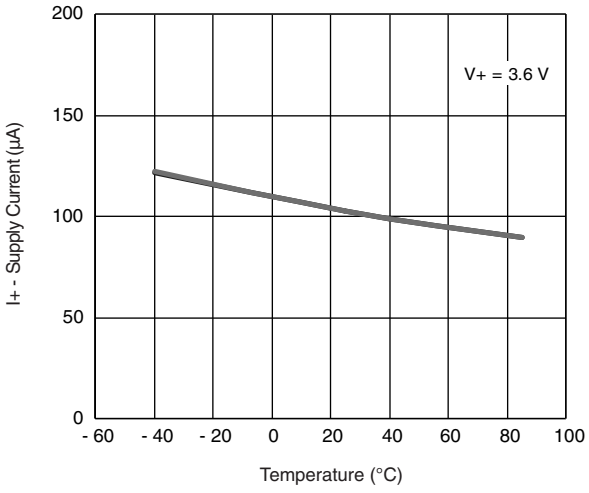
R_{ON} vs. V_{COM} and Supply Voltage



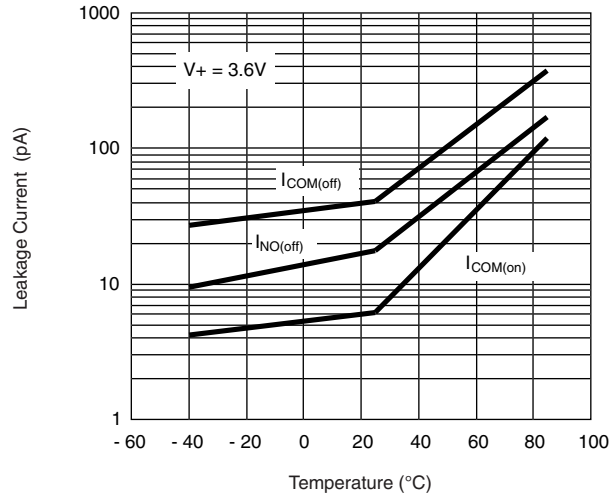
R_{ON} vs. Analog Voltage and Temperature



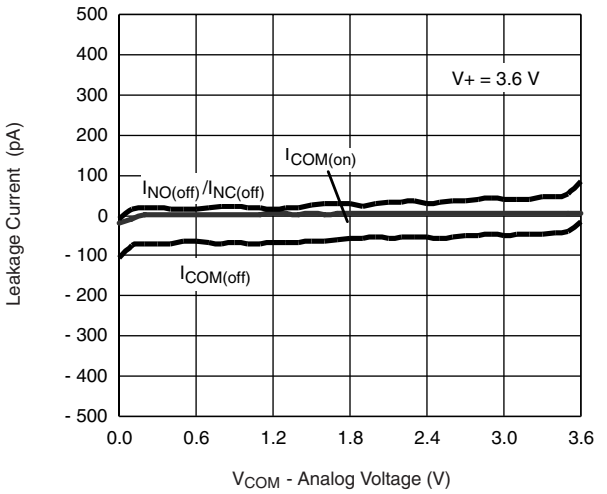
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

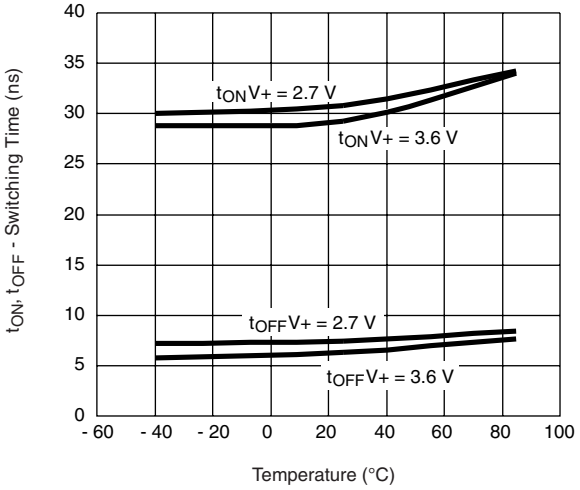


Leakage Current vs. Temperature

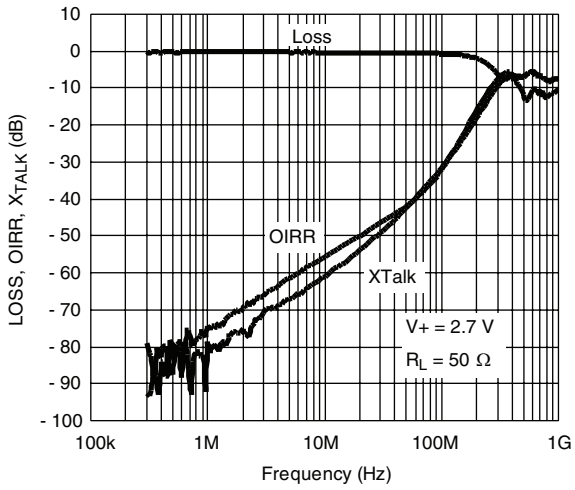


Leakage vs. Analog Voltage

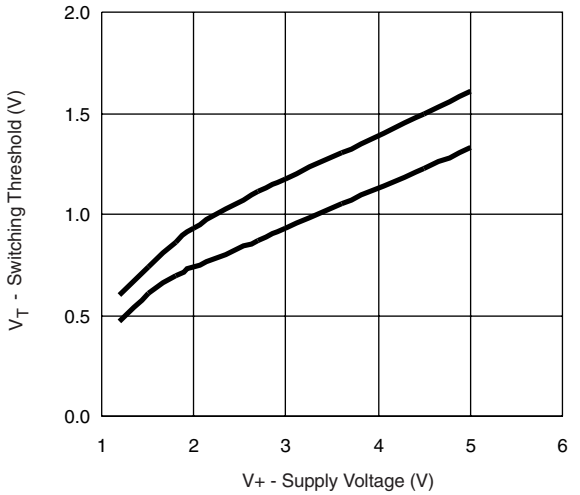
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



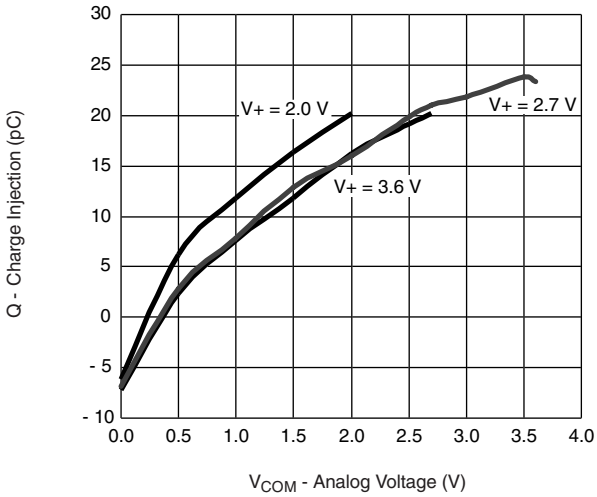
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

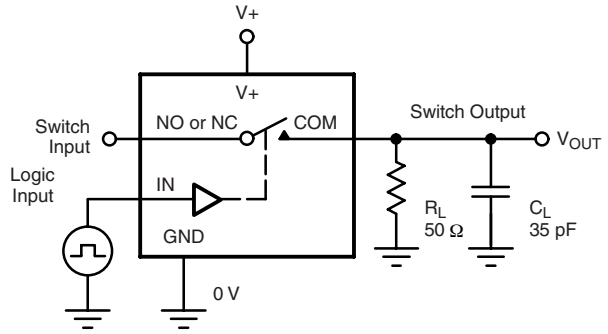


Switching Threshold vs. Supply Voltage



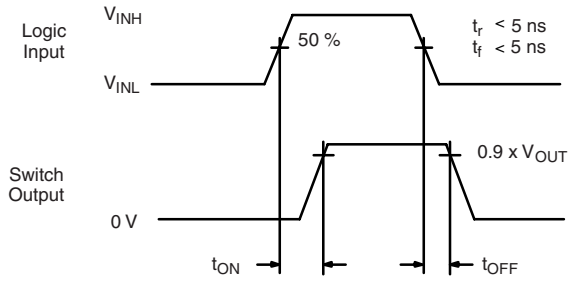
Charge Injection vs. Analog Voltage

TEST CIRCUITS



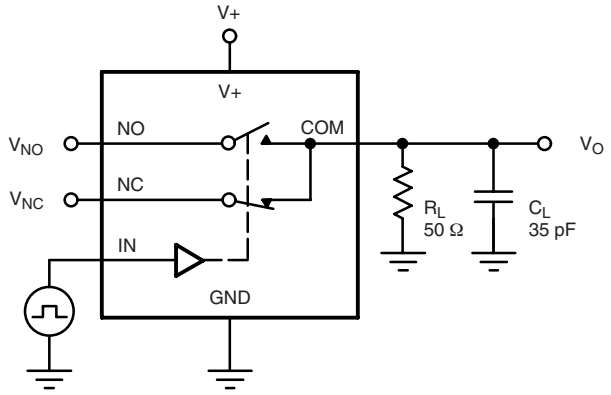
C_L (includes fixture and stray capacitance)

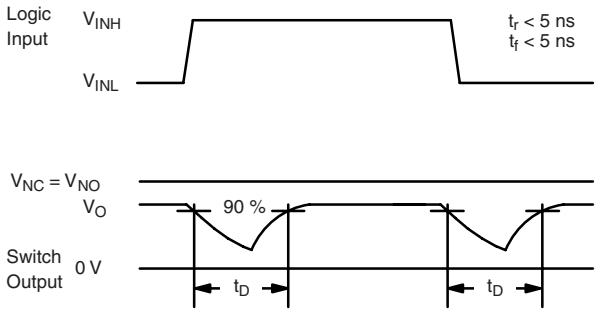
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

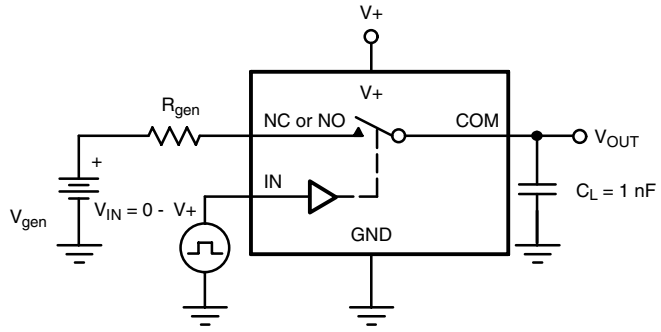
Figure 1. Switching Time

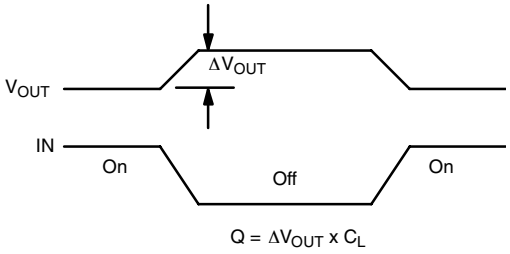




C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

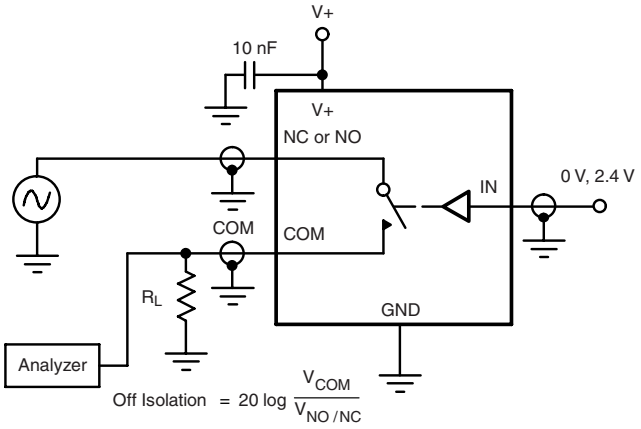


Figure 4. Off-Isolation

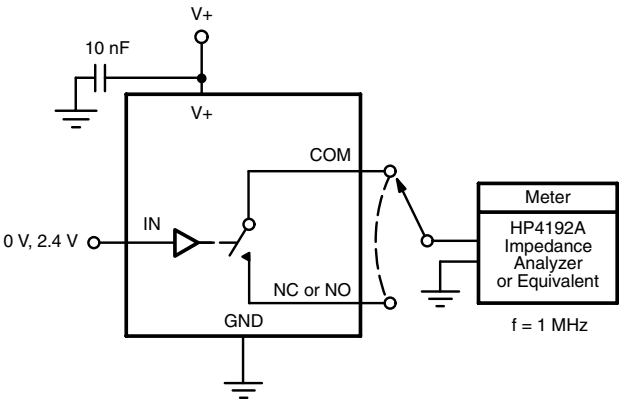
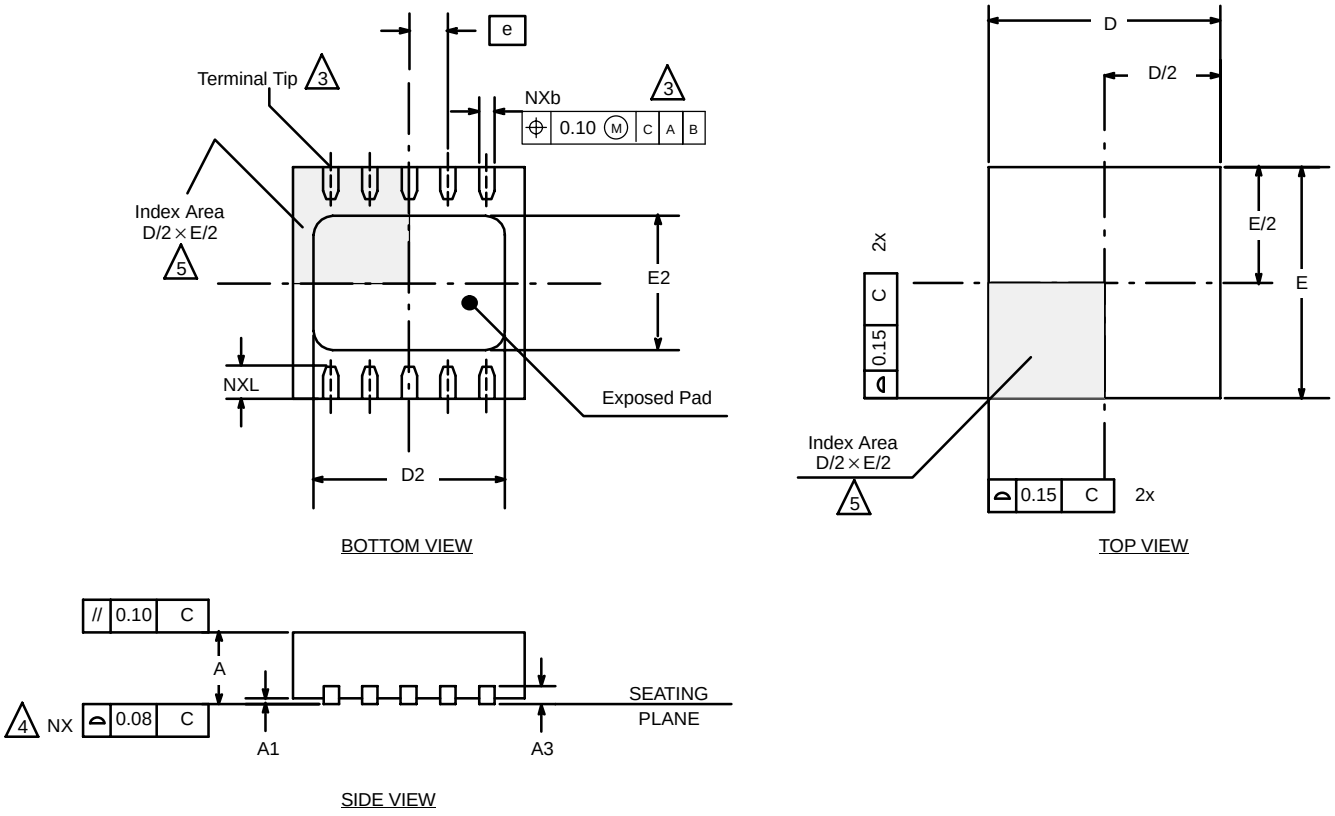


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?74411.

DFN-10 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 BSC			0.008 BSC	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	2.20	2.38	2.48	0.087	0.094	0.098
E		3.00 BSC			0.118 BSC	
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

*Use millimeters as the primary measurement.

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DWG: 5943

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