CY2305
CY2309

Low Cost 3.3 V Zero Delay Buffer

Features

- 10 MHz to 100/133 MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- 60-ps typical cycle-to-cycle jitter (high drive)
- Multiple low skew outputs
  - 85 ps typical output-to-output skew
  - One input drives five outputs (CY2305)
  - One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309)
- Compatible with Pentium-based systems
- Test Mode to bypass phase-locked loop (PLL) (CY2309)
- Packages:
  - 8-pin, 150-mil SOIC package (CY2305)
  - 16-pin 150-mil SOIC or 4.4-mm TSSOP (CY2309)
- 3.3 V operation
- Commercial and industrial temperature ranges

Functional Description

The CY2309 is a low-cost 3.3 V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305 is an 8-pin version of the CY2309. It accepts one reference input, and drives out five low skew clocks. The -1H versions of each device operate at up to 100-/133 MHz frequencies, and have higher drive than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY2309 has two banks of four outputs each, which can be controlled by the select inputs as shown in Select Input Decoding on page 5. If all output clocks are not required, BankB can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

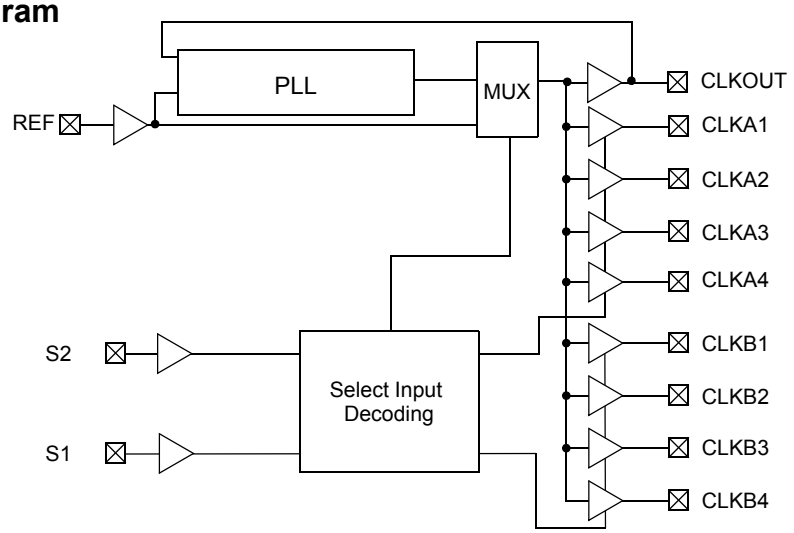
The CY2305 and CY2309 PLLs enter a power-down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 25.0 µA current draw for these parts. The CY2309 PLL shuts down in one additional case as shown in Select Input Decoding on page 5.

Multiple CY2305 and CY2309 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

The CY2305/CY2309 is available in two or three different configurations, as shown in Ordering Information on page 16. The CY2305-1/CY2309-1 is the base part. The CY2305-1H/CY2309-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1.

For a complete list of related documentation, click here.

Logic Block Diagram



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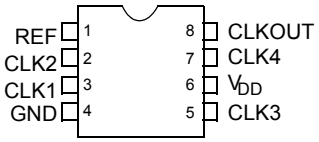
Pin Diagram

Figure 1. 8-pin SOIC pinout
CY2305



Pin Description

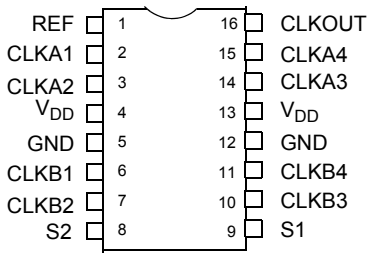
For CY2305

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5-V tolerant input
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3-V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2]	Buffered clock output, internal feedback on this pin

Notes
1. Weak pull down.
2. Weak pull down on all outputs.

Pin Diagram

Figure 2. 16-pin SOIC / TSSOP pinout
CY2309



Pin Description

For CY2309

Pin	Signal	Description
1	REF[3]	Input reference frequency, 5-V tolerant input
2	CLKA1[4]	Buffered clock output, Bank A
3	CLKA2[4]	Buffered clock output, Bank A
4	V_{DD}	3.3-V supply
5	GND	Ground
6	CLKB1[4]	Buffered clock output, Bank B
7	CLKB2[4]	Buffered clock output, Bank B
8	S2[5]	Select input, bit 2
9	S1[5]	Select input, bit 1
10	CLKB3[4]	Buffered clock output, Bank B
11	CLKB4[4]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3-V supply
14	CLKA3[4]	Buffered clock output, Bank A
15	CLKA4[4]	Buffered clock output, Bank A
16	CLKOUT[4]	Buffered output, internal feedback on this pin

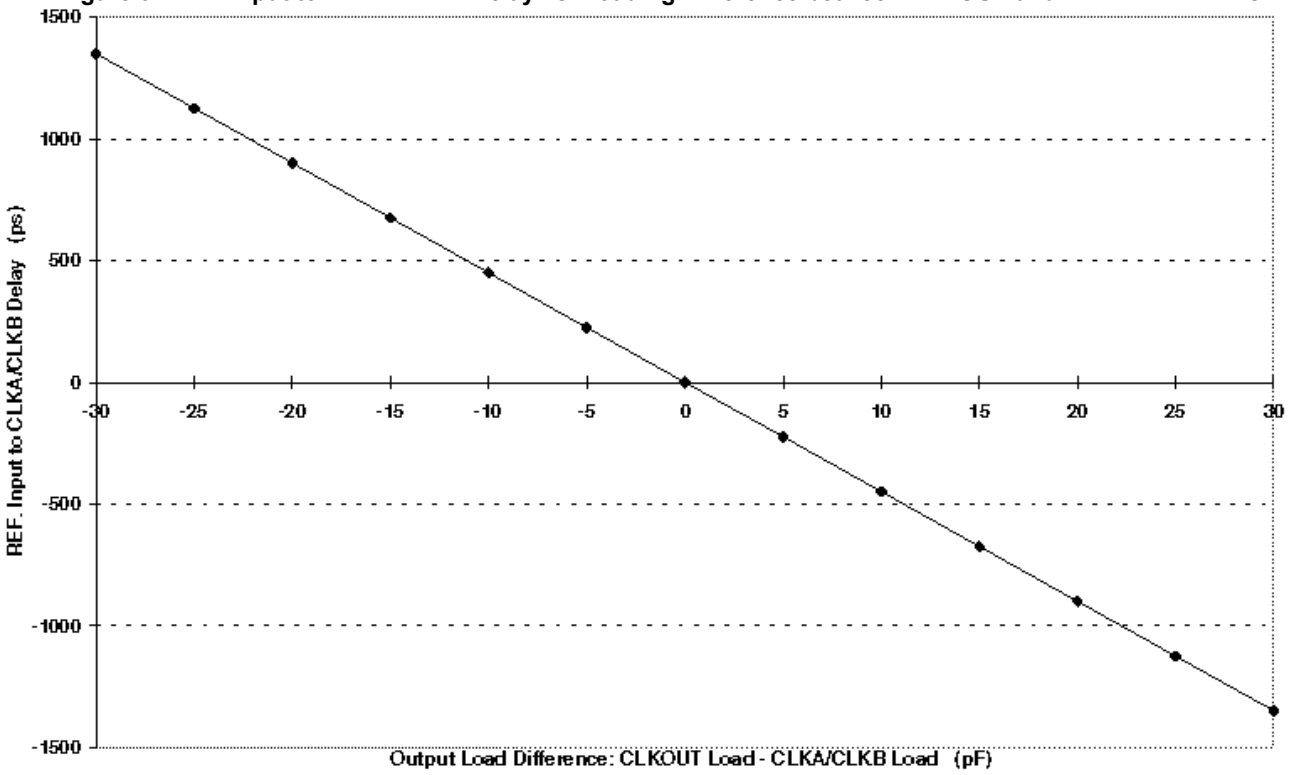
Notes
3. Weak pull down.
4. Weak pull down on all outputs.
5. Weak pull ups on these inputs.

Select Input Decoding

For CY2309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT [6]	Output Source	PLL Shutdown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Figure 3. REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB Pins



Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve zero delay between the input and output. Because the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use Figure 3 to calculate loading differences between the CLKOUT pin and other outputs.

Note

6. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply voltage to ground potential .....–0.5 V to +7.0 V
DC input voltage (Except REF) .....–0.5 V to V_{DD} + 0.5 V
DC input voltage REF .....–0.5 V to 7 V
Storage temperature ..... –65°C to +150°C
Junction temperature ..... 150°C
Static discharge voltage
(per MIL-STD-883, Method 3015) .....> 2,000 V

Operating Conditions

For CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
C_L	Load capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

For CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage [7]		–	0.8	V
V_{IH}	Input HIGH voltage [7]		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output LOW voltage [8]	I_{OL} = 8 mA (–1)	–	0.4	V
		I_{OL} = 12 mA (–1H)			
V_{OH}	Output HIGH voltage [8]	I_{OH} = –8 mA (–1)	2.4	–	V
		I_{OH} = –12 mA (–1H)			
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	12.0	µA
I_{DD}	Supply current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{SS}	–	32.0	mA

Notes
7. REF input has a threshold voltage of V_{DD}/2.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Operating Conditions

For CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	–40	85	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
C_L	Load capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

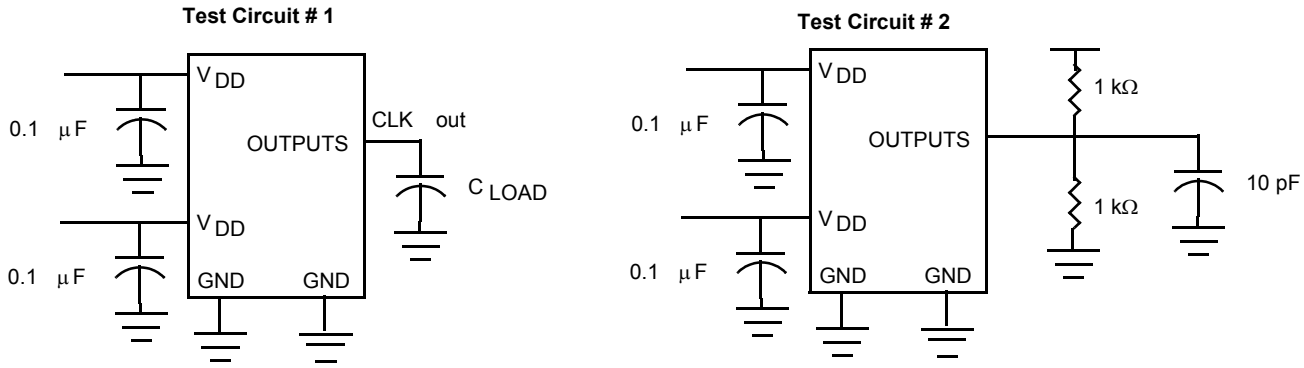
For CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage [9]		–	0.8	V
V_{IH}	Input HIGH voltage [9]		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	100.0	µA
V_{OL}	Output LOW voltage [10]	I_{OL} = 8 mA (–1)	–	0.4	V
		I_{OL} =12 mA (–1H)			
V_{OH}	Output HIGH voltage [10]	I_{OH} = –8 mA (–1)	2.4	–	V
		I_{OH} = –12 mA (–1H)			
I_{DD} (PD mode)	Power-down supply current	REF = 0 MHz	–	25.0	µA
I_{DD}	Supply current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{SS}	–	35.0	mA

Notes
9. REF input has a threshold voltage of $V_{DD}/2$.
10. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Test Circuits

Figure 4. Test Circuits



For parameter t_8 (output slew rate) on -1H devices

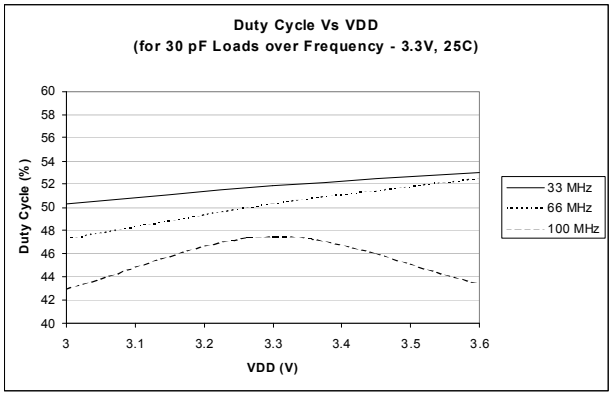
Thermal Resistance

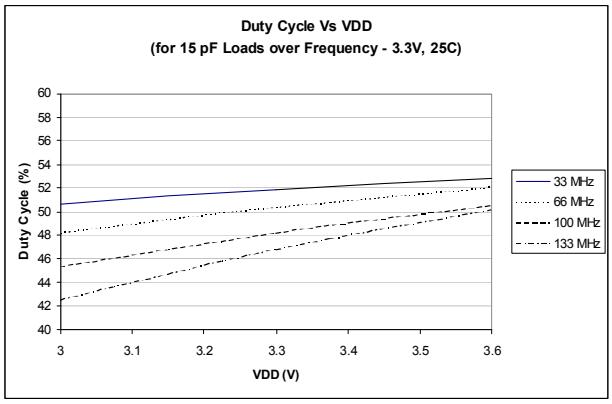
Parameter [11]	Description	Test Conditions	8-pin SOIC	16-pin SOIC	16-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	140	111	117	°C/W
θ_{JC}	Thermal resistance (junction to case)		54	60	22	°C/W

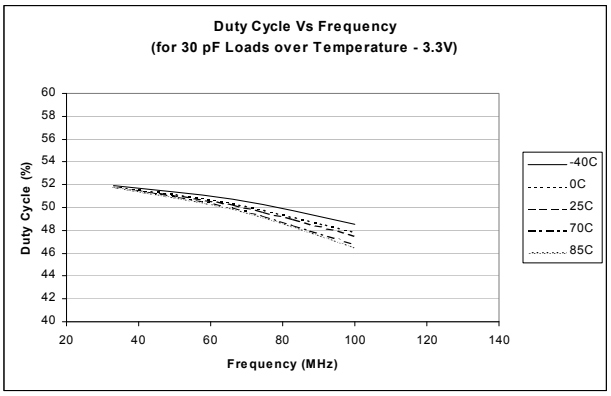
Note
11. These parameters are guaranteed by design and are not tested.

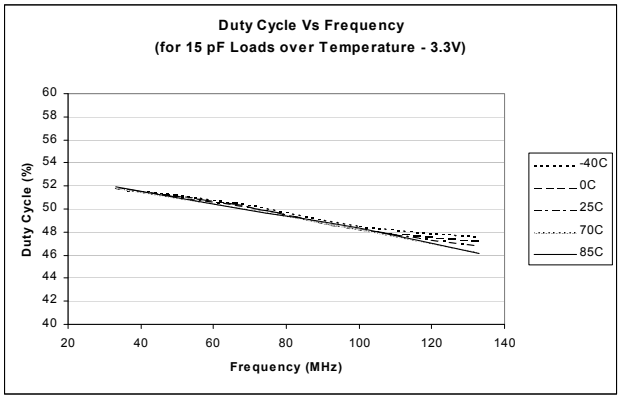
Typical Duty Cycle and I_{DD} Trends

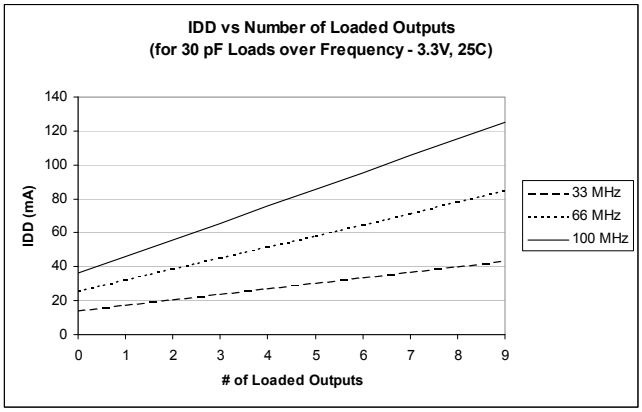
For CY2305-1 and CY2309-1 [12, 13]

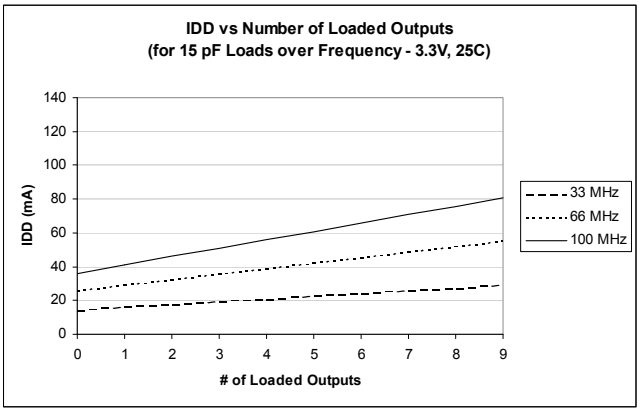










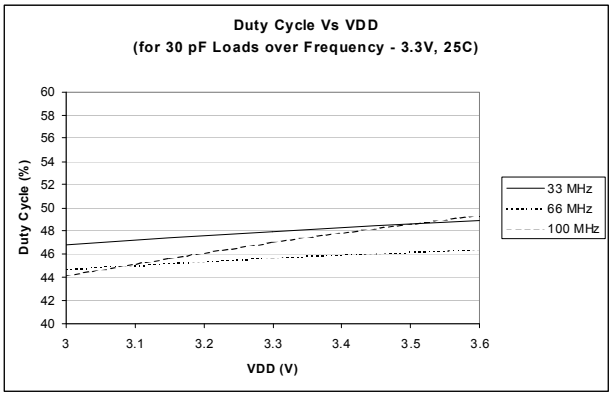


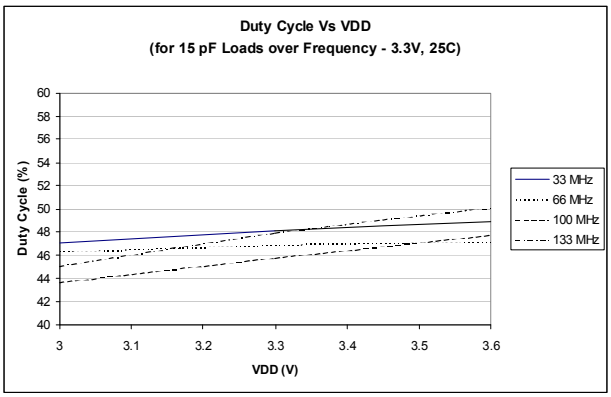
Notes

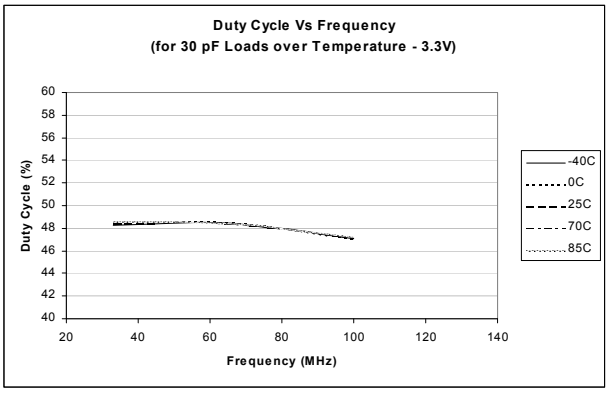
12. Duty cycle is taken from typical chip measured at 1.4 V.
13. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz)).

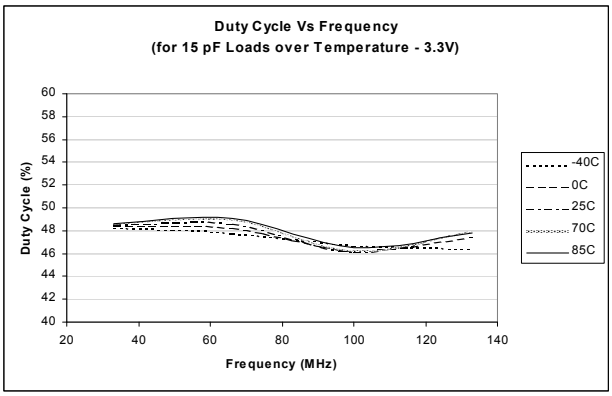
Typical Duty Cycle and I_{DD} Trends

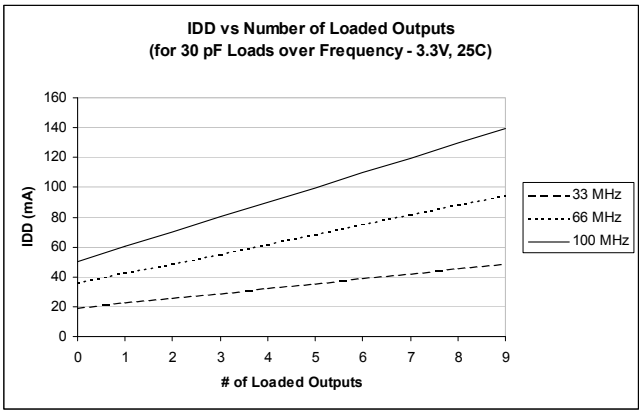
For CY2305-1H and CY2309-1H [14, 15]

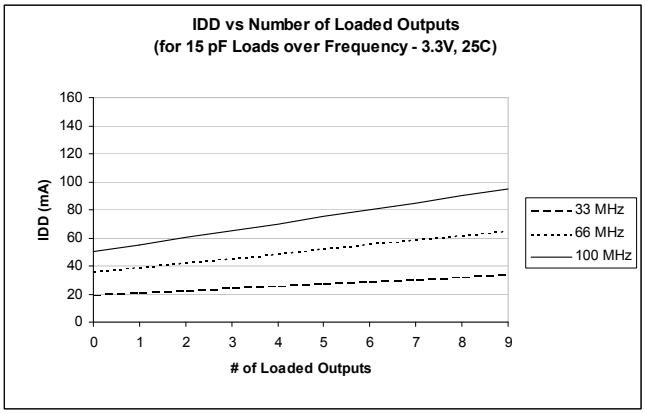












Notes

14. Duty cycle is taken from typical chip measured at 1.4 V.
15. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz)).

Switching Characteristics

For CY2305SC-1 and CY2309SC-1 Commercial Temperature Devices

Parameter [16]	Description	Test Conditions	Min	Typ	Max	Unit
t1	Output frequency	30-pF load	10	–	100	MHz
		10-pF load	10	–	133.33	MHz
t_{DC}	Duty cycle [17] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise time [17]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_4	Fall time [17]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_5	Output-to-output skew [17]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [17]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [17]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew [17]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_J	Cycle-to-cycle jitter [17]	Measured at 66.67 MHz, loaded outputs	–	70	200	ps
t_{LOCK}	PLL lock time [17, 18, 19]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes
16. All parameters specified with loaded outputs.
17. Parameter is guaranteed by design and characterization. Not 100% tested in production.
18. The clock outputs are undefined until PLL is locked.
19. For on the fly change in reference input frequency, PLL lock time is only guaranteed when stop time between change in input reference frequency is > 10 µs, Figure 10.

Switching Characteristics

For CY2305SC-1H and CY2309SC-1H Commercial Temperature Devices

Parameter [20]	Description	Condition	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load	10	–	100	MHz
		10 pF load	10	–	133.33	MHz
t_{DC}	Duty cycle [21] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t_{DC}	Duty cycle [21] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} < 50 MHz	45.0	50.0	55.0	%
t_3	Rise time [21]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_4	Fall time [21]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_5	Output-to-output skew [21]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [21]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [21]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew [21]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_8	Output slew rate [21]	Measured between 0.8 V and 2.0 V using Test Circuit #2	1	–		V/ns
t_J	Cycle-to-cycle jitter [21]	Measured at 66.67 MHz, loaded outputs	–	60	200	ps
t_{LOCK}	PLL lock time [21, 22, 23]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes
20. All parameters specified with loaded outputs.
21. Parameter is guaranteed by design and characterization. Not 100% tested in production.
22. The clock outputs are undefined until PLL is locked.
23. For on the fly change in reference input frequency, PLL lock time is only guaranteed when stop time between change in input reference frequency is > 10 µs, Figure 10.

Switching Characteristics

For CY2305SI-1 and CY2309SI-1 Industrial Temperature Devices

Parameter [24]	Description	Test Conditions	Min	Typ	Max	Unit
t1	Output frequency	30 pF load	10	–	100	MHz
		10 pF load	10	–	133.33	MHz
t_{DC}	Duty cycle [25] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise time [25]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_4	Fall time [25]	Measured between 0.8 V and 2.0 V	–	–	2.50	ns
t_5	Output-to-output skew [25]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [25]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [25]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew [25]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_J	Cycle-to-cycle jitter [25]	Measured at 66.67 MHz, loaded outputs	–	70	200	ps
t_{LOCK}	PLL lock time [25, 26, 27]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes
24. All parameters specified with loaded outputs.
25. Parameter is guaranteed by design and characterization. Not 100% tested in production.
26. The clock outputs are undefined until PLL is locked.
27. For on the fly change in reference input frequency, PLL lock time is only guaranteed when stop time between change in input reference frequency is > 10 µs, Figure 10.

Switching Characteristics

For CY2305SI-1H and CY2309SI-1H Industrial Temperature Devices

Parameter [28]	Description	Conditions	Min	Typ	Max	Unit
t_1	Output frequency	30 pF load	10	–	100	MHz
		10 pF load	10	–	133.33	MHz
t_{DC}	Duty cycle [29] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t_{DC}	Duty cycle [29] = $t_2 \div t_1$	Measured at 1.4 V, F_{out} < 50 MHz	45.0	50.0	55.0	%
t_3	Rise time [29]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_4	Fall time [29]	Measured between 0.8 V and 2.0 V	–	–	1.50	ns
t_5	Output-to output skew [29]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF rising edge to CLKOUT rising edge [29]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF rising edge to CLKOUT rising edge [29]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device-to-device skew [29]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_8	Output slew rate [29]	Measured between 0.8 V and 2.0 V using Test Circuit #2	1	–	–	V/ns
t_J	Cycle-to-cycle jitter [29]	Measured at 66.67 MHz, loaded outputs	–	60	200	ps
t_{LOCK}	PLL lock time [29, 30, 31]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes
28. All parameters specified with loaded outputs.
29. Parameter is guaranteed by design and characterization. Not 100% tested in production.
30. The clock outputs are undefined until PLL is locked.
31. For on the fly change in reference input frequency, PLL lock time is only guaranteed when stop time between change in input reference frequency is > 10 µs, Figure 10.

Switching Waveforms

Figure 5. Duty Cycle Timing

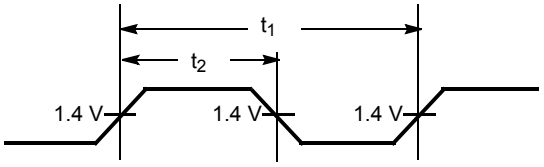


Figure 6. All Outputs Rise/Fall Time

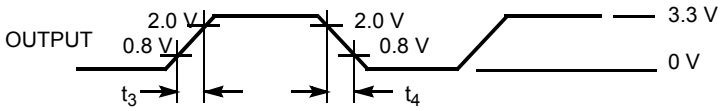


Figure 7. Output-Output Skew

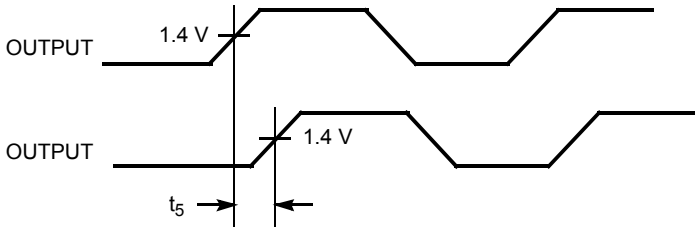


Figure 8. Input-Output Propagation Delay

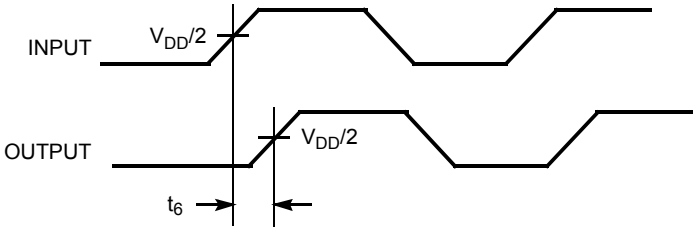


Figure 9. Device-Device Skew

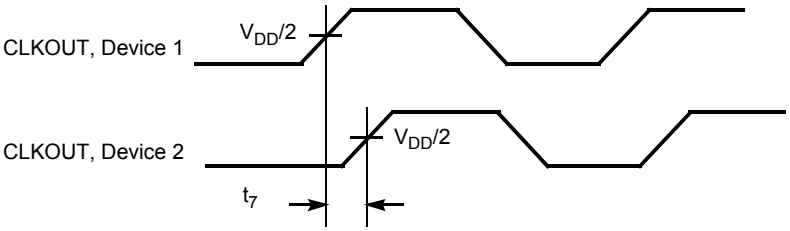
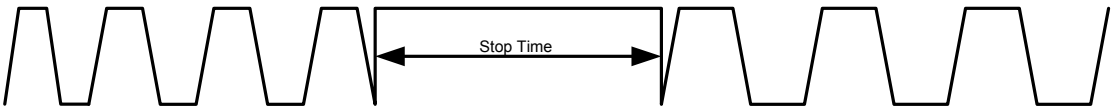


Figure 10. Stop Time between Change in Input Reference Frequency



Ordering Information

For CY2305

Ordering Code	Package Type	Operating Range
CY2305SC-1	8-pin SOIC (150 Mils)	Commercial
CY2305SC-1T	8-pin SOIC (150 Mils) – Tape and Reel	Commercial
Pb-free		
CY2305SXC-1	8-pin SOIC (150 Mils)	Commercial
CY2305SXC-1T	8-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2305SXI-1	8-pin SOIC (150 Mils)	Industrial
CY2305SXI-1T	8-pin SOIC (150 Mils) – Tape and Reel	Industrial
CY2305SXC-1H	8-pin SOIC (150 Mils)	Commercial
CY2305SXC-1HT	8-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2305SXI-1H	8-pin SOIC (150 Mils)	Industrial
CY2305SXI-1HT	8-pin SOIC (150 Mils) – Tape and Reel	Industrial

Ordering Information

For CY2309

Ordering Code	Package Type	Operating Range
Pb-free		
CY2309SXC-1	16-pin SOIC (150 Mils)	Commercial
CY2309SXC-1T	16-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2309SXI-1	16-pin SOIC (150 Mils)	Industrial
CY2309SXI-1T	16-pin SOIC (150 Mils) – Tape and Reel	Industrial
CY2309SXC-1H	16-pin SOIC (150 Mils)	Commercial
CY2309SXC-1HT	16-pin SOIC (150 Mils) – Tape and Reel	Commercial
CY2309SXI-1H	16-pin SOIC (150 Mils)	Industrial
CY2309SXI-1HT	16-pin SOIC (150 Mils) – Tape and Reel	Industrial
CY2309ZXC-1H	16-pin TSSOP (4.4 mm)	Commercial
CY2309ZXC-1HT	16-pin TSSOP (4.4 mm) – Tape and Reel	Commercial
CY2309ZXI-1H	16-pin TSSOP (4.4 mm)	Industrial
CY2309ZXI-1HT	16-pin TSSOP (4.4 mm) – Tape and Reel	Industrial

Ordering Code Definitions

CY 2305 S (X) C – 1 (H) (T)

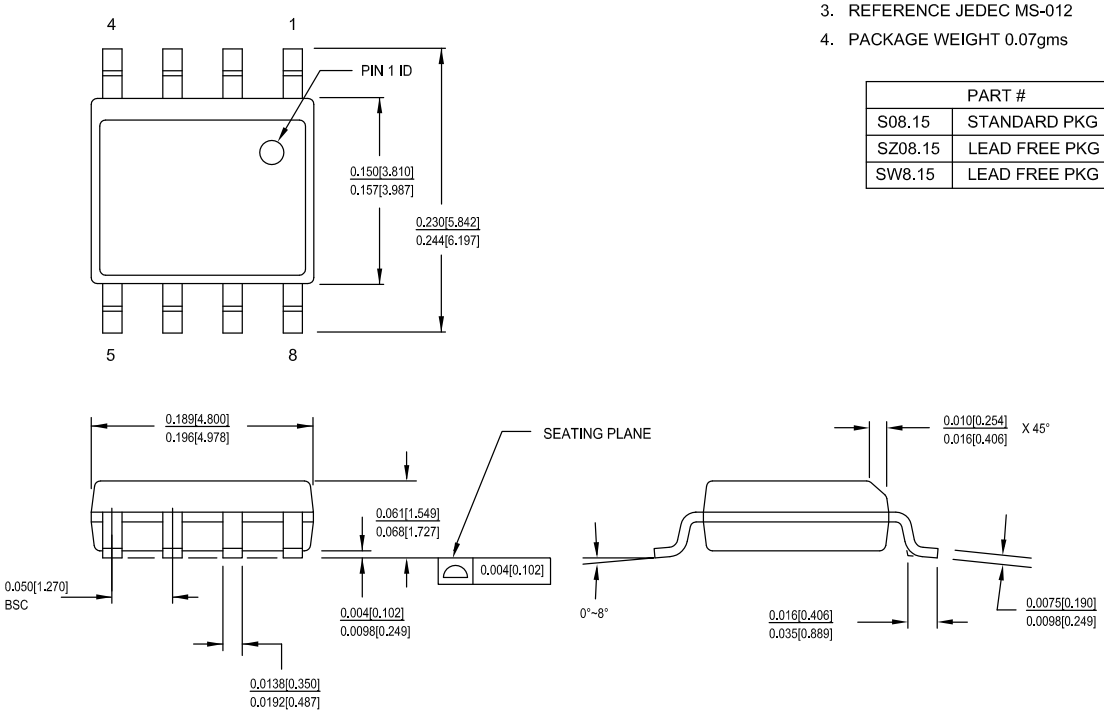
- (T): Tape and reel
- 1 (H): Output Drive:
  - 1 = standard drive
  - 1H = high drive
- C: Temperature Range:
  - C = Commercial
  - I = Industrial
- S (X): Package:
  - S = SOIC, leaded
  - Z = TSSOP, leaded
  - SX = SOIC, Pb-free
  - ZX = TSSOP, Pb-free
- 2305: Base device part number
  - 2305 = 5-output zero delay buffer
  - 2309 = 9-output zero delay buffer
- CY: Company ID: CY = Cypress

Package Drawing and Dimensions

Figure 11. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *H

Package Drawing and Dimensions (continued)

Figure 12. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068

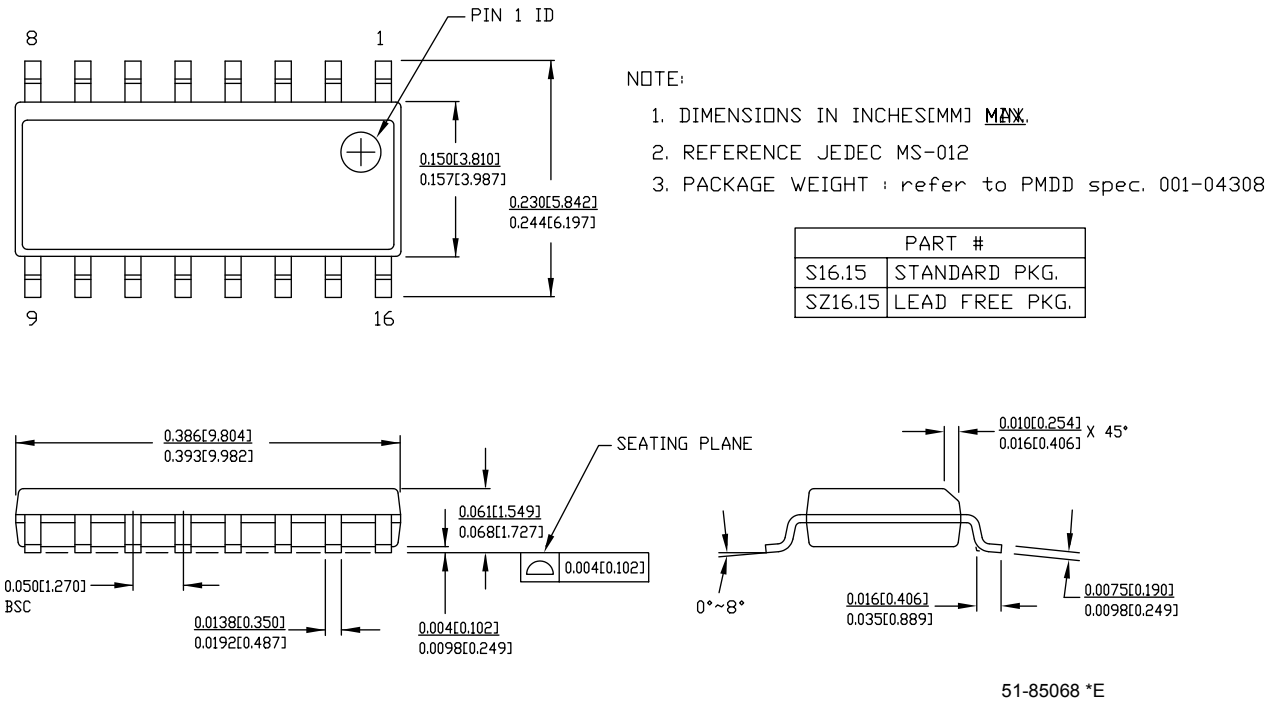
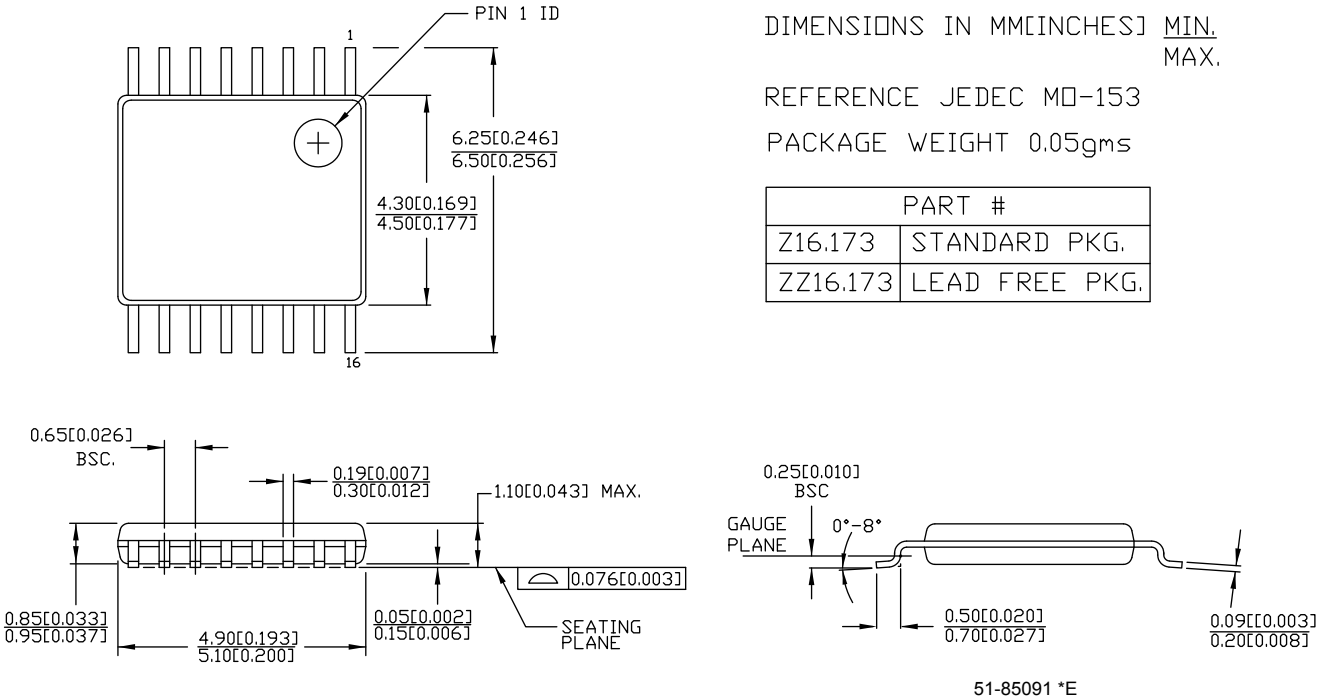


Figure 13. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
PCI	Personal Computer Interconnect
PLL	Phase Locked Loop
SDRAM	Synchronous Dynamic Random Access Memory
SOIC	Small Outline Integrated Circuit
TSSOP	Thin Small Outline Package
ZDB	Zero Delay Buffer

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ms	millisecond
MHz	megahertz
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Errata

This section describes the errata for Cypress Zero Delay Clock Buffers of the family CY2305/CY2309. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CY2305SC-1	All Variants
CY2305SC-1T	All Variants
CY2305SC-1H	All Variants
CY2305SC-1HT	All Variants
CY2305SI-1H	All Variants
CY2305SI-1HT	All Variants
CY2305SXC-1	All Variants
CY2305SXC-1T	All Variants
CY2305SXI-1	All Variants
CY2305SXI-1H	All Variants
CY2305SXC-1HT	All Variants
CY2305SXI-1H	All Variants
CY2305SXI-1HT	All Variants
CY2309NZSXC-1H	All Variants
CY2309NZSXC-1HT	All Variants
CY2309NZSXI-1H	All Variants
CY2309NZSXI-1HT	All Variants
CY2309SC-1HT	All Variants
CY2309SXC-1H	All Variants
CY2309SXC-1HT	All Variants
CY2309SXI-1H	All Variants
CY2309SXI-1HT	All Variants
CY2309ZC-1H	All Variants
CY2309ZC-1HT	All Variants
CY2309ZXC-1H	All Variants
CY2309ZXC-1HT	All Variants
CY2309ZXI-1H	All Variants
CY2309ZXI-1HT	All Variants
CY2309SXC-1	All Variants
CY2309SXC-1T	All Variants
CY2309SXI-1	All Variants
CY2309SXI-1T	All Variants
CY2309SC-1	All Variants
CY2309SC-1T	All Variants
CY2309SXC-1	All Variants
CY2309SXC-1T	All Variants
CY2309SXI-1	All Variants
CY2309SXI-1T	All Variants

CY2305/CY2309 Errata Summary

Items	Part Number	Silicon Revision	Fix Status
Start up lock time issue [CY2305]	All	B	Silicon fixed. New silicon available from WW 25 of 2011
Start up lock time issue [CY2309]	All	B	Silicon fixed. New silicon available from WW 10 of 2013

CY2305/CY2309 Qualification Status

Product Status: In production

Qualification report last updated on 11/27/2012 (http://www.cypress.com/?rID=72595)

1. Start up lock time issue

■ **Problem Definition**

Output of CY2305/CY2309 fails to locks within 1 ms (as per data sheet spec)

■ **Parameters Affected**

PLL lock time

■ **Trigger Condition(S)**

Start up

■ **Scope of Impact**

It can impact the performance of system and its throughput

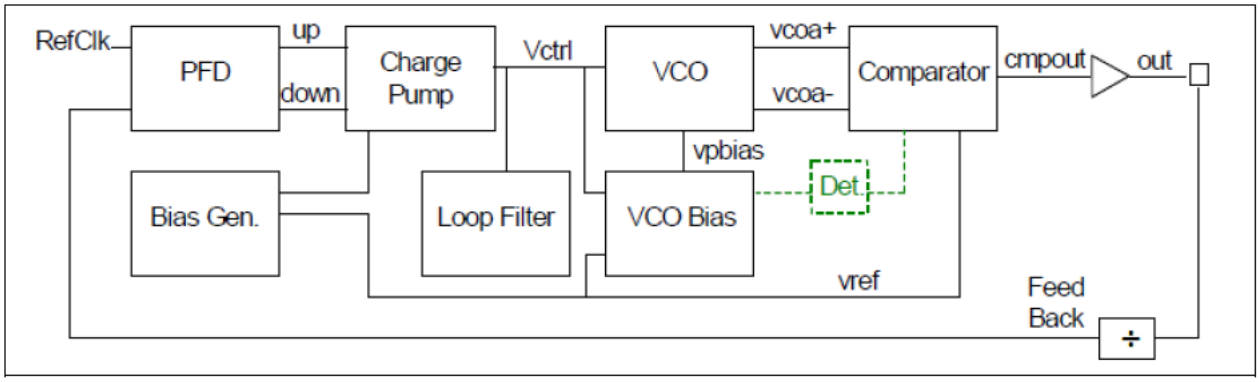
■ **Workaround**

Apply reference input (RefClk) before power up (VDD) Input noise propagates to output due to absence of reference input signal during power up. If reference input is present during power up, the noise will not propagate to output and device will start normally without problems.

■ **Fix Status**

This issue is due to design marginality. Two minor design modifications have been made to address this problem.

- ❒ Addition of VCO bias detector block as shown in the following figure which keeps comparator power down till VCO bias is present and thereby eliminating the propagation of noise to feedback.
- ❒ Bias generator enhancement for successful initialization.



Document History Page

Document Title: CY2305/CY2309, Low Cost 3.3 V Zero Delay Buffer Document Number: 38-07140				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110249	SZV	10/19/01	Change from Spec number: 38-00530 to 38-07140
*A	111117	CKN	03/01/02	Added t6B row to the Switching Characteristics Table; also added the letter "A" to the t6A row Corrected the table title from CY2305SC-IH and CY2309SC-IH to CY2305SI-IH and CY2309SI-IH
*B	117625	HWT	10/21/02	Added eight-pin TSSOP packages (CY2305ZC-1 and CY2305ZC-1T) to the ordering information table. Added the Tape and Reel option to all the existing packages: CY2305SC-1T, CY2305SI-1T, CY2305SC-1HT, CY2305SI-1HT, CY2305ZC-1T, CY2309SC-1T, CY2309SI-1T, CY2309SC-1HT, CY2309SI-1HT, CY2309ZC-1HT, CY2309ZI-1HT
*C	121828	RBI	12/14/02	Power up requirements added to Operating Conditions information
*D	131503	RGL	12/12/03	Added Lead-free for all the devices in the ordering information table
*E	214083	RGL	See ECN	Added a Lead-free with the new coding for all SOIC devices in the ordering information table
*F	291099	RGL	See ECN	Added TSSOP Lead-free devices
*G	390582	RGL	See ECN	Added typical values for jitter
*H	2542461	AESA	07/23/08	Updated template. Added Note "Not recommended for new designs." Added part number CY2305ESXC-1, CY2305ESXC-1T, CY2305ESXI-1, CY2305ESXI-1T, CY2305ESXC-1H, CY2305ESXC-1HT, CY2305ESXI-1H, CY2305ESXI-1HT, CY2309ESXC-1, CY2309ESXC-1T, CY2309ESXI-1, CY2309ESXI-1T, CY2309ESXC-1H, CY2309ESXC-1HT, CY2309ESXI-1H, CY2309ESXI-1HT, CY2309EZXC-1H, CY2309EZXC-1HT, CY2309EZXI-1H, and CY2309EZXI-1HT in ordering information table. Removed part number CY2305SZC-1, CY2305SZC-1T, CY2305SZI-1, CY2305SZI-1T, CY2305SZC-1H, CY2305SZC-1HT, CY2305SZI-1H, CY2305SZI-1HT, CY2309SZC-1, CY2309SZC-1T, CY2309SZI-1, CY2309SZI-1T, CY2309SZC-1H, CY2309SZC-1HT, CY2309SZI-1H, CY2309SZI-1HT, CY2309ZZC-1H, CY2309ZZC-1HT, CY2309ZI-1H, CY2309ZI-1HT, CY2309ZZI-1H, and CY2309ZZI-1HT in Ordering Information table. Changed Lead-Free to Pb-Free.
*I	2565153	AESA	09/18/08	Removed part number CY2305ESXC-1, CY2305ESXC-1T, CY2305ESXI-1, CY2305ESXI-1T, CY2305ESXC-1H, CY2305ESXC-1HT, CY2305ESXI-1H, CY2305ESXI-1HT, CY2309ESXC-1, CY2309ESXC-1T, CY2309ESXI-1, CY2309ESXI-1T, CY2309ESXC-1H, CY2309ESXC-1HT, CY2309ESXI-1H, CY2309ESXI-1HT, CY2309EZXC-1H, CY2309EZXC-1HT, CY2309EZXI-1H, and CY2309EZXI-1HT in ordering information table. Removed note references to note 10 in Pb-Free sections of ordering information table. Changed IDD (PD mode) from 12.0 to 25.0 μA for commercial temperature devices Deleted Duty Cycle parameters for F_{out} < 50 MHz commercial and industrial devices.
*J	2673353	KVM / PYRS	03/13/09	Reverted IDD (PD mode) and Duty Cycle parameters back to the values in revision *H: Changed IDD (PD mode) from 25 to 12 μA for commercial devices. Added Duty Cycle parameters for F_{out} < 50 MHz for commercial and industrial devices.

Document History Page (continued)

Document Title: CY2305/CY2309, Low Cost 3.3 V Zero Delay Buffer Document Number: 38-07140				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	2904641	KVM	04/05/10	Updated Ordering Information: Removed parts CY2305SI-1, CY2305SI-1T, CY2309SI-1, CY2309SI-1H, CY2309SI-1HT, CY2309SI-1T. Updated Package Drawing and Dimensions.
*L	3047136	KVM	10/04/2010	Added Ordering Code Definitions under Ordering Information. Updated Package Drawing and Dimensions. Added Acronyms and Units of Measure.
*M	3146330	CXQ	01/18/2011	Added “Not recommended for new designs” statement to Features on page 1. Added ‘not recommended for new designs’ footnote to all parts in the ordering information table.
*N	3241160	BASH	05/09/2011	Added Footnote 9 on page 6 (CDT 97105). Removed first bullet point “Not recommended for new designs. The CY2305C and CY2309C are form, fit, function compatible devices with improved specifications.” from Features section. (CDT 99798). Removed Footnote 20 and all its references from document. (CDT 99798).
*O	3400613	BASH	10/10/2011	Added Footnote 19 and its reference to all PLL lock time parameters throughout the document. Added Figure 10 for Stop Time Illustration.
*P	3859773	AJU	01/07/2013	Updated Ordering Information (Updated part numbers). Updated Ordering Information (Updated part numbers). Updated Package Drawing and Dimensions: spec 51-85068 – Changed revision from *D to *E.
*Q	3997602	AJU	05/11/2013	Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *E to *F. Added Errata.
*R	4124780	CINM	10/24/2013	Updated to new template. Completing Sunset Review.
*S	4307827	CINM	03/13/2014	Updated Errata.
*T	4578443	TAVA	11/25/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Ordering Information (Updated part numbers). Updated Ordering Information (Updated part numbers).
*U	5206812	TAVA	04/05/2016	Updated Zero Delay and Skew Control: Updated description. Updated Package Drawing and Dimensions: spec 51-85066 – Changed revision from *F to *H. Updated to new template.
*V	5242499	SDHK / PSR	04/26/2016	Updated Electrical Characteristics: Updated details in “Test Conditions” column corresponding to V_{OL} and V_{OH} parameters. Updated Operating Conditions: Added t_{PU} parameter and its details. Updated Electrical Characteristics: Updated details in “Test Conditions” column corresponding to V_{OL} and V_{OH} parameters. Added Thermal Resistance.
*W	5516682	TAVA	11/10/2016	Updated to new template. Completing Sunset Review.
*X	5708778	AESATMP7	04/27/2017	Updated Cypress Logo and Copyright.

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