ADS8686S 16-Channel, 16-Bit, 1-MSPS, Dual, Simultaneous-Sampling ADC With Integrated Analog Front-End

1 Features

- 16-channel, 16-bit ADC with integrated analog front-end
- Dual simultaneous sampling: 8x2 channels
- Supply:
  - Analog: 5 V
  - Digital: 1.8 V to 5 V
- Constant 1-MΩ input impedance front-end
- Independently programmable input ranges with 20% overrange
- Programmable low-pass filter:
  - 15 kHz, 39 kHz, 376 kHz
- Excellent DC and AC performance
- On-chip reference and reference buffer
- Excellent over temperature performance
- Overvoltage input clamp with 8-kV ESD
- Optional cyclic redundancy check (CRC) error checking
- On-chip self diagnostic function
- Temperature range: –40°C to +125°C

2 Applications

- Multifunction relays
- Servo drive position sensors
- Analog input modules
- Data acquisition (DAQ)

3 Description

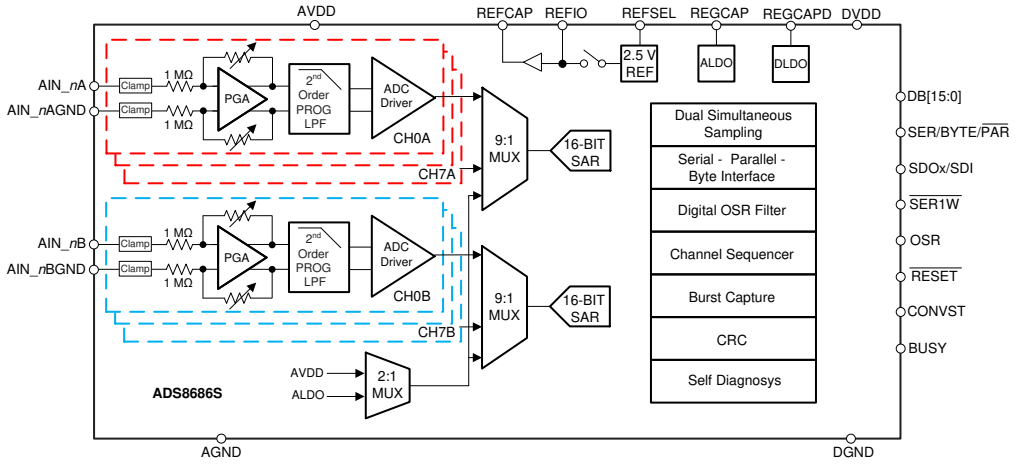
The ADS8686S is a 16-channel data acquisition (DAQ) system based on a dual simultaneous-sampling, 16-bit successive approximation register (SAR) analog-to-digital converter (ADC). The ADS8686S features a complete analog front-end for each channel with an input clamp, 1-MΩ input impedance, independently programmable gain amplifier (PGA), programmable low-pass filter, and an ADC input driver. The device also features a low-drift, precision reference with a buffer to drive the ADCs. A flexible digital interface supporting serial, parallel, and byte communication enables the device to be used with a variety of host controllers.

The ADS8686S can be configured to accept ±10-V, ±5-V, or ±2.5-V bipolar inputs with a 20% overrange option using a single 5-V supply. The high input impedance allows direct connection with sensors and transformers, thus eliminating the need for external driver circuits. The ADS8686S has a highly configurable channel sequencer to reduce the sequencing overhead on the backend controller or processor. The high performance and accuracy, along with zero-latency conversions offered by this device make the ADS8686S a great choice for multiple industrial applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS8686S	LQFP (80)	14.00 mm x 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Device Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision B (May 2020) to Revision C (July 2020)	Page
• Changed AC performance parameters	9

Changes from Revision A (March 2020) to Revision B (May 2020)	Page
• Changed device status from advance information to production data	1

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5 Pin Configuration and Functions

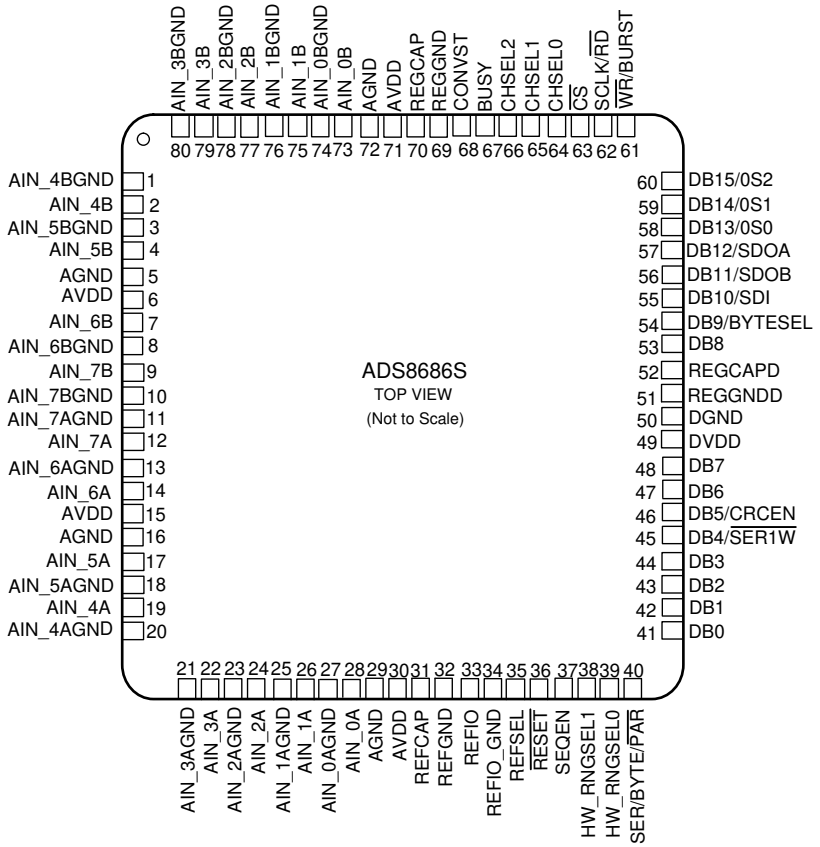

Figure 5-1. PM Package: PZA, 80-Pin LQFP (Top View)

Table 5-1. Pin Functions

NAME	NO.	TYPE[1]	DESCRIPTION
AGND	5, 16, 29, 72	P	Analog supply ground pins
AIN_0AGND	27	AI	Analog input channel 0A: negative input
AIN_0A	28	AI	Analog input channel 0A: positive input
AIN_0BGND	74	AI	Analog input channel 0B: negative input
AIN_0B	73	AI	Analog input channel 0B: positive input
AIN_1AGND	25	AI	Analog input channel 1A: negative input
AIN_1A	26	AI	Analog input channel 1A: positive input
AIN_1BGND	76	AI	Analog input channel 1B: negative input
AIN_1B	75	AI	Analog input channel 1B: positive input
AIN_2AGND	23	AI	Analog input channel 2A: negative input
AIN_2A	24	AI	Analog input channel 2A: positive input
AIN_2BGND	78	AI	Analog input channel 2B: negative input
AIN_2B	77	AI	Analog input channel 2B: positive input
AIN_3AGND	21	AI	Analog input channel 3A: negative input
AIN_3A	22	AI	Analog input channel 3A: positive input
AIN_3BGND	80	AI	Analog input channel 3B: negative input
AIN_3B	79	AI	Analog input channel 3B: positive input
AIN_4AGND	20	AI	Analog input channel 4A: negative input
AIN_4A	19	AI	Analog input channel 4A: positive input
AIN_4BGND	1	AI	Analog input channel 4B: negative input
AIN_4B	2	AI	Analog input channel 4B: positive input

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Table 5-1. Pin Functions (continued)

NAME	NO.	TYPE[1]	DESCRIPTION
AIN_5AGND	18	AI	Analog input channel 5A: negative input
AIN_5A	17	AI	Analog input channel 5A: positive input
AIN_5BGND	3	AI	Analog input channel 5B: negative input
AIN_5B	4	AI	Analog input channel 5B: positive input
AIN_6AGND	13	AI	Analog input channel 6A: negative input
AIN_6A	14	AI	Analog input channel 6A: positive input
AIN_6BGND	8	AI	Analog input channel 6B: negative input
AIN_6B	7	AI	Analog input channel 6B: positive input
AIN_7AGND	11	AI	Analog input channel 7A: negative input
AIN_7A	12	AI	Analog input channel 7A: positive input
AIN_7BGND	10	AI	Analog input channel 7B: negative input
AIN_7B	9	AI	Analog input channel 7B: positive input
AVDD	6, 15, 30, 71	P	Analog supply pins. Decouple these pins to the closest AGND pins. See the *Power Supply Recommendations* section.
BUSY	67	DO	Logic output indicating an ongoing conversion; see the *BUSY (Output)* section.
CHSEL0	64	DI	Logic input pin to select the channel or program the hardware mode sequencer; see the *CHSEL[2:0] (Input)* section.
CHSEL1	65	DI	Logic input pin to select the channel or program the hardware mode sequencer; see the *CHSEL[2:0] (Input)* section.
CHSEL2	66	DI	Logic input pin to select the channel or program the hardware mode sequencer; see the *CHSEL[2:0] (Input)* section.
CONVST	68	DI	Logic input to control the conversion start input for channel group A and channel group B; see the *CONVST (Input)* section.
$\overline{CS}$	63	DI	Active low logic input chip select; see the *CS (Input)* section.
DB0	41	DIO	This pin is the data input/output DB0 (LSB) in parallel and parallel byte interface modes. In serial mode, this pin must be connected to DGND. See the *DB[3:0] (Input/Output)* section.
DB1	42	DIO	This pin is the data input/output DB1 in parallel and parallel byte interface modes. In serial mode, this pin must be connected to DGND. See the *DB[3:0] (Input/Output)* section.
DB2	43	DIO	This pin is the data input/output DB2 in parallel and parallel byte interface modes. In serial mode, this pin must be connected to DGND. See the *DB[3:0] (Input/Output)* section.
DB3	44	DIO	This pin is the data input/output DB3 in parallel and parallel byte interface modes. In serial mode, this pin must be connected to DGND. See the *DB[3:0] (Input/Output)* section.
DB4/ $\overline{SER1W}$	45	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB4 in parallel and parallel byte interface modes. This pin is the logic input pin in serial mode to configure data capture using both SDOA and SDOB or just SDOA. The signal state is latched on the release of a full RESET, and requires an additional full RESET to be reconfigured. See the *DB4/SER1W (Input/Output)* section.
DB5/CRCEN	46	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB5 in parallel and parallel byte interface modes. This pin is the logic input pin in hardware serial mode to enable the cyclic redundancy check (CRC) word. The signal is latched on the release of a full reset, and requires an additional full RESET to be reconfigured. In software mode, this pin must be connected to DGND. See the *DB5/CRCEN (Input/Output)* section.
DB6	47	DIO	This pin is the data input/output DB6 in parallel and parallel byte interface modes. See the *DB[7:6] (Input/Output)* section.
DB7	48	DIO	This pin is the data input/output DB7 in parallel and parallel byte interface modes. See the *DB[7:6] (Input/Output)* section.
DB8	53	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB8 in parallel interface mode. In serial mode, this pin must be connected to DGND. See the *DB8 (Input/Output)* section.

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Table 5-1. Pin Functions (continued)

NAME	NO.	TYPE[1]	DESCRIPTION
DB9/BYTESEL	54	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB9 in parallel interface mode. This pin is the logic input pin that enables the parallel byte interface. The signal is latched on the release of a full RESET, and requires an additional full RESET to be reconfigured. See the *DB9/BYTESEL (Input/Output)* section.
DB10/SDI	55	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB10 in parallel interface mode. This pin is the serial data input that programs the device in software serial mode. Tie this pin to DGND for parallel byte interface mode. See the *DB10/SDI (Input/Output)* section.
DB11/SDOB	56	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB11 in parallel interface mode. This pin is the serial data output port B in serial interface mode if enabled by the DB4/ $\overline{\text{SER1W}}$ pin at full RESET. Tie this pin to DGND when in parallel byte interface mode. See the *DB11/SDOB (Input/Output)* section.
DB12/SDOA	57	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB12 in parallel interface mode. This pin is the serial data output port A in serial interface mode. Tie this pin to DGND when in parallel byte interface mode. See the *DB12/SDOA (Input/Output)* section.
DB13/OS0	58	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB13 in parallel interface mode. This pin is the logic input pin for the oversampling rate (OSR) setting. The signal is latched on the release of a full RESET, and requires an additional full RESET to be reconfigured. See the *DB13/OS0 (Input/Output)* section.
DB14/OS1	59	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB14 in parallel interface mode. This pin is the logic input pin for the OSR setting. The signal is latched on the release of a full RESET, and requires an additional full RESET to be reconfigured. See the *DB14/OS1 (Input/Output)* section.
DB15/OS2	60	DIO	This pin is a multifunctional logic input/output pin. This pin is the data input/output DB15 in parallel interface mode. This pin is the logic input pin for the OSR setting. The signal is latched on the release of a full RESET, and requires an additional full RESET to be reconfigured. See the *DB15/OS2 (Input/Output)* section.
DGND	50	P	Digital ground
DVDD	49	P	Digital supply pin. Decouple with DGND on pin 50 with a minimum 0.1-µF capacitor.
HW_RNGSEL1, HW_RNGSEL0	38, 39	DI	Hardware and software mode selection inputs. Hardware and software mode selection is latched at full reset. In hardware mode, these pins select the input range and are not latched. In software mode, these pins are latched and ignored until the next RESET event. HW_RNGSELx = 00: software mode; the ADS8686S is configured via the software registers. HW_RNGSELx = 01: hardware mode; the analog input range is ±2.5 V. HW_RNGSELx = 10: hardware mode; the analog input range is ±5 V. HW_RNGSELx = 11: hardware mode; the analog input range is ±10 V. See the *HW_RANGESEL[1:0] (Input)* section.
REFCAP	31	AO	Reference amplifier output pin. This pin must be decoupled to REFGND using a low equivalent series resistance (ESR), 10-µF ceramic capacitor. Place this capacitor as close to the REFCAP pin as possible. Do not drive any external load from this pin.
REFGND	32	P	Reference GND. Connect this pin to the AGND plane with the shortest trace possible.
REFIO	33	AIO	This pin acts as an internal reference output when REFSEL is high. This pin functions as an input pin for the external reference when REFSEL is low. Decouple this pin with REFIO_GND on pin 34 using a 0.1-µF capacitor.
REFIO_GND	34	P	REFIO ground. Connect this pin to the AGND plane with the shortest trace possible.
REFSEL	35	DI	Active high logic input to enable the internal reference. See the *REFSEL (Input)* section.
REGCAP	70	P	Voltage output from the internal analog regulator. Decouple this output pin separately to REGGND using a 10-µF capacitor. Place the capacitor close to the REGCAP pin.
REGCAPD	52	P	Voltage output from the internal digital regulator. Decouple this output pin separately to REGGNDD using a 10-µF capacitor. Place the capacitor close to the REGCAPD pin.
REGGND	69	P	Internal analog regulator GND. Connect this pin to the AGND plane with the shortest trace possible.
REGGNDD	51	P	Internal digital regulator GND. Connect this pin to the DGND plane with the shortest trace possible.

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Table 5-1. Pin Functions (continued)

NAME	NO.	TYPE(1)	DESCRIPTION
$\overline{\text{RESET}}$	36	DI	Active low logic input to reset the device digital logic. The duration of the $\overline{\text{RESET}}$ pulse decides the partial or full RESET of the device. See the *RESET (Input)* section.
SCLK/ $\overline{\text{RD}}$	62	DI	This pin is a multifunctional logic input pin. This pin is the logic input pin for the Serial Clock in serial interface mode. This pin is the logic input pin in parallel and parallel byte interface modes. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel and parallel byte modes, the output bus is enabled. See the *SCLK/RD (Input)* section.
SEQEN	37	DI	Active high logic input to enable the channel sequencer in hardware mode. The state is latched with a device full RESET. Tie this pin to DGND in software mode. See the *SEQEN (Input)* section.
SER/BYTE/ $\overline{\text{PAR}}$	40	DI	Logic input to select between serial, parallel byte, or parallel interface mode. Tie this pin to logic high and DB9/BYTESEL to logic low to select the serial interface mode. Tie this pin to logic high and DB9/BYTESEL to logic high to select the parallel BYTE interface mode. Tie this pin to logic low to select the parallel interface mode. The signal state is latched at full RESET, and requires an additional full RESET to be reconfigured. See the *SER/BYTE/PAR (Input)* section.
$\overline{\text{WR}}$/BURST	61	DI	This pin is a multifunctional logic input pin (see the *WR/BURST (Input)* section). $\overline{\text{WR}}$ is the logic input pin to write the register configuration in software parallel and parallel byte interface modes. BURST is the logic input pin to enable burst mode operation in the hardware mode of operation. The signal is latched on the release of a full RESET, and requires an additional full RESET to be reconfigured; see the *Burst Sequencer* section. Tie this pin to DGND when in software serial mode.

(1) AI = analog input, AO = analog output, AIO = analog input/output, DI = digital input, DO = digital output, DIO = digital input/output, P = power supply.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1).

	MIN	MAX	UNIT
AVDD to AGND	–0.3	7	V
DVDD to DGND	–0.3	7	V
AGND to DGND	–0.3	0.3	V
REFGND to AGND	–0.3	0.3	V
AINxP to AGND	–15	15	V
AINxGND to AGND	–15	15	V
REFCAPA, REFCAPB to REFGND	–0.3	5.5	V
REFIO to AGND	–0.3	5.5	V
Digital input to DGND	–0.3	DVDD+0.3	V
Digital output to DGND	–0.3	DVDD+0.3	V
Input current to any pin except supply pins (2)	–10	10	mA
Operating temperature	–40	125	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pin current input or output must be limited to 10 mA or less.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	All pins except analog inputs(1)	±2000	V
			Analog input pins(1)	±8000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		4.75		5.25	V
DVDD	Digital supply voltage		1.71		AVDD	V
ANALOG INPUTS						
V_{FSR}	Full-scale input range (AIN_xx to AIN_xxGND)(1)	Software, hardware selectable range = ±10 V	–10		10	V
		Software, hardware selectable range = ±5 V	–5		5	
		Software, hardware selectable range = ±2.5 V	–2.5		2.5	
		Software selectable range = ±10 V with overrange	–12		12	
		Software selectable range = ±5 V with overrange	–6		6	
		Software selectable range = ±2.5 V with overrange	–3		3	
AIN_*n*X	Operating input voltage, positive input	Software, hardware selectable range = ±10 V	–10		10	V
		Software, hardware selectable range = ±5 V	–5		5	
		Software, hardware selectable range = ±2.5 V	–2.5		2.5	
		Software selectable range = ±10 V with overrange	–12		12	
		Software selectable range = ±5 V with overrange	–6		6	
		Software selectable range = ±2.5 V with overrange	–3		3	
AIN_*n*XGND	Operating input voltage, negative input	All input ranges	–0.3	0	0.3	V
EXTERNAL REFERENCE						
V_{REF}	REFIO voltage		2.495	2.5	2.505	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40		125	℃

(1) Ideal input span; does not include gain or offset error.

6.4 Thermal Information

THERMAL METRIC(1)		ADS8686S PZA (LQFP) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

At AVDD = 5 V, DVDD= 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, internal or external V_{REF} = 2.5 V, LPF option = 1; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = +25°C, AVDD = 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
ANALOG INPUTS						
R_{IN}	Input impedance	Input ranges = ±10 V, ±5 V, ±2.5 V, T_A = 25°C	0.85	1	1.15	MΩ
		20% overrange setting for ±10 V, ±5 V, ±2.5 V, T_A = 25°C	1	1.2	1.4	MΩ
	Input impedance temperature drift	All input ranges		10	25	ppm/°C
	Input capacitance			10		pF
V_{Bias}	Internal bias voltage for analog front-end	Software, hardware selectable range = ±10 V	2.02	2.1	2.16	V
		Software, hardware selectable range = ±5 V	1.72	1.8	1.88	
		Software, hardware selectable range = ±2.5 V	1.37	1.45	1.53	
		Software selectable range = ±10 V with overrange	2.36	2.45	2.54	
		Software selectable range = ±5 V with overrange	1.81	1.9	1.99	
		Software selectable range = ±2.5 V with overrange	1.46	1.55	1.64	
$I_{ANL(IN)}$	Analog input current	All input ranges		(V_{IN} – V_{BIAS}) / R_{IN}		µA
ANALOG INPUT FILTER						
$BW_{(-3\ dB)}$	Analog input LPF bandwidth –3 dB	Filter option 1, range = ±10 V and overrange		39		kHz
		Filter option 1, range = ±5 V, ±2.5 V and overrange		33		
		Filter option 2, all input ranges		15		
		Filter option 3, all input ranges		376		
$BW_{(-0.1\ dB)}$	Analog input LPF bandwidth –0.1 dB	Filter option 1, range = ±10 V and overrange		6.9		kHz
		Filter option 1, range = ±5 V, ±2.5 V and overrange		5.9		
		Filter option 2, all input ranges		3.1		
		Filter option 3, all input ranges		60		

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6.5 Electrical Characteristics (continued)

At AVDD = 5 V, DVDD= 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, internal or external V_{REF} = 2.5 V, LPF option = 1; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = +25°C, AVDD = 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
t_{GROUP}	Group delay	Filter option 1, range = ±10 V and overrange		5.2	6	µs
		Filter option 1, range = ±5 V and overrange		6.2		
		Filter option 1, range = ± 2.5V and overrange		6.2		
		Filter option 2, range = ±10 V and overrange		13.2	15.1	
		Filter option 2, range = ±5 V and overrange		13.2		
		Filter option 2, range = ±2.5 V and overrange		13.3		
		Filter option 3, range = ±10 V and overrange		0.9	1.1	
		Filter option 3, range = ±5 V and overrange		0.9		
		Filter option 3, range = ±2.5 V and overrange		0.94		
	Group delay temperature drift	Filter option 1, range = ±10 V		0.3	5	ns/°C
		Filter option 2, range = ±10 V		0.6	2	
		Filter option 3, range = ±10 V		0.2	1	
	Group delay matching	Filter option 1, range = ±10 V and overrange		20	131	ns
		Filter option 1, range = ±5 V and overrange		24		
		Filter option 1, range = ±2.5 V and overrange		38		
		Filter option 2, range = ±10 V and overrange		52	357	
		Filter option 2, range = ±5 V and overrange		50		
		Filter option 2, range = ±2.5 V and overrange		56		
		Filter option 3, range = ±10 V and overrange		10	104	
		Filter option 3, range = ±5 V and overrange		12		
		Filter option 3, range = ±2.5 V and overrange		24		
DC CHARACTERISTICS						
	Resolution		16			Bits
NMC	No missing codes		16			Bits
DNL	Differential nonlinearity	All input ranges	–0.85	±0.2	0.85	LSB
		Range = ±10 V, T_A = 0°C to 70°C	–0.5	±0.2	0.5	
		Range = ±5 V, T_A = 0°C to 70°C	–0.6	±0.25	0.6	
		Range = ±2.5 V, T_A = 0°C to 70°C	–0.65	±0.35	0.65	

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6.5 Electrical Characteristics (continued)

At AVDD = 5 V, DVDD= 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, internal or external V_{REF} = 2.5 V, LPF option = 1; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = +25°C, AVDD = 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
INL	Integral nonlinearity (2)	All input ranges	–2	±0.7	2	LSB
		Range = ±10 V, T_A = 0°C to 70°C	–1.2	±0.6	1.2	
		Range = ±5 V, T_A = 0°C to 70°C	–1.5	±0.7	1.5	
		Range = ±2.5 V, T_A = 0°C to 70°C	–1.6	±0.75	1.6	
TUE	Total unadjusted error	Range = ±10 V with overrange		±3.5		LSB
		Range = ±10 V		±3		
		Range = ±5 V with overrange		±2.5		
		Range = ±5 V		±2.5		
		Range = ±2.5 V with overrange		±2		
		Range = ±2.5 V		±2		
E_G	Gain error(3)	20% overrange setting, external reference	–80	±6	80	LSB
		Range = ±10 V, ±5 V, ±2.5 V, external reference	–64	±4	64	
		Range = ±10 V, internal reference		±3		
	Gain error matching	Range = ±10 V with overrange		20		LSB
		Range = ±10 V		5	20	
		Range = ±5 V with overrange		12		
		Range = ±5 V		5		
		Range = ±2.5 V with overrange		12		
		Range = ±2.5 V		6		
	Gain error temperature drift	All ranges, external reference		1	10	ppm/°C
		All ranges, internal reference		8	20	
E_O	Offset error	Range = ±10 V with overrange	–4	±0.4	4	mV
		Range = ±10 V	–2.4	±0.3	2.4	
		Range = ±5 V with overrange	–1.8	±0.18	1.8	
		Range = ±5 V	–1.5	±0.15	1.5	
		Range = ±2.5 V with overrange	–1.4	±0.24	1.4	
		Range = ±2.5 V	–1.1	±0.2	1.1	
	Offset error matching	Range = ±10 V with overrange		±0.45		mV
		Range = ±10 V	–3	±0.4	3	
		Range = ±5 V with overrange		±0.3		
		Range = ±5 V		±0.25		
		Range = ±2.5 V with overrange		±0.3		
		Range = ±2.5 V		±0.25		
	Offset error temperature drift	All ranges		0.3	1.5	ppm/°C

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6.5 Electrical Characteristics (continued)

At AVDD = 5 V, DVDD= 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, internal or external V_{REF} = 2.5 V, LPF option = 1; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = +25°C, AVDD = 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
AC CHARACTERISTICS						
SNR	Signal-to-noise ratio, no oversampling (–0.5 dBFS input, 1 kHz)	Filter option 1, range = ±10 V with overrange	89	91.3		dB
		Filter option 1, range = ±10 V	89	91		
		Filter option 1, range = ±5 V with overrange		90.7		
		Filter option 1, range = ±5 V	88	90.5		
		Filter option 1, range = ±2.5 V with overrange		88.2		
		Filter option 1, range = ±2.5 V	85.5	88		
		Filter option 2, range = ±10 V with overrange		92.2		
		Filter option 2, range = ±10 V	90.5	91.9		
		Filter option 2, range = ±5 V with overrange		91.6		
		Filter option 2, range = ±5 V	89.5	91.4		
		Filter option 2, range = ±2.5 V with overrange		89.1		
		Filter option 2, range = ±2.5 V	87.4	88.9		
		Filter option 3, range = ±10 V with overrange		85		
		Filter option 3, range = ±10 V	82	85		
		Filter option 3, range = ±5 V with overrange		82		
		Filter option 3, range = ±5 V		82		
		Filter option 3, range = ±2.5 V with overrange		77		
		Filter option 3, range = ±2.5 V		77		
SNR_{OSR}	Signal-to-noise ratio (–0.5 dBFS input, 1 kHz)	Filter option 1, range = ±10 V, OSR = 2		92.5		dB
		Filter option 1, range = ±10 V, OSR = 4		93.5		

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6.5 Electrical Characteristics (continued)

At AVDD = 5 V, DVDD= 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, internal or external V_{REF} = 2.5 V, LPF option = 1; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = +25°C, AVDD = 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
SINAD	Signal-to-noise distortion ratio, no oversampling (–0.5 dBFS input, 1 kHz)	Filter option 1, range = ±10 V with overrange		90.8		dB
		Filter option 1, range = ±10 V	88.5	90.5		
		Filter option 1, range = ±5 V with overrange		90.2		
		Filter option 1, range = ±5 V	87.5	90		
		Filter option 1, range = ±2.5 V with overrange		87.7		
		Filter option 1, range = ±2.5 V	85.5	87.5		
		Filter option 2, range = ±10 V with overrange		91.3		
		Filter option 2, range = ±10 V	90	91		
		Filter option 2, range = ±5 V with overrange		90.7		
		Filter option 2, range = ±5 V	89	90.5		
		Filter option 2, range = ±2.5 V with overrange		88.2		
		Filter option 2, range = ±2.5 V	86.5	88		
		Filter option 3, range = ±10 V with overrange		85		
		Filter option 3, range = ±10 V	82	85		
		Filter option 3, range = ±5 V with overrange		82		
		Filter option 3, range = ±5 V	79	82		
		Filter option 3, range = ±2.5 V with overrange		78		
		Filter option 3, range = ±2.5 V	75	78		
THD	Total harmonic distortion (4)	Range = ±10 V with overrange		–110		dB
		Range = ±10 V		–110	–95	
		Range = ±5 V with overrange		–110		
		Range = ±5 V		–110		
		Range = ±2.5 V with overrange		–110		
		Range = ±2.5 V		–110		
SFDR	Spurious-free dynamic range (–0.5 dBFS input, 1 kHz)	All input ranges		–108		dB
	Isolation crosstalk (5)	f_{IN} on unselected channel up to 5 kHz		–112		dB
IMD	Intermodulation distortion	fa = 1 kHz, fb = 1.1 kHz, 2nd-order terms		–105		dB
		fa = 1 kHz, fb = 1.1 kHz, 3rd-order terms		–113		

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6.5 Electrical Characteristics (continued)

At AVDD = 5 V, DVDD= 3.3 V, f_{SAMPLE} = 1 MSPS, f_{IN} = 1 kHz, internal or external V_{REF} = 2.5 V, LPF option = 1; minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = +25°C, AVDD = 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN(1)	TYP	MAX(1)	UNIT
INTERNAL REFERENCE OUTPUT						
V_{REF} (6)	Voltage on REFIO pin (configured as output)	0.1-µF capacitor on REFIO pin, T_A = 25°C	2.4975	2.5	2.5025	V
	Reference temperature drift			7	20	ppm/°C
$V_{(REFCAP)}$	Reference buffer output voltage (REFCAP pin)	T_A = 25°C	3.996	4	4.004	V
t_{ON}	Reference turn-on time	10-µF capacitor on REFCAP pin		15		ms
EXTERNAL REFERENCE INPUT						
REF_{LKG}	Reference input leakage current		–1		1	µA
POWER-SUPPLY REQUIREMENTS						
I_{AVDD}	AVDD current with internal reference	Static		55	69	mA
		Dynamic, f_{SAMPLE} = 1 MSPS		59	72	mA
		Power-down		130		µA
	AVDD current with external reference	Static		54	68	mA
		Dynamic, f_{SAMPLE} = 1 MSPS		59	72	mA
		Power-down		130		µA
I_{DVDD}	DVDD current	Static		0.06	0.1	mA
		Dynamic, f_{SAMPLE} = 1 MSPS		0.6	1	mA
		Power-down		1		µA
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 x DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 x DVDD	V
I_{LKG}	Input leakage current			100		nA
	Input capacitance			5		pF
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_O = 500-µA source	0.8 x DVDD		DVDD	V
V_{OL}	Low-level output voltage	I_O = 500-µA sink	0		0.2 x DVDD	V
	Floating state leakage current			1	20	µA
	Floating state output capacitance			5		pF

(1) Preliminary Specifications, subject to change based on characterization
(2) This parameter is the endpoint INL, not best-fit INL.
(3) Gain error calculated after adjusting for offset error, which implies that positive full-scale error = negative full-scale error = gain error ÷ 2.
(4) Calculated on the first nine harmonics of the input frequency.
(5) Isolation crosstalk is measured by applying a full-scale sinusoidal signal up to 160 kHz to a channel, not selected in the multiplexing sequence, and measuring the effect on the output of any selected channel.
(6) Does not include the variation in voltage resulting from solder shift effects.

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6.6 Timing Requirements

At AVDD = 5 V, DVDD = 1.71 V to 5.25 V, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values are at T_A = –40°C to +125°C; typical values are at T_A = 25°C.

		MIN	NOM	MAX	UNIT
DEVICE CONFIGURATION					
$t_{D_\overline{CS}CNV}$	Delay time: $\overline{CS}$ rising edge to CONVST rising edge	50			ns
t_{SU_CHXCNV}	Setup time: CHSELx to CONVST rising edge	50			ns
t_{HT_BSYCHX}	Hold time: BUSY falling edge to CHSELx change	20			ns
t_{PWRUP}	Power supplies settled to $\overline{RESET}$ rising edge	1			ms
t_{DEV_WRITE}	Partial reset: $\overline{RESET}$ rising edge to first falling edge of $\overline{CS}$	50			ns
	Full reset: $\overline{RESET}$ rising edge to first falling edge of $\overline{CS}$	240			µs
$t_{SU_\overline{RST}}$	Partial reset: setup time HW mode configuration inputs to $\overline{RESET}$ rising edge	10			ns
	Full reset: setup time HW mode configuration inputs to $\overline{RESET}$ rising edge	50			µs
$t_{HT_\overline{RST}}$	Partial reset: hold time $\overline{RESET}$ rising edge to HW mode configuration inputs	10			ns
	Full reset: Hold time $\overline{RESET}$ rising edge to HW mode configuration inputs	240			µs
CONVST CONTROL					
t_{ACQ}	Acquisition time: BUSY falling edge to rising edge of trailing CONVST	480			ns
t_{PH_CNV}	CONVST pulse high time	50			ns
t_{PL_CNV}	CONVST pulse low time	50			ns
t_{DEV_STRTUP}	Partial reset setup time: $\overline{RESET}$ rising edge to first rising edge of CONVST	50			ns
	Full reset setup time: $\overline{RESET}$ rising edge to first rising edge of CONVST	15			ms
$t_{PL_\overline{RST}}$	Partial reset	40		500	ns
	Full reset	1.2			µs
DATA READ					
$t_{SU_BSY\ \overline{CS}}$	Setup time: BUSY falling edge to $\overline{CS}$ falling edge, start of data read operation after conversion	20			ns
$t_{DZ_\overline{CS}CNV}$	Delay between $\overline{CS}$ rising edge to CONVST rising edge, end of data read operation after conversion	50			ns
PARALLEL AND BYTE DATA READ					
$t_{SU_\overline{CS}\overline{RD}}$	Setup time: $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	10			ns
$t_{HT_\overline{RD}\overline{CS}}$	Hold time: $\overline{RD}$ rising edge to $\overline{CS}$ rising edge	10			ns
$t_{PH_\overline{RD}}$	$\overline{RD}$ high time	10			ns
$t_{PL_\overline{RD}}$	$\overline{RD}$ low time	30			ns

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6.6 Timing Requirements (continued)

At AVDD = 5 V, DVDD = 1.71 V to 5.25 V, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values are at T_A = –40°C to +125°C; typical values are at T_A = 25°C.

		MIN	NOM	MAX	UNIT
SERIAL DATA READ					
t_{SCLK}	SCLK time period, 1.71 V ≤ DVDD ≤ 2.3 V	50			ns
	SCLK time period, 2.3 V < DVDD ≤ 3 V	25			ns
	SCLK time period, DVDD > 3 V	20			ns
t_{PH_SCLK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{PL_SCLK}	SCLK low time	0.45		0.55	t_{SCLK}
$t_{SU_\overline{CS}CK}$	Setup time: $\overline{CS}$ falling edge to SCLK falling edge DVDD > 3V	10.5			ns
	Setup time: $\overline{CS}$ falling edge to SCLK falling edge 2.3 V < DVDD ≤ 3 V	13.5			ns
	Setup time: $\overline{CS}$ falling edge to SCLK falling edge 1.71 V ≤ DVDD ≤ 2.3 V	20			ns
$t_{HT_CK\,\overline{CS}}$	Hold time: SCLK to $\overline{CS}$ rising time	10			ns
PARALLEL AND BYTE DATA WRITE					
$t_{SU_\overline{CS}\overline{WR}}$	Setup time: $\overline{CS}$ falling edge to $\overline{WR}$ falling edge	10			ns
$t_{HT_\overline{WR}\overline{CS}}$	Hold time: $\overline{WR}$ rising edge to $\overline{CS}$ rising edge	10			ns
$t_{PH_\overline{WR}}$	$\overline{WR}$ high time	20			ns
$t_{PL_\overline{WR}}$	$\overline{WR}$ low time	30			ns
$t_{SU_DIN\,\overline{WR}}$	Setup time: DIN change to $\overline{WR}$ rising edge	30			ns
$t_{HT_\overline{WR}DIN}$	Hold time: $\overline{WR}$ rising edge to DIN change	10			ns
t_{DZ_CONFIG}	Device configuration time: $\overline{WR}$ rising edge to CONVST rising edge	20			ns
SERIAL DATA WRITE					
t_{SU_DINCK}	Setup time: DIN to SCLK falling edge	10			ns
t_{HT_CKDIN}	Hold time: SCLK falling edge to DIN change	8			ns

6.7 Switching Characteristics

At AVDD = 5 V, DVDD = 1.71 V to 5.25 V, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values are at T_A = –40°C to +125°C; typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONVST CONTROL						
t_{CYC}	ADC cycle time	No oversampling, parallel or byte or serial 2-wire mode readback	1			µs
t_{CONV}	Conversion time: CONVST rising edge to BUSY falling edge time, input channels	No oversampling		475	520	ns
		Oversampling by 2		1.4		µs
		Oversampling by 4		3.2		µs
		Oversampling by 8		6.7		µs
		Oversampling by 16		13.7		µs
		Oversampling by 32		27.9		µs
		Oversampling by 64		55.9		µs
		Oversampling by 128		112		µs

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6.7 Switching Characteristics (continued)

At AVDD = 5 V, DVDD = 1.71 V to 5.25 V, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 1 MSPS (unless otherwise noted); minimum and maximum values are at T_A = –40°C to +125°C; typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CONV_DIAG}	Conversion time: CONVST rising edge to BUSY falling edge time, diagnostic channels	No oversampling		525	570	ns
		Oversampling by 2		1.4		µs
		Oversampling by 4		3.2		µs
		Oversampling by 8		6.7		µs
		Oversampling by 16		13.7		µs
		Oversampling by 32		27.9		µs
		Oversampling by 64		55.9		µs
		Oversampling by 128		112		µs
t_{D_CNVBSY}	Delay between CONVST rising edge to BUSY rising edge	Manual mode			32	ns
PARALLEL AND BYTE DATA READ						
$t_{D_\overline{RD}DB}$	Delay time: $\overline{RD}$ falling edge to new data on DB[15:0]				30	ns
$t_{DHZ_\overline{CS}DB}$	Delay time: $\overline{CS}$ rising edge to DB[15:0] becoming tri-state	1.71 V ≤ DVDD ≤ 2.3 V			20	ns
	Delay time: $\overline{CS}$ rising edge to DB[15:0] becoming tri-state	DVDD > 2.3 V			12	ns
SERIAL DATA READ						
$t_{D_\overline{CS}DO}$	Delay time: $\overline{CS}$ falling edge to SDOA and SDOB becoming valid (out of tri-state)	1.71 V ≤ DVDD ≤ 2.3 V			16	ns
	Delay time: $\overline{CS}$ falling edge to SDOA and SDOB becoming valid (out of tri-state)	DVDD > 2.3 V			9	ns
t_{H_CKDO}	Hold time: SCLK rising edge to data hold on SDOA and SDOB	1.71 V ≤ DVDD ≤ 2.3 V	3			ns
	Hold time: SCLK rising edge to data hold on SDOA and SDOB	2.3 V ≤ DVDD ≤ 3 V	3			ns
	Hold time: SCLK rising edge to data hold on SDOA and SDOB	DVDD > 3 V	2.8			ns
t_{D_CKDO}	Delay time: SCLK rising edge to valid data on SDOA and SDOB	1.71 V ≤ DVDD ≤ 2.3 V			20	ns
	Delay time: SCLK rising edge to valid data on SDOA and SDOB	2.3 V < DVDD ≤ 3 V			12	ns
	Delay time: SCLK rising edge to valid data on SDOA and SDOB	DVDD > 3 V			10	ns
$t_{DHZ_\overline{CS}DO}$	Delay time: $\overline{CS}$ rising edge to SDOA and SDOB becoming tri-state	1.71 V ≤ DVDD ≤ 2.3 V			20	ns
	Delay time: CS rising edge to SDOA and SDOB becoming tri-state	DVDD > 2.3 V			10	ns

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6.8 Timing Diagrams: Universal

All figures in this section are at AVDD = 4.75 V to 5.25 V, DVDD = 1.71 V to AVDD, V_{REFIO} = 2.5 V external reference and internal reference, and T_A = −40°C to +125°C (unless otherwise noted); the interface timing tested used a load capacitance of 30 pF, dependent on DVDD and load capacitance for the serial interface (see Table 7-10).

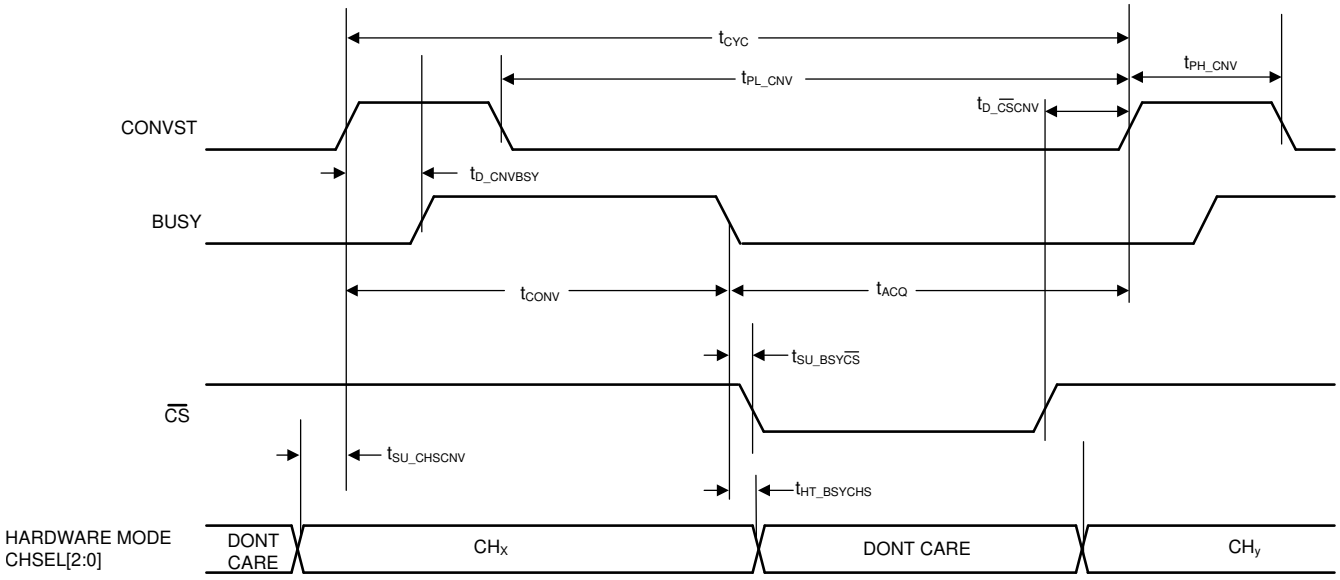

Figure 6-1. Universal Timing Diagram Across All Interfaces

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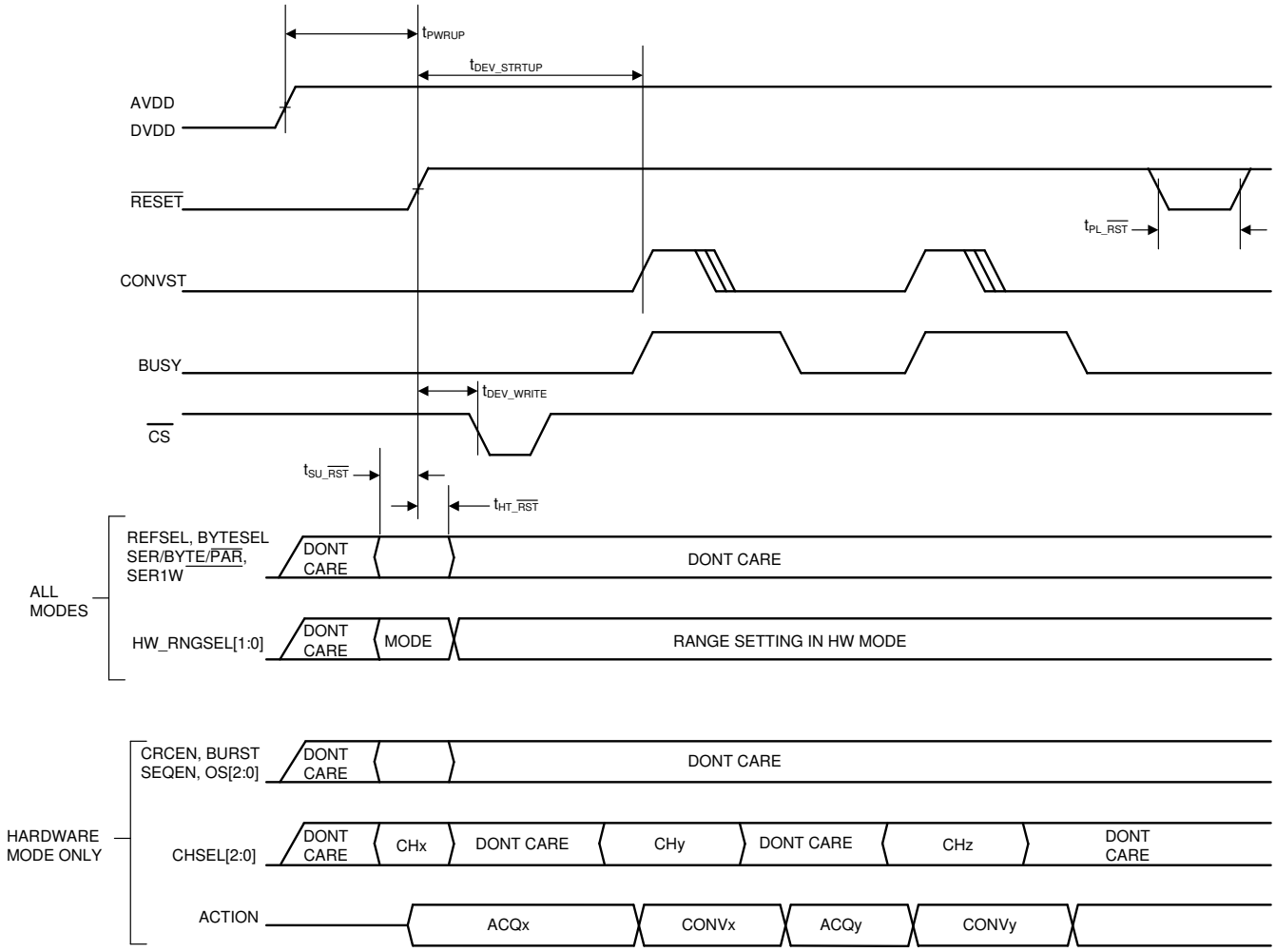

Figure 6-2. Reset Timing

6.9 Timing Diagrams: Parallel Data Read

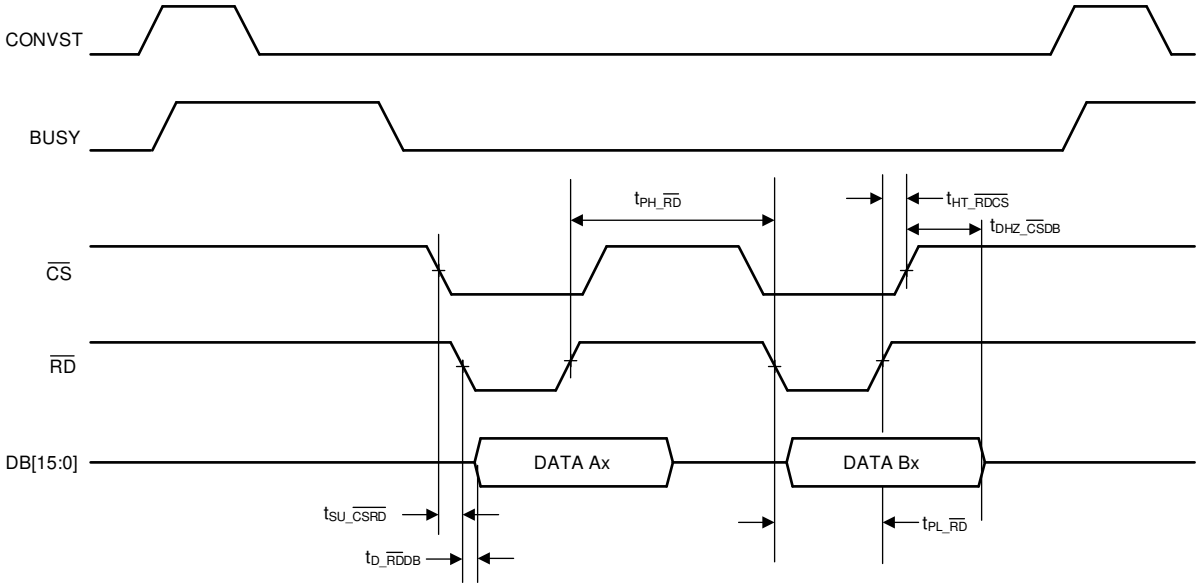

Figure 6-3. Parallel Read Timing Diagram

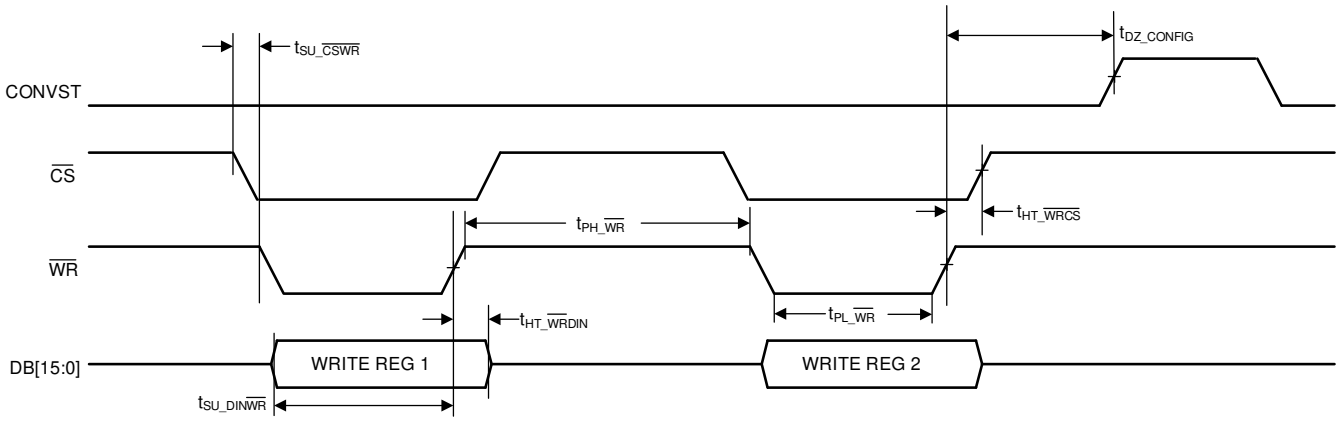

Figure 6-4. Parallel Write Timing Diagram

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6.10 Timing Diagrams: Serial Data Read

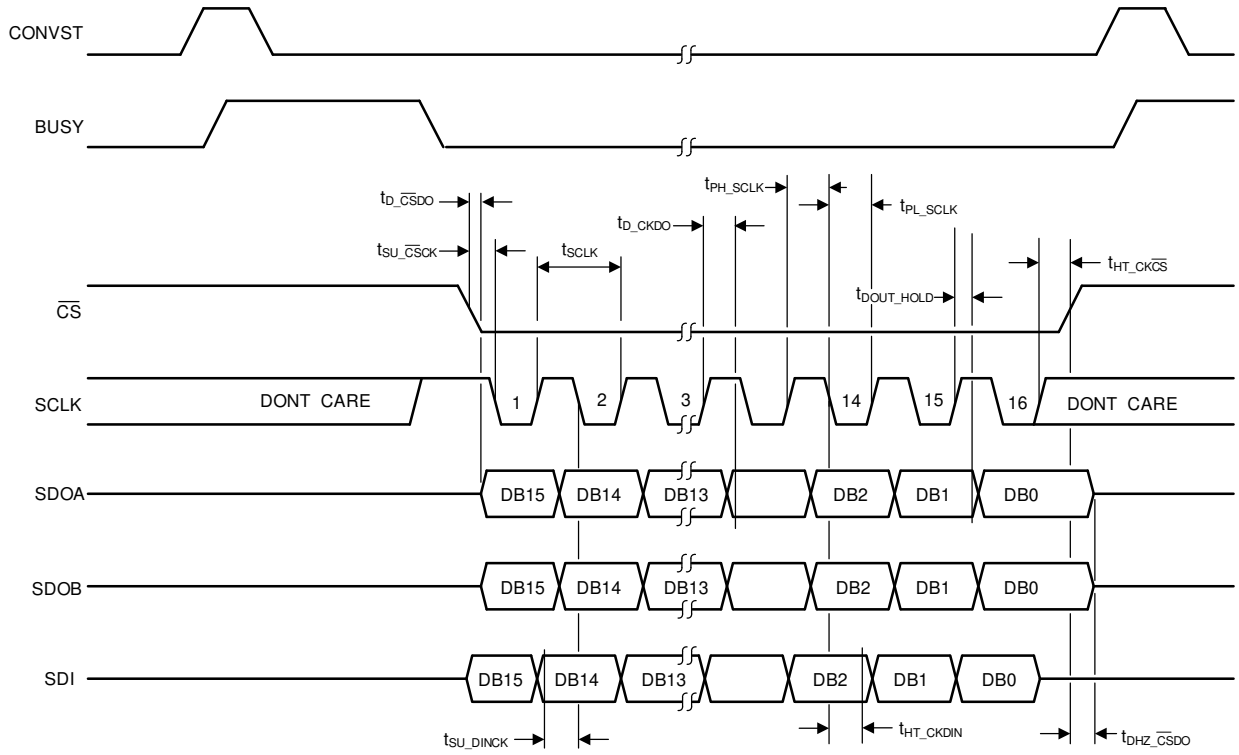
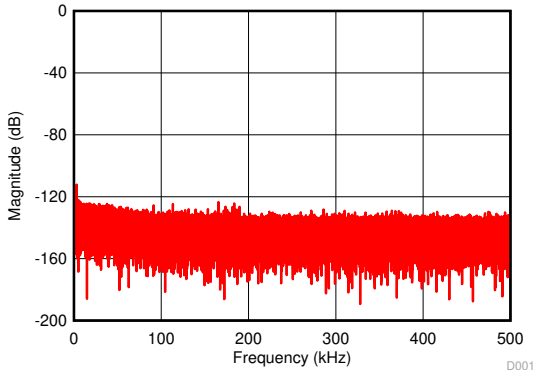


Figure 6-5. Serial Timing Diagram

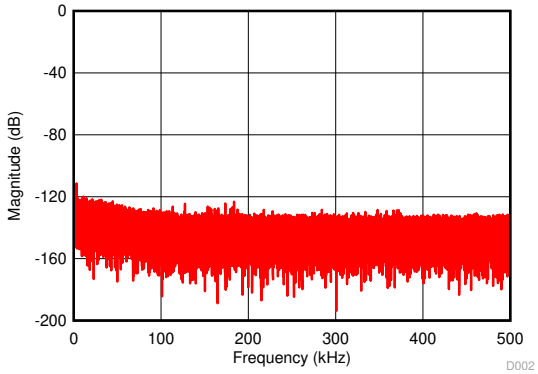
6.11 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)



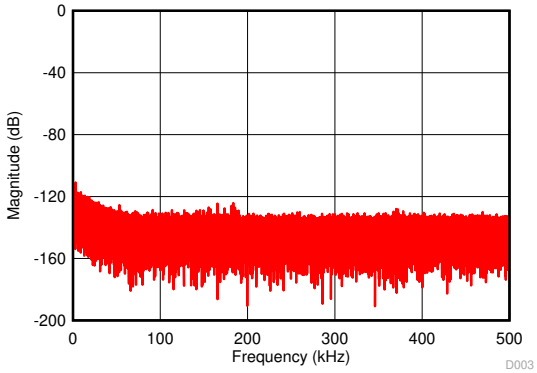
Number of points = 256k, SNR = 90.73 dB,
SINAD = 90.65 dB, THD = –110 dB, SFDR = 112.2 dB

Figure 6-6. Typical FFT Plot (±10 V, Normal Mode, Filter Option 1)



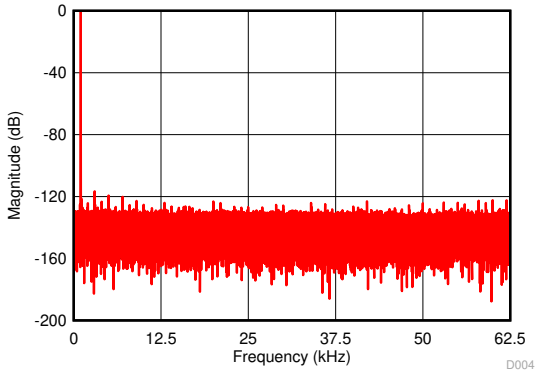
Number of points = 256k, SNR = 89.56 dB,
SINAD = 89.47 dB, THD = –110.83 dB, SFDR = 110.69 dB

Figure 6-7. Typical FFT Plot (±5 V, Normal Mode, Filter Option 1)



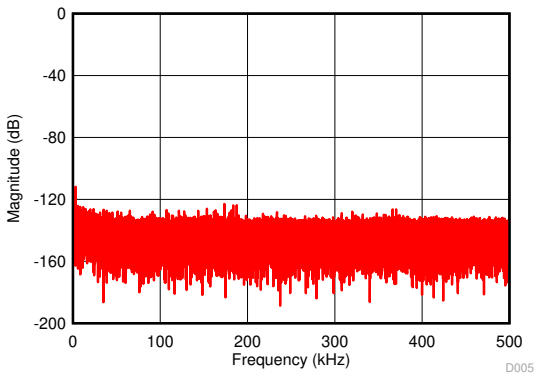
Number of points = 256k, SNR = 89.03 dB,
SINAD = 88.89 dB, THD = –107.25 dB, SFDR = 110.46 dB

Figure 6-8. Typical FFT Plot (±2.5 V, Normal Mode, Filter Option 1)



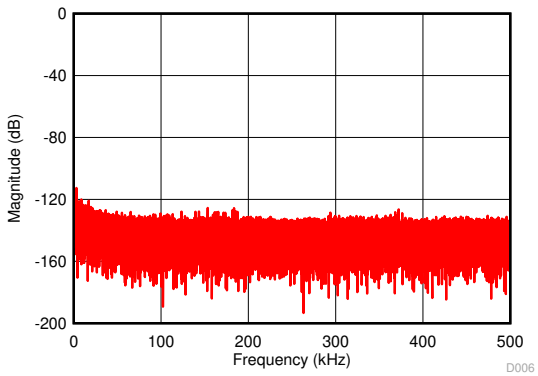
Number of points = 256k, SNR = 90.27 dB,
SINAD = 90.24 dB, THD = –111.9 dB, SFDR = 116.04 dB

Figure 6-9. Typical FFT Plot (±10 V, Burst Mode, Filter Option 1)



Number of points = 256k, SNR = 91.93 dB,
SINAD = 91.82 dB, THD = –110.04 dB, SFDR = 111.95 dB

Figure 6-10. Typical FFT Plot (±10 V, Normal Mode, Filter Option 2)



Number of points = 256k, SNR = 90.99 dB,
SINAD = 90.87 dB, THD = –111.91 dB, SFDR = 111.1 dB

Figure 6-11. Typical FFT Plot (±5 V, Normal Mode, Filter Option 2)

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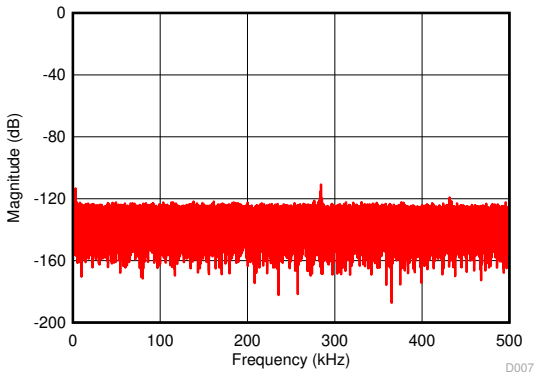
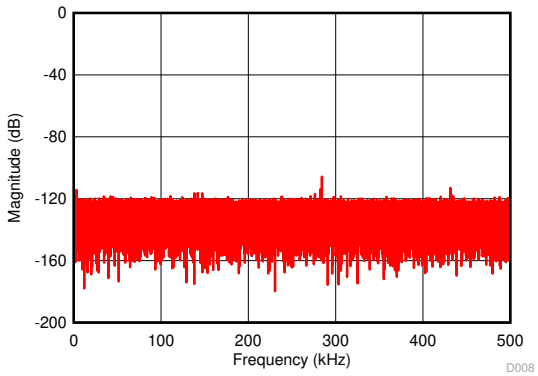
6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)



Number of points = 256k, SNR = 84.29 dB,
SINAD = 84.27 dB, THD = –110 dB, SFDR = 113.6 dB

Figure 6-12. Typical FFT Plot (±10 V, Normal Mode, Filter Option 3)



Number of points = 256k, SNR = 81.10 dB,
SINAD = 81.01 dB, THD = –110.8 dB, SFDR = 113.56 dB

Figure 6-13. Typical FFT Plot (±5 V, Normal Mode, Filter Option 3)

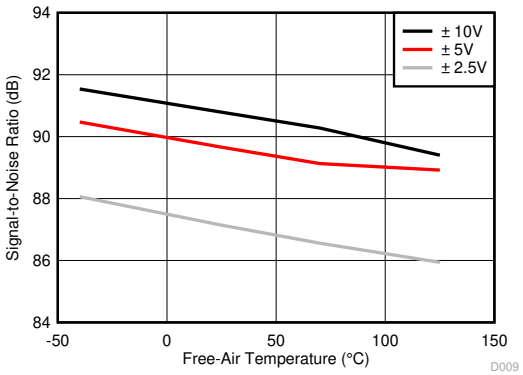


Figure 6-14. SNR vs Free-Air Temperature (Filter Option 1)

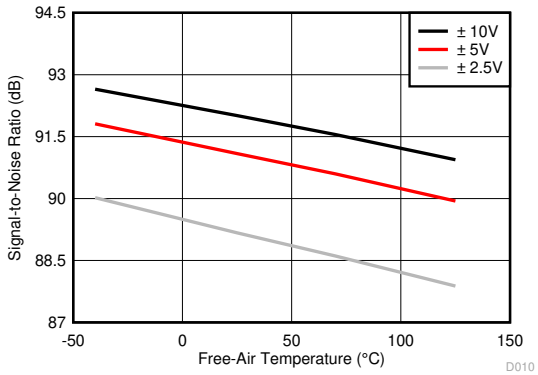


Figure 6-15. SNR vs Free-Air Temperature (Filter Option 2)

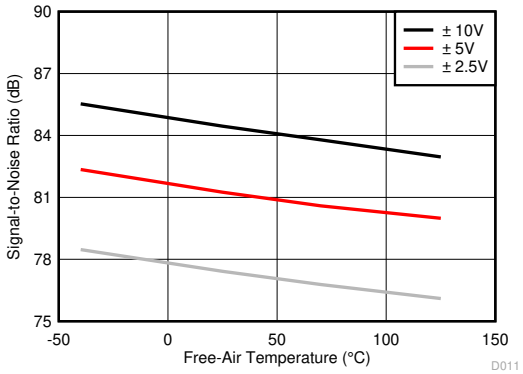


Figure 6-16. SNR vs Free-Air Temperature (Filter Option 3)

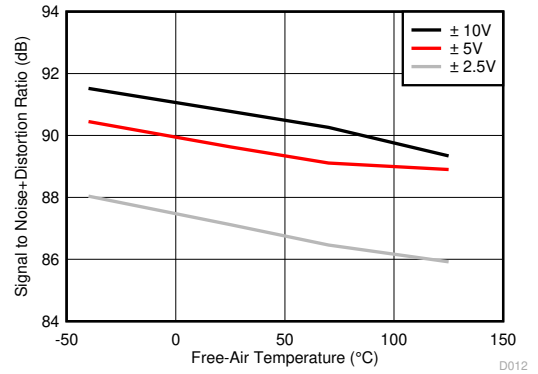


Figure 6-17. SINAD vs Free-Air Temperature (Filter Option 1)

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6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)

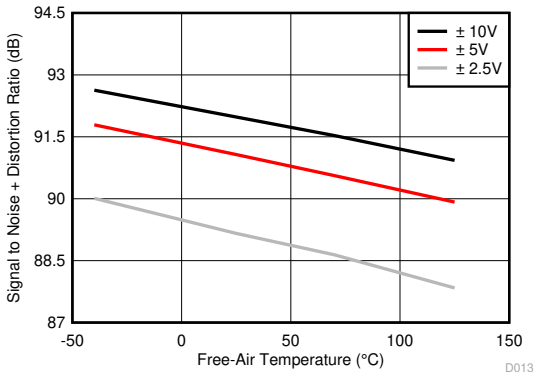

Figure 6-18. SINAD vs Free-Air Temperature (Filter Option 2)

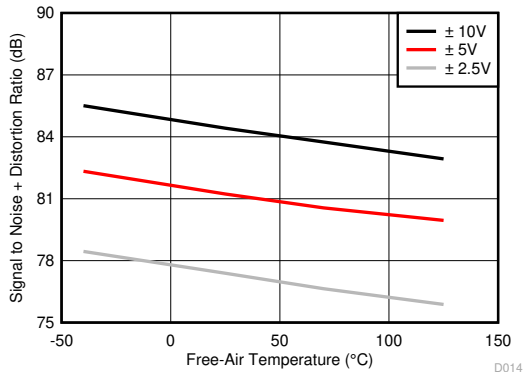

Figure 6-19. SINAD vs Free-Air Temperature (Filter Option 3)

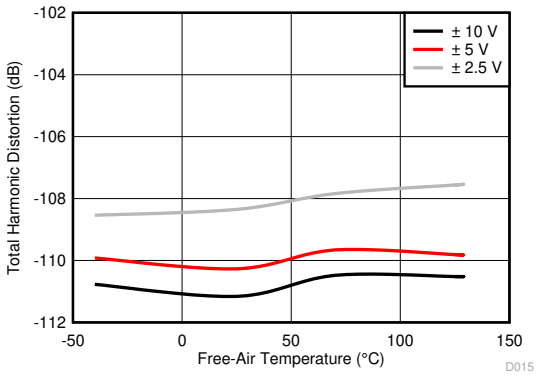

Figure 6-20. THD vs Free-Air Temperature (Filter Option 1)

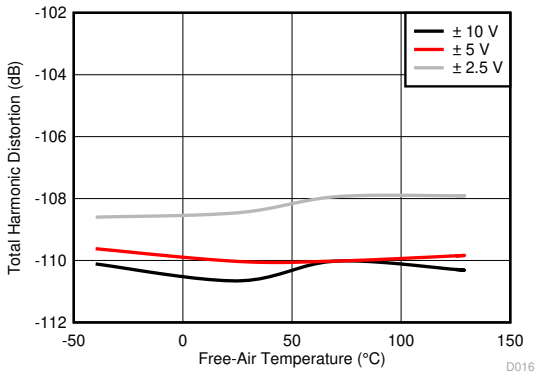

Figure 6-21. THD vs Free-Air Temperature (Filter Option 2)

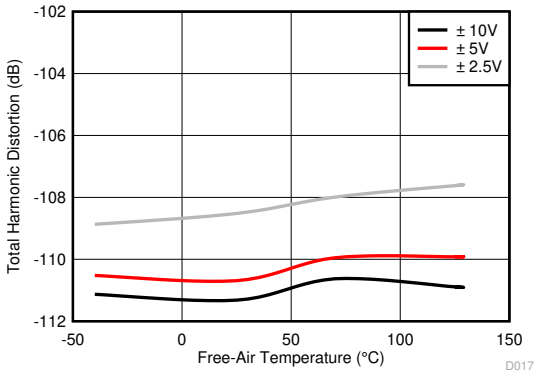

Figure 6-22. THD vs Free-Air Temperature (Filter Option 3)

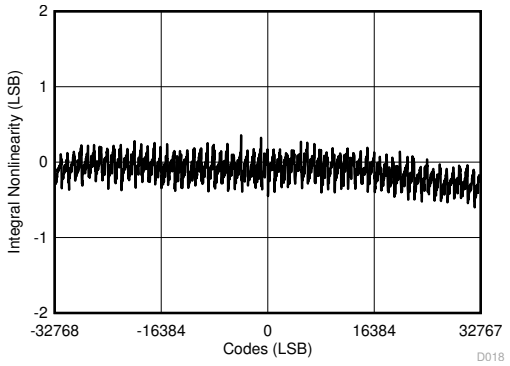

Figure 6-23. Typical INL for All Codes (±10 V)

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6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)

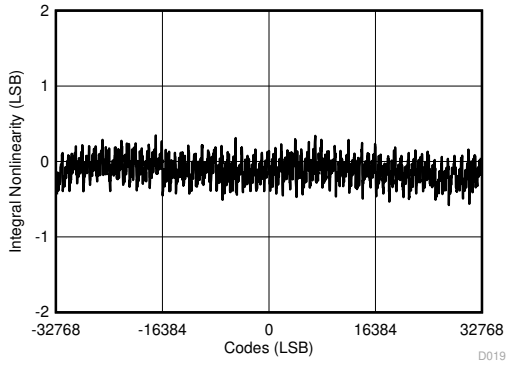


Figure 6-24. Typical INL for All Codes (±5 V)

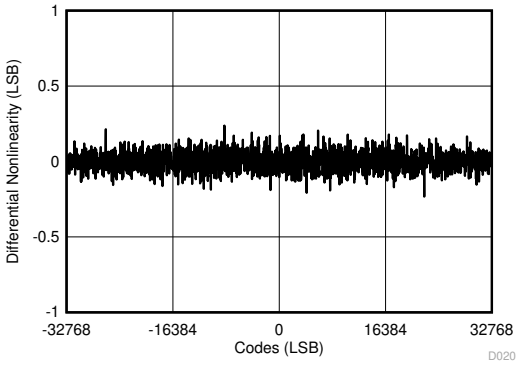


Figure 6-25. Typical DNL for All Codes (±10 V)

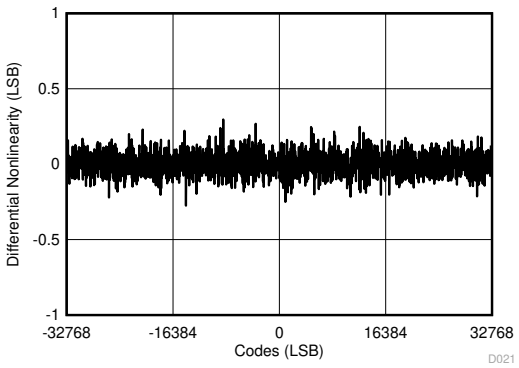
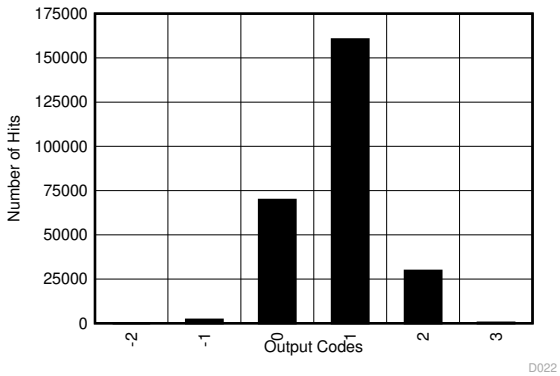
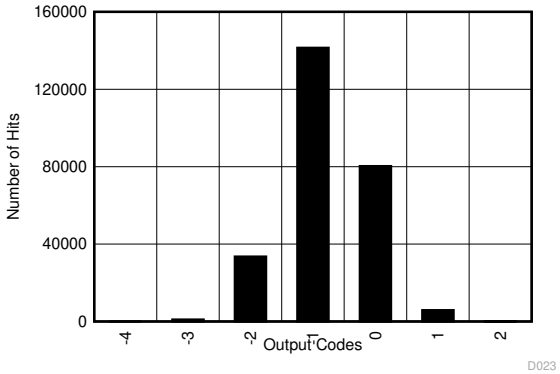


Figure 6-26. Typical DNL for All Codes (±5 V)



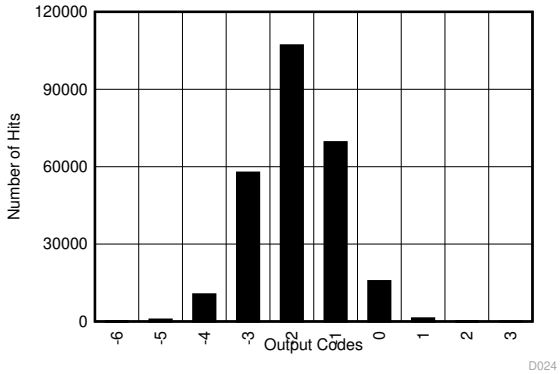
Mean = 0.83, sigma = 0.62, number of hits = 256k, V_{IN} = 0 V

Figure 6-27. Typical Offset Error Histogram (±10 V)



Mean = –0.78, sigma = 0.7, number of hits = 256k, V_{IN} = 0 V

Figure 6-28. Typical Offset Error Histogram (±5 V)



Mean = -1.91, sigma = 0.97, number of hits = 256k, V_{IN} = 0 V

Figure 6-29. Typical Offset Error Histogram (±2.5 V)

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6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)

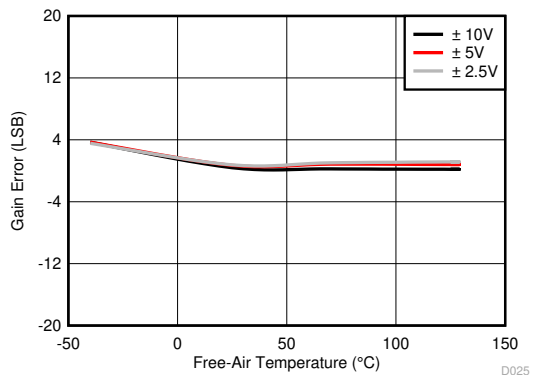

Figure 6-30. Gain Error vs Free-Air Temperature

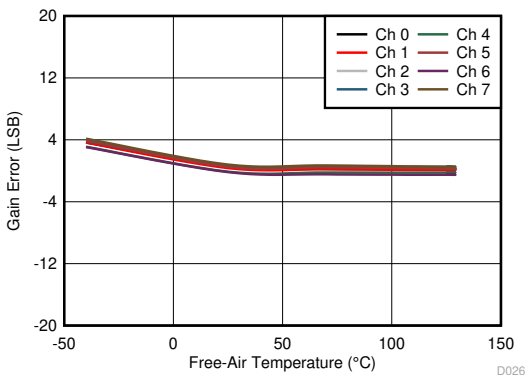

Figure 6-31. Gain Error vs Free-Air Temperature (±10 V, Across Channels)

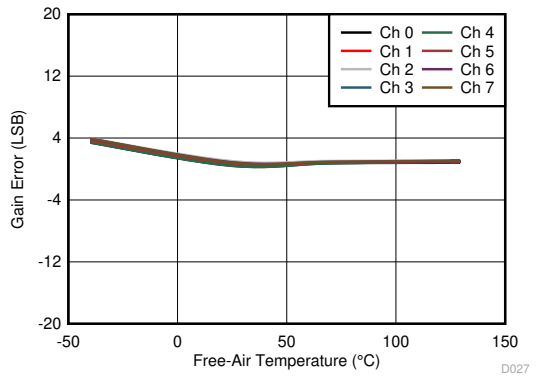

Figure 6-32. Gain Error vs Free-Air Temperature (±5 V, Across Channels)

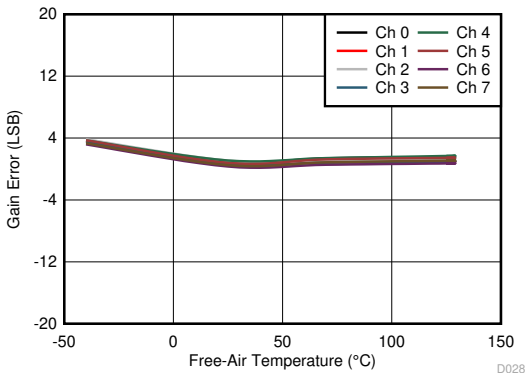

Figure 6-33. Gain Error vs Free-Air Temperature (±2.5 V, Across Channels)

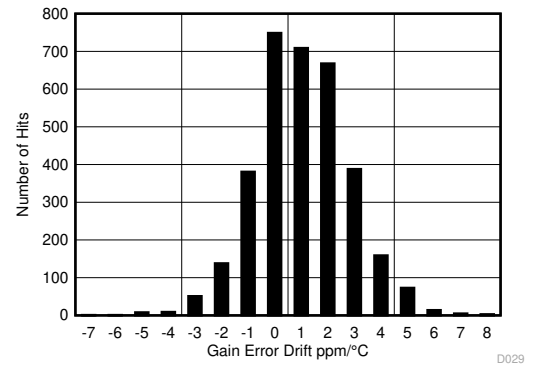

Figure 6-34. Gain Error Drift Histogram

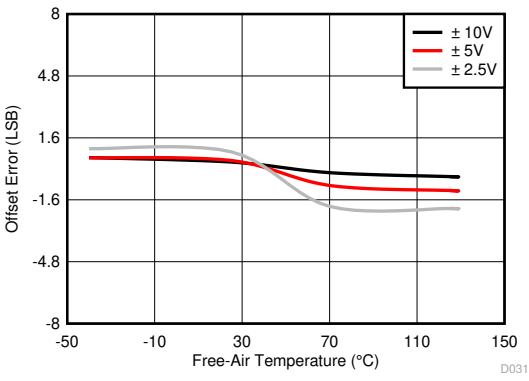

Figure 6-35. Offset Error vs Free-Air Temperature

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6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)

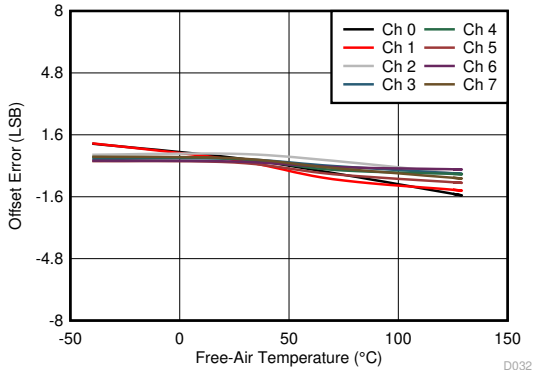

Figure 6-36. Offset Error vs Free-Air Temperature (±10 V, Across Channels)

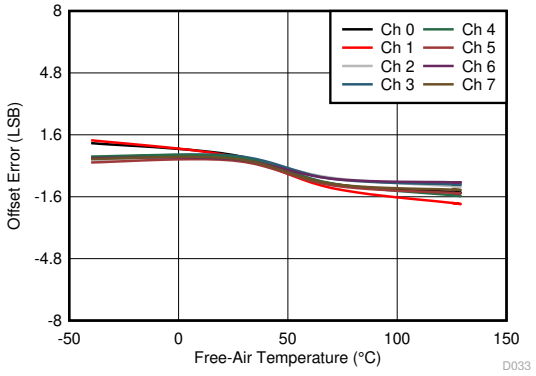

Figure 6-37. Offset Error vs Free-Air Temperature (±5 V, Across Channels)

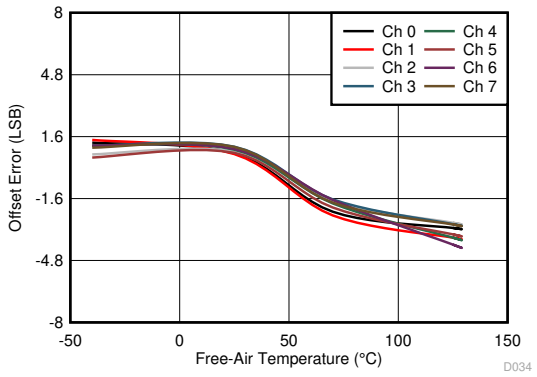

Figure 6-38. Offset Error vs Free-Air Temperature (±2.5 V, Across Channels)

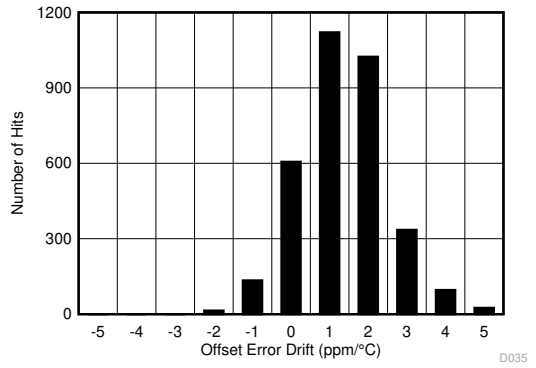

Figure 6-39. Offset Error Drift Histogram

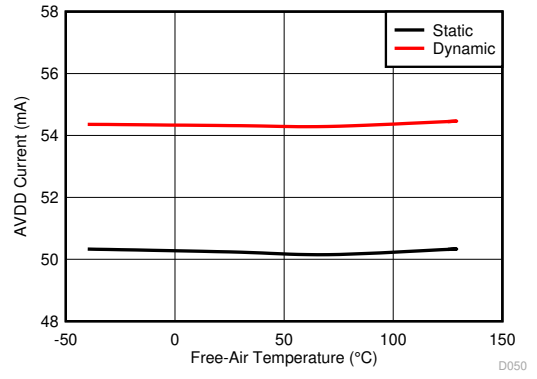

Figure 6-40. AVDD Current vs Free-Air Temperature

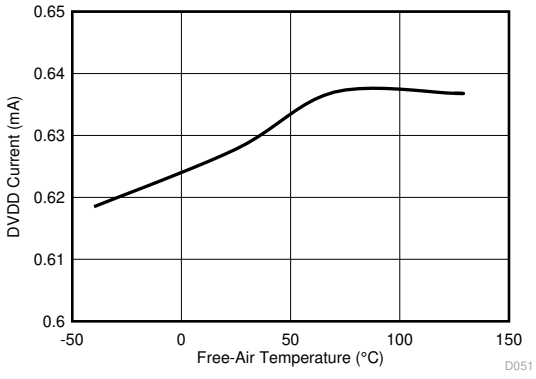

Figure 6-41. DVDD Current vs Free-Air Temperature

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6.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 1 MSPS (unless otherwise noted)

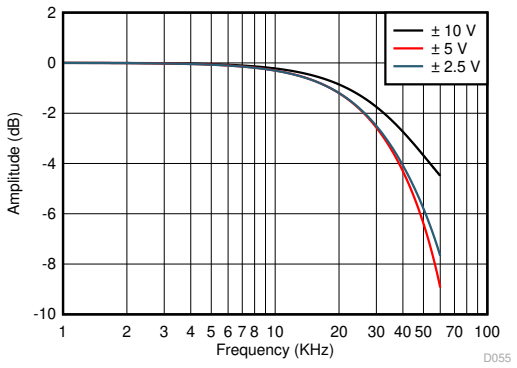

Figure 6-42. Frequency Response Across Ranges (Filter Option 1)

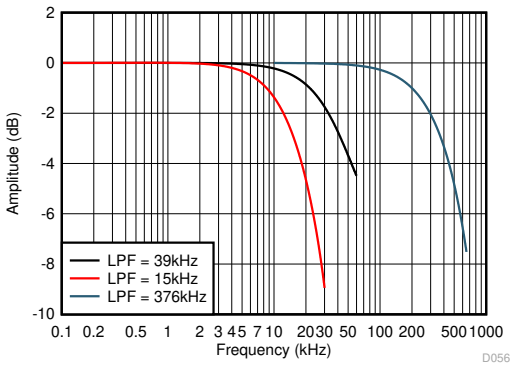

Figure 6-43. Frequency Response Across LPF Settings (±10 V)

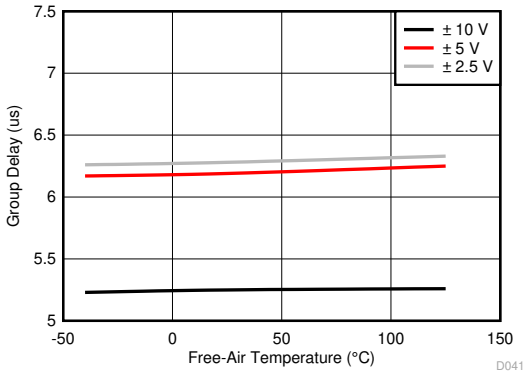

Figure 6-44. Group Delay vs Free-Air Temperature (Filter Option 1)

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7 Detailed Description

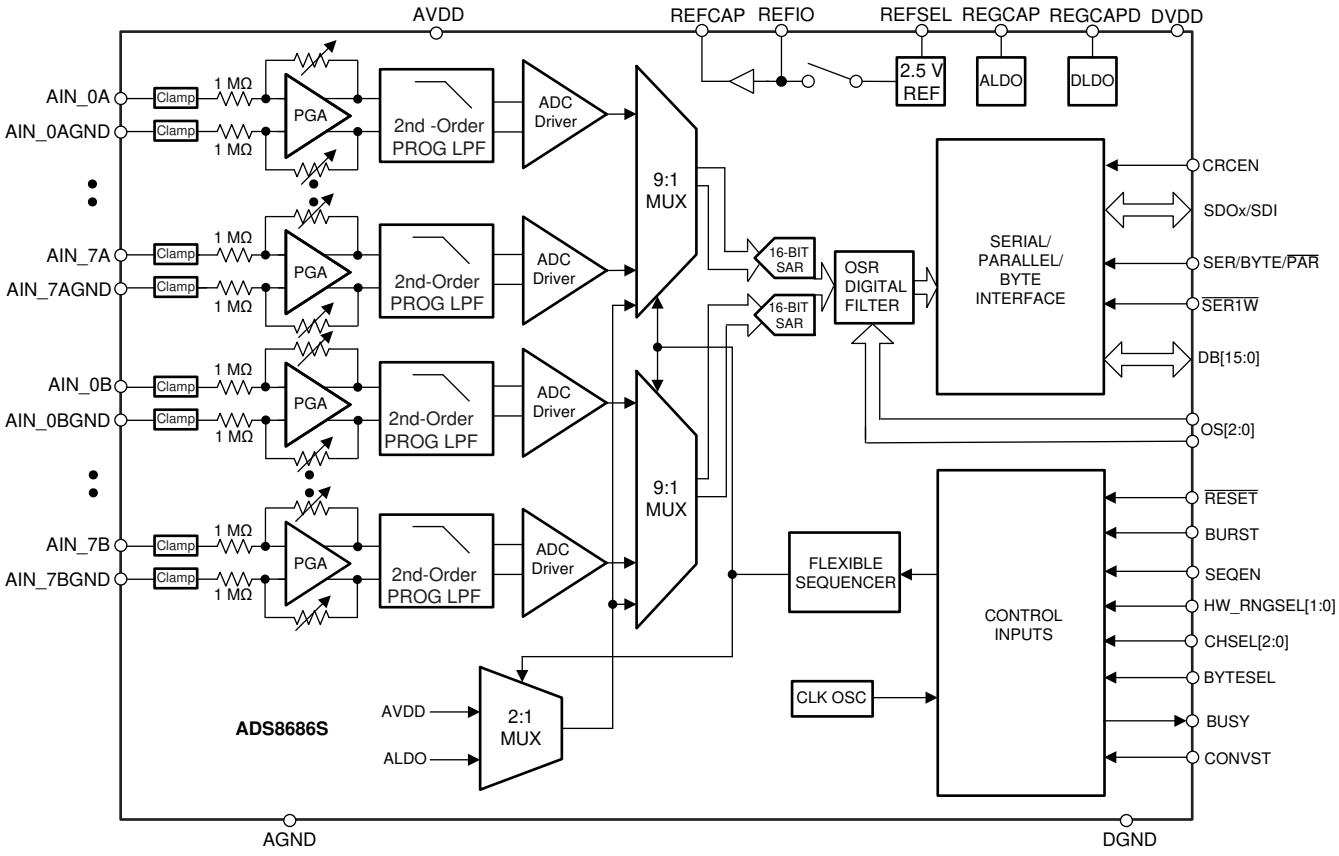
7.1 Overview

The ADS8686S is a 16-bit data acquisition system (DAQ) with 16-channel analog inputs. Each analog input channel consists of an input clamp protection circuit, a programmable gain amplifier (PGA), a second-order programmable low-pass filter followed by an analog-to-digital (ADC) driver. The ADC driver outputs are connected through a dual 8:1 multiplexer (MUX) to a dual simultaneous sampling 16-bit ADC. The overall system can achieve a maximum throughput of 1 MSPS per ADC. The device features a 2.5-V internal reference with a fast-settling buffer, a programmable digital averaging filter to improve noise performance, a flexible channel sequencer, and high-speed parallel, byte, and serial interfaces for communication with a wide variety of digital hosts.

The device operates from a single 5-V analog supply and can accommodate true bipolar input signals . The programmable analog signal range includes ±10-V, ±5-V, and ±2.5-V options with 20% overrange. The input clamp protection circuitry can tolerate voltages up to ±15 V. The device offers a constant 1-MΩ resistive input impedance irrespective of the sampling frequency or the selected input range.

The device can be operated in hardware or software mode by controlling the HW_RNGSELx pins. In hardware mode, the device is configured by pin control. In software mode, the device is configured by the control registers accessed through the parallel, byte, or serial interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

The ADS8686S incorporates dual, simultaneous sampling, 16-bit successive approximation register (SAR) analog-to-digital converters (ADCs). Each ADC is connected to eight analog input channels through a multiplexer. The device has a total of 16 analog inputs. Each analog input channel has two input pins, AIN_0A, AIN_0B and AIN_0AGND, AIN_0BGND to AIN_7A, AIN_7B and AIN_7AGND, AIN_7BGND. The positive inputs (AIN_nA, AIN_nB) are the single-ended analog inputs and the negative inputs (AIN_nAGND, AIN_nBGND) are tied to AGND. Figure 7-1 shows the simplified circuit schematic for each analog input channel, including the input clamp protection circuit, PGA, low-pass filter, high-speed ADC driver, multiplexer, and a precision 16-bit SAR ADC.

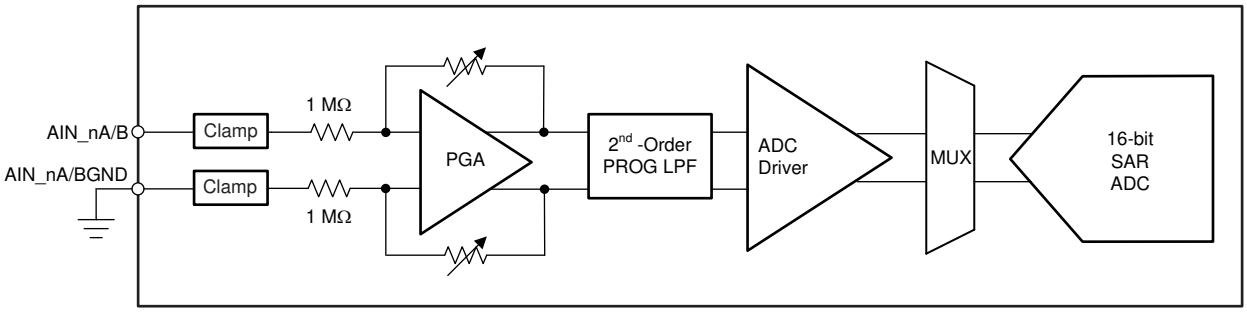


Figure 7-1. Front-End Circuit Schematic for the Selected Analog Input Channel

The device samples the voltage difference (AIN_nA, AIN_nB – AIN_nAGND, AIN_nBGND) between the selected analog input channel pins. The device allows a ±0.3-V range on the AIN_nAGND, AIN_nBGND pin for all analog input channels. Use this feature in modular systems where the sensor or signal conditioning block is further away from the ADC on the board and when a difference in the ground potential of the sensor or signal conditioner from the ADC ground is possible. In such cases, running separate wires from the AIN_nAGND, AIN_nBGND pin of the device to the sensor or signal conditioning ground is recommended

The ADS8686S also has on-chip diagnostic channels to monitor the AVDD supply and an on-chip, low-dropout regulator (LDO). Channels can be selected for conversion by controlling the CHSELx pins in hardware mode or through the channel register control in software mode. The device supports dynamic channel selection or the on-chip sequencer can be enabled to scan the channels in a preprogrammed manner. In hardware mode, simultaneous sampling is restricted to the corresponding A and B channel (that is, channel AIN_0A is always sampled with channel AIN_0B). The diagnostic channels cannot be sampled in the hardware mode of operation. Software mode is required to sample the diagnostic channels. In software mode, any AIN_nA channel can be selected with any AIN_nB channel for simultaneous sampling.

7.3.2 Analog Input Impedance

Each analog input channel in the device presents a constant resistive impedance of 1 MΩ. The input impedance for each channel is independent of the configured range of the ADC, or the oversampling mode. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance. Bipolar, high-voltage power supplies are not required in the system because this ADC does not require any high-voltage, front-end drivers. In most applications, the signal sources or sensor outputs can be directly connected to the ADC input, thus significantly simplifying the design of the signal chain.

In order to maintain the dc accuracy of the system, matching the external source impedance on the AIN_nA, AIN_nB input pin with an equivalent resistance on the AIN_nAGND, AIN_nBGND pin is recommended (see Figure 7-4). This matching helps cancel any additional offset error contributed by the external resistance.

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7.3.3 Input Clamp Protection Circuit

Figure 7-2 shows the analog input circuitry of the ADS8686S. The device features an internal clamp protection circuit on each of the 16 analog input channels.

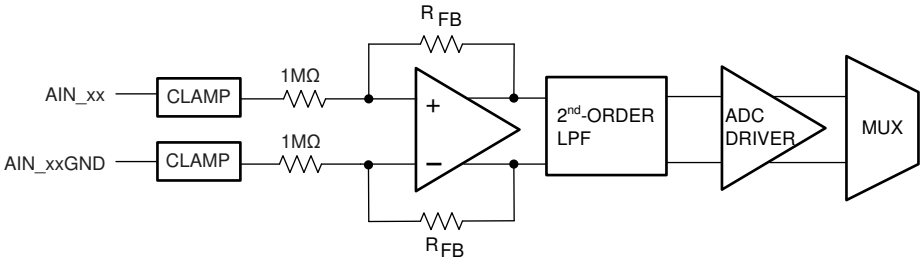

Figure 7-2. Analog Input Circuitry

The input clamp protection circuit on the ADS8686S allows each analog input to swing up to a maximum voltage of ±15 V. Beyond an input voltage of ±15 V, the input clamp circuit turns on and still operates from the single 5-V supply. Figure 7-3 shows a typical current versus voltage characteristic curve for the input clamp. There is no current flow in the clamp circuit for input voltages up to ±15 V. Beyond this voltage, the input clamp circuit turns on.

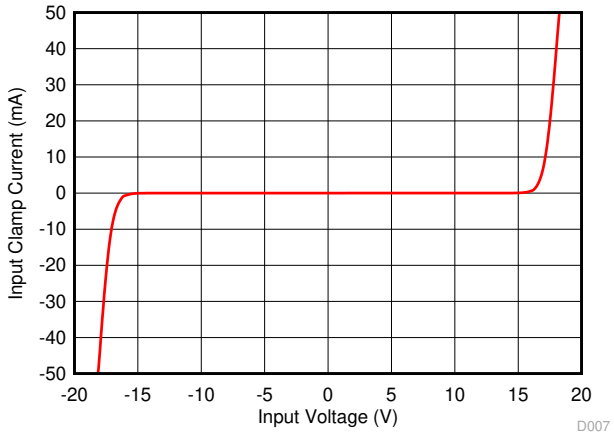

Figure 7-3. Input Protection Clamp Profile, Input Clamp Current vs Source Voltage

For input voltages above the clamp threshold, make sure that the input current never exceeds the absolute maximum rating (see the *Absolute Maximum Ratings* table) of ±10 mA to prevent any damage to the device. Figure 7-4 shows that a small series resistor placed in series with the analog inputs is an effective way to limit the input current. In addition to limiting the input current, this resistor can also provide an antialiasing, low-pass filter (LPF) when coupled with a capacitor. To maintain the dc accuracy of the system, matching the external source impedance on the AIN_nA, AIN_nB input pin with an equal resistance on the AIN_nAGND AIN_nBGND pin is recommended. This matching helps cancel any additional offset error contributed by the external resistance.

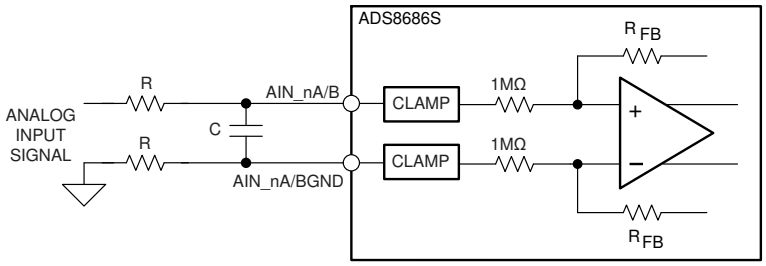

Figure 7-4. Input Resistance Matching on the Analog Input

The input overvoltage protection clamp on the ADS8686S is intended to control transient excursions on the input pins. Leaving the device in a state where the clamp circuit is activated for extended periods of time in normal or power-down mode is not recommended because this fault condition can degrade device performance and reliability. Using external protection circuits is also recommended as a secondary protection scheme to protect the device. Using external protection devices helps protect against surges, electrostatic discharge (ESD), and electrical fast transient (EFT) conditions.

7.3.4 Programmable Gain Amplifier (PGA)

The device offers a programmable gain amplifier (PGA) at each individual analog input channel that converts the input single-ended signal into a fully differential signal to drive the internal 16-bit ADC. The PGA also adjusts the common-mode level of the input signal before being fed into the ADC to provide the maximum usage of the ADC input dynamic range.

The logic levels on the range select pins, HW_RNGSEL[1:0], determine the analog input range of all analog input channels (see the *HW_RANGESEL[1:0] (Input)* section). If both range select pins are tied to a logic low, the analog input range is determined in software mode through the input range registers (see the *Register Maps* section for details). In software mode, an individual analog input range can be configured per channel. The device also supports a 20% overrange feature on all input channels in software mode. Program the D[7:0] bits from the 0x08H and 0x0AH registers to individually enable the overrange feature for channels AIN_xA. Program the same value in both registers. Program the D[7:0] bits from the 0x09H and 0x0Bh registers to individually enable the overrange feature for channels AIN_xB. Program the same value in both registers. See the 0x0AH and 0x0BH register details for the programmed register values. The programmed range of the selected channel is increased by 20%. For example, if channel AIN_0A is programmed for a ±10-V range with the overrange feature, the resultant input range is ±12 V.

In hardware mode, the range selected by the HW_RNGSEL[1:0] pins is applicable for all channels. A logic change on the HW_RNGSEL[1:0] pins has an immediate effect on the analog input range; however, there is typically a settling time of approximately 120 µs in addition to the normal acquisition time requirement for the low-pass filter option 2.

Table 7-1 lists the various gain settings achievable with the HW_RNGSEL[1:0] pin settings.

Table 7-1. Analog Input Range Selection

HW_RNGSEL1	HW_RNGSEL0	ANALOG INPUT RANGE
0	0	Configured as per the input range register programming
0	1	±2.5 V
1	0	±5 V
1	1	±10 V

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7.3.5 Second-Order, Programmable, Low-Pass Filter (LPF)

In order to mitigate the noise of the front-end amplifiers and gain resistors of the PGA, each analog input channel of the ADS8686S features a second-order, programmable, antialiasing, low-pass filter (LPF) at the output of the PGA.

Table 7-2 lists the various programmable LPF options available in the device. The programmable LPF options are available in the software mode of operation.

Table 7-2. Programmable LPF Settings

LPF OPTION	REGISTER SETTING	RANGE	LPF CORNER FREQUENCY
LPF 1	0x00b	±10 V, ±12 V	39 kHz
LPF 1	0x00b	±5 V, ±2.5 V, ±6 V, ±3 V	33 kHz
LPF 2	0x01b	All ranges	15 kHz
LPF 3	0x10b	All ranges	376 kHz

Figure 7-5 shows the magnitude response of the analog antialiasing filter for the various range and filter options.

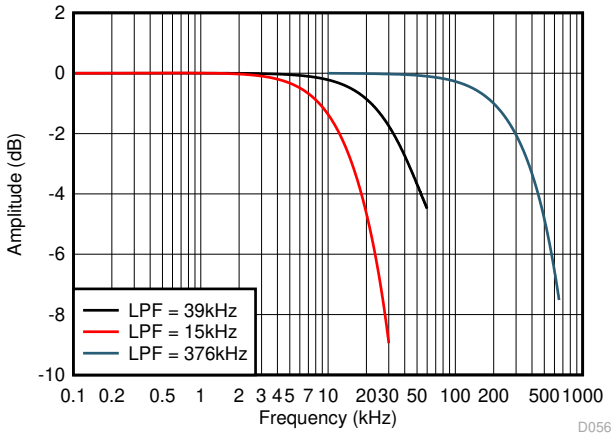

Figure 7-5. Second-Order LPF Magnitude Response

7.3.6 ADC Driver

In order to meet the performance of a 16-bit, SAR ADC at the maximum sampling rate (1 MSPS), the capacitors at the input of the ADC must be successfully charged and discharged during the acquisition time window. The ADC inputs must settle to better than 16-bit accuracy before any sampled analog voltage is converted. This drive requirement at the ADC inputs necessitates the use of a high-bandwidth, low-noise, and stable amplifier buffer. The ADS8686S features an integrated input driver as part of the signal chain for each analog input, thus simplifying the signal chain design.

7.3.7 Multiplexer

The ADS8686S features 16-channel analog inputs. The analog inputs are grouped in two sets of eight channels, AIN_xA and AIN_xB. These groups of eight channels are connected to two 16-bit SAR ADCs through a highly configurable 9:1 multiplexer (MUX). Apart from the eight channels, the MUX is also connected to an internal 2:1 MUX. The 2:1 MUX can be configured to monitor internal nodes for diagnostic purposes.

In hardware mode, the multiplexer channel selection is controlled by the CHSEL[2:0] pin status. The CHSEL[2:0] pin status, when RESET is released, determines the initial channel pair to be configured. Consequently, the CHSEL[2:0] pin status is monitored during the device conversion time to decide the next state for the MUX connection. In hardware mode, the internal diagnostic channels cannot be accessed.

In software mode, the multiplexer channel selection is controlled by programming the appropriate device register.

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In hardware and software modes, the sequencer and burst modes can be enabled to reduce the software overhead for cycling through the MUX; see the *Sequencer* section for more details.

7.3.8 Digital Filter and Noise

The ADS8686S features an optional digital second-order sinc filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. As explained in Table 7-3, the oversampling ratio of the digital filter is determined by the configuration of the OS[2:0] pins in hardware mode or through the OS bits programming in software mode. When enabled, the oversampling is applicable for all channels. The overall throughput of the ADC decreases proportionally with the increase to the oversampling ratio. When the oversampling ratio increases, there is a proportional improvement in the SNR performance and decrease in the bandwidth of the input signal.

In oversampling mode, the ADC takes the first sample for each channel at the rising edge of the CONVST signal. After converting the first sample, the subsequent samples are taken by an internally generated sampling control signal. The samples are then averaged to reduce the noise of the signal chain as well as to improve the SNR of the ADC. The final output is also decimated to provide a 16-bit output for each channel.

If oversampling is enabled with the sequencer in burst mode, the extra samples are gathered for a given channel before the sequencer moves on to the next channel.

Table 7-3. Oversampling Bit Decoding

OSx PINS, OS BITS	OSR	LPF OPTION	TYPICAL SNR (dB)						−3-dB BANDWIDTH (kHz)
			±2.5-V RANGE	±3-V RANGE	±5-V RANGE	±6-V RANGE	±10-V RANGE	±12-V RANGE	±10-V RANGE
000	No OSR	LPF 1	86.99	87.32	89.55	89.69	90.69	90.53	39.4
001	2	LPF 1	87.6	87.89	90.25	90.4	91.53	91.35	39.4
010	4	LPF 1	88.04	88.36	90.89	91.01	92.37	92.17	37.5
011	8	LPF 1	88.74	89.07	91.65	97.79	93.29	93.08	32.0
100	16	LPF 1	89.97	90.28	92.76	92.92	94.4	94.21	22.4
101	32	LPF 1	91.98	92.21	94.33	94.45	95.65	95.53	12.9
110	64	LPF 1	93.61	93.95	95.68	95.83	96.8	96.69	6.8
111	128	LPF 1	95.53	95.9	97.27	97.42	97.97	98.01	3.4
000	No OSR	LPF 2	89.05	89.35	90.98	91.11	91.92	91.85	15.4
001	2	LPF 2	89.94	90.18	91.91	92.01	92.94	92.84	15.4
010	4	LPF 2	90.4	90.65	92.62	92.73	93.82	93.72	15.3
011	8	LPF 2	90.81	91.08	93.2	93.31	94.53	94.42	14.8
100	16	LPF 2	91.39	91.7	93.82	93.95	95.19	95.07	13.3
101	32	LPF 2	92.74	92.96	94.84	94.95	95.99	95.87	10.1
110	64	LPF 2	93.85	94.2	95.91	96.04	96.88	96.85	6.2
111	128	LPF 2	95.62	95.94	97.28	97.47	98.04	98.02	3.4
000	No OSR	LPF 3	77.29	77.33	81.12	81.25	84.33	83.58	399.9
001	2	LPF 3	80.11	80.34	83.79	83.95	86.77	86.26	210.3
010	4	LPF 3	82.97	83.24	86.52	86.67	89.25	88.87	108.8
011	8	LPF 3	85.82	86.1	89.14	89.31	91.58	91.28	55.0
100	16	LPF 3	88.53	88.81	91.56	91.73	93.59	93.38	27.6
101	32	LPF 3	91.26	91.5	93.78	93.89	95.28	95.12	13.8
110	64	LPF 3	93.29	93.64	95.49	95.6	96.62	96.52	6.9
111	128	LPF 3	95.46	95.79	97.1	97.27	97.94	97.89	3.5

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7.3.9 Reference

The ADS8686S can operate with either an internal or external reference along with an internal gain amplifier. The internal or external reference selection is determined by an external REFSEL pin, as explained in the *REFSEL (Input)* section. The REFIO pin outputs the internal band-gap voltage (in internal reference mode) or functions as an input to the external reference voltage (in external reference mode). In both cases, the on-chip amplifier is always enabled. Use this internal amplifier to gain the reference voltage and drive the actual reference input of the internal ADC core for maximizing performance. The REFCAP (pin 31) must be decoupled with REFGND (pin 32) using a 10-µF, X5R, or X7R ceramic capacitor.

7.3.9.1 Internal Reference

The device has an internal 2.5-V (nominal value) band-gap reference. In order to select the internal reference, the REFSEL pin must be tied high or connected to DVDD. When the internal reference is used, REFIO (pin 33) becomes an output pin with the internal reference value. A 100-nF (minimum) decoupling capacitor, as illustrated in Figure 7-6, is recommended to be placed between the REFIO pin and REFIO_GND (pin 34). The capacitor must be placed as close to the REFIO pin as possible. The output impedance of the internal band-gap creates a low-pass filter with this capacitor to band-limit the noise of the band-gap output. Using a smaller capacitor increases the reference noise in the system, thus degrading SNR and SINAD performance. Do not use the REFIO pin to drive external AC or DC loads because of the limited current output capability of the pin. The REFIO pin can be used as a reference source if followed by a suitable op amp buffer.

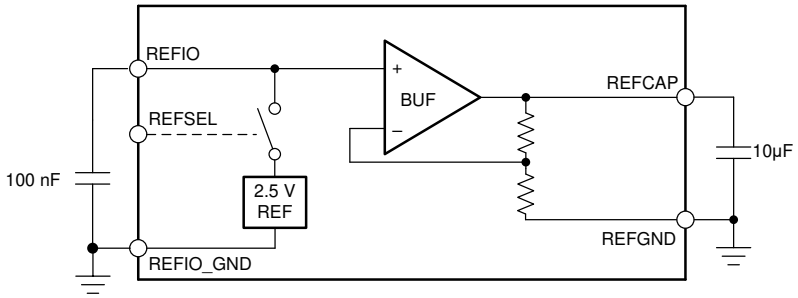

Figure 7-6. Reference Circuitry

7.3.9.2 External Reference

For applications that require a reference voltage with a lower temperature drift or a common reference voltage for multiple devices, the ADS8686S offers a provision to use an external reference by using the internal buffer to drive the ADC reference. To select external reference mode, either tie the REFSEL pin low or connect this pin to DGND. In this mode, an external 2.5-V reference must be applied at REFIO (pin 33), which becomes a high-impedance input pin. Any low-drift, small-size external reference can be used in this mode because the internal buffer is optimally designed to handle the dynamic loading on the ADC reference input. The output of the external reference must be filtered to minimize the resulting effect of the reference noise on system performance. Figure 7-7 depicts a typical connection diagram for this mode.

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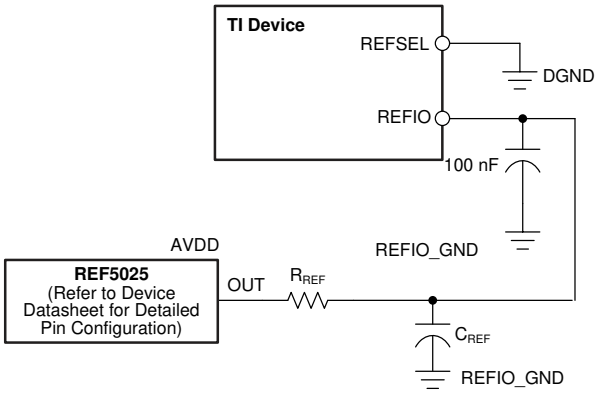

Figure 7-7. Device Connections for Using an External 2.5-V Reference

7.3.9.3 Supplying One V_{REF} to Multiple Devices

For applications that require multiple ADS8686S devices, using the same reference voltage source for all the ADCs helps eliminate any potential errors in the system resulting from mismatch between multiple reference sources.

Figure 7-8 shows the recommended connection diagram for an application that uses one device in internal reference mode and provides the reference source for other devices. The device used as the source of the voltage reference is bypassed by a 10-µF capacitor on the REFIO pin, whereas the other devices are bypassed with a 100-nF capacitor.

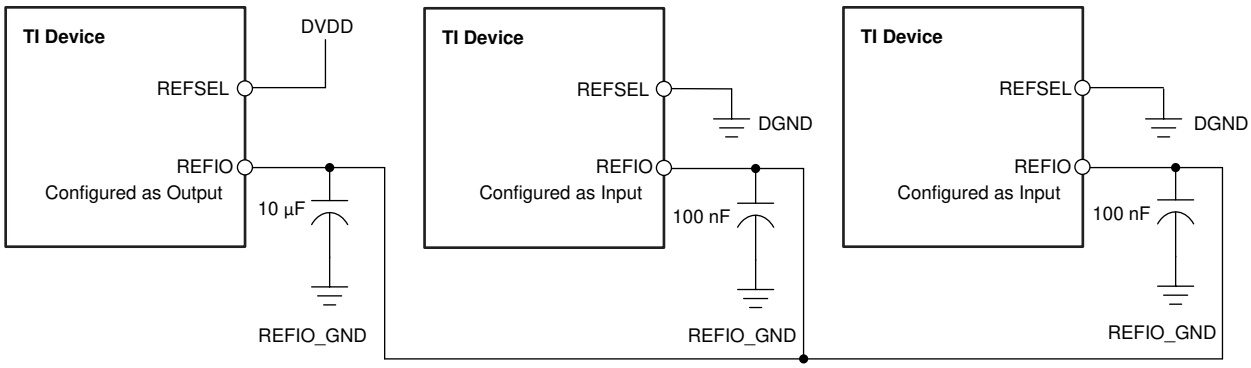

Figure 7-8. Multiple Devices Connected with an Internal Reference from One Device

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Figure 7-9 shows the recommended connection diagram for an application that uses an external voltage reference (such as the REF5025) to provide the reference source for multiple devices.

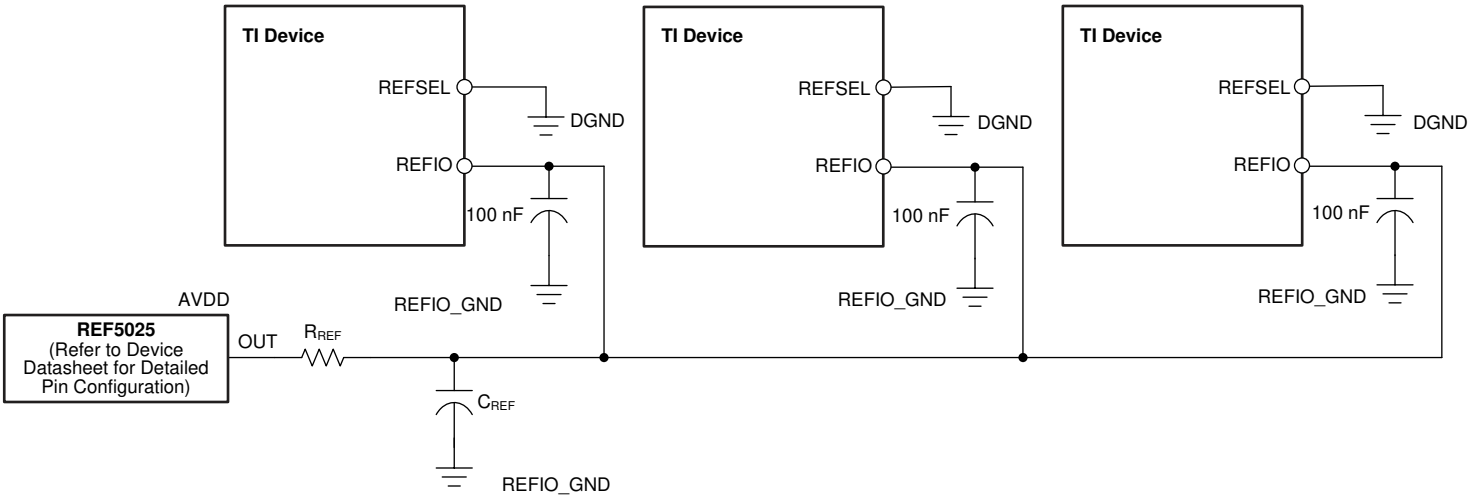

Figure 7-9. Multiple Devices Connected Using an External Reference

7.3.10 ADC Transfer Function

The ADS8686S outputs 16 bits of conversion data in binary twos complement format for all ranges. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB and 3/2 LSB). The LSB size is the full-scale range ÷ 65,536 for the ADS8686S. Figure 7-10 and Table 7-4 show the ideal transfer characteristics for the ADS8686S. The LSB size is dependent on the analog input range selected.

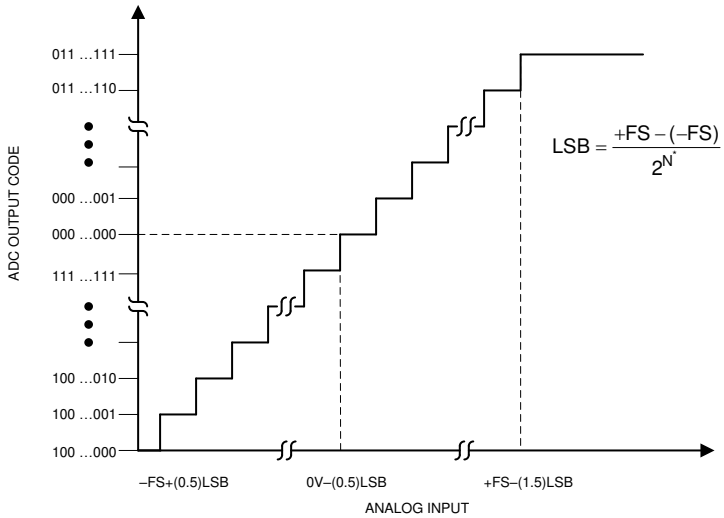

Figure 7-10. Transfer Characteristics

Table 7-4. ADC Full-Scale Range and LSB Size for Different Ranges

RANGE (V)	+FS (V)	MIDSCALE (V)	–FS (V)	LSB (µV)
±12	12	0	–12	366
±10	10	0	–10	305
±6	6	0	–6	183
±5	5	0	–5	152
±3	3	0	–3	92
±2.5	2.5	0	–2.5	76

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7.4 Device Functional Modes

7.4.1 Device Interface: Pin Description

Multiple digital pins of the ADS8686S are dual function. The pin functionality is decided by the status of the HW_RNGSELx pins at reset. Table 7-6 outlines the pin functionality in the different modes of operation and interface modes.

7.4.1.1 REFSEL (Input)

The REFSEL pin is a digital input pin that enables selection between the internal or external reference mode of operation for the device. If the REFSEL pin is set to logic high, then the internal reference is enabled and selected. If this pin is set to logic low, then the internal band-gap reference circuit is disabled and powered down. In this mode, an external reference voltage must be provided to the REFIO pin. Under both conditions, the internal reference buffer is always enabled.

The REFSEL pin status is latched when the $\overline{\text{RESET}}$ pin transitions from low to high. After the reference is configured the changes to the logic level of REFSEL signal are ignored.

7.4.1.2 $\overline{\text{RESET}}$ (Input)

The $\overline{\text{RESET}}$ pin is an active-low digital input. A dedicated reset pin allows the device to be reset at any time in an asynchronous manner. The ADS8686S offers two reset modes: full and partial. The $\overline{\text{RESET}}$ pin must be held low to enter one of the reset modes. The duration of the pulled low time decides the reset mode. A partial reset does not affect the programmed values in the software mode or the latched values in the hardware mode of operation. The partial reset reinitializes the internal modules of the device. A full reset programs the device to operate in the default state. The device must always be reset after power-up as well as after recovery from shut-down mode when all the supplies and references have settled to the required accuracy. If the reset is issued during an ongoing conversion process, then the device aborts the conversion and output data are invalid. If the reset signal is applied during a data read operation, then the output data registers are all reset to zero.

In order to initiate the next conversion cycle after deactivating a reset condition, allow for a minimum time delay between the rising edge of the $\overline{\text{RESET}}$ input and the rising edge of the CONVST input (see the *Timing Requirements* table). Any violation in this timing requirement can result in corrupting the results from the next conversion.

7.4.1.3 SEQEN (Input)

The SEQEN pin is a digital input pin that enables the internal channel sequencer mode for data capture in the hardware mode of operation. If the SEQEN pin is set to logic high when the device exits the full reset, then the channel sequencer is enabled. The device cycles through the channel sequence with the CONVST signal based on the burst mode selection setting. See the *Sequencer* section for further details.

7.4.1.4 HW_RANGESEL[1:0] (Input)

The HW_RNGSEL pins are digital input pins that select hardware or software mode of operation. The status of these pins are latched at full reset to choose between the software or hardware mode of operation. In hardware mode of operation, the pins also select the analog input range for all the input channels. See the *Operation Mode* section for further details.

7.4.1.5 SER/BYTE/$\overline{\text{PAR}}$ (Input)

The SER/BYTE/$\overline{\text{PAR}}$ is a digital input pin that selects the digital interface option for device communication along with the DB9/BYTESEL pin. If the SER/BYTE/$\overline{\text{PAR}}$ pin is set to logic low at full reset, the parallel interface is selected. If the SER/BYTE/$\overline{\text{PAR}}$ pin is set to logic high at full reset, the serial or byte interface is selected based on the status of the DB9/BYTESEL pin. See the *Programming* section for further details.

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7.4.1.6 DB[3:0] (Input/Output)

The DB[3:0] are digital input/output pins.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use these pins to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use these pins to read data from the device. See the *Parallel Interface* section for further details.

In software byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] = 00), use these pins to program the device during the write operation and read data during the read operation. See the *Parallel Byte Interface* section for further details.

In hardware byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] ≠ 00), use these pins to read data from the device. See the *Parallel Byte Interface* section for further details.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0) tie these pins to DGND.

7.4.1.7 DB4/$\overline{\text{SER1W}}$ (Input/Output)

DB4/$\overline{\text{SER1W}}$ is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In software byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Byte Interface* section for further details.

In hardware byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Byte Interface* section for further details.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0) this pin determines if the device serial data output is available only on the SDOA pin or on both the SDOA and SDOB pins. The status is latched at the release of a full reset. If $\overline{\text{SER1W}}$ is low, the serial output is available on SDOA only. If $\overline{\text{SER1W}}$ is high, the serial output is available on SDOA and SDOB. See the *Serial Interface* section for further details.

7.4.1.8 DB5/CRCEN (Input/Output)

DB5/CRCEN is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In software byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Byte Interface* section for further details.

In hardware byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Byte Interface* section for further details.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0) this pin acts as the CRC enable input. The status is latched at the release of a full reset. If CRCEN is high, an additional CRC word is sent after the last conversion result. If CRCEN is low, the CRC word is not sent out. See the *Interface Diagnosis: SELF TEST and CRC* section for further details.

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7.4.1.9 DB[7:6] (Input/Output)

The DB[7:6] are digital input/output pins.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use these pins to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use these pins to read data from the device. See the *Parallel Interface* section for further details.

In software byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] = 00), use these pins to program the device during the write operation and read data during the read operation. See the *Parallel Byte Interface* section for further details.

In hardware byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] ≠ 00), use these pins read data from the device. See the *Parallel Byte Interface* section for further details.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0) tie these pins to DGND.

7.4.1.10 DB8 (Input/Output)

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from device. See the *Parallel Interface* section for further details.

In byte and serial interface modes (SER/BYTE/$\overline{\text{PAR}}$ = 1), tie this pin to DGND.

7.4.1.11 DB9/BYTESEL (Input/Output)

DB9/BYTESEL is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte and serial interface modes (SER/BYTE/$\overline{\text{PAR}}$ = 1), this pin is not used for device communication and is programmed as a device input. The status of this pin is latched at a full reset to determine the byte or serial interface modes. If BYTESEL is high, the byte interface mode is selected. If BYTESEL is low, the serial interface mode is selected. Any digital activity on this pin is ignored after the signal is latched.

7.4.1.12 DB10/SDI (Input/Output)

DB10/SDI is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), tie this pin to DGND.

In software serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0, HW_RNGSEL[1:0] = 00) this pin acts as the serial data input for device programmability. See the *Serial Interface* section for further details.

In hardware serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0, HW_RNGSEL[1:0] ≠ 00), tie this pin to DGND.

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7.4.1.13 DB11/SDOB (Input/Output)

DB11/SDOB is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), tie this pin to DGND.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0) this pin acts as the serial data output B. See the *Serial Interface* section for further details.

7.4.1.14 DB12/SDOA (Input/Output)

DB12/SDOA is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), tie this pin to DGND.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0) this pin acts as the serial data output A. See the *Serial Interface* section for further details.

7.4.1.15 DB13/OS0 (Input/Output)

DB13/OS0 is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), tie this pin to DGND.

In hardware serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0, HW_RNGSEL[1:0] ≠ 00) this pin acts as the oversampling selection bit 0. The status of this pin is latched at the release of a full reset. See the *Digital Filter and Noise* section for further details.

7.4.1.16 DB14/OS1 (Input/Output)

DB14/OS1 is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), tie this pin to DGND.

In hardware serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0, HW_RNGSEL[1:0] ≠ 00) this pin acts as the oversampling selection bit 1. The status of this pin is latched at the release of a full reset. See the *Digital Filter and Noise* section for further details.

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7.4.1.17 DB15/OS2 (Input/Output)

DB15/OS2 is a dual-function digital input/output pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to program the device during the write operation and read data during the read operation. See the *Parallel Interface* section for further details.

In hardware parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] ≠ 00), use this pin to read data from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), tie this pin to DGND.

In hardware serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0, HW_RNGSEL[1:0] ≠ 00) this pin acts as the oversampling selection bit 2. The status of this pin is latched at the release of a full reset. See the *Digital Filter and Noise* section for further details.

7.4.1.18 $\overline{\text{WR}}$/BURST (Input)

$\overline{\text{WR}}$/BURST is dual-function digital input pin.

In software parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0, HW_RNGSEL[1:0] = 00), use this pin to control the device write operation. The $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals together enable DB[15:0] as the digital input to program the device. See the *Parallel Interface* section for further details.

In software byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1, HW_RNGSEL[1:0] = 00), use this pin to control the device write operation. The $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals together enable DB[7:0] as the digital input to program the device. See the *Parallel Byte Interface* section for further details.

In software serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0, HW_RNGSEL[1:0] = 00), tie this pin to DGND.

In hardware mode (HW_RNGSEL[1:0] ≠ 00) this pin acts as the burst mode enable. The status of this pin is latched at the release of a full reset. If the BURST pin is set to logic high, then burst mode is enabled. If the BURST pin is set to logic low, then burst mode is disabled. See the *Burst Sequencer* section for further details.

7.4.1.19 SCLK/$\overline{\text{RD}}$ (Input)

SCLK/$\overline{\text{RD}}$ is dual-function digital input pin.

In serial interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 0), all synchronous access to the device are timed with respect to rising edge of the SCLK signal. See the *Serial Interface* section for further details.

In parallel interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 0), use this pin to control the device read operation. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals together enable DB[15:0] as the digital output to read from the device. See the *Parallel Interface* section for further details.

In byte interface mode (SER/BYTE/$\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1), use this pin to control the device read operation. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals together enable DB[7:0] as the digital output to read from the device. See the *Parallel Byte Interface* section for further details.

7.4.1.20 $\overline{\text{CS}}$ (Input)

$\overline{\text{CS}}$ is active-low, chip-select digital input signal.

A rising edge on the $\overline{\text{CS}}$ signal programs all data lines in tri-state mode. This function allows multiple devices to share the same output data lines. The falling edge of the $\overline{\text{CS}}$ signal marks the beginning of the output data transfer frame in any interface mode of operation for the device.

In the parallel and byte interface modes, both the $\overline{\text{CS}}$ and $\overline{\text{WR}}$ or $\overline{\text{RD}}$ input pins must be driven low to enable the digital bus for writing to registers or reading the conversion data (DB[15:0] for parallel and DB[7:0] for byte interface).

In serial mode, the falling edge of the $\overline{\text{CS}}$ signal initiates the data communication using a standard SPI interface in mode 00.

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7.4.1.21 CHSEL[2:0] (Input)

CHSEL[2:0] are digital input pins.

In hardware mode (HW_RNGSEL[1:0] ≠ 00, SEQEN = 0), these input pins select the channel for the next conversion. See the *Hardware Mode* section for further details.

In hardware sequence mode (HW_RNGSEL[1:0] ≠ 00, SEQEN = 1), these input pins select the last channel pair in the hardware sequence. See the *Hardware Mode Sequencer* section for further details.

In software mode (HW_RNGSEL[1:0] = 00), tie these pin to DGND.

7.4.1.22 BUSY (Output)

BUSY is an active-high digital output pin.

BUSY is an active-high digital output signal. This pin goes to logic high after the rising edge of the CONVST signal, indicating that the front-end, track-and-hold circuits for the selected input channels are in hold mode and that the ADC conversion has started. When the BUSY signal goes high, any activity on the CONVST input has no effect on the device. The BUSY output remains high until the conversion process is complete and the conversion data are latched into the output data registers for read out. If the conversion data are read for the previous conversion when BUSY is high, make sure that the data read operation is complete before the falling edge of the BUSY output.

In the burst mode of operation, the BUSY pin goes to logic high after the rising edge of the CONVST signal. The BUSY signal stays high until all conversions in the sequence are complete. See the *Burst Sequencer* section for further details.

7.4.1.23 CONVST (Input)

CONVST is an active-high digital input pin.

The rising edge of the CONVST pin, when BUSY is low, initiates a new conversion on the selected input channel pair from channel group A and channel group B. For normal mode and sequencer mode of operation, every CONVST signal performs one conversion of the selected channel pair based on the oversampling setting.

For burst mode of operation only one CONVST signal is needed for the sequencer to cycle through the channel sequence. The BUSY signal is held high during this duration.

7.4.2 Device Modes of Operation

The ADS8686S supports multiple modes of operation that can be enabled using the hardware or software modes of control. The device enters hardware or software mode based on the status of the HW_RNGSEL[1:0] pins at a full reset. In hardware mode, all device configurations are controlled by pin control and access to the internal registers is prohibited. In software mode, the interface and reference configurations are controlled by the respective pins. All other device configurations are enabled though register access only. To switch between hardware mode to software mode or vice-versa, a full reset is required.

7.4.2.1 Shutdown Mode

The ADS8686S supports a low-power shutdown mode in which the entire internal circuitry is powered down and all registers are cleared and reset to the default values. In shutdown mode the total power consumption of the device is 700 µW.

In order to enter shutdown mode, keep the $\overline{\text{RESET}}$ pin low for greater than 1.2 µs.

The device exits shutdown mode when the $\overline{\text{RESET}}$ pin is set from low to high. At this time, the device exits shutdown mode and enters the hardware or software mode of operation based on the status of the HW_RNGSEL[1:0] pins. The power-up time to perform a register write in software mode is approximately 240 µs. A conversion can be initiated after 15 ms.

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7.4.2.2 Operation Mode

7.4.2.2.1 Hardware Mode

The device enters hardware mode if the HW_RNGSEL[1:0] pins are set to either 01, 10, or 11 at the time of a full reset. In hardware mode, the device operates with restricted functionality. All device functionality is configured through the pin control. The logic levels of the following signals at a full reset configure the functionality of the ADS8686S: CRC, BURST, SEQEN, SER/BYTE/ $\overline{\text{PAR}}$, DB9/BYESEL, DB8, and OSx. Table 7-5 provides a summary of the signals that are latched by the device on the release of a full reset. After the device is configured, a full reset through the $\overline{\text{RESET}}$ pin is required to exit the configuration and set up an alternate configuration. The data communication interface selected also dictates the functionality available in hardware mode. Table 7-6 provides a full list of the functionality available in hardware parallel, byte, or serial mode.

Table 7-5. Summary of Hardware Pin Behavior

SIGNAL	LATCHED AT FULL RESET		READ AT RESET		READ WHEN BUSY		EDGE DRIVEN	
	HW MODE	SW MODE	HW MODE	SW MODE	HW MODE	SW MODE	HW MODE	SW MODE
REFSEL	Yes	Yes						
SEQEN	Yes							
HW_RNGSELx (range change)			Yes	Yes			Yes	
HW_RNGSELx (HW or SW mode)	Yes	Yes						
CRCEN	Yes	No						
OSx	Yes	No						
BURST	Yes	No						
CHSELx			Yes		Yes			
$\overline{\text{SER1W}}$	Yes	Yes						
SER/BYTE/ $\overline{\text{PAR}}$	Yes	Yes						
DB9/BYTESEL	Yes	Yes						

Table 7-6. Pin Functionality Overview

PIN NAME	OPERATION MODE					
	SOFTWARE, HW_RNGSELx = 00			HARDWARE, HW_RNGSELx ≠ 00		
	SERIAL, SER/BYTE/ $\overline{\text{PAR}}$ = 1, DB9/ BYTESEL = 0	PARALLEL BYTE, SER/BYTE/ $\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1	PARALLEL, SER/ BYTE/ $\overline{\text{PAR}}$ = 0	SERIAL, SER/BYTE/ $\overline{\text{PAR}}$ = 1, DB9/ BYTESEL = 0	PARALLEL BYTE, SER/BYTE/ $\overline{\text{PAR}}$ = 1, DB9/BYTESEL = 1	PARALLEL, SER/ BYTE/ $\overline{\text{PAR}}$ = 0
CHSELx	No function, connect to DGND	No function, connect to DGND	No function, connect to DGND	CHSELx	CHSELx	CHSELx
SCLK/ $\overline{\text{RD}}$	SCLK	$\overline{\text{RD}}$	$\overline{\text{RD}}$	SCLK	$\overline{\text{RD}}$	$\overline{\text{RD}}$
$\overline{\text{WR}}$/BURST	Connect to DGND	$\overline{\text{WR}}$	$\overline{\text{WR}}$	BURST	BURST	BURST
DB[15:13]/OS[0:2]	Connect to DGND	Connect to DGND	DB15 to DB13	OSx	Connect to DGND	DB15 to DB13
DB12/SDOA	SDOA	Connect to DGND	DB12	SDOA	Connect to DGND	DB12
DB11/SDOB	SDOB, leave floating for serial 1-wire mode	Connect to DGND	DB11	SDOB	Connect to DGND	DB11
DB10/SDI	SDI	Connect to DGND	DB10	Connect to DGND	Connect to DGND	DB10
DB9/BYTESEL	Connect to DGND	Connect to DVDD	DB9	Connect to DGND	Connect to DVDD	DB9
DB8 to DB6, DB3 to DB0	Connect to DGND	DB8 to DB6, DB3 to DB0	DB8 to DB6, DB3 to DB0	Connect to DGND	DB8 to DB6, DB3 to DB0	DB8 to DB6, DB3 to DB0
DB5/CRCEN	Connect to DGND	DB5	DB5	CRCEN	DB5	DB5
DB4/ $\overline{\text{SER1W}}$	$\overline{\text{SER1W}}$	DB4	DB4	$\overline{\text{SER1W}}$	DB4	DB4
HW_RNGSELx	Connect to DGND	Connect to DGND	Connect to DGND	Configure analog input range	Configure analog input range	Configure analog input range
SEQEN	Connect to DGND	Connect to DGND	Connect to DGND	SEQEN	SEQEN	SEQEN
REFSEL	REFSEL	REFSEL	REFSEL	REFSEL	REFSEL	REFSEL

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In hardware mode, the CHSELx and HW_RNGSELx control signals can change their state during device operation and have an immediate effect on the device configuration.

The CHSELx pins are read at reset to determine the first analog input channel pair to be acquired for conversion. In the sequencer mode of operation, the CHSELx pins configure the settings for the sequencer. See the *Sequencer* section for additional details. The CHSELx pin status must be kept constant during the ADC conversion process (that is, between the CONVST rising edge and the BUSY falling edge). The status of the CHSELx pins is read during this time to select the next channel pair for conversion or to modify the hardware sequencer setting.

The HW_RNGSELx signals program the analog input range. The selected input range is applied to all 16 analog input channels. A logic change on these pins has an immediate effect on the analog input range. Allow for a typical settling time of 120 µs, in addition to the normal acquisition time requirement after the range change. The recommended practice is to hardwire the range select pins according to the desired input range for the system signals.

7.4.2.2.2 Software Mode

In software mode, all configuration settings can be controlled except for the reference and interface by programming the on-chip registers. All functionality of the ADS8686S is available when software mode is selected. Table 7-5 provides a summary of the signals that are latched by the device on the release of a full reset, depending on the mode of operation chosen.

7.4.2.3 Reset Functionality

The ADS8686S supports two reset modes: full and partial. The reset mode selected is dependent on the length of the reset low pulse.

A partial reset is applied when the $\overline{\text{RESET}}$ pin is held low between 40 ns and 500 ns. A partial reset reinitializes the sequencer, digital filter, SPI, and SAR ADC modules.

The ongoing conversion result is discarded on completion of a partial reset. The partial reset does not affect the register values programmed in software mode or the user configuration latched in hardware and software modes. In software mode, a dummy conversion is required after a partial reset.

After the release of a partial reset, the device is fully functional after 50 ns and a dummy conversion can be initiated.

A full reset is applied when the $\overline{\text{RESET}}$ pin is held low for a minimum of 1.2 µs. A full reset configures the device to its default power-on state. Hardware or software mode, the internal or external reference, and the type of interface are configured when the ADS8686S is released from a full reset.

At power-up, the $\overline{\text{RESET}}$ signal must be kept low until the AVDD and DVDD supplies are stable. The $\overline{\text{RESET}}$ signal can be released after the supplies ramp to stable operating conditions. The logic level of the HW_RNGSELx, REFSEL, SER/BYTE/ $\overline{\text{PAR}}$, DB9/BYTESEL, and DB4/ $\overline{\text{SER1W}}$ pins are latched when the $\overline{\text{RESET}}$ pin is released to determine the device configuration.

After 15 ms from releasing $\overline{\text{RESET}}$, the device is completely reconfigured and a conversion can be initiated.

In hardware mode, the DB8CRCEN, OSx, BURST, and SEQEN pin status is also latched when the $\overline{\text{RESET}}$ pin transitions from low to high in full reset mode. The changes to these signals are ignored after they are latched until the next full reset. In hardware mode, the analog input range (HW_RNGSELx signals) can be configured during either a full or a partial reset or during normal operation, but hardware or software mode selection requires a full reset to reconfigure when this setting is latched.

In hardware mode, the CHSELx and HW_RNGSELx pins are monitored at release from both a full and a partial reset to perform the following actions:

- Select the first analog input channel pair to acquire for conversion
- Configure the sequencer
- Select the analog input voltage range

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The CHSELx signals are not latched at reset. The channel pair selected for next conversion, or the hardware sequencer, can be reconfigured during normal operation by setting and maintaining the CHSELx signal level before the CONVST rising edge, and holding the signal state constant until BUSY is held high by the device. See the *Channel Selection* section for further details.

The HW_RNGSELx signals are not latched in hardware mode. A logic change on these pins has an immediate effect on the range selected. See the *Programmable Gain Amplifier (PGA)* section for additional details.

In software mode, all device functionality is configured by controlling the on-chip registers. Figure 7-11 shows the device reset configuration and Table 7-6 lists an overview of the pin functionality.

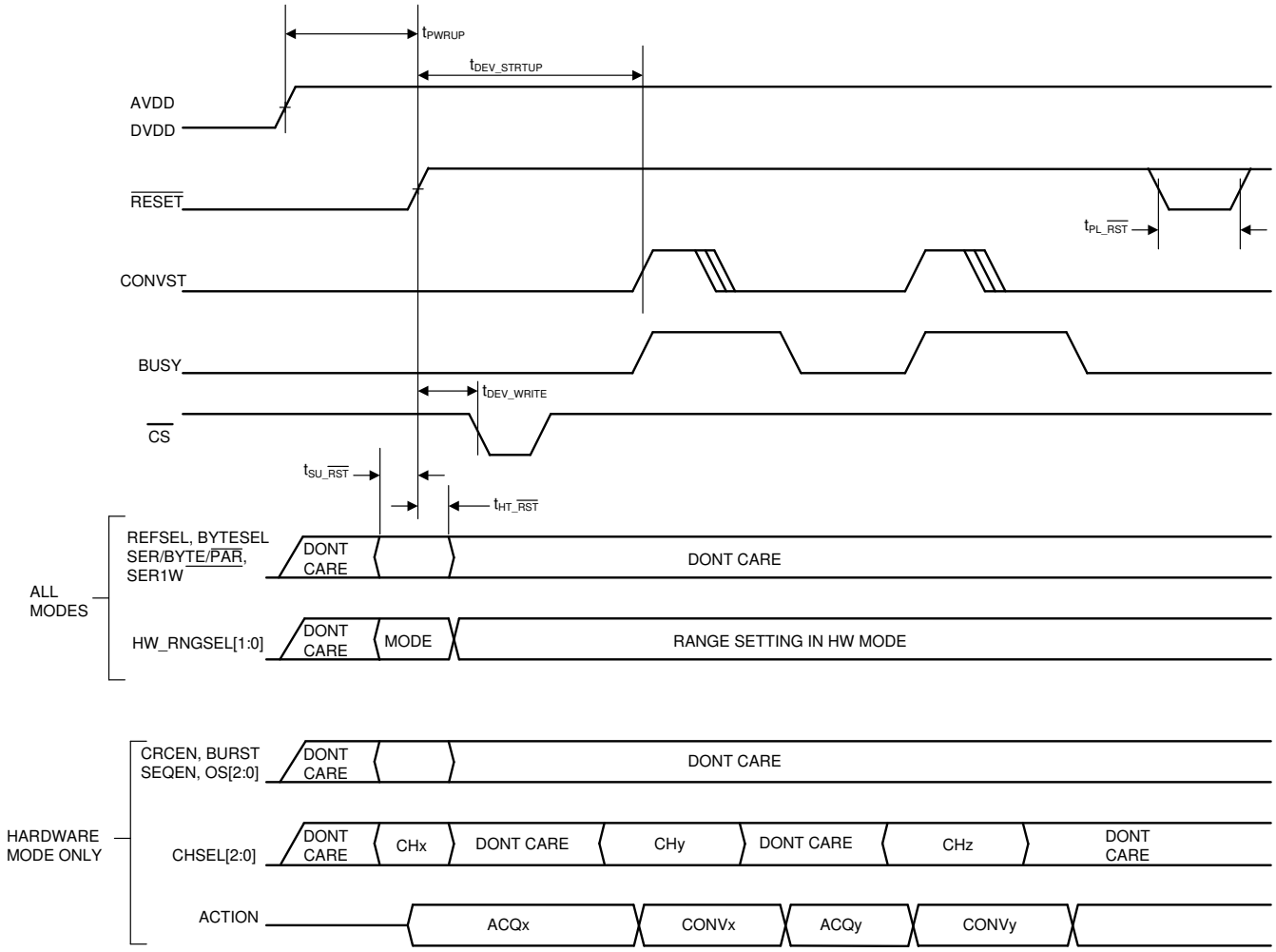

Figure 7-11. ADS8686S Configuration at Reset

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7.4.2.4 Channel Selection

7.4.2.4.1 Hardware Mode Channel Selection

In hardware mode, the logic level of the CHSELx signals during an ongoing conversion determine the channel pair for next conversion. Table 7-7 lists the CHSELx signal decoding information. After a full or partial reset, the CHSELx signal status at the rising edge of the reset signal determines the initial channel pair to sample and convert when the first CONVST signal is available. Set the CHSELx signals to the required channel before CONVST goes from low to high and maintain the status until BUSY goes from high to low, indicating the conversion complete. The device samples the CHSELx status during conversion to select the channel pair for the next conversion. The multiplexer then establishes a relevant connection between the ADC driver of the selected channel and SAR ADC. Figure 7-12 shows a timing diagram of how this mode is selected.

Table 7-7. CHSELx Pin Decoding

CHANNEL SELECTION INPUT PIN			ANALOG INPUT CHANNELS FOR CONVERSION
CHSEL2	CHSEL1	CHSEL0	
0	0	0	AIN_0A, AIN_0B
0	0	1	AIN_1A, AIN_1B
0	1	0	AIN_2A, AIN_2B
0	1	1	AIN_3A, AIN_3B
1	0	0	AIN_4A, AIN_4B
1	0	1	AIN_5A, AIN_5B
1	1	0	AIN_6A, AIN_6B
1	1	1	AIN_7A, AIN_7B

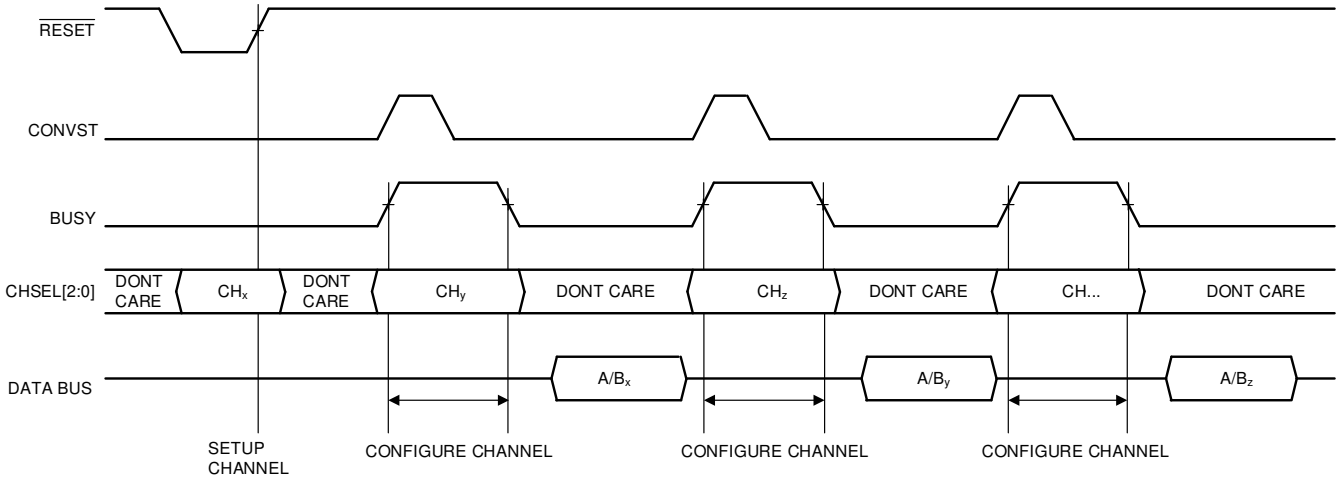

Figure 7-12. Hardware Mode Channel Conversion Setting

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7.4.2.4.2 Software Mode Channel Selection

In software mode, the channels for conversion are selected by programming the relevant channel register. On power-up or after a reset, the default channels selected for conversion are channel AIN_0A and channel AIN_0B. See Figure 7-13, Figure 7-14, and Figure 7-15 for additional details regarding the channel selection.

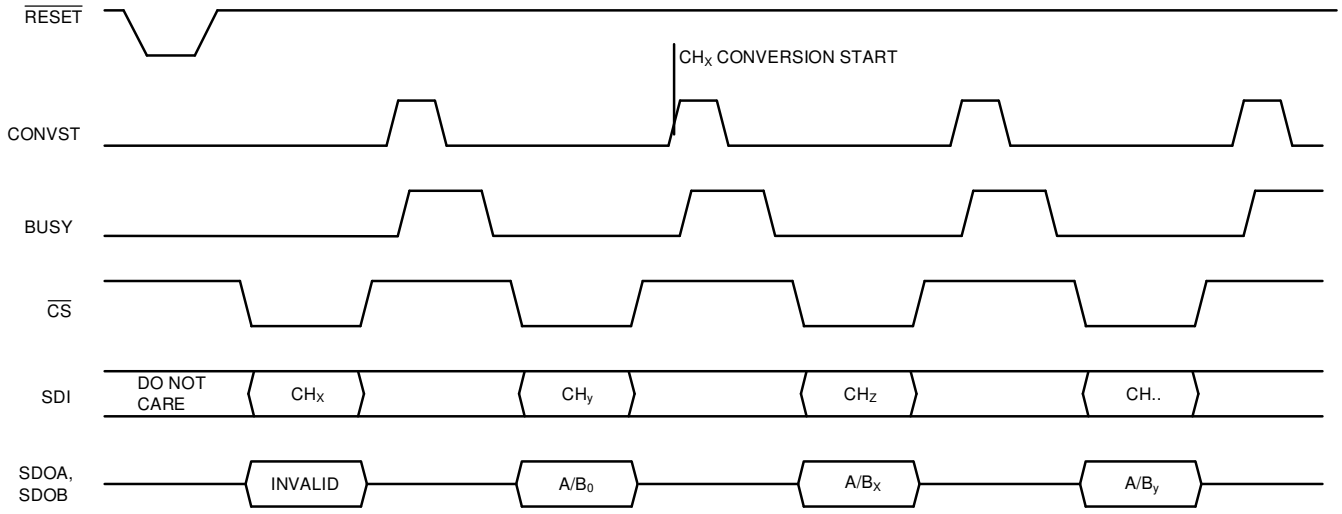

Figure 7-13. Software Serial Mode Channel Conversion Setting

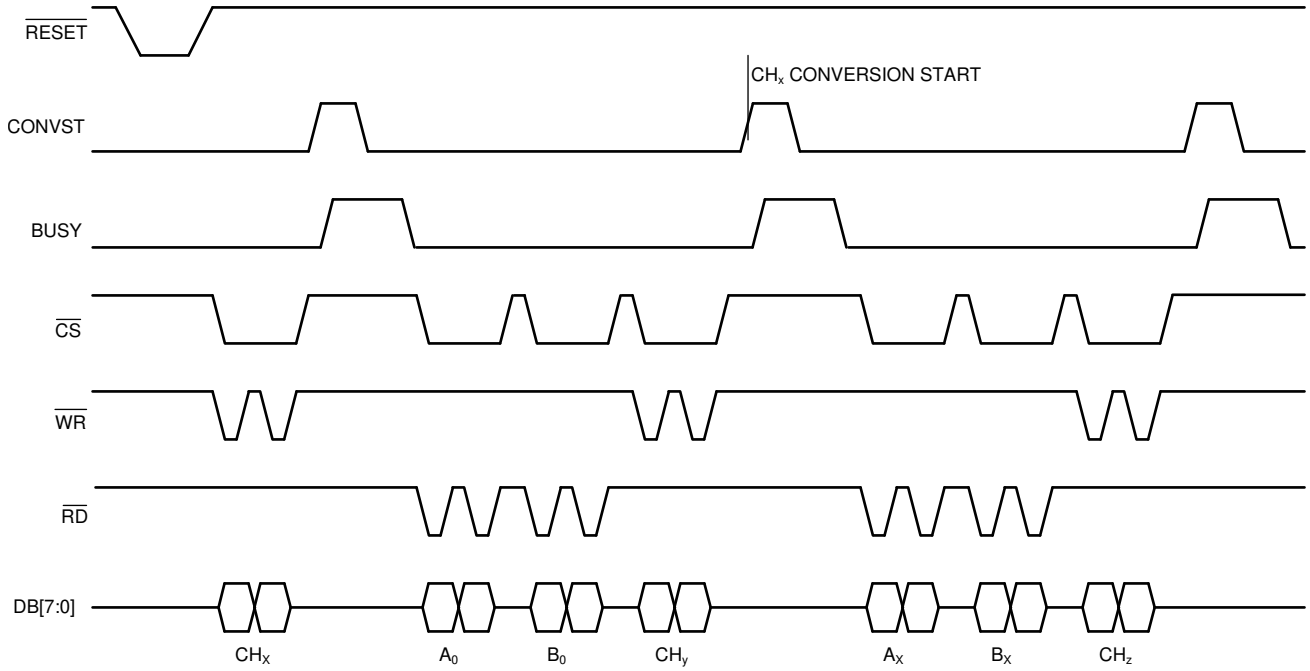

Figure 7-14. Software Parallel Byte Mode Channel Conversion Setting

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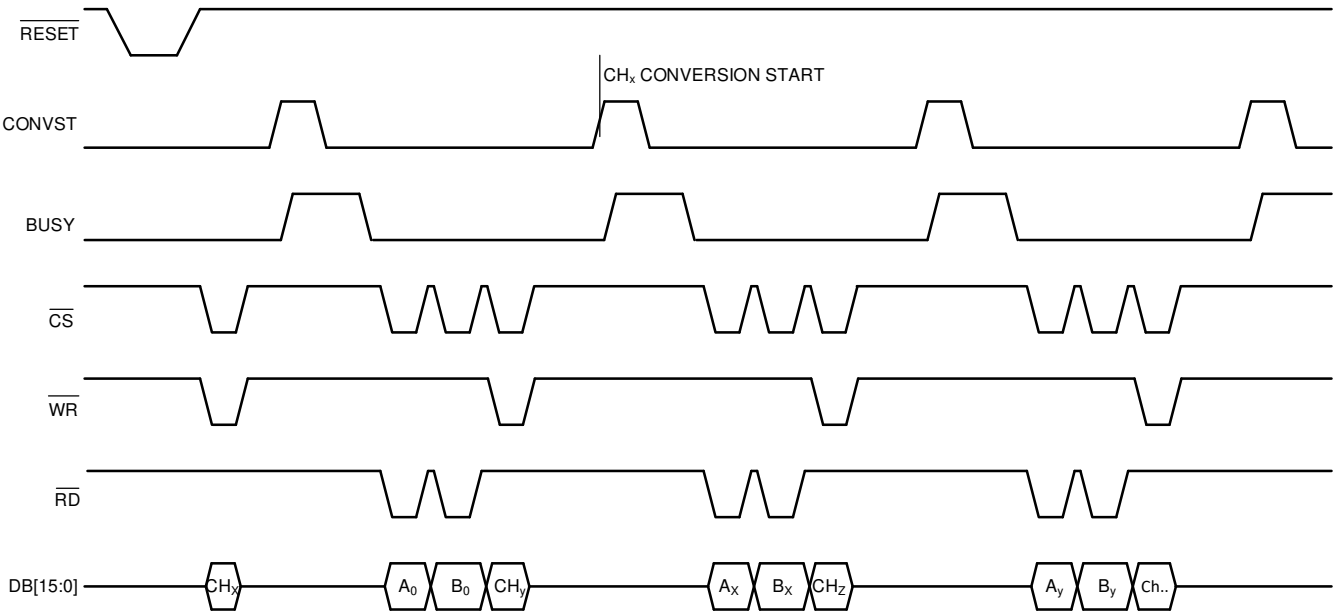

Figure 7-15. Software Parallel Mode Channel Conversion Setting

7.4.2.5 Sequencer

The ADS8686S features a highly configurable sequencer functionality. The sequencer enables selection of the internal MUX connection in a predetermined order. This architecture helps reduce the software overhead on the host controller to configure the next channel for conversion.

A complete set of sequencer functionality and configurability is available in software mode. The sequencer stack has 32 unique configurable sequence steps. All channels, including the diagnostic channel, can be randomly programmed in any order. Additionally, any channel AIN_*n*A input can be paired with any channel AIN_*n*B input or diagnostic channel.

The sequencer can be operated with or without the burst function enabled. With the burst function enabled, only one CONVST pulse is required to convert every channel in a sequence. With burst mode disabled, one CONVST pulse is required for every conversion step in the sequence. See the *Burst Sequencer* section for additional details on operating in burst mode.

7.4.2.5.1 Hardware Mode Sequencer

In hardware mode, the sequencer has limited functionality. The sequencer always selects a particular channel pair (for example, AIN_nA and AIN_nB).

In hardware mode, the sequencer is controlled by the SEQEN pin and the CHSEL[2:0] pins. The logic level of the SEQEN pin is latched when $\overline{\text{RESET}}$ transitions from logic low to high after a full reset. Table 7-8 explains the sequencer setting based on the logic state of the SEQEN pin after a full reset. A full reset is required to exit sequencer mode and to setup an alternate configuration.

Table 7-8. Hardware Mode Sequencer Configuration

SEQEN	INTERFACE MODE
0	Sequencer disabled
1	Sequencer enabled

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When the sequencer is enabled, the logic levels of the CHSEL[2:0] pins determine the number of channel pairs selected for the conversion in the sequence. The CHSEL[2:0] pins at the time when $\overline{\text{RESET}}$ is released determine the initial settings for the channels to convert in the first sequence. To reconfigure the sequence channels selected for a conversion thereafter, set the CHSEL[2:0] pins to the required setting for the duration of the BUSY pulse for the final conversion in the sequence. Table 7-9 explains the relationship between the CHSEL[2:0] pin to the channel pairs selected in the sequence. See Figure 7-16 for further timing sequence details.

Table 7-9. CHSELx Pin Decoding Sequencer

CHANNEL SELECTION INPUT PIN			ANALOG INPUT CHANNELS FOR SEQUENTIAL CONVERSION
CHSEL2	CHSEL1	CHSEL0	
0	0	0	AIN_0A, AIN_0B only
0	0	1	AIN_0A, AIN_0B to AIN_1A, AIN_1B
0	1	0	AIN_0A, AIN_0B to AIN_2A, AIN_2B
0	1	1	AIN_0A, AIN_0B to AIN_3A, AIN_3B
1	0	0	AIN_0A, AIN_0B to AIN_4A, AIN_4B
1	0	1	AIN_0A, AIN_0B to AIN_5A, AIN_5B
1	1	0	AIN_0A, AIN_0B to AIN_6A, AIN_6B
1	1	1	AIN_0A, AIN_0B to AIN_7A, AIN_7B

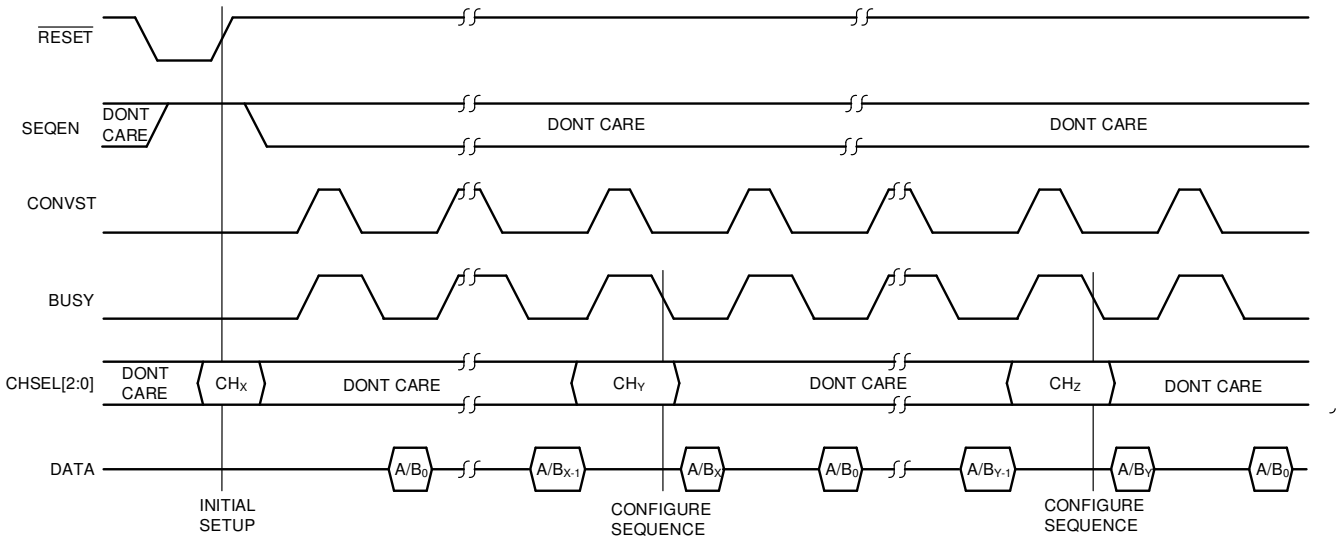

Figure 7-16. Hardware Mode Sequencer Configuration

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7.4.2.5.2 Software Mode Sequencer

In software mode, the ADS8686S offers a 32-stack, fully configurable sequencer. The configuration register and sequencer stack registers can be programmed by using the parallel, byte, or serial interface.

Each stack register has two 4-bit fields to control each individual MUX. This structure allows any input from channel AIN_nA to be paired with any input from channel AIN_nB, or to any diagnostic channel. The sequencer depth is programmable from 1 to 32. The sequencer depth is determined by setting the SSRENx bit in the sequencer stack register corresponding to the last step. The channels to convert are selected by programming the ASELx and BSELx bits in each sequence stack register for the depth required.

The sequencer is activated by setting the SEQEN bit in the configuration register to 1.

The recommended procedure to configure and enable the sequencer (see Figure 7-17 for additional information) is as follows:

1. Program the analog input range for the required analog input channels.
2. Program the sequencer stack registers (S_0, S_1,...S_n) to select the channels for the sequence.
3. Set the SSRENx bit in the last required sequence step.
4. Set the SEQEN bit in the configuration register.
5. Provide a dummy CONVST pulse.
6. Provide additional CONVST pulses and read the conversion results.

After all sequence steps are cycled through, the sequence automatically restarts from the first element in the sequencer stack with the next CONVST pulse.

Following a partial reset, the sequencer pointer is repositioned to the first layer of the stack, but the register programmed values remain unchanged.

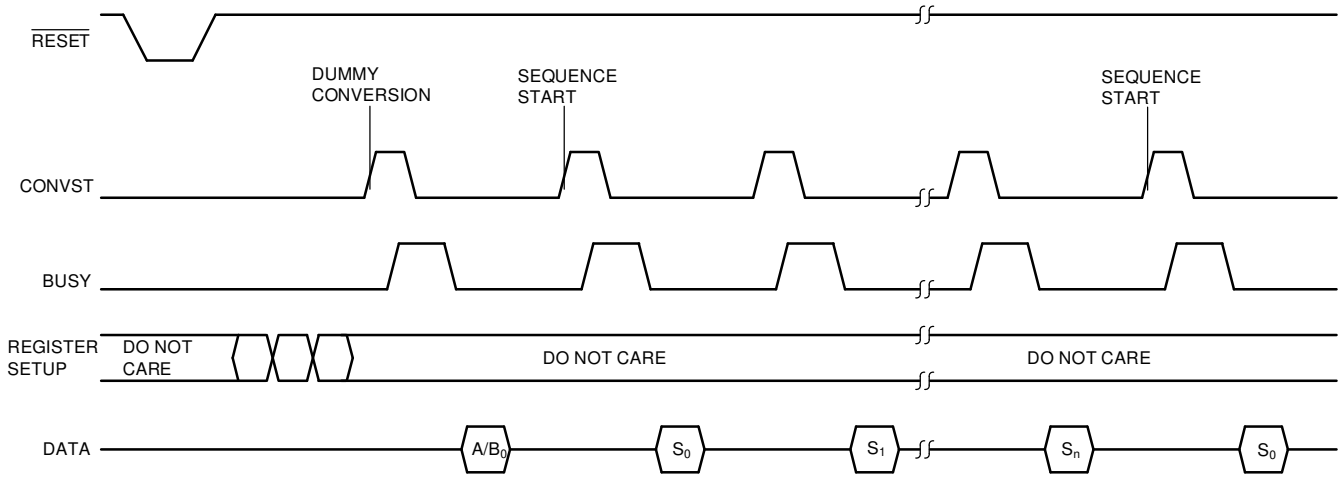

Figure 7-17. Software Mode Sequencer Configuration

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7.4.2.6 Burst Sequencer

The ADS8686S offers an additional feature for burst mode capture. This feature is applicable only if the sequencer feature is enabled.

With the burst feature enabled, one CONVST pulse initiates conversion of all channels configured in the sequencer. Thus, for a sequencer configured for four channel pairs, only one CONVST pulse must be provided in BURST with the sequencer configuration instead of four CONVST pulses in the sequencer only configuration.

When configured, the burst sequence is initiated at the rising edge of CONVST. The BUSY pin goes high and remains high until all conversions in the sequence are complete. If OSR mode is enabled, the sequencer captures the required samples for a given channel pair before moving to the next channel pair in sequencer. The conversion results are available for readback after the BUSY pin goes low.

The number of data reads required in the burst sequence are dependent on the length of the sequence configured.

The conversion results are presented on the data bus (parallel, byte, or serial) in the same order as the programmed sequence.

The throughput rate of the ADS8686S is limited in burst mode because each channel pair requires an acquisition, conversion, and readback time. Equation 1 estimates the time taken to complete a sequence with the number of channel pairs, N.

$$t_{BURST} = (t_{CONV} + 50\ ns) + (N - 1)\ (t_{ACQ} + t_{CONV}) + N(t_{RB}) \quad (1)$$

where

- t_{CONV} is the typical conversion time
- t_{ACQ} is the typical acquisition time
- t_{RB} is the time required to read back the conversion results in either serial 1-wire, serial 2-wire, parallel byte, or parallel mode

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7.4.2.6.1 Hardware Mode Burst Sequencer

In hardware mode, set both the BURST and SEQEN pins to logic high to enable burst sequencer mode. The device latches these inputs when the $\overline{\text{RESET}}$ signal transitions from logic low to high after a full reset event. To exit the burst mode of operation, a full reset is needed.

When the burst sequencer is enabled, the logic levels of the CHSEL[2:0] pins determine the channels selected for the conversion in the burst sequence. The CHSEL[2:0] pins at the time that $\overline{\text{RESET}}$ is released determines the initial settings for the channels to convert in the burst sequence. To reconfigure the channels selected for conversion after a reset, set the CHSEL[2:0] pins to the required setting for the duration of the next BUSY pulse. Figure 7-18 shows a timing diagram of this mode.

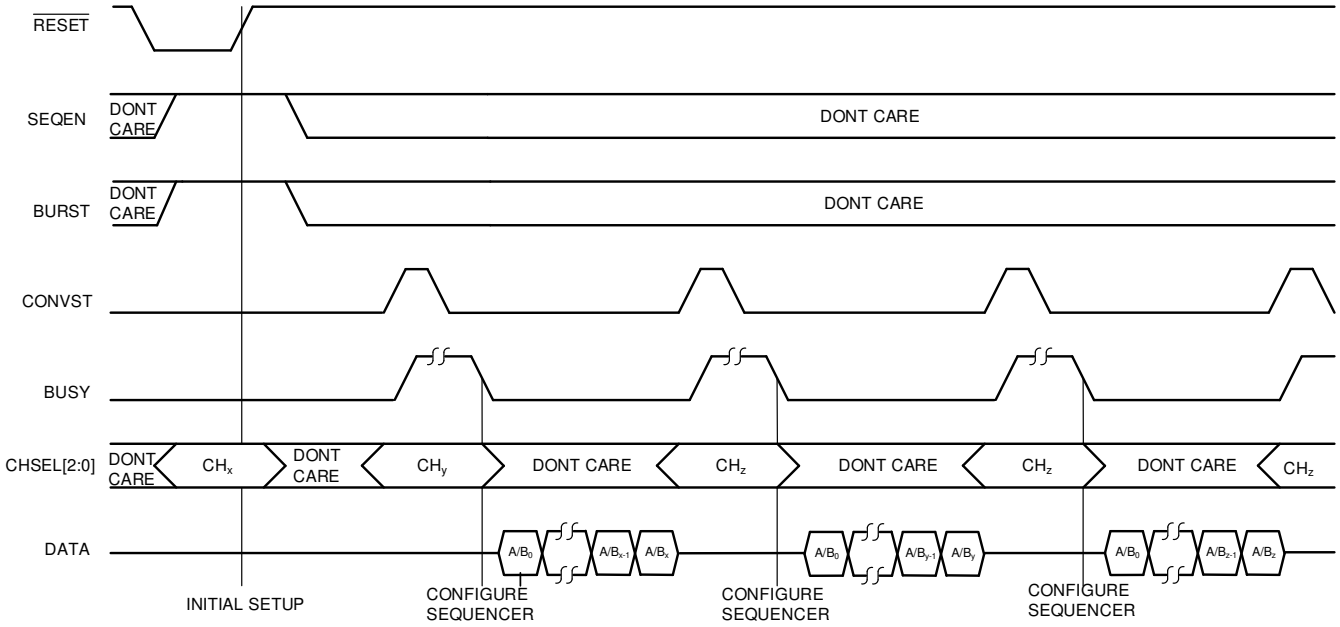

Figure 7-18. Burst Sequencer, Hardware Mode

7.4.2.6.2 Software Mode Burst Sequencer

In software mode, program the BURST bit in the configuration register to enable burst function. Enable this setting along with the SEQEN bit by programming the configuration register. Figure 7-19 shows a timing diagram for this mode.

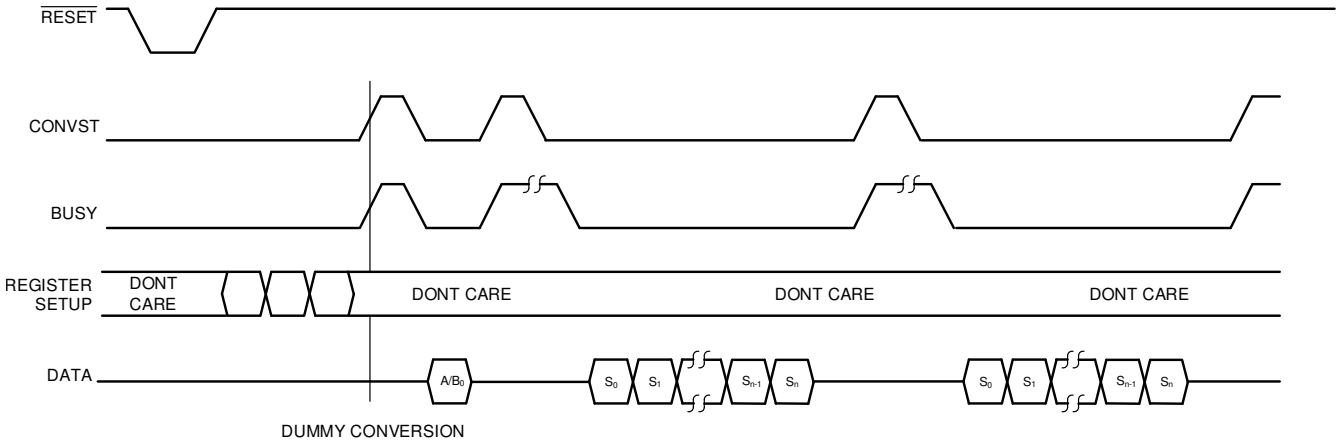

Figure 7-19. Burst Sequencer, Software Mode

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7.4.2.7 Diagnostics

7.4.2.7.1 Analog Diagnosis

The ADS8686S supports monitoring of the internal nodes AVDD and ALDO, respectively, along with the 16 analog inputs, AIN_nA and AIN_nB, by using the SAR ADCs. These channels can be monitored in the software mode of operation by programming the channel register (see the *Register Maps* section) to the corresponding channel identifier. The diagnostic channels can also be added to the sequencer stack.

Equation 2 defines the expected output for each diagnostic channel. Figure 7-20 and Figure 7-21 show the transfer function for each diagnostic channel.

$$\text{AVDD Code} = \frac{\left((4 \times \text{AVDD}) - \text{V}_{\text{REFCAP}}\right) \times 32{,}768}{5 \times \text{V}_{\text{REFCAP}}}$$

$$\text{ALDO Code} = \frac{((10 \times \text{ALDO}) - (7 \times \text{V}_{\text{REFCAP}})) \times 32{,}768}{10 \times \text{V}_{\text{REFCAP}}} \quad (2)$$

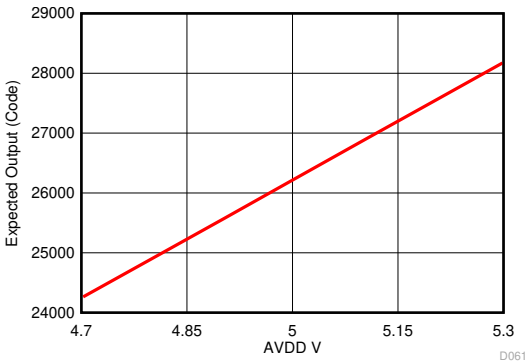

Figure 7-20. AVDD vs Expected Output Code

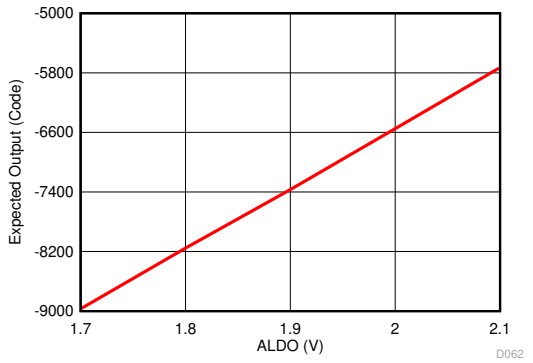

Figure 7-21. ALDO vs Expected Output Code

7.4.2.7.2 Interface Diagnosis: SELF TEST and CRC

The ADS8686S features a communication self-test mode and a cyclic redundancy check (CRC) mode. These features help diagnose any issues with the digital interface between the host and the device.

The communication self test can be enabled by programming the communication self-test channel in the channel register (see the *Register Maps* section). When enabled, the device forces the conversion result register to a known fixed output. When the conversion code is read, code 0xAAAA is output as the conversion code of ADC A, and code 0x5555 is output as the conversion code of ADC B. This feature can be accessed in the software mode of operation and is not supported in the hardware mode of operation.

The ADS8686S supports a CRC checksum mode to improve interface robustness by detecting errors in data. The CRC feature is available in both software (serial, byte, and parallel) mode and hardware (serial only) mode. The CRC feature is not available in hardware parallel or hardware byte modes. The CRC result is stored in the status register. Enabling the CRC feature enables the status register and vice versa.

In hardware mode, set the CRCEN pin to logic high when the ADS8686S is released from a full reset to enable the CRC feature. The logic level of the CRCEN pin is latched when the $\overline{\text{RESET}}$ pin is released. A full reset is required to exit the function and setup an alternative configuration. With CRC enabled, the content of the status register is appended to the conversion result (see the STATUS register in the *Register Maps* section for details regarding the CRC data structure).

In software mode, the CRC function is enabled by setting either the CRCEN bit or the STATUSEN bit in the configuration register to 1.

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If the CRC function is enabled, a CRC is calculated on the conversion results for channel AIN_nA and channel AIN_nB. The CRC is calculated and transferred on the serial, byte, or parallel interface after the conversion results are transmitted, depending on the configuration of the device. The hamming distance varies in relation to the number of bits in the conversion result. For conversions with less than or equal to 119 bits, the hamming distance is 4. For more than 119 bits, the hamming distance is 1 (that is, 1-bit errors are always detected).

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The following is a pseudocode description of how the CRC is implemented in the ADS8686S:

```
crc = 8'b0;
i = 0;
x = number of conversion channel pairs;
for (i=0, i<x, i++) begin
crc1 = crc_out(An,Crc);
crc = crc_out(Bn,Crc1);
i = i +1;
end
```

Where the function crc_out(data, crc) is:

```
crc_out[0] = data[14] ^ data[12] ^ data[8] ^ data[7] ^ data[6] ^ data[0] ^ crc[0] ^ crc[4] ^ crc[6];
crc_out[1] = data[15] ^ data[14] ^ data[13] ^ data[12] ^ data[9] ^ data[6] ^ data[1] ^ data[0] ^
crc[1] ^ crc[4] ^ crc[5] ^ crc[6] ^ crc[7];
crc_out[2] = data[15] ^ data[13] ^ data[12] ^ data[10] ^ data[8] ^ data[6] ^ data[2] ^ data[1] ^
data[0] ^ crc[0] ^ crc[2] ^ crc[4] ^ crc[5] ^ crc[7];
crc_out[3] = data[14] ^ data[13] ^ data[11] ^ data[9] ^ data[7] ^ data[3] ^ data[2] ^ data[1] ^
crc[1] ^ crc[3] ^ crc[5] ^ crc[6];
crc_out[4] = data[15] ^ data[14] ^ data[12] ^ data[10] ^ data[8] ^ data[4] ^ data[3] ^ data[2] ^
crc[0] ^ crc[2] ^ crc[4] ^ crc[6] ^ crc[7];
crc_out[5] = data[15] ^ data[13] ^ data[11] ^ data[9] ^ data[5] ^ data[4] ^ data[3] ^ crc[1] ^
crc[3] ^ crc[5] ^ crc[7];
crc_out[6] = data[14] ^ data[12] ^ data[10] ^ data[6] ^ data[5] ^ data[4] ^ crc[2] ^ crc[4] ^
crc[6];
crc_out[7] = data[15] ^ data[13] ^ data[11] ^ data[7] ^ data[6] ^ data[5] ^ crc[3] ^ crc[5] ^
crc[7];
```

The initial CRC word used by the ADS8686S is an 8-bit word equal to zero. The XOR operation described in the preceding code is executed to calculate each bit of the CRC word for the conversion result, An. This CRC word (crc1) is then used as the starting point for calculating the CRC word (crc) for the conversion result, Bn. The process repeats cyclically for each channel pair converted.

Depending on the mode of operation of the ADS8686S, the status register value is appended to the conversion data and read out through an extra read command over the serial, byte, or parallel interface. The XOR calculation can be repeated, as described in the preceding code for the received conversion results to check whether both CRC words match. Figure 7-22 describes how the CRC word is appended to the data for each mode of operation.

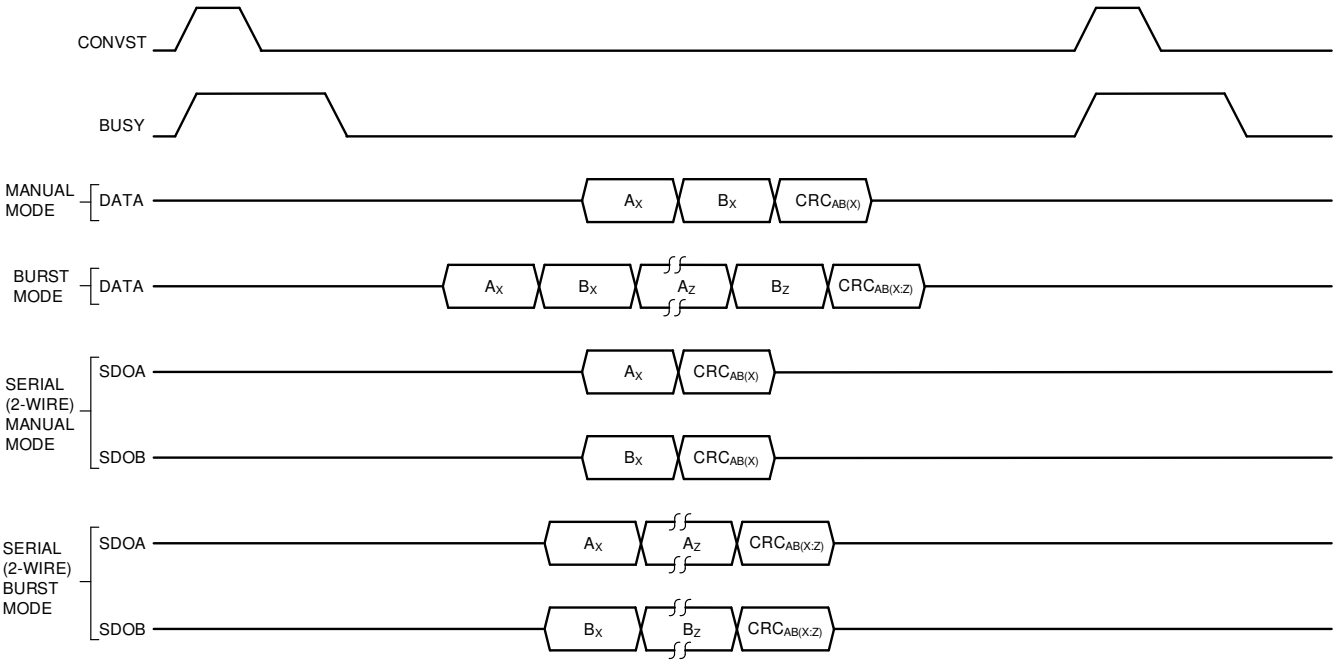

Figure 7-22. CRC Readback for All Modes

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7.5 Programming

The ADS8686S can operate in hardware or software mode of operation. The logic level of HW_RNGSEL[1:0] when the device is released from a full reset determines the mode of operation. If HW_RNGSEL[1:0] = 0b00, the device enters software mode, for any other setting the hardware mode is selected.

Communicate with the device using any of the three interfaces: parallel, parallel byte, or serial. The interface is selected based on the logic levels of the SERIAL/BYTE/ $\overline{\text{PAR}}$ pin (pin 40) and the DB9/BYTESEL pin (pin 54) when the device is released from a full reset.

In hardware mode, capture the conversion data from the device using the interface selected. All other device settings are controlled by the device pin control.

In software mode, the conversion data can be captured and programmed, and the on-chip registers contents can be read using the interface selected.

7.5.1 Parallel Interface

The ADS8686S supports the parallel interface communication using the $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and DB[15:0] signals. To read the data over the parallel bus, tie the SER/BYTE/ $\overline{\text{PAR}}$ pin low when the device is released from a full reset.

7.5.1.1 Reading Conversion Results

A channel conversion is initiated when the CONVST signal transitions from low to high. The BUSY signal goes high and stays high to indicate an ongoing conversion. A data read cycle can be initiated after the BUSY signal goes low, indicating that the conversion is complete.

The ADS8686S can read the conversion results using the parallel data bus with standard $\overline{\text{CS}}$, $\overline{\text{RD}}$, and DB[15:0] signals. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ input signals are internally gated to enable the data lines, DB15 to DB0. These signal leave their high-impedance state when both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low.

The rising edge of the $\overline{\text{CS}}$ input signal places the bus into tri-state, and the falling edge of the $\overline{\text{CS}}$ input signal takes the bus out of the high-impedance state. $\overline{\text{CS}}$ is the control signal that enables the data lines; this function allows multiple ADS8686S devices to share the same parallel data bus.

The number of required read operations depends on the device configuration. A minimum of two reads are required to read the conversion result for the simultaneously sampled A and B channels. If additional functions (such as CRC, status, and burst mode) are enabled, the number of required readbacks increases accordingly.

The $\overline{\text{RD}}$ pin reads data from the output conversion results register. Applying a sequence of $\overline{\text{RD}}$ pulses to the $\overline{\text{RD}}$ pin of the ADS8686S clocks the conversion results out from each channel onto the parallel bus, DB15 to DB0. The first $\overline{\text{RD}}$ falling edge after BUSY goes low and $\overline{\text{CS}}$ is pulled low clocks out the conversion result from channel Ax. The next $\overline{\text{RD}}$ falling edge updates the bus with the channel Bx conversion result. Figure 7-23 shows the parallel data read timing diagram.

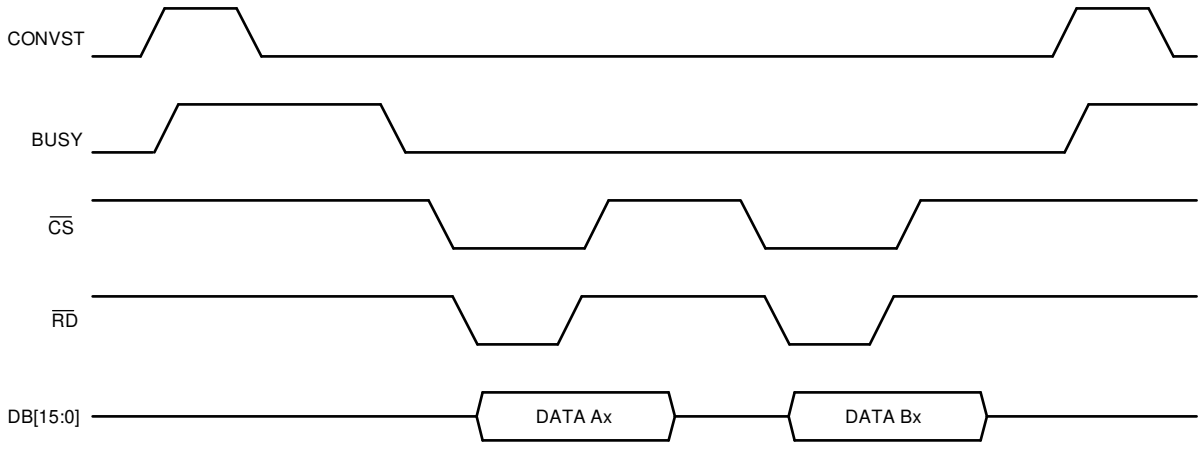

Figure 7-23. Parallel Interface Conversion Readback

7.5.1.2 Writing Register Data

The ADS8686S supports on-chip register access in software mode. A single register write command is performed by a single 16-bit parallel access through the parallel bus (DB15 to DB0), $\overline{CS}$, and $\overline{WR}$ signals. The 16-bit data to be fed on the DB[15:0] pins is determined by the register to be addressed and the device settings needed for the application. See the *Register Maps* section to determine the register content. Pull the $\overline{CS}$ pin low to take the DB[15:0] pins out of high-impedance state. Pull the $\overline{WR}$ pin low to configure the DB[15:0] pins as digital inputs. The host drives the DB[15:0] pins with the data to program the on-chip register. When the register is programmed, pull the $\overline{WR}$ pin high. Data are latched into the device on the rising edge of $\overline{WR}$. Figure 7-24 shows the parallel register write timing diagram.

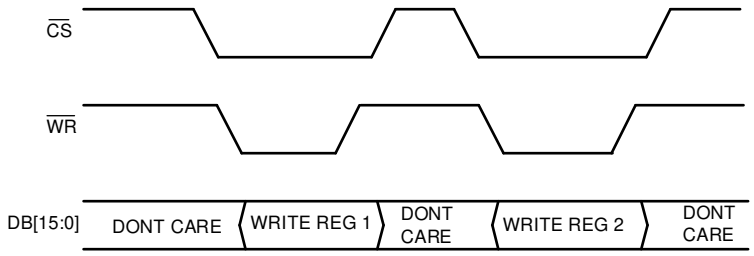

Figure 7-24. Parallel Interface Register Write

7.5.1.3 Reading Register Data

The ADS8686S supports on-chip register access in software mode. A single register read command is performed by a two 16-bit parallel data access through the parallel bus (DB15 to DB0), $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ signals. See the *Register Maps* section to determine the data to be driven on the DB[15:0] pins. Pull the $\overline{CS}$ pin low to take the DB[15:0] pins out of high-impedance state. Pull the $\overline{WR}$ pin low to configure the DB[15:0] pins as digital input. The host drives the DB[15:0] pins with the data to enable read operation for the register selected. Pull the $\overline{WR}$ pin high. The register address is latched into the device on the rising edge of $\overline{WR}$. The device transfers the register data to the output register. Pull the $\overline{RD}$ pin low to configure the DB[15:0] pins as digital outputs. The device outputs the register content on the DB[15:0] pins. The host can read the data on the rising edge of the $\overline{RD}$ pin. Figure 7-25 shows the parallel register read timing diagram.

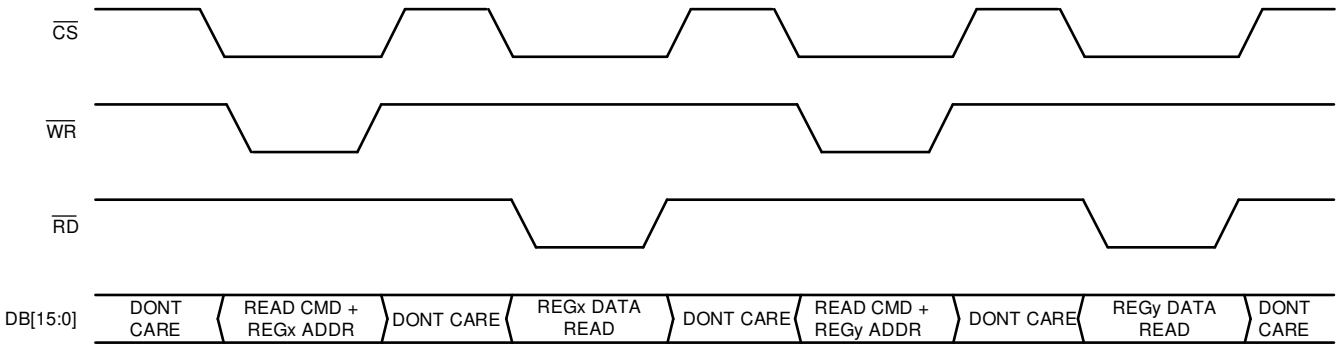

Figure 7-25. Parallel Interface Register Read

7.5.2 Parallel Byte Interface

The ADS8686S supports parallel byte interface communication using the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and DB[7:0] signals. To read the data over the parallel byte bus, tie the SER/BYTE/ $\overline{PAR}$ pin and the DB9/BYTESEL pin to a logic high state when the device is released from a full reset.

7.5.2.1 Reading Conversion Results

A channel conversion is initiated when the CONVST signal transitions from low to high. The BUSY signal goes high and stays high to indicate an ongoing conversion. A data read cycle can be initiated after the BUSY signal goes low, indicating that the conversion is complete.

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The ADS8686S can read the conversion results using the parallel data bus with standard $\overline{CS}$, $\overline{RD}$, and DB[7:0] signals. The $\overline{CS}$ and $\overline{RD}$ input signals are internally gated to enable the data lines, DB7 to DB0. These signals leave their high-impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low.

The rising edge of the $\overline{CS}$ input signal places the bus into tri-state, and the falling edge of the $\overline{CS}$ input signal takes the bus out of the high-impedance state. $\overline{CS}$ is the control signal that enables the data lines; this function allows multiple ADS8686S devices to share the same parallel data bus.

The number of required read operations depends on the device configuration. A minimum of four reads are required to read the conversion result for the simultaneously sampled A and B channels. If additional functions (such as CRC, status, and burst mode) are enabled, the number of required readbacks increases accordingly.

The $\overline{RD}$ pin reads data from the output conversion results register. Applying a sequence of $\overline{RD}$ pulses to the $\overline{RD}$ pin of the ADS8686S clocks the conversion results out from each channel onto the parallel bus, DB7 to DB0. The first two $\overline{RD}$ pulses after BUSY goes low and $\overline{CS}$ pulled low clocks out the MSB followed by the LSB of the conversion result from channel Ax. The next two $\overline{RD}$ pulses update the bus with the channel Bx conversion result. Figure 7-26 shows the parallel data read timing diagram.

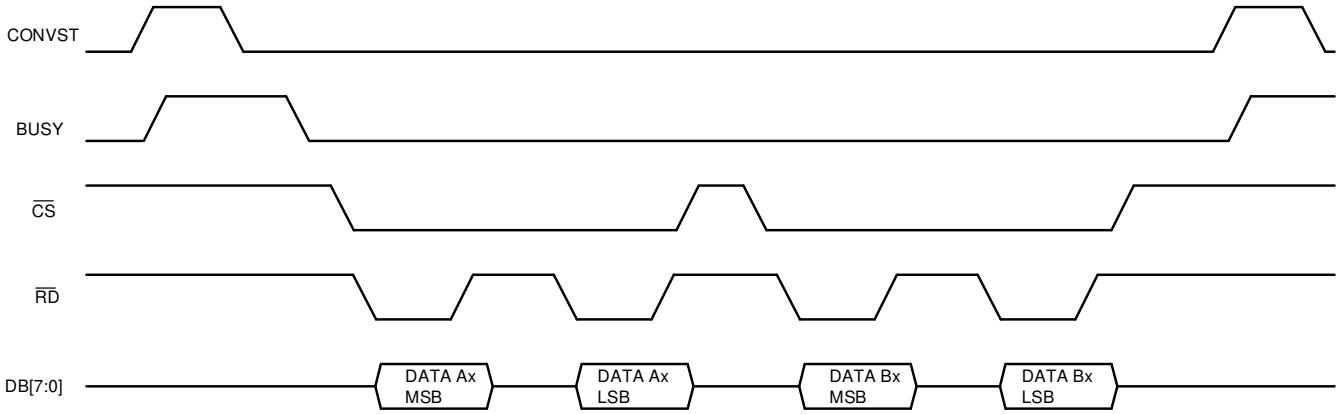

Figure 7-26. Parallel Byte Interface Conversion Readback

7.5.2.2 Writing Register Data

The ADS8686S supports on-chip register access in software mode. A single register write command is performed by a 16-bit access through the parallel byte bus (DB7 to DB0), $\overline{CS}$, and $\overline{WR}$ signals. The 16-bit data to be fed on the DB[7:0] pins is determined by the register to be addressed and the device settings needed for the application. See the *Register Maps* section to determine the register content. Pull the $\overline{CS}$ pin low to take the DB[7:0] pins out of high-impedance state. Pull the $\overline{WR}$ pin low to configure the DB[7:0] pins as digital inputs. The host drives the DB[7:0] pins with the MSB of data to program the on-chip register. When the MSB is programmed, pull the $\overline{WR}$ pin high. Repeat the same procedure to drive the LSB of the data to program on-chip register. Data are latched into the device on the rising edge of the second $\overline{WR}$ pulse. Any additional byte accesses are ignored. Pull the $\overline{CS}$ pin high to terminate the resister write operation. Figure 7-27 shows the parallel register write timing diagram.

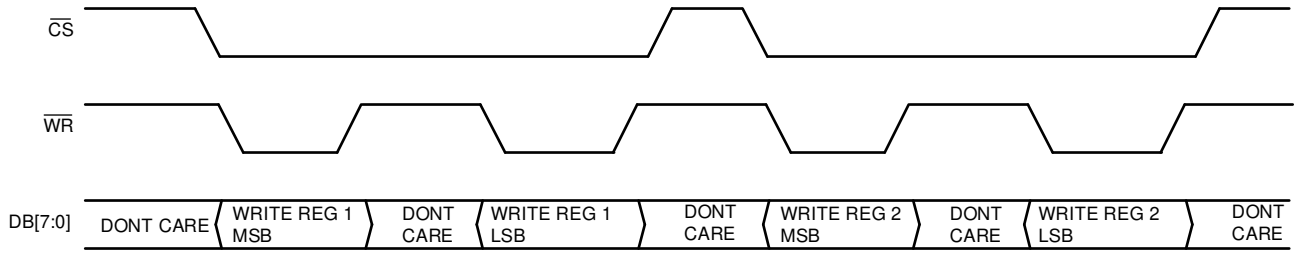

Figure 7-27. Parallel Byte Interface Register Write

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7.5.2.3 Reading Register Data

The ADS8686S supports on-chip register access in software mode. A single register read command is performed by a quad, 8-bit parallel byte data access through the parallel bus (DB7 to DB0), $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ signals. See the *Register Maps* section to determine the data to be driven on the DB[7:0] pins. Pull the $\overline{CS}$ pin low to take the DB[7:0] pins out of high-impedance state. Pull the $\overline{WR}$ pin low to configure the DB[7:0] pins as digital inputs. The host drives the DB[7:0] pins with the MSB data to enable the read operation for the register selected. Pull the $\overline{WR}$ pin high. Repeat the previous step with the LSB data of the register read operation. The register address is latched into the device on the second rising edge of $\overline{WR}$. The device transfers the register data to the output register. Pull the $\overline{RD}$ pin low to configure the DB[7:0] pins as digital outputs. The device outputs the register content on the DB[7:0] pins in two transactions of eight bits each. The host can read the data on the rising edge of the $\overline{RD}$ pin. Figure 7-28 shows the parallel byte register read timing diagram.

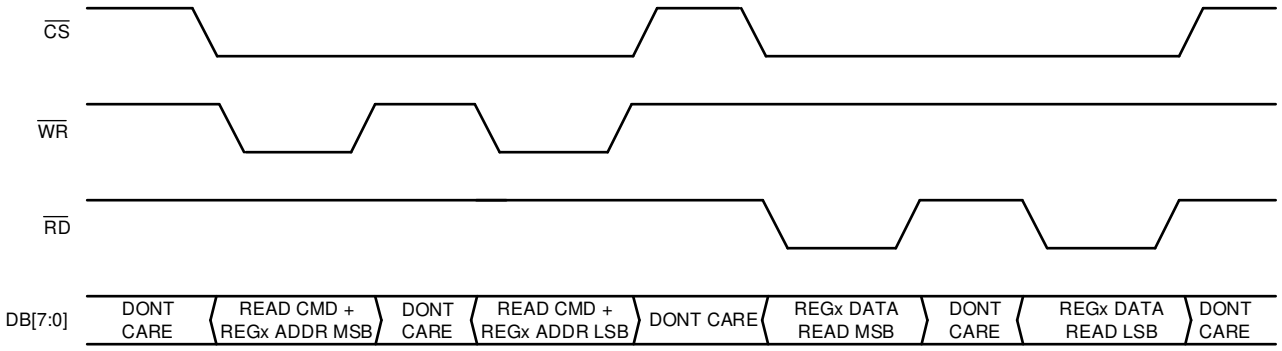

Figure 7-28. Parallel Byte Interface Register Read

7.5.3 Serial Interface

The ADS8686S supports serial (SPI) interface communication using the $\overline{CS}$, SCLK, SDI, SDOA, and SDOB signals. To read the data using the serial interface, tie the SER/BYTE/ $\overline{PAR}$ pin high and the DB9/BYTESEL pin low when the device is released from a full reset.

The ADS8686S supports data capture in serial interface mode using two output pins, SDOA and SDOB. Data can be read back from the ADS8686S by using serial 1-wire or serial 2-wire mode.

In serial 2-wire mode, conversion results from channel AIN_0A to channel AIN_7A appear on SDOA, and conversion results from channel AIN_0B to channel AIN_7B appear on SDOB. In serial 1-wire mode, conversion results from channel AIN_0B to channel AIN_7B are interlaced with the conversion results from channel AIN_0A to channel AIN_7A. To achieve the maximum throughput, serial 2-wire mode must be used.

Tie the DB4/ $\overline{SER1W}$ pin to logic high to configure the device to operate in serial 2-wire mode. Tie the DB4/ $\overline{SER1W}$ pin to logic low to configure the device to operate in serial 1-wire mode. Serial 1-wire or 2-wire mode is configured when the ADS8686S is released from a full reset.

7.5.3.1 Reading Conversion Results

A channel conversion is initiated when the CONVST signal transitions from low to high. The BUSY signal goes high and stays high to indicate an ongoing conversion. A data read cycle can be initiated after the BUSY signal goes low, indicating that the conversion is complete.

The $\overline{CS}$ falling edge takes the data output lines, SDOA and SDOB, out of tri-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, SDOA and SDOB. Figure 7-29 illustrates a read of two simultaneous conversion results using two SDOx lines on the ADS8686S. If the status register is appended to the conversion results or operates in sequencer burst mode where multiples of 16 SCLK transfers access data from the ADS8686S, hold $\overline{CS}$ low for the entire data frame. Data can also be clocked out using just the SDOA line. For the ADS8686S to access both the channel AIN_xA and channel AIN_xB conversion results on the SDOA line, a total of 32 SCLK cycles is required. Frame these 32 SCLK cycles using one $\overline{CS}$ signal, or individually frame each group of 16 SCLK cycles using the $\overline{CS}$ signal. The disadvantage of using just serial 1-wire mode is that the throughput rate is reduced.

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Leave the unused SDOB line unconnected in serial 1-wire mode. If using SDOA as a single serial data output line, the channel results are output in the following order: AIN_xA and AIN_xB. Figure 7-30 shows a 1-wire, serial readback operation.

The speed at which the data can be read back in serial interface mode is dependent on the SPI frequency, DVDD supply, and the capacitance of the load on the SDO line, C_{LOAD}. Table 7-10 shows a summary of the maximum speed achievable for various conditions.

Table 7-10. SPI Frequency versus Load Capacitance and DVDD

DVDD (V)	C_{LOAD} (pF)	SPI FREQUENCY (MHz)
1.8 to 3	20	40
3 to 5	30	50

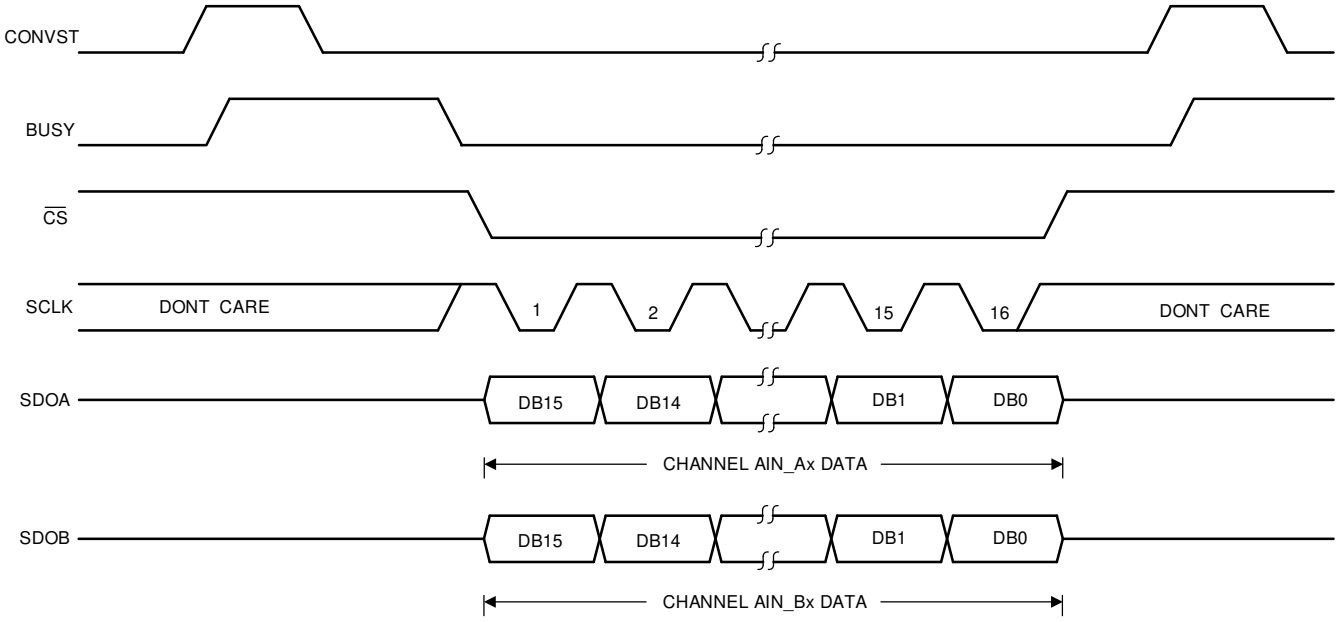

Figure 7-29. Serial Interface, 2-Wire Mode

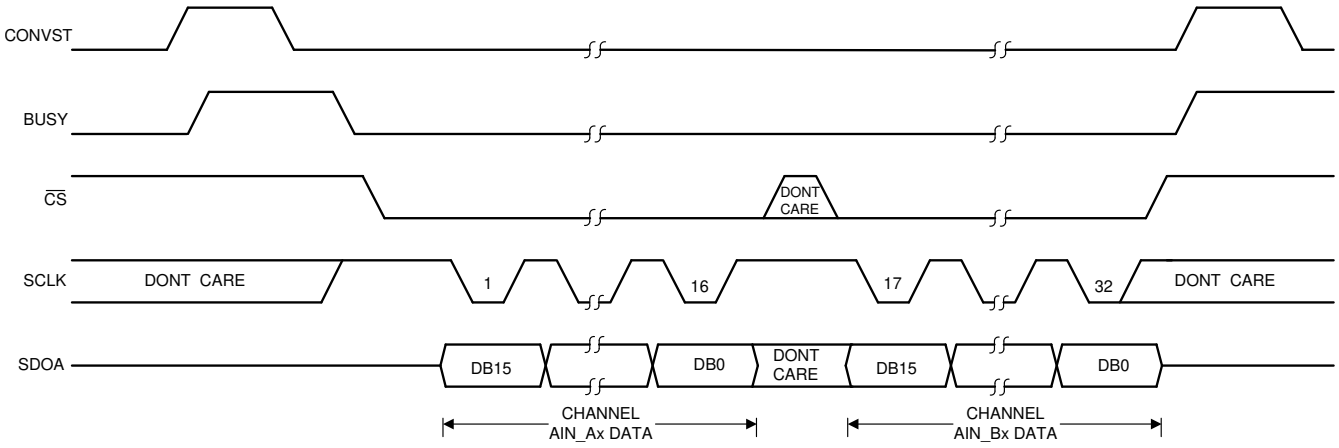

Figure 7-30. Serial Interface, 1-Wire Mode

7.5.3.2 Writing Register Data

The ADS8686S on-chip registers can be written to by using the serial interface in software mode. A register write command requires the 16-bit data frame to be sent on the SDI pin. Table 7-11 depicts the format for a write command. Bit D15 must be set to 1 to select a write command. The D[14:9] bits contain the register address.

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The subsequent nine bits (D[8:0]) contain the data to be written to the selected register. Figure 7-31 shows a typical serial write command.

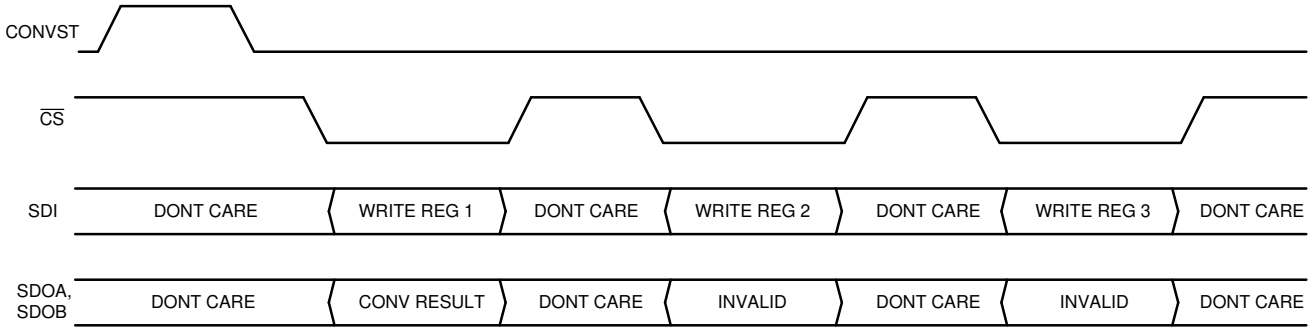

Figure 7-31. Serial Interface Register Write

Table 7-11. Write Command Message Configuration

MSB																LSB
D15	D14	D13	D12	D11	D10	D9	D8	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/ $\overline{R}$	REGADDR[5:0]						Data[8:0]									
1	Register address						Data to write									

7.5.3.3 Reading Register Data

The ADS8686S on-chip registers can be read to by using the serial interface in software mode. The register data content are shared only on the SDOA line irrespective of the serial 1-wire or serial 2-wire mode of operation. A register read is performed by issuing a register read command along with the register address followed by an additional SPI command that can be either a valid command or no operation (NOP). Table 7-12 shows the format for a read command. Bit D15 must be set to 0 to select a read command. The D[14:9] bits contain the register address. The subsequent nine bits (D[8:0]) are ignored. See the *Register Maps* section for a complete list of register addresses. Figure 7-32 shows a typical serial read command.

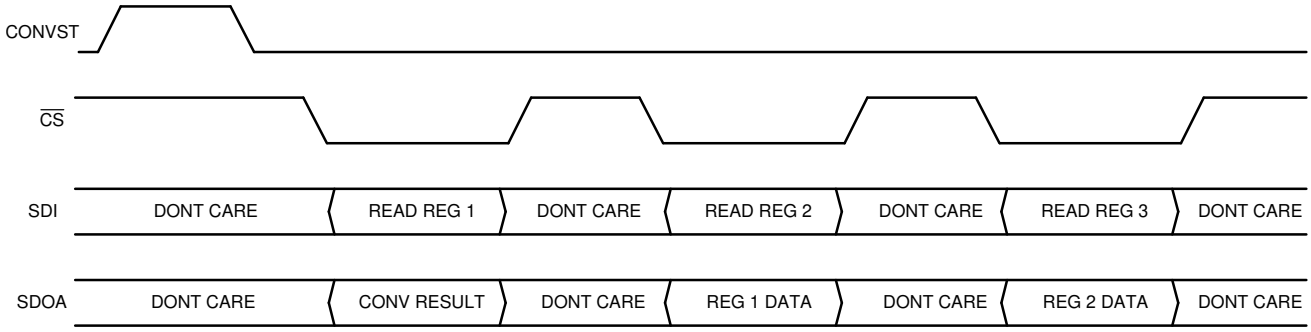

Figure 7-32. Serial Interface Register Read

Table 7-12. Read Command Message Configuration

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W/ $\overline{R}$	REGADDR[5:0]						Data[8:0]								
0	Register address						Do not care								

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7.6 Register Maps

7.6.1 Page1 Registers

Table 7-13 lists the Page1 registers. All register offset addresses not listed in Table 7-13 should be considered as reserved locations and the register contents should not be modified.

Table 7-13. Page1 Registers

ADDRESS	ACRONYM	SECTION
0x2	CONFIGURATION	Section 7.6.1.1
0x3	CHANNEL_SEL	Section 7.6.1.2
0x4	RANGE_A1	Section 7.6.1.3
0x5	RANGE_A2	Section 7.6.1.4
0x6	RANGE_B1	Section 7.6.1.5
0x7	RANGE_B2	Section 7.6.1.6
0x8	STATUS	Section 7.6.1.7
0xA	OVER_RANGE_SETTING_A	Section 7.6.1.8
0xB	OVER_RANGE_SETTING_B	Section 7.6.1.9
0xD	LPF_CONFIG	Section 7.6.1.10
0x10	Device_ID	Section 7.6.1.11
0x20	SEQ_STACK_0	Section 7.6.1.12
0x21	SEQ_STACK_1	Section 7.6.1.13
0x22	SEQ_STACK_2	Section 7.6.1.14
0x23	SEQ_STACK_3	Section 7.6.1.15
0x24	SEQ_STACK_4	Section 7.6.1.16
0x25	SEQ_STACK_5	Section 7.6.1.17
0x26	SEQ_STACK_6	Section 7.6.1.18
0x27	SEQ_STACK_7	Section 7.6.1.19
0x28	SEQ_STACK_8	Section 7.6.1.20
0x29	SEQ_STACK_9	Section 7.6.1.21
0x2A	SEQ_STACK_10	Section 7.6.1.22
0x2B	SEQ_STACK_11	Section 7.6.1.23
0x2C	SEQ_STACK_12	Section 7.6.1.24
0x2D	SEQ_STACK_13	Section 7.6.1.25
0x2E	SEQ_STACK_14	Section 7.6.1.26
0x2F	SEQ_STACK_15	Section 7.6.1.27
0x30	SEQ_STACK_16	Section 7.6.1.28
0x31	SEQ_STACK_17	Section 7.6.1.29
0x32	SEQ_STACK_18	Section 7.6.1.30
0x33	SEQ_STACK_19	Section 7.6.1.31
0x34	SEQ_STACK_20	Section 7.6.1.32
0x35	SEQ_STACK_21	Section 7.6.1.33
0x36	SEQ_STACK_22	Section 7.6.1.34
0x37	SEQ_STACK_23	Section 7.6.1.35
0x38	SEQ_STACK_24	Section 7.6.1.36
0x39	SEQ_STACK_25	Section 7.6.1.37
0x3A	SEQ_STACK_26	Section 7.6.1.38
0x3B	SEQ_STACK_27	Section 7.6.1.39
0x3C	SEQ_STACK_28	Section 7.6.1.40
0x3D	SEQ_STACK_29	Section 7.6.1.41
0x3E	SEQ_STACK_30	Section 7.6.1.42
0x3F	SEQ_STACK_31	Section 7.6.1.43

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Complex bit access types are encoded to fit into small table cells. Table 7-14 shows the codes that are used for access types in this section.

Table 7-14. Page1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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7.6.1.1 CONFIGURATION Register (Address = 0x2) [reset = 0x400]

CONFIGURATION is shown in Figure 7-33 and described in Table 7-15.

Return to the Table 7-13.

Figure 7-33. CONFIGURATION Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-10b						R-0b
7	6	5	4	3	2	1	0
SDEF	BURSTEN	SEQEN	OSR[2:0]			STATUSEN	CRCEN
R-0b	R/W-0b	R/W-0b	R/W-0b			R/W-0b	R/W-0b

Table 7-15. CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	10b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7	SDEF	R	0b	Self diagnosis error flag. 0b = Test passed. The ADS8686S has configured itself successfully after power-up. 1b = Test failed. A device reset is required.
6	BURSTEN	R/W	0b	Burst mode control. 0b = Burst mode is disabled. 1b = Burst mode is enabled.
5	SEQEN	R/W	0b	Channel sequencer control. 0b = Channel sequencer is disabled. 1b = Channel sequencer is enabled.
4-2	OSR[2:0]	R/W	0b	Oversampling ratio (OSR) configuration. 0b = OSR disabled. 1b = OSR = 2 samples. 10b = OSR = 4 samples. 11b = OSR = 8 samples. 100b = OSR = 16 samples. 101b = OSR = 32 samples. 110b = OSR = 64 samples. 111b = OSR = 128 samples.
1	STATUSEN	R/W	0b	Status register output control. 0b = Status register contents are not appended to conversion result. 1b = Status register contents are appended to conversion result.
0	CRCEN	R/W	0b	Data output CRC control. The STATUSEN and CRCEN bits have identical functionality.

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7.6.1.2 CHANNEL_SEL Register (Address = 0x3) [reset = 0x600]

CHANNEL_SEL is shown in Figure 7-34 and described in Table 7-16.

Return to the Table 7-13.

Figure 7-34. CHANNEL_SEL Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-11b						R-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-16. CHANNEL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	11b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. 0b = AIN_0B 1b = AIN_1B 10b = AIN_2B 11b = AIN_3B 100b = AIN_4B 101b = AIN_5B 110b = AIN_6B 111b = AIN_7B 1000b = AVDD 1001b = ALDO 1011b = Fixed digital code 0x5555.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. 0b = AIN_0A 1b = AIN_1A 10b = AIN_2A 11b = AIN_3A 100b = AIN_4A 101b = AIN_5A 110b = AIN_6A 111b = AIN_7A 1000b = AVDD 1001b = ALDO 1011b = Fixed digital code 0xAAAA.

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7.6.1.3 RANGE_A1 Register (Address = 0x4) [reset = 0x8FF]

RANGE_A1 is shown in Figure 7-35 and described in Table 7-17.

Return to the Table 7-13.

Figure 7-35. RANGE_A1 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-100b						R-0b
7	6	5	4	3	2	1	0
AIN_3A[1:0]		AIN_2A[1:0]		AIN_1A[1:0]		AIN_0A[1:0]	
R/W-11b		R/W-11b		R/W-11b		R/W-11b	

Table 7-17. RANGE_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7-6	AIN_3A[1:0]	R/W	11b	Channel AIN_3A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
5-4	AIN_2A[1:0]	R/W	11b	Channel AIN_2A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
3-2	AIN_1A[1:0]	R/W	11b	Channel AIN_1A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
1-0	AIN_0A[1:0]	R/W	11b	Channel AIN_0A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.

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7.6.1.4 RANGE_A2 Register (Address = 0x5) [reset = 0xAFF]

RANGE_A2 is shown in Figure 7-36 and described in Table 7-18.

Return to the Table 7-13.

Figure 7-36. RANGE_A2 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-101b						R-0b
7	6	5	4	3	2	1	0
AIN_7A[1:0]		AIN_6A[1:0]		AIN_5A[1:0]		AIN_4A[1:0]	
R/W-11b		R/W-11b		R/W-11b		R/W-11b	

Table 7-18. RANGE_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access.. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7-6	AIN_7A[1:0]	R/W	11b	Channel AIN_7A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
5-4	AIN_6A[1:0]	R/W	11b	Channel AIN_6A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
3-2	AIN_5A[1:0]	R/W	11b	Channel AIN_5A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
1-0	AIN_4A[1:0]	R/W	11b	Channel AIN_4A voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.

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7.6.1.5 RANGE_B1 Register (Address = 0x6) [reset = 0xCFF]

RANGE_B1 is shown in Figure 7-37 and described in Table 7-19.

Return to the Table 7-13.

Figure 7-37. RANGE_B1 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-110b						R-0b
7	6	5	4	3	2	1	0
AIN_3B[1:0]		AIN_2B[1:0]		AIN_1B[1:0]		AIN_0B[1:0]	
R/W-11b		R/W-11b		R/W-11b		R/W-11b	

Table 7-19. RANGE_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7-6	AIN_3B[1:0]	R/W	11b	Channel AIN_3B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
5-4	AIN_2B[1:0]	R/W	11b	Channel AIN_2B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
3-2	AIN_1B[1:0]	R/W	11b	Channel AIN_1B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
1-0	AIN_0B[1:0]	R/W	11b	Channel AIN_0B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.

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7.6.1.6 RANGE_B2 Register (Address = 0x7) [reset = 0xEFF]

RANGE_B2 is shown in Figure 7-38 and described in Table 7-20.

Return to the Table 7-13.

Figure 7-38. RANGE_B2 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-111b						R-0b
7	6	5	4	3	2	1	0
AIN_7B[1:0]		AIN_6B[1:0]		AIN_5B[1:0]		AIN_4B[1:0]	
R/W-11b		R/W-11b		R/W-11b		R/W-11b	

Table 7-20. RANGE_B2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7-6	AIN_7B[1:0]	R/W	11b	Channel AIN_7B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
5-4	AIN_6B[1:0]	R/W	11b	Channel AIN_6B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = input Range = ± 10 V.
3-2	AIN_5B[1:0]	R/W	11b	Channel AIN_5B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = Input Range = ± 10 V.
1-0	AIN_4B[1:0]	R/W	11b	Channel AIN_4B voltage range selection. 0b = Input Range = ± 10 V. 1b = Input Range = ± 2.5 V. 10b = Input Range = ± 5 V. 11b = input Range = ± 10 V.

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7.6.1.7 STATUS Register (Address = 0x8) [reset = 0x0]

STATUS is shown in Figure 7-39 and described in Table 7-21.

Return to the Table 7-13.

Figure 7-39. STATUS Register

15	14	13	12	11	10	9	8
CHSEL_A_ID[3:0]				CHSEL_B_ID[3:0]			
R-0b				R-0b			
7	6	5	4	3	2	1	0
CRC[7:0]							
R-0b							

Table 7-21. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	CHSEL_A_ID[3:0]	R	0b	Channel index for the last converted channel using ADC A. Refer to register 0x03 CHSEL_A description to decode channel index.
11-8	CHSEL_B_ID[3:0]	R	0b	Channel index for the last converted channel using ADC B. Refer to register 0x03 CHSEL_B description to decode channel index.
7-0	CRC[7:0]	R	0b	8-bit CRC computation result. Refer to CRC section for further details.

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7.6.1.8 OVER_RANGE_SETTING_A Register (Address = 0xA) [reset = 0x1400]

OVER_RANGE_SETTING_A is shown in Figure 7-40 and described in Table 7-22.

Return to the Table 7-13.

Figure 7-40. OVER_RANGE_SETTING_A Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-1010b						R-0b
7	6	5	4	3	2	1	0
AIN_7A_OVER_RANGE	AIN_6A_OVER_RANGE	AIN_5A_OVER_RANGE	AIN_4A_OVER_RANGE	AIN_3A_OVER_RANGE	AIN_2A_OVER_RANGE	AIN_1A_OVER_RANGE	AIN_0A_OVER_RANGE
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-22. OVER_RANGE_SETTING_A Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	1010b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7	AIN_7A_OVER_RANGE	R/W	0b	AIN_7A over range control. 0b = Channel AIN_7A range as programmed in register 0x05. 1b = Enable 20% Overrange for Channel AIN_7A range set as programmed in register 0x05.
6	AIN_6A_OVER_RANGE	R/W	0b	AIN_6A over range control. 0b = Channel AIN_6A range as programmed in register 0x05. 1b = Enable 20% Overrange for Channel AIN_6A range set as programmed in register 0x05.
5	AIN_5A_OVER_RANGE	R/W	0b	AIN_5A over range control. 0b = Channel AIN_5A range as programmed in register 0x05. 1b = Enable 20% Overrange for Channel AIN_5A range set as programmed in register 0x05.
4	AIN_4A_OVER_RANGE	R/W	0b	AIN_4A over range control. 0b = Channel AIN_4A range as programmed in register 0x05. 1b = Enable 20% Overrange for Channel AIN_4A range set as programmed in register 0x05.
3	AIN_3A_OVER_RANGE	R/W	0b	AIN_3A over range control. 0b = Channel AIN_3A range as programmed in register 0x04. 1b = Enable 20% Overrange for Channel AIN_3A range set as programmed in register 0x04.
2	AIN_2A_OVER_RANGE	R/W	0b	AIN_2A over range control. 0b = Channel AIN_2A range as programmed in register 0x04. 1b = Enable 20% Overrange for Channel AIN_2A range set as programmed in register 0x04.
1	AIN_1A_OVER_RANGE	R/W	0b	AIN_1A over range control 0b = Channel AIN_1A range as programmed in register 0x04 1b = Enable 20% Overrange for Channel AIN_1A range set as programmed in register 0x04

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Table 7-22. OVER_RANGE_SETTING_A Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AIN_0A_OVER_RANGE	R/W	0b	AIN_0A over range control. 0b = Channel AIN_0A range as programmed in register 0x04. 1b = Enable 20% Overrange for Channel AIN_0A range set as programmed in register 0x04.

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7.6.1.9 OVER_RANGE_SETTING_B Register (Address = 0xB) [reset = 0x1600]

OVER_RANGE_SETTING_B is shown in Figure 7-41 and described in Table 7-23.

Return to the Table 7-13.

Figure 7-41. OVER_RANGE_SETTING_B Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-1011b						R-0b
7	6	5	4	3	2	1	0
AIN_7B_OVER_RANGE	AIN_6B_OVER_RANGE	AIN_5B_OVER_RANGE	AIN_4B_OVER_RANGE	AIN_3B_OVER_RANGE	AIN_2B_OVER_RANGE	AIN_1B_OVER_RANGE	AIN_0B_OVER_RANGE
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-23. OVER_RANGE_SETTING_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	1011b	Selects this register for read / write operation. Write register address to access this register.
8	RESERVED	R	0b	Reserved. Reads return 0b.
7	AIN_7B_OVER_RANGE	R/W	0b	AIN_7B over range control. 0b = Channel AIN_7B range as programmed in register 0x07. 1b = Enable 20% Overrange for Channel AIN_7B range set as programmed in register 0x07.
6	AIN_6B_OVER_RANGE	R/W	0b	AIN_6B over range control. 0b = Channel AIN_6B range as programmed in register 0x07. 1b = Enable 20% Overrange for Channel AIN_6B range set as programmed in register 0x07.
5	AIN_5B_OVER_RANGE	R/W	0b	AIN_5B over range control. 0b = Channel AIN_5B range as programmed in register 0x07. 1b = Enable 20% Overrange for Channel AIN_5B range set as programmed in register 0x07.
4	AIN_4B_OVER_RANGE	R/W	0b	AIN_4B over range control. 0b = Channel AIN_4B range as programmed in register 0x07. 1b = Enable 20% Overrange for Channel AIN_4B range set as programmed in register 0x07.
3	AIN_3B_OVER_RANGE	R/W	0b	AIN_3B over range control 0b = Channel AIN_3B range as programmed in register 0x06 1b = Enable 20% Overrange for Channel AIN_3B range set as programmed in register 0x06
2	AIN_2B_OVER_RANGE	R/W	0b	AIN_2B over range control. 0b = Channel AIN_2B range as programmed in register 0x06. 1b = Enable 20% Overrange for Channel AIN_2B range set as programmed in register 0x06.
1	AIN_1B_OVER_RANGE	R/W	0b	AIN_1B over range control. 0b = Channel AIN_1B range as programmed in register 0x06. 1b = Enable 20% Overrange for Channel AIN_1B range set as programmed in register 0x06.

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Table 7-23. OVER_RANGE_SETTING_B Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AIN_0B_OVER_RANGE	R/W	0b	AIN_0B over range control. 0b = Channel AIN_0B range as programmed in register 0x06. 1b = Enable 20% Overrange for Channel AIN_0B range set as programmed in register 0x06.

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7.6.1.10 LPF_CONFIG Register (Address = 0xD) [reset = 0x1A00]

LPF_CONFIG is shown in Figure 7-42 and described in Table 7-24.

Return to the Table 7-13.

Figure 7-42. LPF_CONFIG Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-1101b						R-0b
7	6	5	4	3	2	1	0
RESERVED						LPF_CONFIG[1:0]	
R-0b						R/W-0b	

Table 7-24. LPF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	1101b	Selects this register for read / write operation. Write register address to access this register.
8-2	RESERVED	R	0b	Reserved. Reads return 0b.
1-0	LPF_CONFIG[1:0]	R/W	0b	Analog low pass filter configuration control. The setting is applied to input channels. 0b = LPF cutoff frequency = 39 kHz 1b = LPF cutoff frequency = 15 kHz 10b = LPF cutoff frequency = 376 kHz

7.6.1.11 Device_ID Register (Address = 0x10) [reset = 0x2002]

Device_ID is shown in Figure 7-43 and described in Table 7-25.

Return to the Table 7-13.

Figure 7-43. Device_ID Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						RESERVED
R/W-0b	R/W-10000b						R-0b
7	6	5	4	3	2	1	0
RESERVED						DEVICE_ID[1:0]	
R-0b						R-10b	

Table 7-25. Device_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	10000b	Selects this register for read / write operation. Write register address to access this register.
8-2	RESERVED	R	0b	
1-0	DEVICE_ID[1:0]	R	10b	Device identification register.

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7.6.1.12 SEQ_STACK_0 Register (Address = 0x20) [reset = 0x4000]

SEQ_STACK_0 is shown in Figure 7-44 and described in Table 7-26.

Return to the Table 7-13.

Figure 7-44. SEQ_STACK_0 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100000b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-26. SEQ_STACK_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100000b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.13 SEQ_STACK_1 Register (Address = 0x21) [reset = 0x4211]

SEQ_STACK_1 is shown in Figure 7-45 and described in Table 7-27.

Return to the Table 7-13.

Figure 7-45. SEQ_STACK_1 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100001b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-1b				R/W-1b			

Table 7-27. SEQ_STACK_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100001b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	1b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-27. SEQ_STACK_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	1b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.14 SEQ_STACK_2 Register (Address = 0x22) [reset = 0x4422]

SEQ_STACK_2 is shown in Figure 7-46 and described in Table 7-28.

Return to the Table 7-13.

Figure 7-46. SEQ_STACK_2 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100010b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-10b				R/W-10b			

Table 7-28. SEQ_STACK_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100010b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	10b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	10b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.15 SEQ_STACK_3 Register (Address = 0x23) [reset = 0x4633]

SEQ_STACK_3 is shown in Figure 7-47 and described in Table 7-29.

Return to the Table 7-13.

Figure 7-47. SEQ_STACK_3 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100011b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-11b				R/W-11b			

Table 7-29. SEQ_STACK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100011b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	11b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-29. SEQ_STACK_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	11b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.16 SEQ_STACK_4 Register (Address = 0x24) [reset = 0x4844]

SEQ_STACK_4 is shown in Figure 7-48 and described in Table 7-30.

Return to the Table 7-13.

Figure 7-48. SEQ_STACK_4 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100100b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-100b				R/W-100b			

Table 7-30. SEQ_STACK_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100100b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	100b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	100b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.17 SEQ_STACK_5 Register (Address = 0x25) [reset = 0x4A55]

SEQ_STACK_5 is shown in Figure 7-49 and described in Table 7-31.

Return to the Table 7-13.

Figure 7-49. SEQ_STACK_5 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100101b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-101b				R/W-101b			

Table 7-31. SEQ_STACK_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100101b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	101b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-31. SEQ_STACK_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	101b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.18 SEQ_STACK_6 Register (Address = 0x26) [reset = 0x4C66]

SEQ_STACK_6 is shown in Figure 7-50 and described in Table 7-32.

Return to the Table 7-13.

Figure 7-50. SEQ_STACK_6 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100110b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-110b				R/W-110b			

Table 7-32. SEQ_STACK_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100110b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	110b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	110b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.19 SEQ_STACK_7 Register (Address = 0x27) [reset = 0x4F77]

SEQ_STACK_7 is shown in Figure 7-51 and described in Table 7-33.

Return to the Table 7-13.

Figure 7-51. SEQ_STACK_7 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-100111b						R/W-1b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-111b				R/W-111b			

Table 7-33. SEQ_STACK_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	100111b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	1b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	111b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-33. SEQ_STACK_7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	111b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.20 SEQ_STACK_8 Register (Address = 0x28) [reset = 0x5000]

SEQ_STACK_8 is shown in Figure 7-52 and described in Table 7-34.

Return to the Table 7-13.

Figure 7-52. SEQ_STACK_8 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101000b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-34. SEQ_STACK_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101000b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.21 SEQ_STACK_9 Register (Address = 0x29) [reset = 0x5200]

SEQ_STACK_9 is shown in Figure 7-53 and described in Table 7-35.

Return to the Table 7-13.

Figure 7-53. SEQ_STACK_9 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101001b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-35. SEQ_STACK_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101001b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-35. SEQ_STACK_9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.22 SEQ_STACK_10 Register (Address = 0x2A) [reset = 0x5400]

SEQ_STACK_10 is shown in Figure 7-54 and described in Table 7-36.

Return to the Table 7-13.

Figure 7-54. SEQ_STACK_10 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101010b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-36. SEQ_STACK_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101010b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.23 SEQ_STACK_11 Register (Address = 0x2B) [reset = 0x5600]

SEQ_STACK_11 is shown in Figure 7-55 and described in Table 7-37.

Return to the Table 7-13.

Figure 7-55. SEQ_STACK_11 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101011b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-37. SEQ_STACK_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101011b	Selects this register for read / write operation Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-37. SEQ_STACK_11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.24 SEQ_STACK_12 Register (Address = 0x2C) [reset = 0x5800]

SEQ_STACK_12 is shown in Figure 7-56 and described in Table 7-38.

Return to the Table 7-13.

Figure 7-56. SEQ_STACK_12 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101100b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-38. SEQ_STACK_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101100b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.25 SEQ_STACK_13 Register (Address = 0x2D) [reset = 0x5A00]

SEQ_STACK_13 is shown in Figure 7-57 and described in Table 7-39.

Return to the Table 7-13.

Figure 7-57. SEQ_STACK_13 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101101b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-39. SEQ_STACK_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101101b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-39. SEQ_STACK_13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.26 SEQ_STACK_14 Register (Address = 0x2E) [reset = 0x5C00]

SEQ_STACK_14 is shown in Figure 7-58 and described in Table 7-40.

Return to the Table 7-13.

Figure 7-58. SEQ_STACK_14 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101110b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-40. SEQ_STACK_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101110b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.27 SEQ_STACK_15 Register (Address = 0x2F) [reset = 0x5E00]

SEQ_STACK_15 is shown in Figure 7-59 and described in Table 7-41.

Return to the Table 7-13.

Figure 7-59. SEQ_STACK_15 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-101111b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-41. SEQ_STACK_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	101111b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-41. SEQ_STACK_15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.28 SEQ_STACK_16 Register (Address = 0x30) [reset = 0x6000]

SEQ_STACK_16 is shown in Figure 7-60 and described in Table 7-42.

Return to the Table 7-13.

Figure 7-60. SEQ_STACK_16 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110000b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-42. SEQ_STACK_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110000b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.29 SEQ_STACK_17 Register (Address = 0x31) [reset = 0x6200]

SEQ_STACK_17 is shown in Figure 7-61 and described in Table 7-43.

Return to the Table 7-13.

Figure 7-61. SEQ_STACK_17 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110001b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-43. SEQ_STACK_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110001b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-43. SEQ_STACK_17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.30 SEQ_STACK_18 Register (Address = 0x32) [reset = 0x6400]

SEQ_STACK_18 is shown in Figure 7-62 and described in Table 7-44.

Return to the Table 7-13.

Figure 7-62. SEQ_STACK_18 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110010b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-44. SEQ_STACK_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110010b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.31 SEQ_STACK_19 Register (Address = 0x33) [reset = 0x6600]

SEQ_STACK_19 is shown in Figure 7-63 and described in Table 7-45.

Return to the Table 7-13.

Figure 7-63. SEQ_STACK_19 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110011b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-45. SEQ_STACK_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.

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Table 7-45. SEQ_STACK_19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-9	REGADDR[5:0]	R/W	110011b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.32 SEQ_STACK_20 Register (Address = 0x34) [reset = 0x6800]

SEQ_STACK_20 is shown in Figure 7-64 and described in Table 7-46.

Return to the Table 7-13.

Figure 7-64. SEQ_STACK_20 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110100b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-46. SEQ_STACK_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110100b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.33 SEQ_STACK_21 Register (Address = 0x35) [reset = 0x6A00]

SEQ_STACK_21 is shown in Figure 7-65 and described in Table 7-47.

Return to the Table 7-13.

Figure 7-65. SEQ_STACK_21 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110101b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

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Figure 7-65. SEQ_STACK_21 Register (continued)

Table 7-47. SEQ_STACK_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110101b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.34 SEQ_STACK_22 Register (Address = 0x36) [reset = 0x6C00]

SEQ_STACK_22 is shown in Figure 7-66 and described in Table 7-48.

Return to the Table 7-13.

Figure 7-66. SEQ_STACK_22 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-110110b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-48. SEQ_STACK_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110110b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.35 SEQ_STACK_23 Register (Address = 0x37) [reset = 0x6E00]

SEQ_STACK_23 is shown in Figure 7-67 and described in Table 7-49.

Return to the Table 7-13.

Figure 7-67. SEQ_STACK_23 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN

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Figure 7-67. SEQ_STACK_23 Register (continued)

R/W-0b	R/W-110111b	R/W-0b

7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-49. SEQ_STACK_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	110111b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.36 SEQ_STACK_24 Register (Address = 0x38) [reset = 0x7000]

SEQ_STACK_24 is shown in Figure 7-68 and described in Table 7-50.

Return to the Table 7-13.

Figure 7-68. SEQ_STACK_24 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111000b						R/W-0b

7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-50. SEQ_STACK_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111000b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.37 SEQ_STACK_25 Register (Address = 0x39) [reset = 0x7200]

SEQ_STACK_25 is shown in Figure 7-69 and described in Table 7-51.

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Return to the Table 7-13.

Figure 7-69. SEQ_STACK_25 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111001b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-51. SEQ_STACK_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111001b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.38 SEQ_STACK_26 Register (Address = 0x3A) [reset = 0x7400]

SEQ_STACK_26 is shown in Figure 7-70 and described in Table 7-52.

Return to the Table 7-13.

Figure 7-70. SEQ_STACK_26 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111010b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-52. SEQ_STACK_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111010b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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7.6.1.39 SEQ_STACK_27 Register (Address = 0x3B) [reset = 0x7600]

SEQ_STACK_27 is shown in Figure 7-71 and described in Table 7-53.

Return to the Table 7-13.

Figure 7-71. SEQ_STACK_27 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111011b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-53. SEQ_STACK_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111011b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.40 SEQ_STACK_28 Register (Address = 0x3C) [reset = 0x7800]

SEQ_STACK_28 is shown in Figure 7-72 and described in Table 7-54.

Return to the Table 7-13.

Figure 7-72. SEQ_STACK_28 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111100b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-54. SEQ_STACK_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111100b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.

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Table 7-54. SEQ_STACK_28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.41 SEQ_STACK_29 Register (Address = 0x3D) [reset = 0x7A00]

SEQ_STACK_29 is shown in Figure 7-73 and described in Table 7-55.

Return to the Table 7-13.

Figure 7-73. SEQ_STACK_29 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111101b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-55. SEQ_STACK_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111101b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

7.6.1.42 SEQ_STACK_30 Register (Address = 0x3E) [reset = 0x7C00]

SEQ_STACK_30 is shown in Figure 7-74 and described in Table 7-56.

Return to the Table 7-13.

Figure 7-74. SEQ_STACK_30 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111110b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-56. SEQ_STACK_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.

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Table 7-56. SEQ_STACK_30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-9	REGADDR[5:0]	R/W	111110b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting

7.6.1.43 SEQ_STACK_31 Register (Address = 0x3F) [reset = 0x7E00]

SEQ_STACK_31 is shown in Figure 7-75 and described in Table 7-57.

Return to the Table 7-13.

Figure 7-75. SEQ_STACK_31 Register

15	14	13	12	11	10	9	8
W/ $\overline{R}$	REGADDR[5:0]						SSREN
R/W-0b	R/W-111111b						R/W-0b
7	6	5	4	3	2	1	0
CHSEL_B[3:0]				CHSEL_A[3:0]			
R/W-0b				R/W-0b			

Table 7-57. SEQ_STACK_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	W/ $\overline{R}$	R/W	0b	Register read write access. 0b = Selects the register for read access. 1b = Selects the register for write access.
14-9	REGADDR[5:0]	R/W	111111b	Selects this register for read / write operation. Write register address to access this register.
8	SSREN	R/W	0b	Sequence stack return control. 0b = Move to next stack register after ongoing conversion complete. 1b = Move to first stack register after ongoing conversion complete.
7-4	CHSEL_B[3:0]	R/W	0b	Channel selection control for ADC B. Refer to register 0x03 CHSEL_B field description for individual selection setting.
3-0	CHSEL_A[3:0]	R/W	0b	Channel selection control for ADC A. Refer to register 0x03 CHSEL_A field description for individual selection setting.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADS8686S is a fully integrated data acquisition system (DAQ) based on a 16-bit, 8 x 2 channel successive approximation (SAR) analog-to-digital converter (ADC) with dual simultaneous sampling. The dual ADC architecture enables the ADS8686S to sample two analog channels simultaneously. This feature is important for voltage and current measurement in power automation applications. The device includes an integrated analog front-end for each input channel and an integrated voltage reference with a precision reference buffer. As such, this device does not require any additional active circuits for driving the reference analog input pins of the ADC. The ADS8686S also offers features such as higher throughput, burst mode, and a flexible channel sequencer, making the device an excellent choice for protection and measurement applications in power automation systems.

8.2 Typical Applications

8.2.1 8x2 Channel Data Acquisition System (DAQ) for Power Automation

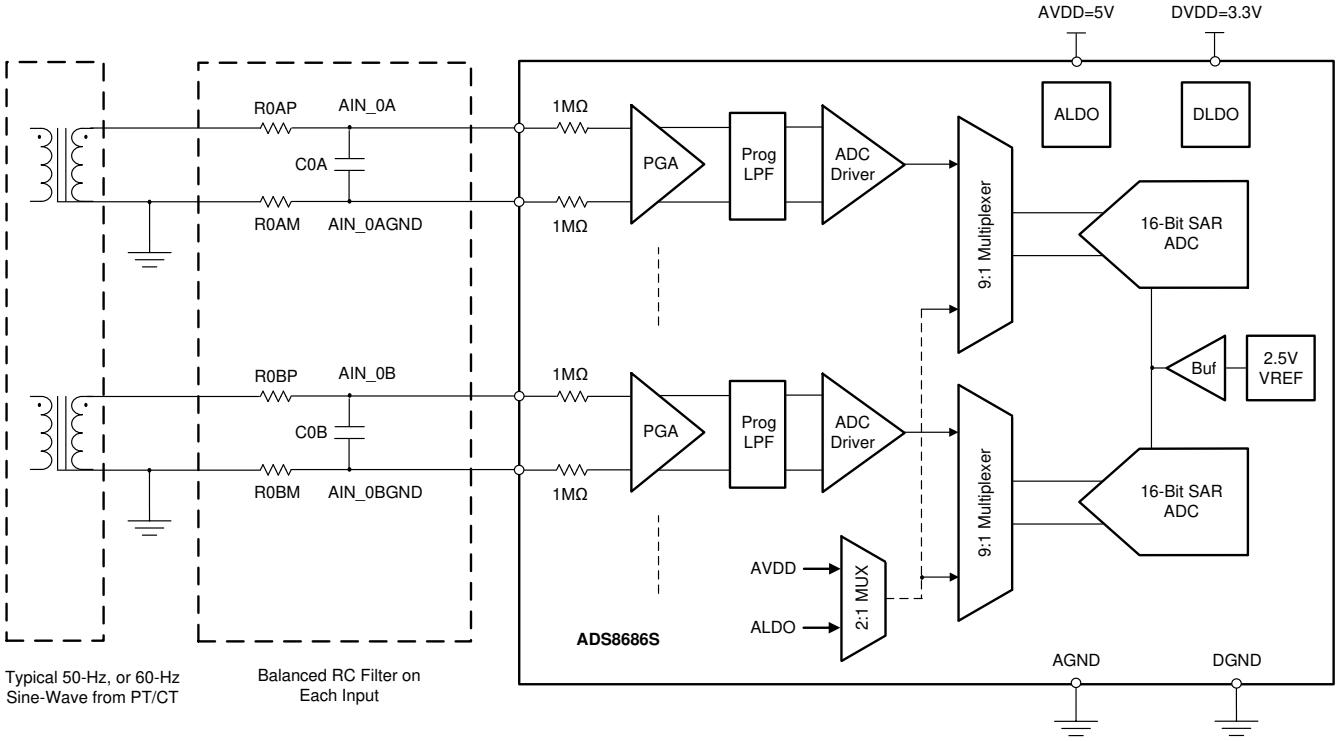

Figure 8-1. DAQ for Power Automation Using the ADS8686S

The application example in Figure 8-1 shows the measurement of electrical variables in a power system. The key electrical parameters include amplitude, frequency, and phase measurement of the voltage and current on the power lines. These parameters are important to enable metrology in the power automation system to perform harmonic analysis, power factor calculation, power quality assessment, and so forth.

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8.2.1.1 Design Requirements

The key design requirements specify the:

- Output range of the potential transformers
- Output range of the current transformers
- Number of harmonics to be acquired
- Number of samples per cycle
- Fundamental frequency of the power system
- Input impedance required from the analog front-end for each channel
- Type of signal conditioning required from the analog front-end for each channel

8.2.1.2 Detailed Design Procedure

For the ADS8686S, each channel incorporates an analog front-end composed of a programmable gain amplifier (PGA), programmable analog low-pass filter (LPF), and an ADC input driver. The analog input for each channel presents a constant resistive impedance of 1 MΩ (1.2 MΩ for the 20% overrange setting) independent of the ADC sampling frequency. The high input impedance of the analog front-end circuit allows direct connection to potential transformers (PT) and current transformers (CT). The ADC inputs can support up to ±10-V, ±5-V, and ±2.5-V bipolar inputs with a 20% overrange option for each input and the integrated signal conditioning eliminates the need for external amplifiers or ADC driver circuits.

The PT and CT used in the power system, as illustrated in Figure 8-1, usually have a ±10-V or ±5-V output range. Although the PT and CT provide isolation from the power system, a series resistor (R_{XAP} or$_{RXBP}$) must be placed on the analog input channels. The series resistor helps limit the input current to ±10 mA to protect the ADC.

An LPF is usually used on each analog input channel to eliminate high-frequency noise pickup and minimize aliasing. Figure 8-2 shows a circuit example of the recommended configuration for an input RC filter. A balanced RC filter configuration matches the external source resistance on the positive path (R_{XAP} or R_{XBP}) with an equal resistance on the negative path (R_{XAM} or R_{XBM}). Matching the source impedance in the positive and negative path allows for better common-mode noise rejection and helps in maintaining the dc accuracy of the system by canceling any additional gain error contributed by the external series resistance.

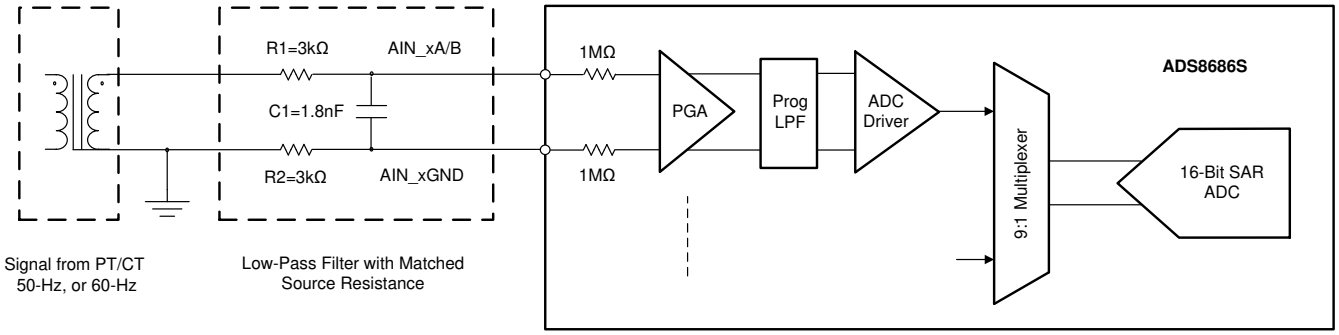

Figure 8-2. Input RC Low-Pass Filter

The primary goal of the data acquisition system illustrated in Figure 8-1 is to measure up to 50 harmonics in a 60-Hz power network. Thus, the analog front-end must have sufficient bandwidth, as shown in Equation 3, to detect signals up to 3060 Hz.

$$f_{min} = (50 + 1) \times 60Hz = 3060Hz \quad (3)$$

The pass band of the low-pass filter configuration shown in Figure 8-2 is determined by the –3-dB frequency, calculated according to Equation 4.

$$f_{-3dB} = \frac{1}{2\pi \times (R1 + R2) \times C1} = \frac{1}{2\pi \times (3k\Omega + 3k\Omega) \times 1.8nF} = 14.7kHz \quad (4)$$

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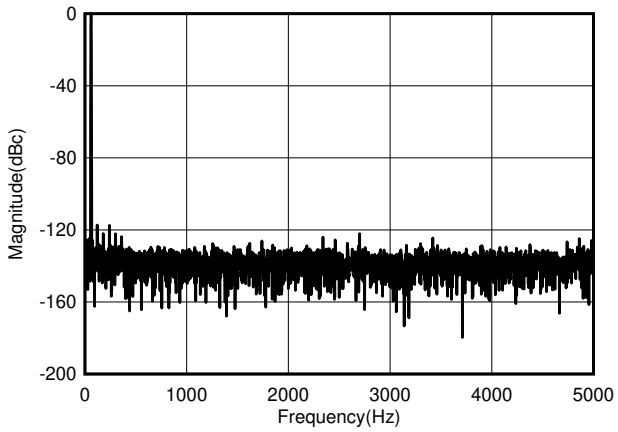
The value of C1 is selected as 1.8 nF, a standard capacitance value available in C0G type and 0603-size surface-mount components. In combination with the R1 and R2 resistors, this LPF provides sufficient bandwidth to accommodate the required 50 harmonics for the input signal of 60 Hz.

8.2.1.3 Application Curve

Figure 8-3 shows the frequency spectrum of the data acquired by the ADS8686S for a sinusoidal, ±10-V input at 60-Hz frequency.

The ac performance parameters measured by this design are:

- SNR = 89.0 dB; SINAD = 89.0 dB
- THD = –112.4 dB; SFDR = 117.2 dB



f_{IN} = 60 Hz, f_S = 1 MSPS

Figure 8-3. Captured Frequency Spectrum

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8.2.2 Input Protection for Electrical Overstress

For applications that require protection against overvoltage or fast transient events beyond the specified absolute maximum ratings of the device, an external protection clamp circuit using transient voltage suppressors (TVS) or a Schottky diode is recommended. Figure 8-4 shows the TVS (DxA or DxB) protection on each channel. A proper TVS diode must be selected to protect the specific ADC device. A standoff voltage between 10 V to 15 V of the bidirectional TVS diode can be used to protect the ADS8686S if the ADCs input range is configured as ±10-V. The breakdown voltage of the selected TVS diode must be less than the specified absolute maximum input voltage ratings of the device, which is ±15 V on the ADS8686S.

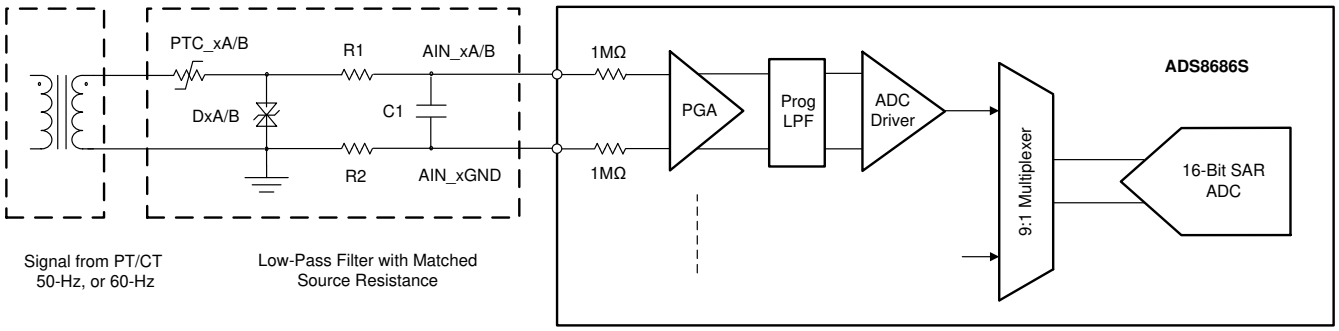

Figure 8-4. Input Protection for Electrical Overstress

The positive temperature coefficient (PTC) fuses (PTC_xA or PTC_xB) are placed in series to protect the circuit by changing from a low-resistance to a high-resistance state in response to an overcurrent during fault condition. This PTC fuse behavior is useful for the input protection circuit because the series resistance is low in the normal un-tripped state and keeps the distortion relatively low. The PTC offers high series resistance in the tripped state to limit the fault current and power dissipation. Along with the TVS diode, the PTC clamps the overdriven signal. See the *Electrical Overstress on Data Converters* video series for a theoretical explanation of overstress on data converters.

Figure 8-5 shows a high-voltage continuous input overvoltage sinusoidal wave signal (60 V_{PP}) on the left side and a clamped signal on the right side with a PTC fuse (PTS120660V005) from Eaton Electronics™ and a bidirectional TVS diode (SMBJ12CA) from ON Semiconductor® on the ADS8686SEVM. The external bidirectional TVS diode is turned on and the overvoltage sinusoidal wave signal is clamped to a ±14.5 V_{PEAK}, which is less than the ±15-V absolute maximum input voltage ratings of the ADS8686S device, so the ADC device is protected from the overvoltage input signal. For detailed information about input protection to the ADS8686S, see the *Input Protection for High-Voltage ADC Circuit With TVS Diode and PTC-Fuse* application book.

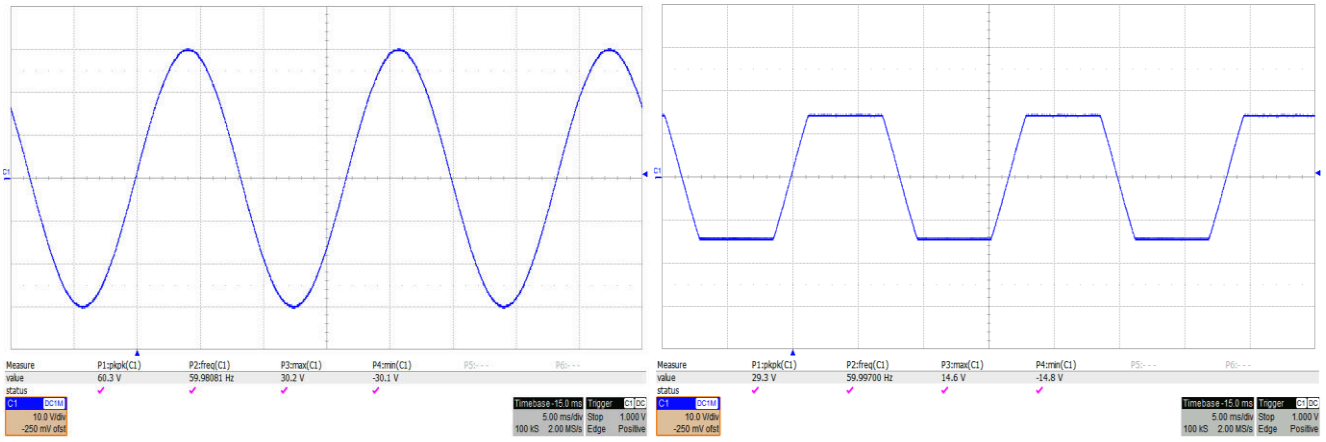

Figure 8-5. Input Protection Response Using a PTC Diode, a TVS Diode, and the ADS8686S

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9 Power Supply Recommendations

9.1 Power Supplies

The ADS8686S has two independent power supplies, AVDD and DVDD. The AVDD supply provides power to the ADC and the analog circuits. The DVDD supply provides power to the digital interface. The AVDD and DVDD supplies can be set independently to voltages within the permissible range. Decouple both the AVDD and the DVDD supply with a 10-µF capacitor in parallel with a 100-nF capacitor.

Figure 9-1 shows the effect of using the recommended decoupling capacitor on the power-supply rejection ratio (PSRR) performance of the device.

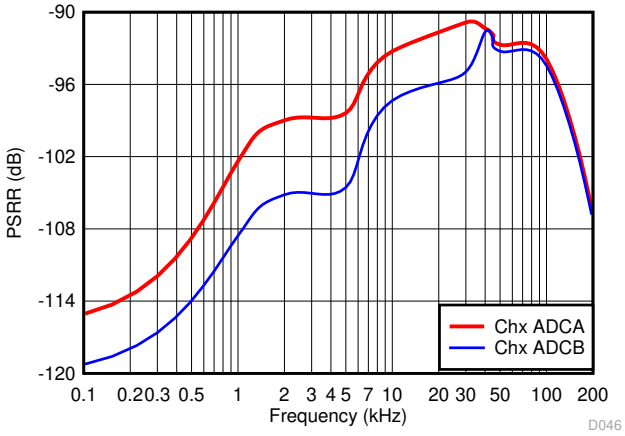

Figure 9-1. PSRR Across Frequency

The ADS8686S generates the additional required supplies using the internal LDO regulators. Decouple the analog LDO (ALDO) with a 10-µF capacitor between the REGCAP and REGGND pins. Decouple the digital LDO (DLDO) with a 10-µF capacitor between the REGCAPD and REGGNDD pins.

The ADS8686S is robust to power-supply sequencing (that is, the AVDD and DVDD can be powered up in random order). The recommended sequence is to power up DVDD first, followed by AVDD. Hold $\overline{\text{RESET}}$ low until both supplies are stabilized.

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10 Layout

10.1 Layout Guidelines

Figure 10-1 and Figure 10-2 illustrate a printed circuit board (PCB) layout example for the ADS8686S.

- Keep the analog signal away from the digital lines. This layout keeps the analog input and reference signals away from digital noise.
- Use a single common ground plane. For designs requiring split analog and digital ground planes, the analog and digital ground planes must be at the same potential joined together in close proximity to the device.
- Power sources to the ADS8686S must be clean and well-bypassed. As a result of dynamic currents during conversion, each AVDD pin must have a decoupling capacitor to keep the supply voltage stable. Use wide traces or a dedicated analog supply plane to minimize trace inductance and reduce glitches. Use a 10-µF and 0.1-µF ceramic capacitor in close proximity to each analog (AVDD) supply pins (pins 6, 15, 30, and 71) and the digital supply (pin 49).
- Connect the AVDD supply pins (pins 71 and 30) to bypass capacitors on both the top and bottom layers with an isolated via. Use a separate via to connect the bypass capacitors to the AVDD plane.
- Decouple the REFCAP pin (pin 31) with a 10-µF, 0805-size capacitor placed in close proximity to the device pin. Avoid placing vias between the REFCAP pin and the decoupling capacitor.
- Decouple the REGCAP pin (pin 70) with a 10-µF and a 0.1-µF ceramic capacitor placed in close proximity to the device pin. Avoid placing vias between the REGCAP pin and the decoupling capacitor.
- Decouple the REGCAPD pin (pin 52) with a 10-µF and a 0.1-µF ceramic capacitor placed in close proximity to the device pin. Avoid placing vias between the REGCAPD pin and the decoupling capacitor.
- If the internal reference of the device is used, decouple the REFIO pin to REFIO_GND with a 10-µF, X7R-grade, 0603-size ceramic capacitor. Place the capacitor on the top layer, close to the device pin. Avoid placing vias between the REFIO pin and the decoupling capacitor.
- Connect all ground pins (AGND) to the ground plane using short, low-impedance paths and independent vias to the ground plane.

10.2 Layout Examples

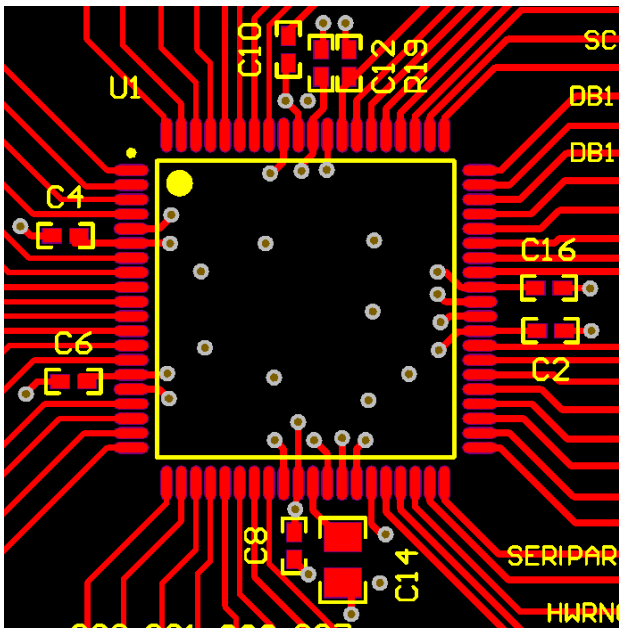

Figure 10-1. Top Layer Layout

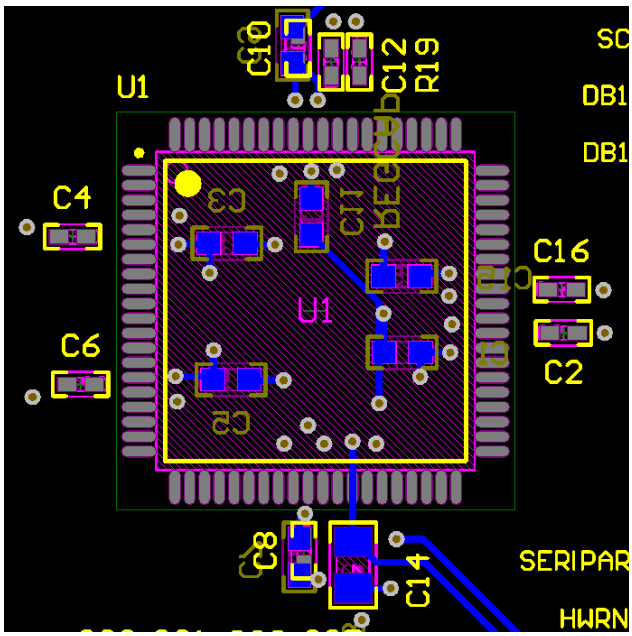

Figure 10-2. Bottom Layer Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For development support see the following:

Texas Instruments, *Electrical Overstress on Data Converters* video series

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

-
- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *Input Protection for High-Voltage ADC Circuit With TVS Diode and PTC-Fuse* application book

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8686SIPZA	Active	Production	LQFP (PZA) | 80	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8686S
ADS8686SIPZA.A	Active	Production	LQFP (PZA) | 80	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8686S
ADS8686SIPZAG4	Active	Production	LQFP (PZA) | 80	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8686S
ADS8686SIPZAG4.A	Active	Production	LQFP (PZA) | 80	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8686S
ADS8686SIPZAR	Active	Production	LQFP (PZA) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8686S
ADS8686SIPZAR.A	Active	Production	LQFP (PZA) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8686S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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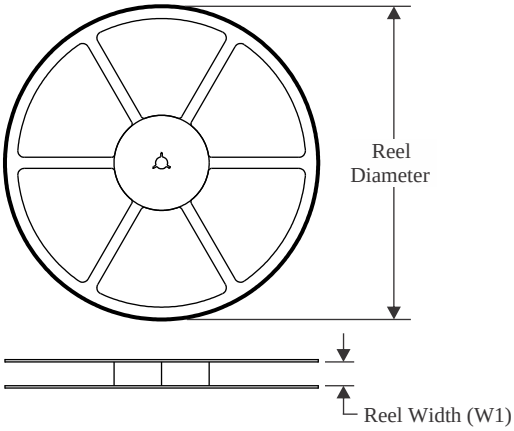
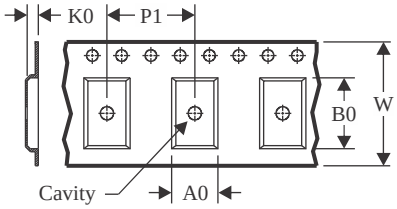
TAPE AND REEL INFORMATION

REEL DIMENSIONS

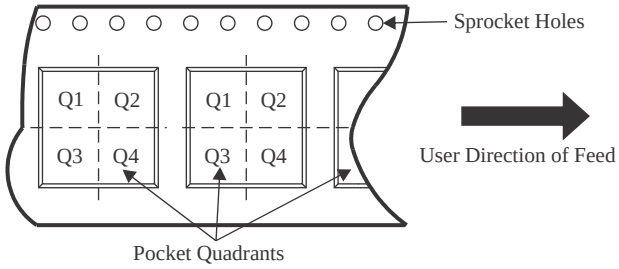


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

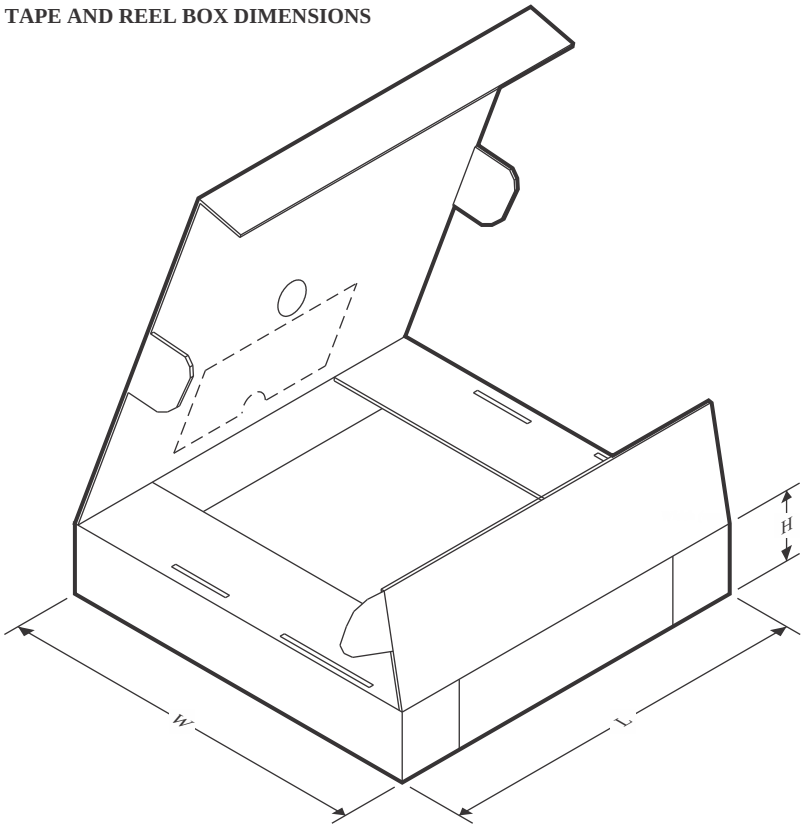
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8686SIPZAR	LQFP	PZA	80	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

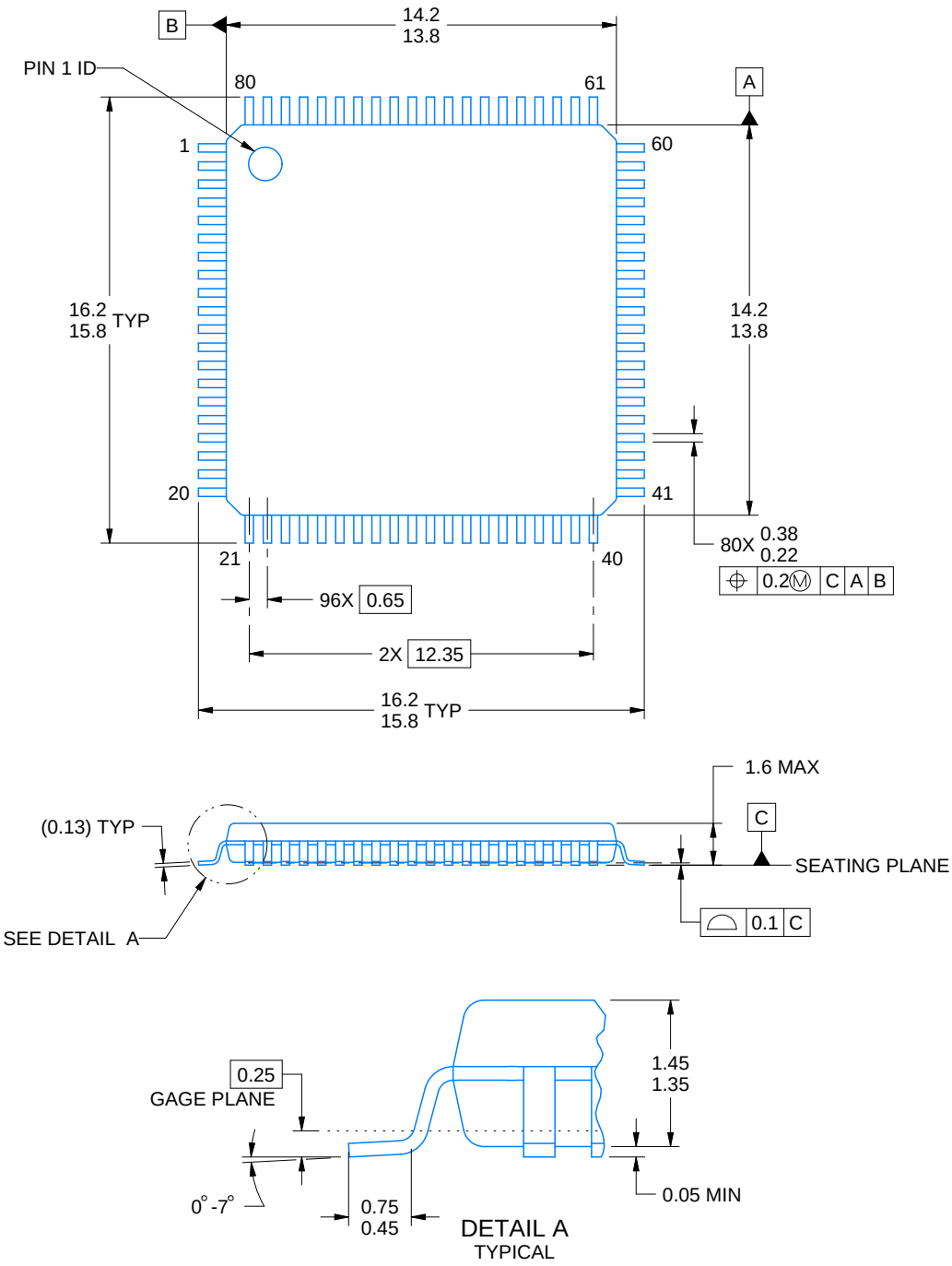
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8686SIPZAR	LQFP	PZA	80	1000	350.0	350.0	43.0

PACKAGE OUTLINE

PZA0080A

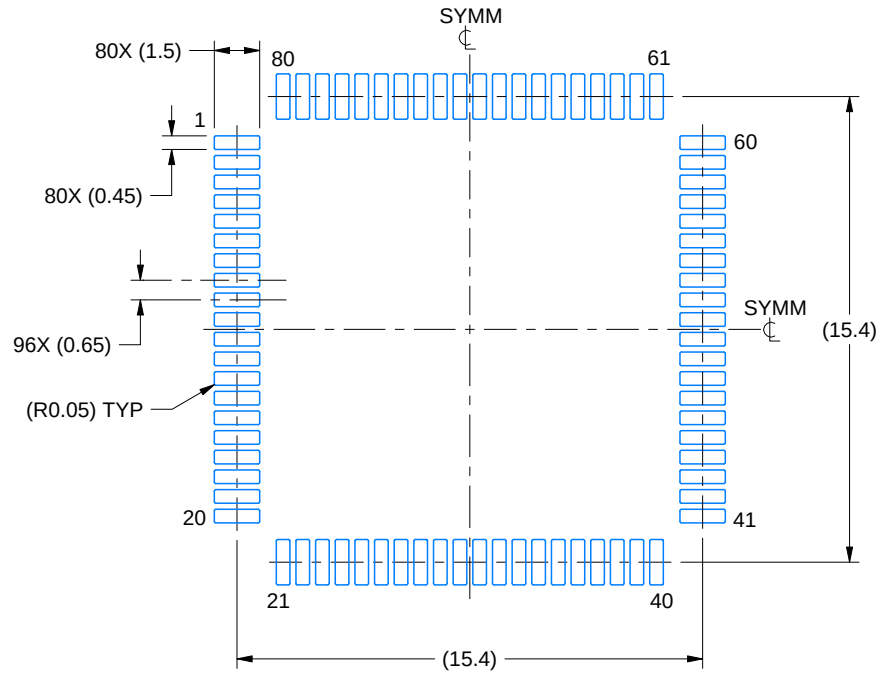
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

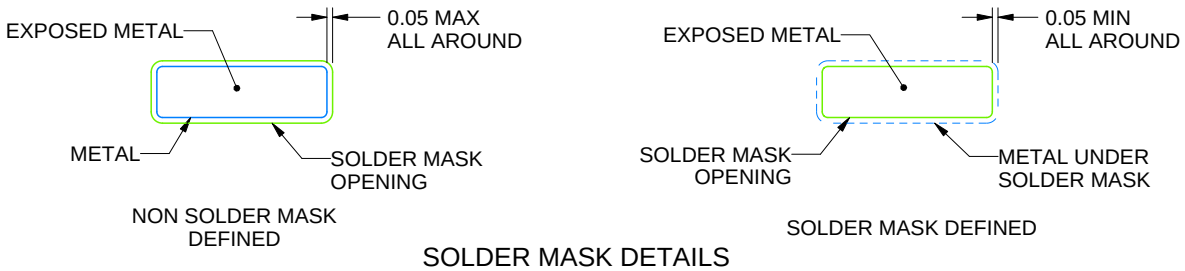


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 4X

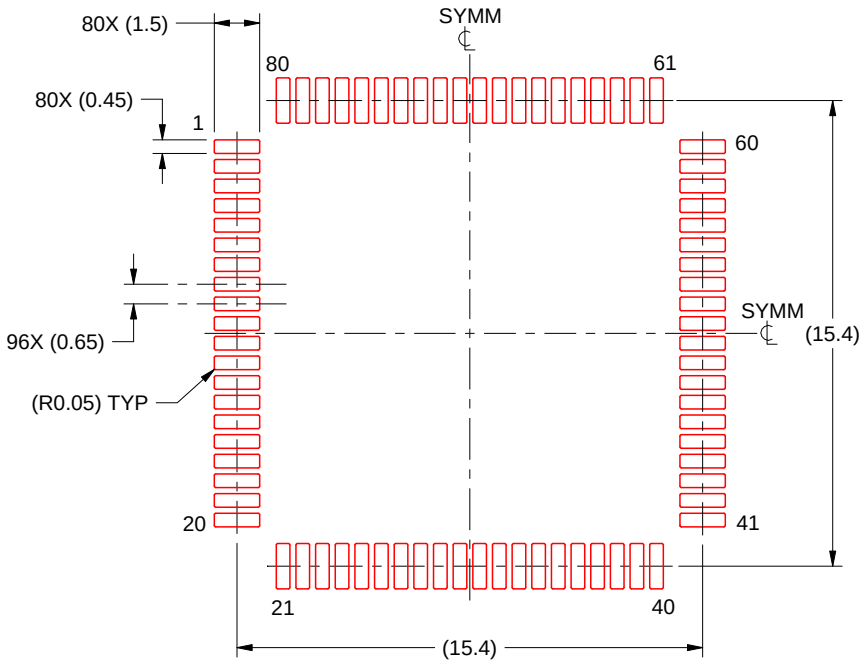


SOLDER MASK DETAILS

4219780/A 01/2020

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 4X

4219780/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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