100 MHz to 6 GHz TruPwr™ Detector

ADL5500

FEATURES

True rms response
Excellent temperature stability
±0.1 dB accuracy vs. temperature over top 8 dB of input range
Up to 30 dB input dynamic range at 3.9 GHz
50 Ω input impedance
1250 mV rms, +15 dBm, maximum input
Single-supply operation: 2.7 V to 5.5 V
Low power: 3 mW at 3 V supply
RoHS compliant

APPLICATIONS

Measurement of CDMA2000, W-CDMA, and QPSK-/QAM-based OFDM, and other complex modulation waveforms
RF transmitter or receiver power measurement

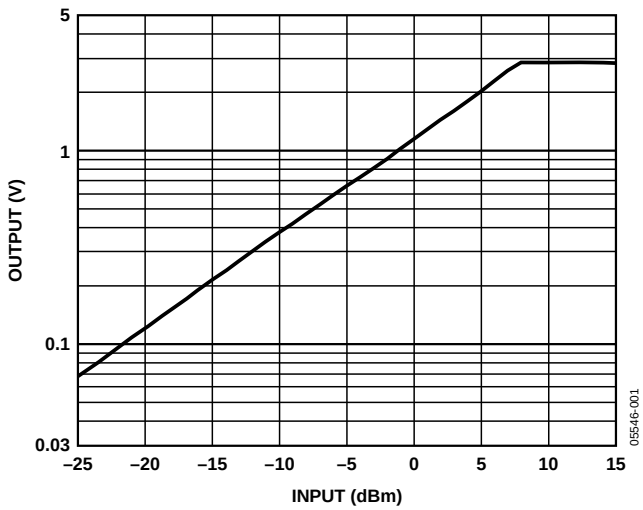

Figure 1. Output vs. Input Level, Supply 3 V, Frequency 1.9 GHz

GENERAL DESCRIPTION

The ADL5500 is a mean-responding power detector for use in high frequency receiver and transmitter signal chains from 100 MHz to 6 GHz. It is easy to apply, requiring only a single supply between 2.7 V and 5.5 V and a power supply decoupling capacitor. The input is internally ac-coupled and has a nominal input impedance of 50 Ω. The output is a linear-responding dc voltage with a conversion gain of 6.4 V/V rms at 900 MHz. The on-chip, 1 kΩ series resistance at the output combined with an external shunt capacitor creates a low-pass filter response that reduces the residual ripple in the dc output voltage.

The ADL5500 is intended for true power measurement of simple and complex waveforms. The device is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as CDMA2000, W-CDMA, and QPSK/QAM-based OFDM waveforms.

The ADL5500 offers excellent temperature stability with near 0 dB measurement error across temperature. The high accuracy range, centered around +3 dBm at 900 MHz, offers ±0.1 dB error from −40°C to +85°C over an 8.5 dB range. The ADL5500 reduces calibration requirements with low drift across a 30 dB range over temperature and process variations.

The ADL5500 operates from −40°C to +85°C and is available in a 4-ball, 1.0 mm × 1.0 mm wafer-level chip scale package. It is fabricated on a proprietary high f_T silicon bipolar process.

FUNCTIONAL BLOCK DIAGRAM

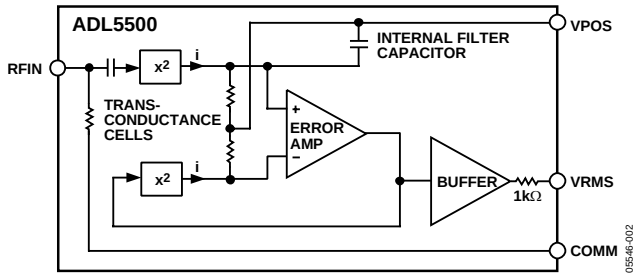

Figure 2.

Rev. A
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REVISION HISTORY

2/06—Rev 0 to Rev. A

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7/05—Revision 0: Initial Version

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SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, C_{FLT} = 10 nF, light condition ≤ 600 LUX, unless otherwise noted.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	100		6000	MHz
RMS CONVERSION (f = 100 MHz)	Input RFIN to output VRMS				
Input Impedance			94‖3		Ω‖pF
Input Return Loss			10		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		5		dB
±0.25 dB Error[3]	V_S = 3 V		17.5		dB
	V_S = 5 V		20		dB
±1 dB Error[3]	V_S = 3 V		25		dB
	V_S = 5 V		29		dB
±2 dB Error[3]	V_S = 3 V		28.5		dB
	V_S = 5 V		33		dB
Maximum Input Level	±0.25 dB error[3]		6		dBm
Minimum Input Level	±1 dB error[3]		−18.5		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		6.1		V/V rms
	V_S = 5 V	4.6		7.2	V/V rms
Output Intercept[4]			0.03		V
	V_S = 5 V	−20		+100	mV
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.43		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.14		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0032		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0042		dB/°C
RMS CONVERSION (f = 450 MHz)	Input RFIN to output VRMS				
Input Impedance			75‖1.4		Ω‖pF
Input Return Loss			12.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		8		dB
±0.25 dB Error[3]	V_S = 3 V		19		dB
	V_S = 5 V		24		dB
±1 dB Error[3]	V_S = 3 V		24.5		dB
	V_S = 5 V		29		dB
±2 dB Error[3]	V_S = 3 V		27.5		dB
	V_S = 5 V		33		dB
Maximum Input Level	±0.25 dB error[3]		5		dBm
Minimum Input Level	±1 dB error[3]		−19.5		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		6.9		V/V rms
Output Intercept[4]			0.03		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.8		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.16		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0020		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0023		dB/°C

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Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 900 MHz)	Input RFIN to output VRMS				
Input Impedance			62‖1.1		Ω‖pF
Input Return Loss			13		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		8.5		dB
±0.25 dB Error[3]	V_S = 3 V		19.5		dB
	V_S = 5 V		23		dB
±1 dB Error[3]	V_S = 3 V		24.5		dB
	V_S = 5 V		29		dB
±2 dB Error[3]	V_S = 3 V		28		dB
	V_S = 5 V		32		dB
Maximum Input Level	±0.25 dB error[3]		6		dBm
Minimum Input Level	±1 dB error[3]		−19		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		6.4		V/V rms
Output Intercept[4]			0.04		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.61		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.15		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ +85°C		0.0018		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0023		dB/°C
RMS CONVERSION (f = 1900 MHz)	Input RFIN to output VRMS				
Input Impedance			43‖0.9		Ω‖pF
Input Return Loss			11.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		7		dB
±0.25 dB Error[3]	V_S = 3 V		20		dB
	V_S = 5 V		23		dB
±1 dB Error[3]	V_S = 3 V		26		dB
	V_S = 5 V		30		dB
±2 dB Error[3]	V_S = 3 V		31.5		dB
	V_S = 5 V		33		dB
Maximum Input Level	±0.25 dB error[3]		8		dBm
Minimum Input Level	±1 dB error[3]		−19.5		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		5.0		V/V rms
Output Intercept[4]			0.02		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		2.02		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.11		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0017		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0031		dB/°C

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Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 2350 MHz)	Input RFIN to output VRMS				
Input Impedance			37‖0.9		Ω‖pF
Input Return Loss			9		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		5		dB
±0.25 dB Error[3]	V_S = 3 V		5		dB
	V_S = 5 V		10		dB
±1 dB Error[3]	V_S = 3 V		28.5		dB
	V_S = 5 V		32		dB
±2 dB Error[3]	V_S = 3 V		32		dB
	V_S = 5 V		36		dB
Maximum Input Level	±0.25 dB error[3]		8		dBm
Minimum Input Level	±1 dB error[3]		−19.5		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		4.5		V/V rms
Output Intercept[4]			0.02		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		1.82		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.11		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0027		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0046		dB/°C
RMS CONVERSION (f = 2700 MHz)	Input RFIN to output VRMS				
Input Impedance			34‖0.8		Ω‖pF
Input Return Loss			8.5		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		5		dB
±0.25 dB Error[3]	V_S = 3 V		5		dB
	V_S = 5 V		8.5		dB
±1 dB Error[3]	V_S = 3 V		28.5		dB
	V_S = 5 V		32		dB
±2 dB Error[3]	V_S = 3 V		33		dB
	V_S = 5 V		36		dB
Maximum Input Level	±0.25 dB error[3]		9		dBm
Minimum Input Level	±1 dB error[3]		−19.5		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		4.2		V/V rms
Output Intercept[4]			0.02		V
Output Voltage—High Power In	P_{IN} =+5 dBm, 400 mV rms		1.67		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.1		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0030		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0049		dB/°C

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Parameter	Condition	Min	Typ	Max	Unit
RMS CONVERSION (f = 3900 MHz)	Input RFIN to output VRMS				
Input Impedance			30||0.6		Ω||pF
Input Return Loss			9		dB
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.1 dB Error[2]	Delta from 25°C, V_S = 5 V		2		dB
±0.25 dB Error[3]	V_S = 3 V		5.5		dB
	V_S = 5 V		8		dB
±1 dB Error[3]	V_S = 3 V		28.5		dB
	V_S = 5 V		32		dB
±2 dB Error[3]	V_S = 3 V		34		dB
	V_S = 5 V		36.5		dB
Maximum Input Level	±0.25 dB error[3]		12		dBm
Minimum Input Level	±1 dB error[3]		−17		dBm
Conversion Gain	VOUT = (Gain × V_{IN}) + Intercept		3.2		V/V rms
Output Intercept[4]			0.02		V
Output Voltage—High Power In	P_{IN} = +5 dBm, 400 mV rms		1.28		V
Output Voltage—Low Power In	P_{IN} = −21 dBm, 20 mV rms		0.08		V
Temperature Sensitivity	P_{IN} = −5 dBm				
	25°C ≤ T_A ≤ 85°C		0.0035		dB/°C
	−40°C ≤ T_A ≤ +25°C		−0.0066		dB/°C
OUTPUT OFFSET	No signal at RFIN		40	150	mV
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.7		5.5	V
Quiescent Current	No signal at RFIN[5]		1.0		mA

[1] The available output swing, and hence the dynamic range, is altered by the supply voltage; see Figure 8.
[2] Error referred to delta from 25°C response; see Figure 16 through Figure 21.
[3] Error referred to best-fit line at 25°C
[4] Calculated using linear regression.
[5] Supply current is input level dependant; see Figure 6.

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage V_S	5.5 V
VRMS	0 V, V_S
RFIN	1.25 V rms
Equivalent Power, re 50 Ω	15 dBm
Internal Power Dissipation	150 mW
θ_{JA} (WLCSP)	260°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

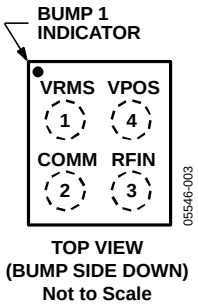

Figure 3. 4-Ball WLCSP Pin Configuration

Table 3. Pin Function Descriptions

Ball No.	Mnemonic	Description
1	VRMS	Output Pin. Rail-to-rail voltage output with limited current drive capability. The output has an internal 1 kΩ series resistance. High resistive loads are recommended to preserve output swing.
2	COMM	Device Ground Pin.
3	RFIN	Signal Input Pin. Internally ac-coupled after internal termination resistance. Nominal 50 Ω input impedance.
4	VPOS	Supply Voltage Pin. Operational range 2.7 V to 5.5 V.

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TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5.0 V, C_{FLT} = 10 nF, light condition ≤ 600 LUX, Colors: black = +25°C, blue = −40°C, red = +85°C, unless otherwise noted.

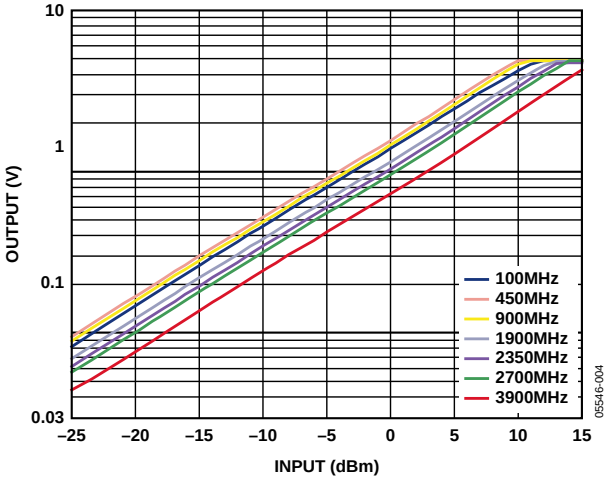

Figure 4. Output vs. Input Level, Frequencies 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 3900 MHz, Supply 5.0 V

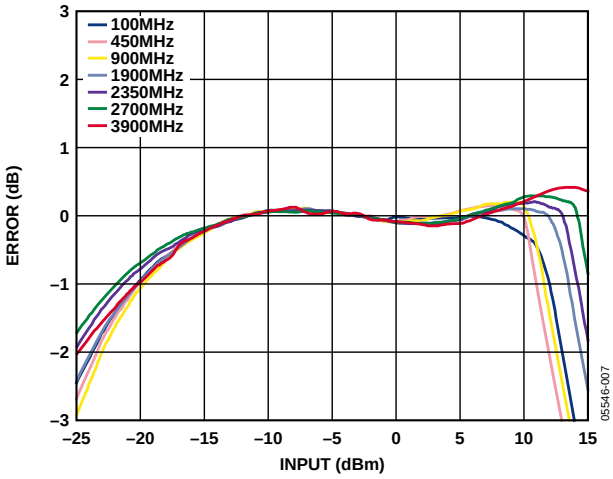

Figure 7. Linearity Error vs. Input Level, Frequencies 100 MHz, 450 MHz, 900 MHz, 1900 MHz, 2350 MHz, 2700 MHz, and 3900 MHz, Supply 5.0 V

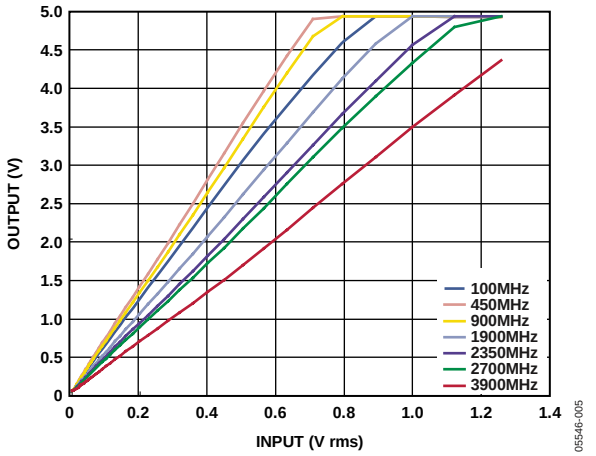

Figure 5. Output vs. Input Level (Linear Scale), Frequencies 100 MHz, 450 MHz, 900 MHz,1900 MHz, 2350 MHz, 2700 MHz, and 3900 MHz, Supply 5.0 V

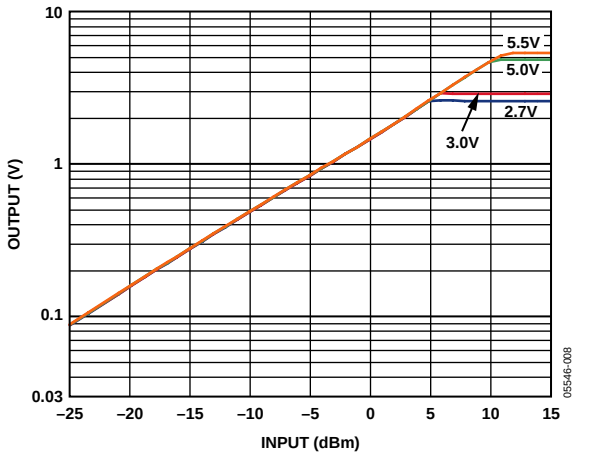

Figure 8. Output vs. Input Level, Supply 2.7 V, 3.0 V, 5.0 V, and 5.5 V, Frequency 900 MHz

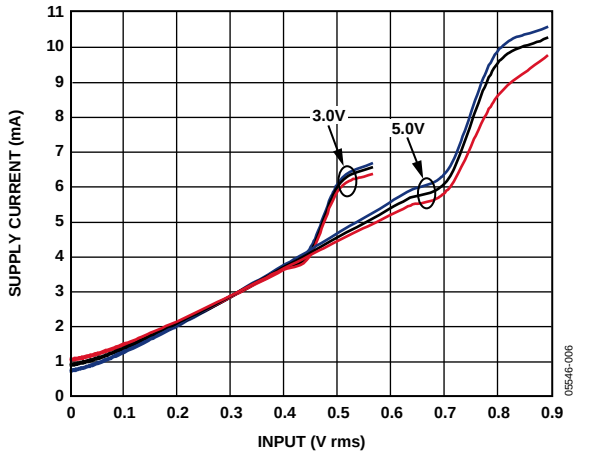

Figure 6. Supply Current vs. Input Level, Supplies 3.0 V and 5.0 V, Temperatures −40°C, +25°C, and +85°C

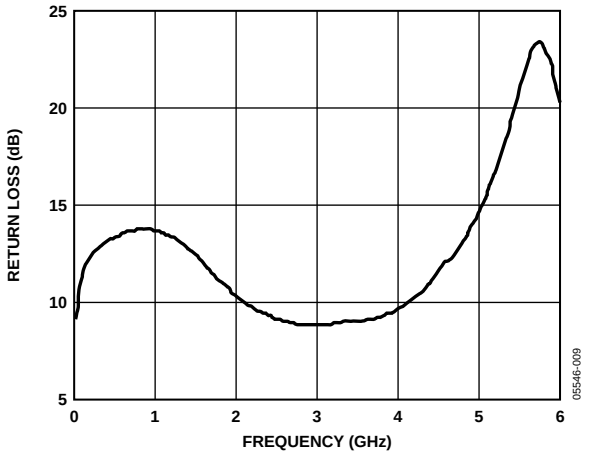

Figure 9. Return Loss vs. Frequency

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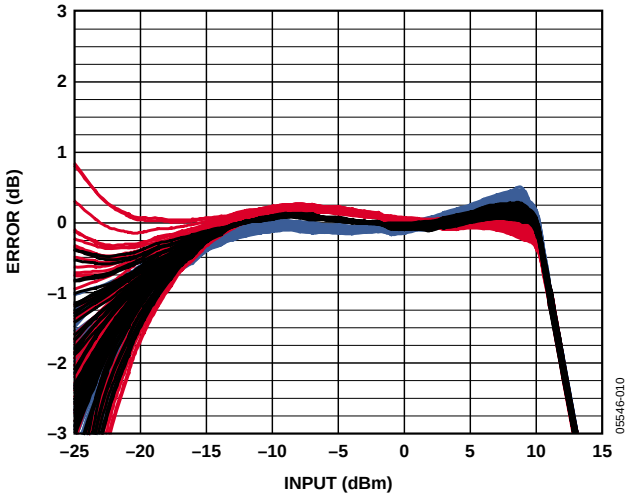

Figure 10. Temperature Drift Distributions for 55 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 450 MHz, Supply 5.0 V

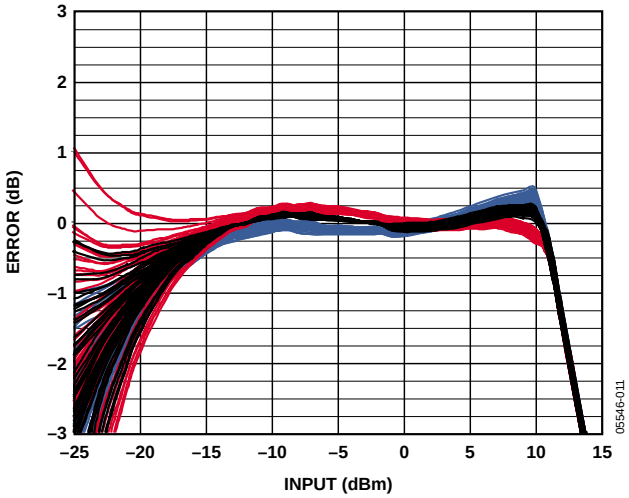

Figure 11. Temperature Drift Distributions for 55 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 900 MHz, Supply 5.0 V

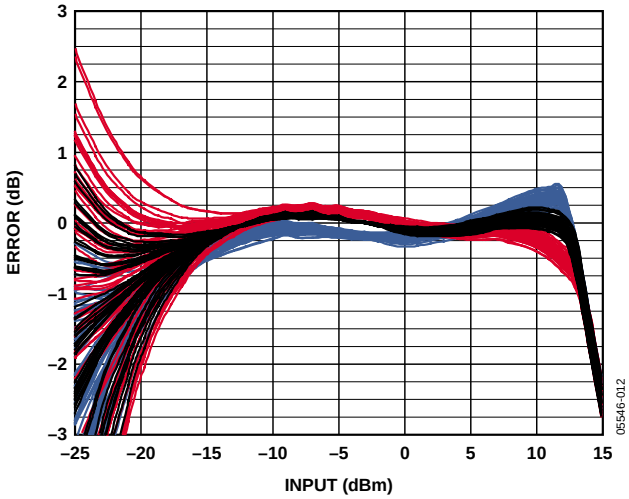

Figure 12. Temperature Drift Distributions for 55 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 1900 MHz, Supply 5.0 V

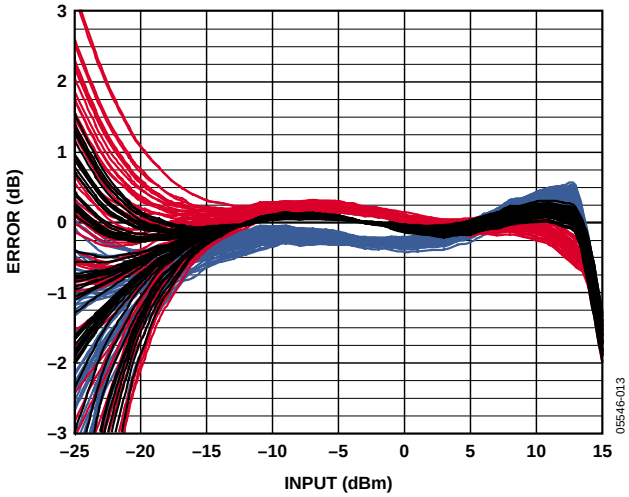

Figure 13. Temperature Drift Distributions for 55 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 2350 MHz, Supply 5.0 V

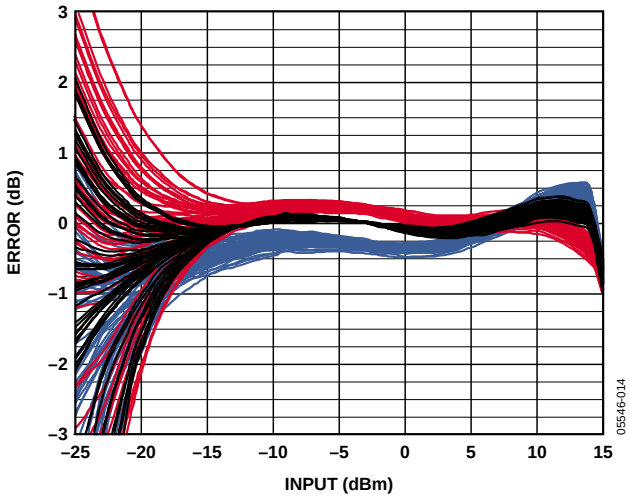

Figure 14. Temperature Drift Distributions for 55 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 2700 MHz, Supply 5.0 V

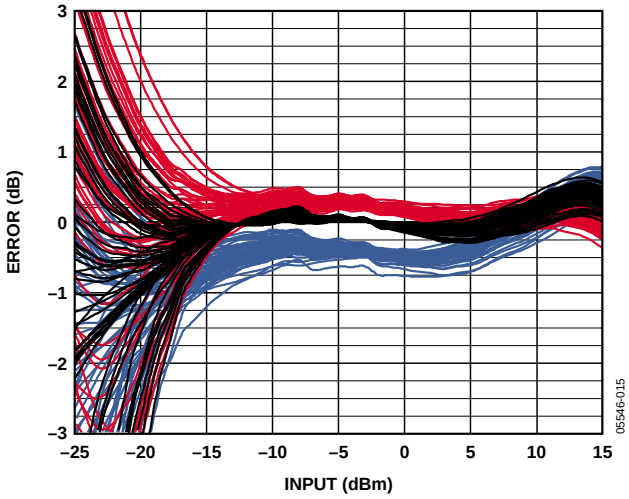

Figure 15. Temperature Drift Distributions for 55 Devices at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 3900 MHz, Supply 5.0 V

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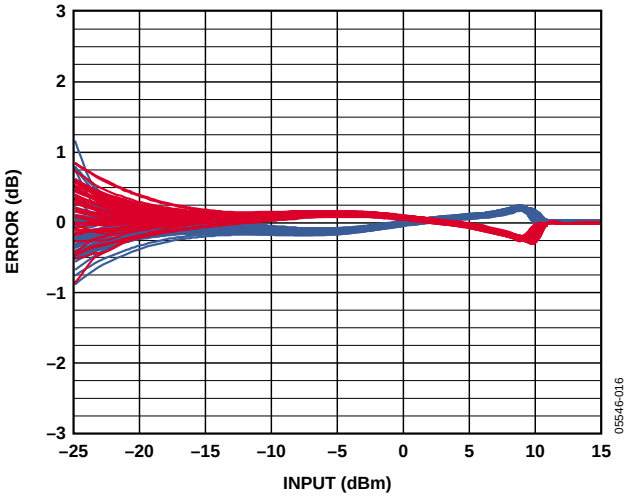

Figure 16. Output Delta from +25°C Output Voltage for 55 Devices at −40°C and +85°C, Frequency 450 MHz, Supply 5.0 V

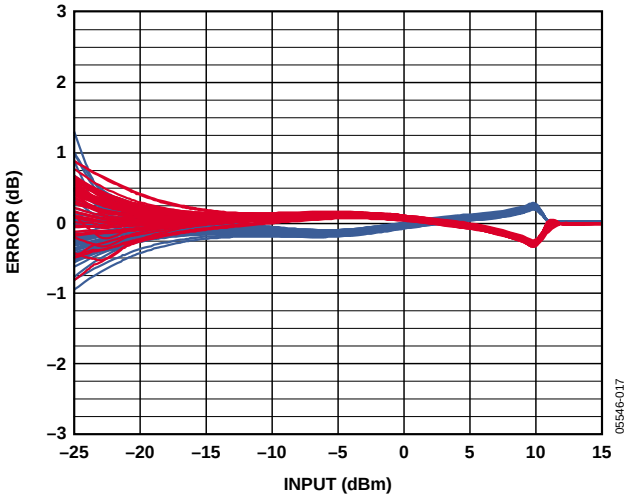

Figure 17. Output Delta from +25°C Output Voltage for 55 Devices at −40°C and +85°C, Frequency 900 MHz, Supply 5.0 V

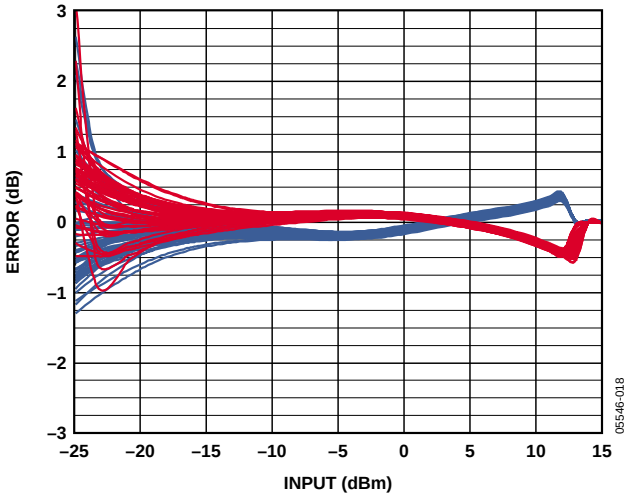

Figure 18. Output Delta from +25°C Output Voltage for 55 Devices at −40°C and +85°C, Frequency 1900 MHz, Supply 5.0 V

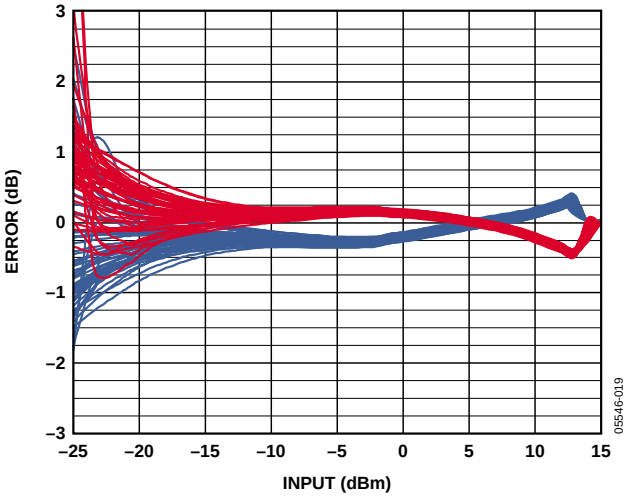

Figure 19. Output Delta from +25°C Output Voltage for 55 Devices at −40°C and +85°C, Frequency 2350 MHz, Supply 5.0 V

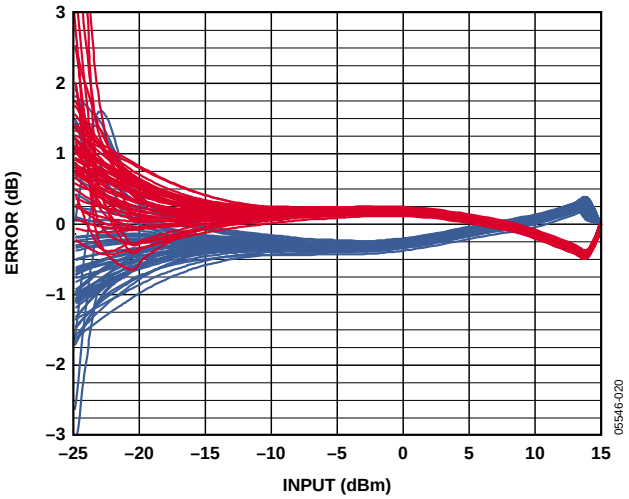

Figure 20. Output Delta from +25°C Output Voltage for 55 Devices at −40°C and +85°C, Frequency 2700 MHz, Supply 5.0 V

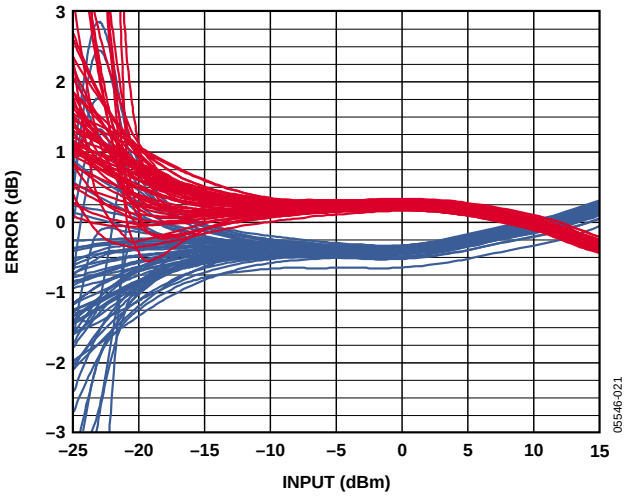

Figure 21. Output Delta from +25°C Output Voltage for 55 Devices at −40°C and +85°C, Frequency 3900 MHz, Supply 5.0 V

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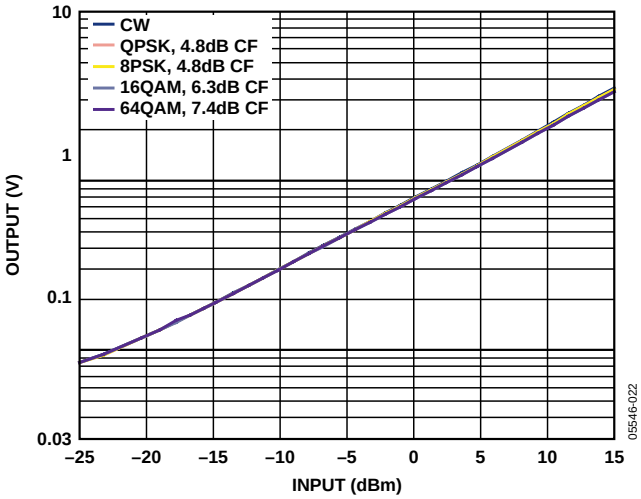

Figure 22. Output vs. Input Level with Different Waveforms, 10 MHz Signal BW for All Modulated Signals, Supply 5.0 V, Frequency 1900 MHz

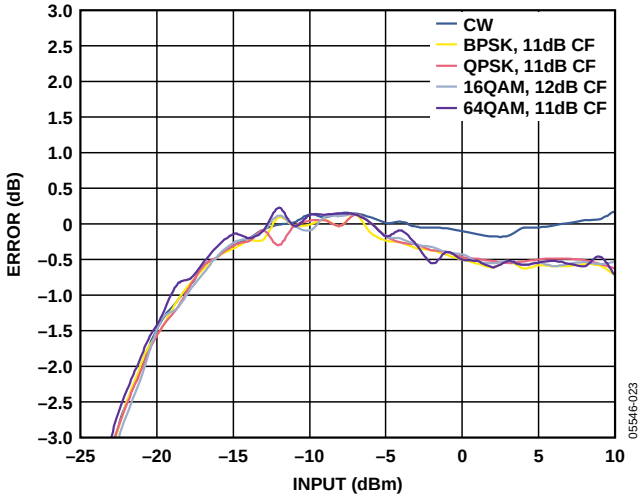

Figure 23. Error from CW Linear Reference vs. Input Level for Various 802.16 OFDM Waveforms at 2.35 GHz, 10 MHz Signal BW and 256 Subcarriers for All Modulated Signals, Supply 5.0 V

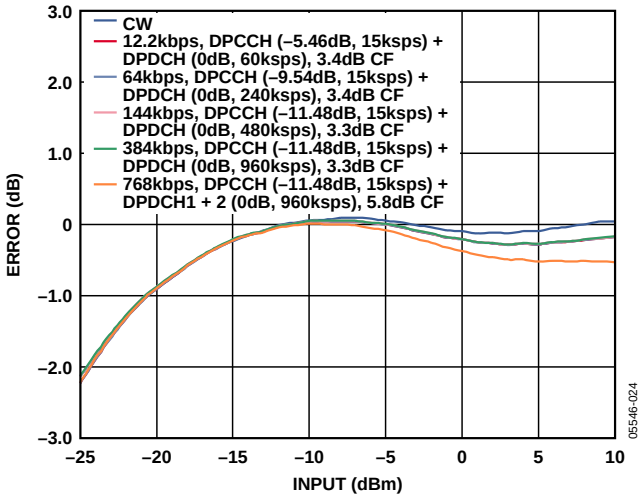

Figure 24. Error from CW Linear Reference vs. Input with Various WCDMA Up Link Waveforms at 1900 MHz

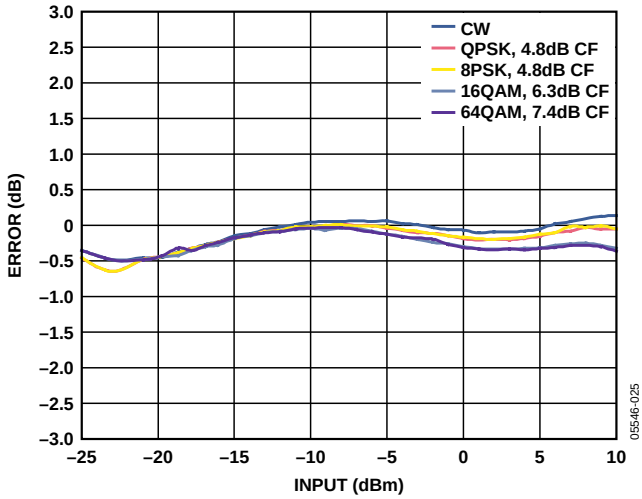

Figure 25. Error from CW Linear Reference vs. Input with Different Waveforms, 10 MHz Signal BW for All Modulated Signals, Supply 5.0 V, Frequency 1900 MHz

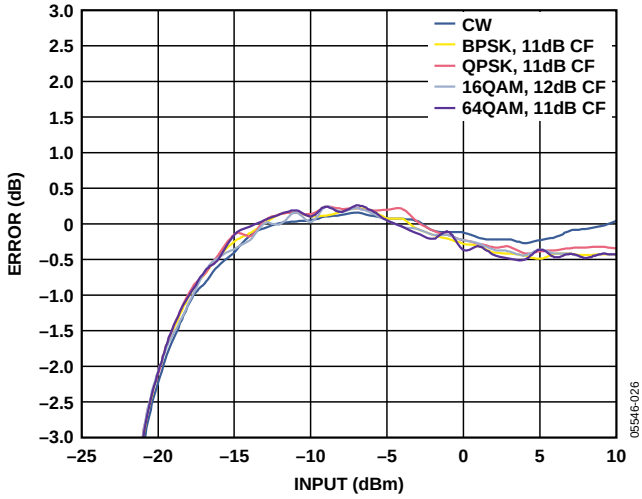

Figure 26. Error from CW Linear Reference vs. Input Level for Various 802.16 OFDM Waveforms at 3.5 GHz, 10 MHz Signal BW and 256 Subcarriers for All Modulated Signals, Supply 5.0 V

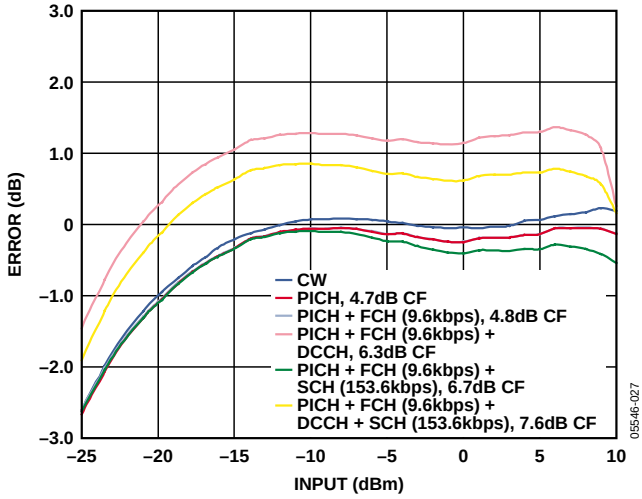

Figure 27. Error from CW Linear Reference vs. Input with Various CDMA2000 Reverse Link Waveforms at 900 MHz

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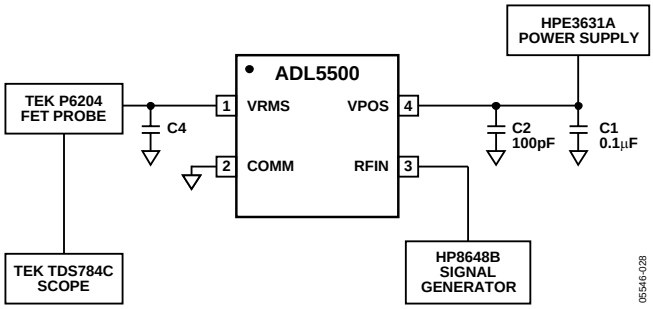

Figure 28. Hardware Configuration for Output Response to Modulated Pulse Input

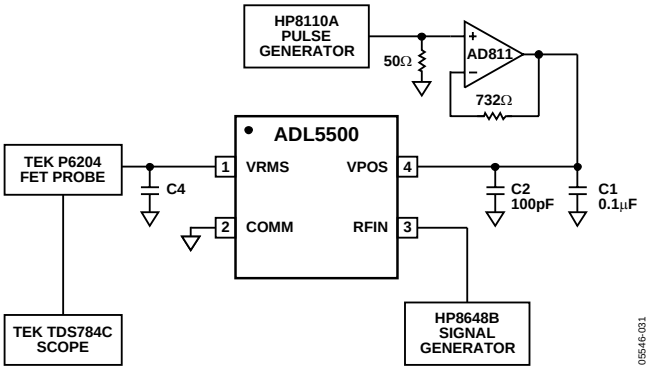

Figure 31. Hardware Configuration for Output Response to Power Supply Gating Measurements

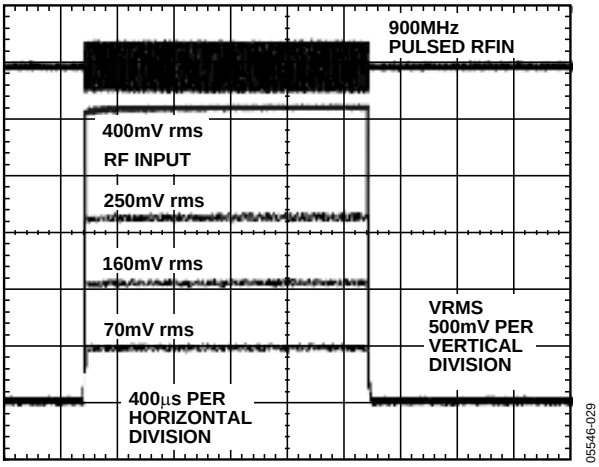

Figure 29. Output Response to Modulated Pulse Input for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, No Filter Capacitor

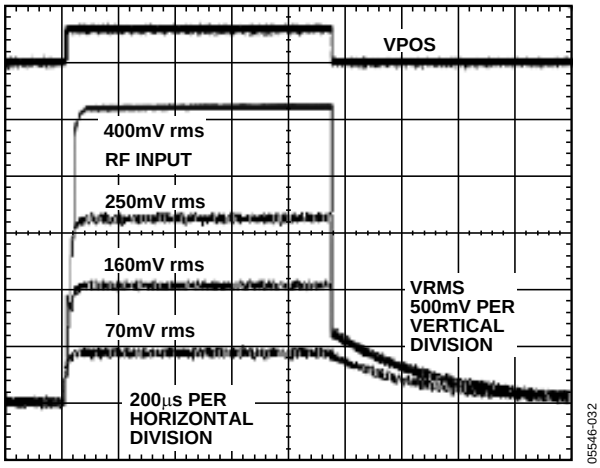

Figure 32. Output Response to Gating on Power Supply for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, 0.01 µF Filter Capacitor

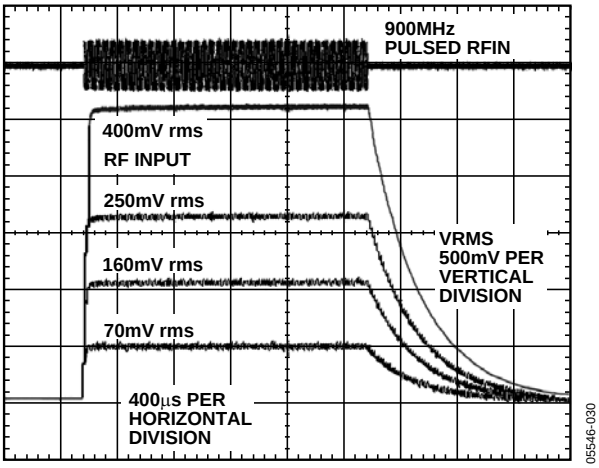

Figure 30. Output Response to Modulated Pulse Input for Various RF Input Levels, Supply 3 V, Modulation Frequency 900 MHz, 0.01 µF Filter Capacitor

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CIRCUIT DESCRIPTION

The ADL5500 is an rms-responding (mean power) detector that provides an approach to the exact measurement of RF power that is independent of waveform. It achieves this function by using a proprietary technique in which the outputs of two identical squaring cells are balanced by the action of a high-gain error amplifier.

The signal to be measured is applied to the input of the first squaring cell through the input matching network. The input is matched to offer a broadband 50 Ω input impedance from 100 MHz to 6 GHz. The input matching network has a high-pass corner frequency of approximately 90 MHz.

The ADL5500 responds to the voltage, V_{IN}, at its input by squaring this voltage to generate a current proportional to V_{IN}^2. This current is applied to an internal load resistor in parallel with a capacitor, followed by a low-pass filter, which extracts the mean of V_{IN}^2. Although essentially voltage responding, the associated input impedance calibrates this port in terms of equivalent power. Therefore, 1 mW corresponds to a voltage input of 224 mV rms referenced to 50 Ω. Because both the squaring cell input impedance and the input matching network are frequency dependent, the conversion gain is a function of signal frequency.

The voltage across the low-pass filter, whose frequency can be arbitrarily low, is applied to one input of an error-sensing amplifier. A second identical voltage-squaring cell is used to close a negative feedback loop around this error amplifier. This second cell is driven by a fraction of the quasi-dc output voltage of the ADL5500. When the voltage at the input of the second squaring cell is equal to the rms value of V_{IN}, the loop is in a stable state, and the output then represents the rms value of the input.

By completing the feedback path through a second squaring cell, identical to the one receiving the signal to be measured, several benefits arise. First, scaling effects in these cells cancel; therefore, the overall calibration can be accurate, even though the open-loop response of the squaring cells taken separately need not be. Note that in implementing rms-dc conversion, no reference voltage enters into the closed-loop scaling. Second, the tracking in the responses of the dual cells remains very close over temperature, leading to excellent stability of calibration.

The squaring cells have very wide bandwidth with an intrinsic response from dc to microwave. However, the dynamic range of such a system is small due in part to the much larger dynamic range at the output of the squaring cells. There are practical limitations to the accuracy of sensing very small error signals at the bottom end of the dynamic range, arising from small random offsets that limit the attainable accuracy at small inputs.

On the other hand, the squaring cells in the ADL5500 have a Class-AB aspect; the peak input is not limited by its quiescent bias condition but is determined mainly by the eventual loss of square-law conformance. Consequently, the top end of their response range occurs at a large input level (approximately 700 mV rms) while preserving a reasonably accurate square-law response. The maximum usable range is, in practice, limited by the output swing. The rail-to-rail output stage can swing from a few millivolts above ground to within 100 mV below the supply. An example of the output induced limit, given a conversion gain of 6.4 V/V rms at 900 MHz and assuming a maximum output of 2.9 V with a 3 V supply, has a maximum input of 2.9 V rms/6.4 or 450 mV rms.

FILTERING

An important aspect of rms-dc conversion is the need for averaging (the function is root-mean-square). The on-chip averaging in the square domain has a corner frequency of approximately 150 kHz and is sufficient for common modulation signals, such as CDMA, WCDMA, and QPSK-/QAM-based OFDM (for example, WLAN and WiMAX). It ensures the accuracy of rms measurement for these signals; however, it leaves significant ripple on the output. To reduce this ripple, an external shunt capacitor can be used at the output to form a low-pass filter with the on-chip 1 kΩ resistance (see the Selecting the Output Low-Pass Filter Network section).

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APPLICATIONS

BASIC CONNECTIONS

Figure 33 shows the basic connections for the ADL5500. The device is powered by a single supply of between 2.7 V and 5.5 V with a quiescent current of 1.0 mA. The VPOS pin is decoupled using 100 pF and 0.1 μF capacitors.

The ADL5500 RF input does not require external termination components because it is internally matched for an overall broadband input impedance of 50 Ω.

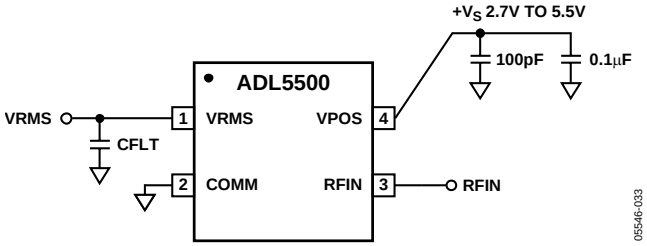

Figure 33. Basic Connections for ADL5500

OUTPUT SWING

At 900 MHz, the output voltage is nominally 6.4 times the input rms voltage (a conversion gain of 6.4 V/V rms). The output voltage swings from near ground to 4.9 V on a 5.0 V supply.

Figure 34 shows the output swing of the ADL5500 to a CW input for various supply voltages. It is clear from Figure 34 that operating the device at lower supply voltages reduces dynamic range as the output headroom decreases.

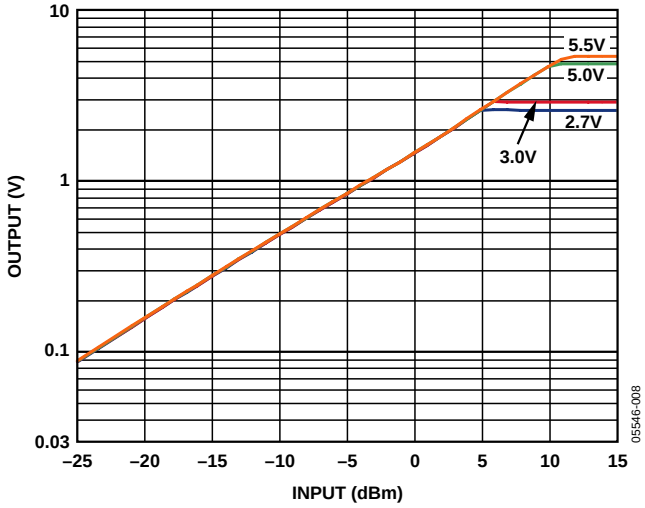

Figure 34. Output Swing for Supply Voltages of 2.7 V, 3.0 V, 5.0 V, and 5.5 V

LINEARITY

Because the ADL5500 is a linear-responding device, plots of output voltage vs. input voltage result in a straight line. It is more useful to plot the error on a logarithmic scale, as shown in Figure 35. The deviation of the plot for the ideal straight-line characteristic is caused by output clipping at the high end and by signal offsets at the low end. However, it should be noted that offsets at the low end can be either positive or negative; therefore, this plot could also trend upwards at the low end. Figure 10 through Figure 15 show error distributions for a large population of devices.

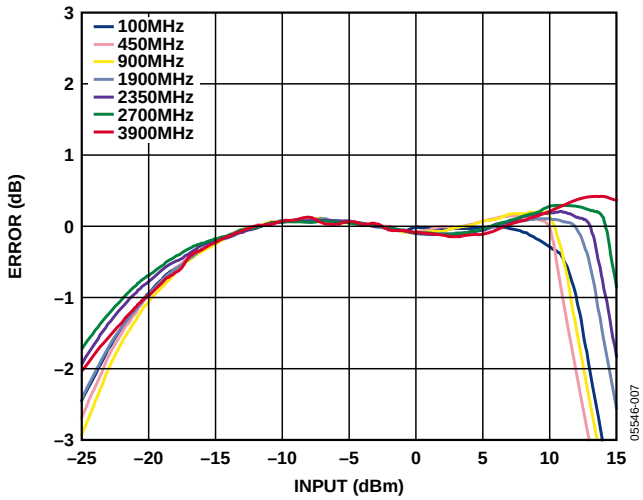

Figure 35. Representative Unit, Error in dB vs. Input Level, V_S = 5.0 V

It is also apparent in Figure 35 that the error plot tends to shift to the right with increasing frequency. The squaring cell has an input impedance that decreases with frequency. The matching network compensates for the change and maintains the input impedance at a nominal 50 Ω. The result is a decrease in the actual voltage across the squaring cell as the frequency increases, reducing the conversion gain. Similarly, conversion gain is less at frequencies near 100 MHz because of the small on-chip coupling capacitor.

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INPUT COUPLING USING A SERIES RESISTOR

Figure 36 shows a technique for coupling the input signal into the ADL5500 that can be applicable where the input signal is much larger than the input range of the ADL5500. A series resistor combines with the input impedance of the ADL5500 to attenuate the input signal. Because this series resistor forms a divider with the frequency dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being tapped off in RF power transmission applications. If the resistor is large compared to the transmission line's impedance, the VSWR of the system is relatively unaffected.

Figure 36. Attenuating the Input Signal

MULTIPLE RF INPUTS

Figure 37 shows a technique for combining multiple RF input signals to the ADL5500. Some applications can share a single detector for multiple bands. Three 16.5 Ω resistors in a T-network combine the three 50 Ω terminations (including the ADL5500). The broadband resistive combiner ensures each port of the T-network sees a 50 Ω termination. Because there is only 6 dB of isolation from one port of the combiner to the other ports, only one band should be active at a time.

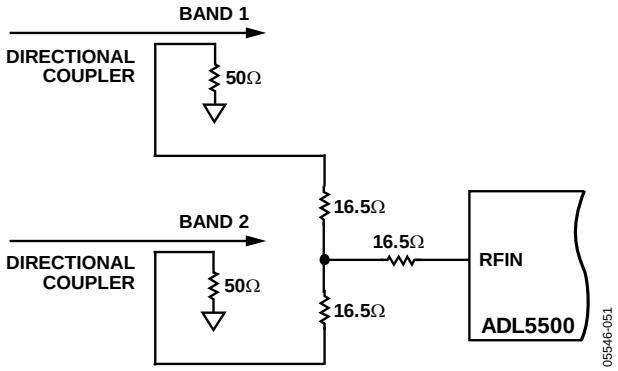

Figure 37. Combining Multiple RF Input Signals

SELECTING THE OUTPUT LOW-PASS FILTER NETWORK

The ADL5500's internal filter capacitor provides averaging in the square domain but leaves some residual ac on the output. Signals with high peak-to-average ratios, such as W-CDMA or CDMA2000, can produce ac-residual levels on the ADL5500 dc output. To reduce the effects of these low frequency components in the waveforms, some additional filtering is required.

The output of the ADL5500 can be filtered by placing a capacitor between VRMS (Pin 1) and ground. The combination of the on-chip 1 kΩ output series resistance and the external shunt capacitor forms a low-pass filter to reduce the residual ac.

Table 4 shows the effect of several capacitor values for various communications standards with high peak-to-average ratios along with the residual ripple at the output, in peak-to-peak and rms volts. Note that large load capacitances increase the turn-on and pulse response times (see Figure 29 and Figure 30).

Table 4. Waveform and Output Filter Effects on Residual AC

Waveform	C_{FILT}	Output V dc	Residual AC mV p-p	Residual AC mV rms
64QAM (7.4 dB CF)	0.01 µF	0.5	7.0	1.4
		1.0	7.4	1.5
		2.0	7.6	1.6
	0.1 µF	0.5	6.7	1.4
		1.0	7.2	1.5
		2.0	7.4	1.5
W-CDMA RL (3.4 dB CF)	0.01 µF	0.5	10	1.7
		1.0	16	2.4
		2.0	45	5.6
	0.1 µF	0.5	7	1.5
		1.0	9	1.6
		2.0	14	2.3
CDMA2000 UL (6.7 dB CF)	0.01 µF	0.5	46	6
		1.0	85	13
		2.0	191	27
	0.1 µF	0.5	17	3
		1.0	31	5
		2.0	68	9

POWER CONSUMPTION AND POWER-ON/-OFF RESPONSE

The quiescent current consumption of the ADL5500 varies with the size of the input signal from approximately 1 mA for no signal up to 6 mA at an input level of 0.7 V rms (10 dBm, re 50 Ω). If the input is driven beyond this point, the supply current increases sharply (as shown in Figure 6). There is little variation in quiescent current with power supply voltage.

The ADL5500 can be disabled by simply removing the power to the device. Figure 32 shows a plot of the output response to the supply being turned on (that is, VPOS is pulsed) with an output shunt capacitor of 0.01 µF. Again, the turn-on time is influenced strongly by the size of the output shunt capacitor.

To improve the falling edge of the supply gating response and the pulse response, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps discharge the capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section).

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OUTPUT DRIVE CAPABILITY AND BUFFERING

The ADL5500 is capable of sourcing an output current of approximately 3 mA. The output current is sourced through the on-chip 1 kΩ series resistor; therefore, any load resistor forms a voltage divider with this on-chip resistance. It is recommended that the ADL5500 drive high resistive loads to preserve output swing (preferably >100 kΩ). If an application requires driving a low resistance load, a simple buffering circuit can be used, as shown in Figure 40. Similar circuits can be used to increase or decrease the nominal conversion gain (see Figure 38 and Figure 39). In Figure 39, the AD8031 buffers a resistive divider to give half of the slope. In Figure 38, the op amp's gain of two doubles the slope. Using other resistor values, the slope can be changed to an arbitrary value. The AD8031 rail-to-rail op amp, used in these examples, can swing from 50 mV to 4.95 V on a single 5 V supply and operates at supply voltages down to 2.7 V. If high output current is required (>10 mA), the AD8051, which also has rail-to- rail capability, can be used down to a supply voltage of 3 V. It can deliver up to 45 mA of output current.

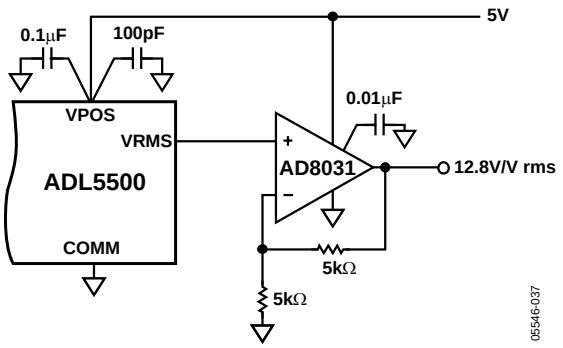

Figure 38. Output Buffering Options, Slope of 12.8 V/V rms at 900 MHz

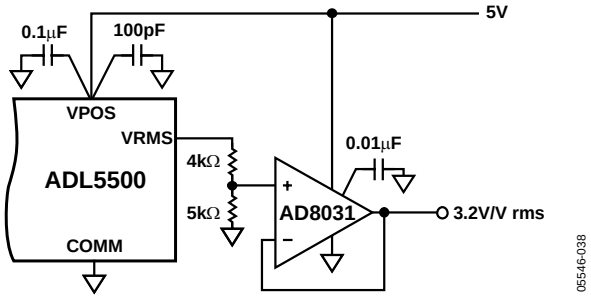

Figure 39. Output Buffering Options, Slope of 3.2 V/V rms at 900 MHz

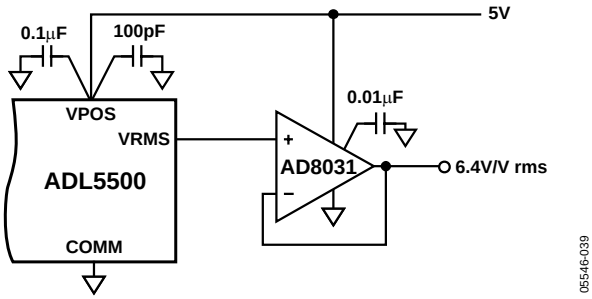

Figure 40. Output Buffering Options, Slope of 6.4 V/V rms at 900 MHz

VRMS OUTPUT OFFSET

The ADL5500 has a ±1 dB error detection range of about 30 dB, as shown in Figure 10 to Figure 15. The error is referred to the best fit line defined in the linear region of the output response. Below an input power of −20 dBm, the response is no longer linear and begins to lose accuracy. In addition, depending on the supply voltage, saturation of the output limits the detection accuracy above 10 dBm. Calibration points should be chosen in the linear region, avoiding the nonlinear ranges at the high and low extremes.

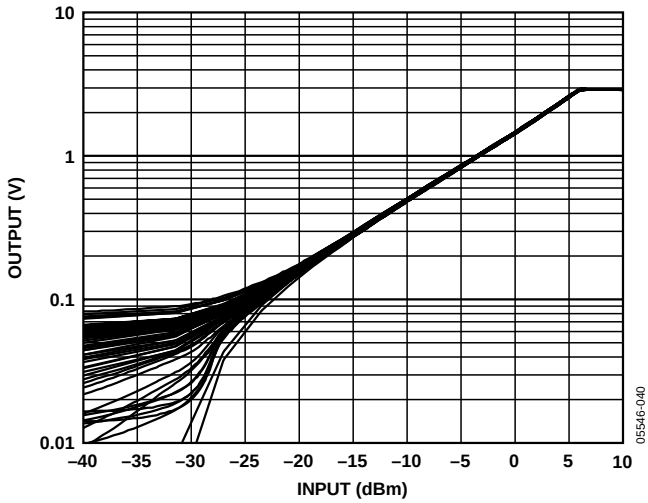

Figure 41. Output vs. Input Level Distribution of 55 Devices, Frequency 900 MHz, Supply 3.0 V

Figure 41 shows the distribution of the output response vs. the input power for multiple devices. The ADL5500 loses accuracy at low input powers as the output response begins to fan out. As the input power is reduced, the spread of the output response increases along with the error. Although some devices follow the ideal linear response at very low input powers, not all devices continue the ideal linear regression to a near 0 V y-intercept. Some devices exhibit output responses that rapidly decrease and some flatten out. With no RF signal applied, the ADL5500 has a typical output offset of 40 mV (with a maximum of 150 mV).

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DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two input power levels to the ADL5500 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. The best fit line is characterized by calculating the slope and intercept using the following equations:

$$Slope = (V_{RMS2} - V_{RMS1})/(V_{IN2} - V_{IN1}) \quad (1)$$

$$Intercept = V_{RMS1} - (Slope \times V_{IN1}) \quad (2)$$

where:

V_{IN} is the rms input voltage to RFIN.

V_{RMS} is the voltage output at VRMS.

Once slope and intercept have been calculated, an equation can be written that allows calculation of an (unknown) input power based on the measured output voltage.

$$V_{IN} = (V_{RMS} - Intercept)/Slope \quad (3)$$

For an ideal (known) input power, the law conformance error of the measured data can be calculated as

$$ERROR\ (\text{dB}) = 20 \times \log\left[(V_{RMS,\ MEASURED} - Intercept)/(Slope \times V_{IN,\ IDEAL})\right] \quad (4)$$

Figure 42 includes a plot of the error at 25°C, the temperature at which the ADL5500 is calibrated. Note that the error is not zero. This is because the ADL5500 does not perfectly follow the ideal linear equation, even within its operating region. The error at the calibration points is, however, equal to zero by definition.

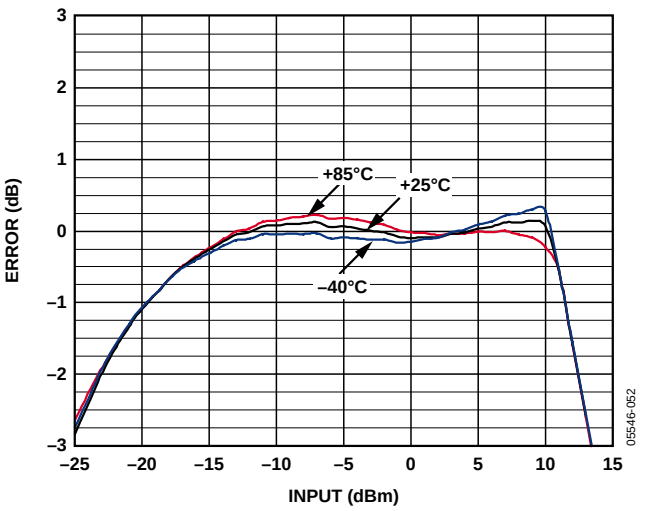

Figure 42. Error from Linear Reference vs. Input at –40°C, +25°C, and +85°C vs. +25°C Linear Reference, Frequency 900 MHz, Supply 5.0 V

Figure 42 also includes error plots for the output voltage at –40°C and +85°C. These error plots are calculated using the slope and intercept at +25°C. This is consistent with calibration in a mass-production environment where calibration at temperature is not practical.

CALIBRATION FOR IMPROVED ACCURACY

Another way of presenting the error function of the ADL5500 is shown in Figure 43. In this case, the dB error at hot and cold temperatures is calculated with respect to the transfer function at ambient. This is a key difference in comparison to the previous plots. Up to now, the errors have been calculated with respect to the ideal linear transfer function at ambient. When this alternative technique is used, the error at ambient becomes equal to 0 by definition (see Figure 43).

This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) response at ambient. The linearity and dynamic range tend to be improved artificially with this type of plot because the ADL5500 does not perfectly follow the ideal linear equation (especially outside of its linear operating range). Achieving this level of accuracy in an end application requires calibration at multiple points in the device's operating range.

In some applications, very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power. The ADL5500 offers a tight error distribution in the high input power range, as shown in Figure 43. The high accuracy range, centered around +3 dBm at 900 MHz, offers 8.5 dB of ±0.1 dB detection error over temperature. Multiple point calibration at ambient temperature in the reduced range offers precise power measurement with near 0 dB error from –40°C to +85°C.

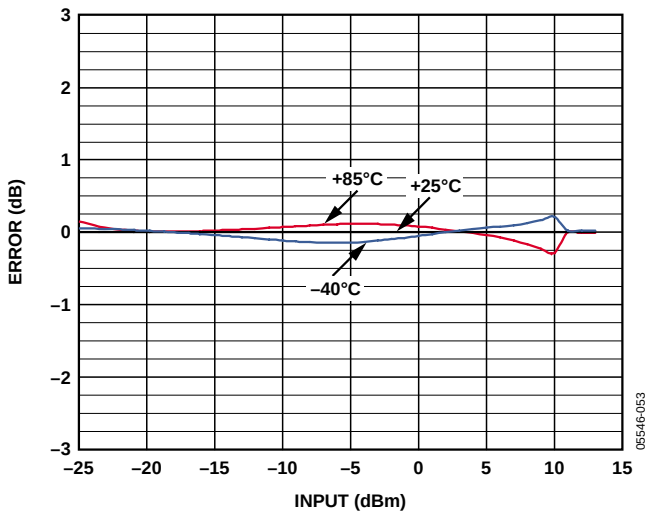

Figure 43. Error from +25°C Output Voltage at –40°C, +25°C, and +85°C After Ambient Normalization, Frequency 900 MHz, Supply 5.0 V

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The high accuracy range center varies over frequency. At 900 MHz, the region is centered at approximately 3 dBm. At higher frequencies, the high accuracy range is centered at higher input powers (see Figure 16 to Figure 21).

DRIFT OVER A REDUCED TEMPERATURE RANGE

Figure 44 shows the error over temperature for a 1.9 GHz input signal. Error due to drift over temperature consistently remains within ±0.25 dB and only begins to exceed this limit when the ambient temperature goes above +50°C and below −10°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

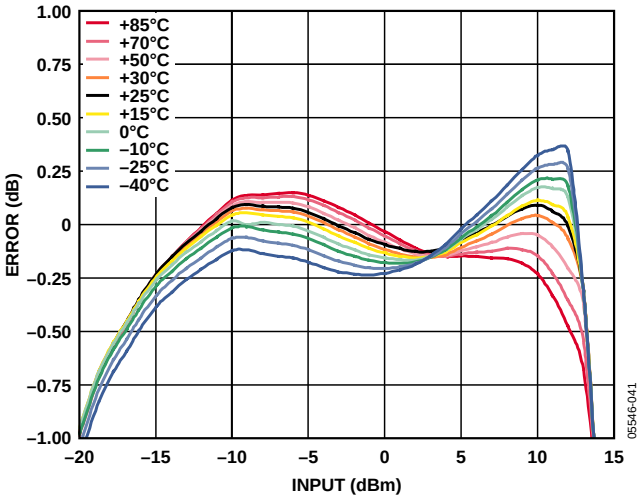

Figure 44. Typical Drift at 1.9 GHz for Various Temperatures

OPERATION ABOVE 4.0 GHz

The ADL5500 works at frequencies above 4.0 GHz, but exhibits slightly higher output voltage temperature drift. Figure 45 and Figure 46 show the error distributions of six devices at 5.0 GHz and 6.0 GHz over temperature. Although the temperature drift is larger than at lower frequencies, the error distributions at each temperature remain tight throughout the central linear region. Due to the repeatability of the drift from part-to-part, compensation can be applied to reduce the effects of temperature drift.

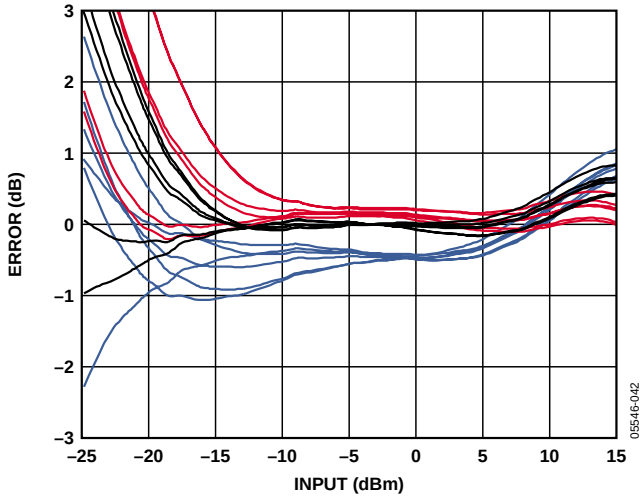

Figure 45. Temperature Drift Distributions for Six Devices at −40°C, +25°C, and +85°C After Ambient Normalization, Frequency 5.0 GHz, Supply 5.0 V

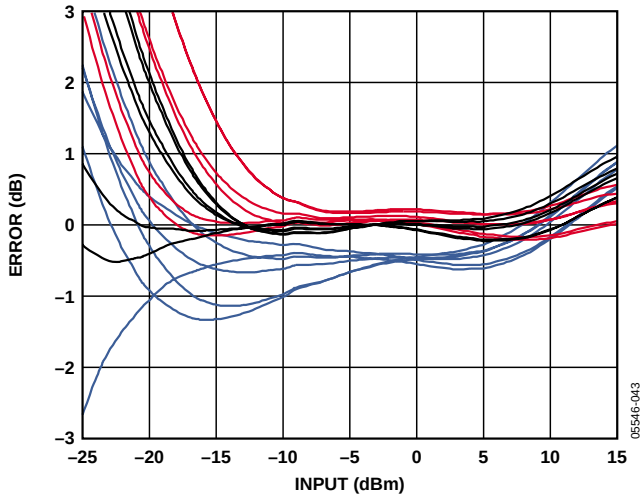

Figure 46. Temperature Drift Distributions for Six Devices at −40°C, +25°C, and +85°C After Ambient Normalization, Frequency 6.0 GHz, Supply 5.0 V

DEVICE HANDLING

The wafer-level chip scale package consists of solder bumps connected to the active side of the die. The part is lead-free with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 Application Note for additional information. WLCSP devices are bumped die; therefore, the exposed die can be sensitive to light, which can influence specified limits. Lighting in excess of 600 LUX can degrade performance.

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EVALUATION BOARD

Figure 48 shows the schematic of the ADL5500 evaluation board. The layout and silkscreen of the evaluation board layers are shown in Figure 49 to Figure 52. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by 100 pF and 0.01 µF capacitors. Table 5 details the various configuration options of the evaluation board.

Problems caused by impedance mismatch can arise using the evaluation board to examine the ADL5500 performance. One way to reduce these problems is to put a coaxial 3 dB attenuator on the RFIN SMA connector. Mismatches at the source, cable, and cable interconnection, as well as those occurring on the evaluation board, can cause these problems.

A simple (and common) example of such a problem is triple travel due to mismatch at both the source and the evaluation board. Here the signal from the source reaches the evaluation board and mismatch causes a reflection. When that reflection reaches the source mismatch, it causes a new reflection, which travels back to the evaluation board, adding to the original signal incident at the board. The resultant voltage varies with both cable length and frequency dependence on the relative phase of the initial and reflected signals. Placing the 3 dB pad at the input of the board improves the match at the board and thus reduces the sensitivity to mismatches at the source. When such precautions are taken, measurements are less sensitive to cable length and other fixture issues. In an actual application when the distance between ADL5500 and source is short and well-defined, this 3 dB attenuator is not needed.

Land Pattern and Soldering Information

Figure 47 shows the land pattern used on the ADL5500 evaluation board. Pad diameters of 0.28 mm are used with a solder paste mask opening of 0.38 mm. For the RF input trace, a trace width of 0.30 mm is used, which corresponds to a 50 Ω characteristic impedance for the dielectric material being used (FR4). All traces going to the pads are tapered down to 0.15 mm. For the RFIN line, the length of the tapered section is 0.20 mm.

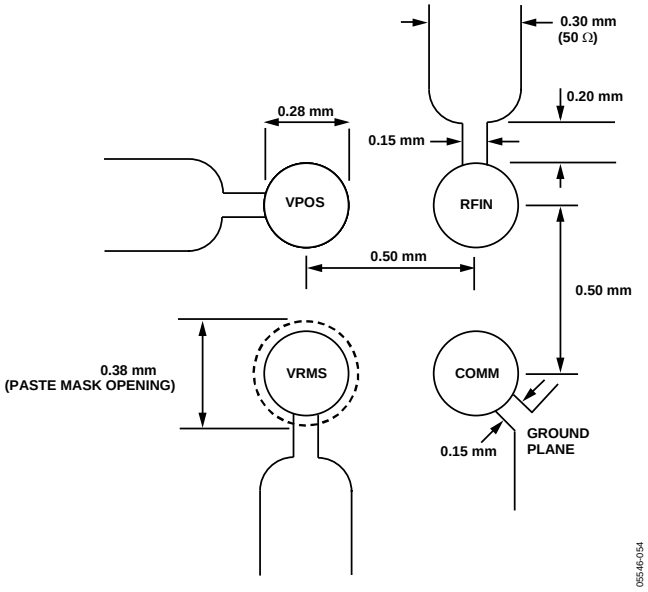

Figure 47. Land Pattern Used on the ADL5500 Evaluation Board

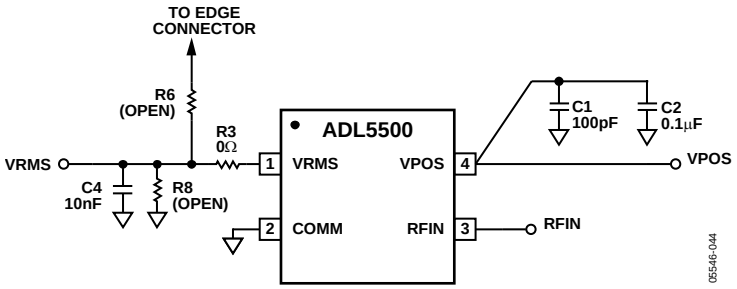

Figure 48. Evaluation Board Schematic

Table 5. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and Supply Vector Pins.	Not Applicable
C1, C2	Power Supply Decoupling. The nominal supply decoupling of 0.01 µF and 100 pF.	C1 = 0.01 µF (Size 0402) C2 = 100 pF (Size 0402)
R3, R8, C4	Output Filtering. The combination of the internal 1 kΩ output resistance and C4 produce a low-pass filter to reduce output ripple. The output can also be scaled down using the resistor divider pads, R3 and R8. In addition, resistors and capacitors can be placed in C4 and R8 to load test VRMS.	R3 = 0 Ω (Size 0402) R8 = Open (Size 0402) C4 = 10 nF (Size 0402)
R6	Alternate Interface. R6 allows VOUT to be accessible from the edge connector, which is only used for characterization.	R6 = Open (Size 0402)

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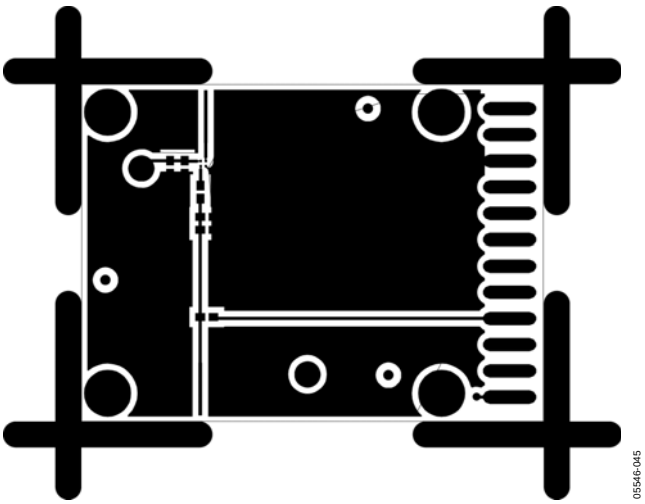

Figure 49. Layout of Component Side (WLCSP)

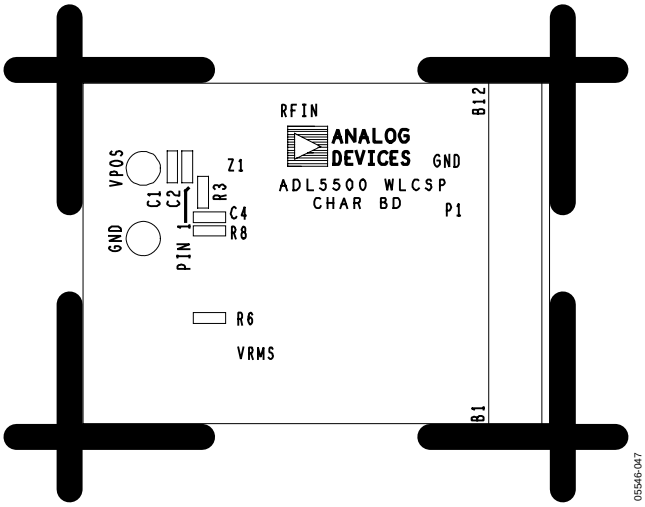

Figure 51. Silkscreen of Component Side (WLCSP)

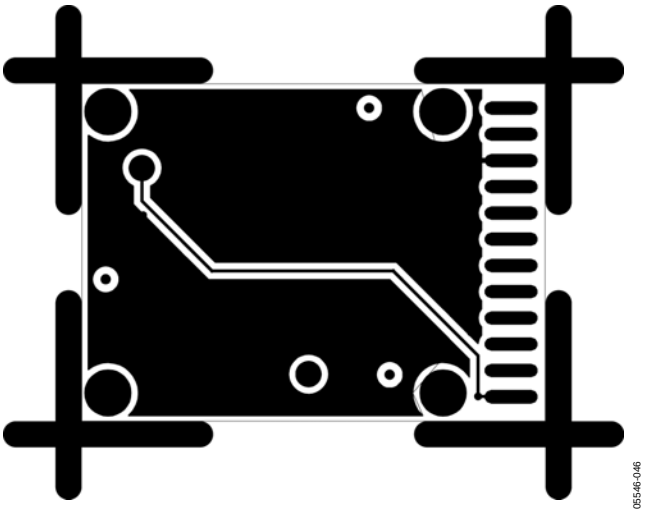

Figure 50. Layout of Circuit Side (WLCSP)

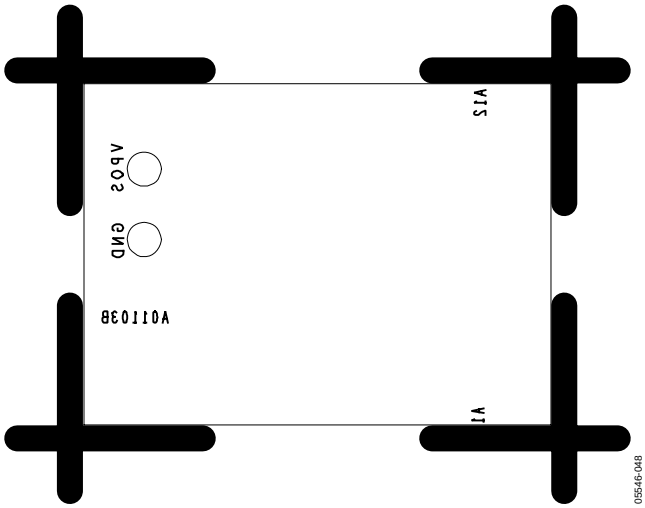

Figure 52. Silkscreen of Circuit Side (WLCSP)

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OUTLINE DIMENSIONS

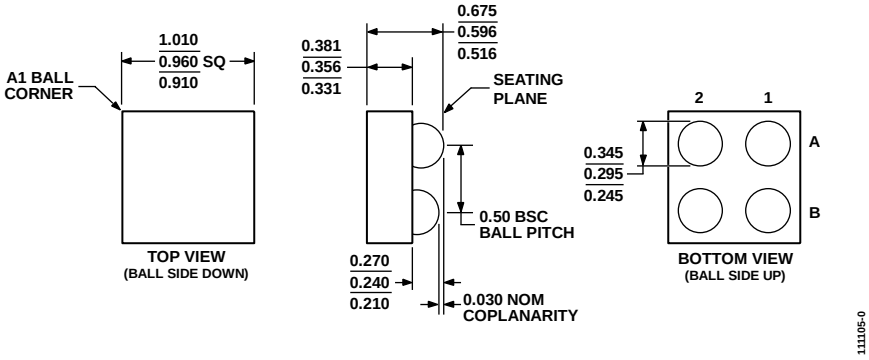

Figure 53. 4-Ball Wafer-Level Chip Scale Package [WLCSP]
(CB-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5500ACBZ-P7[1]	–40°C to +85°C	4-Ball WLCSP, 7″ Pocket Tape and Reel	CB-4	Q06	3,000
ADL5500ACBZ-P2[1]	–40°C to +85°C	4-Ball WLCSP, 7″ Pocket Tape and Reel	CB-4	Q06	250
ADL5500-EVALZ[1]		Evaluation Board			

[1] Z = Pb-free part.

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NOTES

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