CCD Signal Processor with V-Driver and *Precision Timing*™ Generator

AD9923

FEATURES

Integrated 15-channel V-driver
12-bit 36 MHz analog-to-digital converter (ADC)
Similar register map to AD9994
5-field, 10-phase vertical clock support
Complete on-chip timing generator
***Precision Timing* core with <600 ps resolution**
Correlated double sampler (CDS)
6 dB to 42 dB 10-bit variable gain amplifier (VGA)
Black level clamp with variable level control
On-chip 3 V horizontal and RG drivers
2-phase and 4-phase H-clock modes
Electronic and mechanical shutter support
On-chip driver for external crystal
On-chip sync generator with external sync input
8 mm × 8 mm CSPBGA package with 0.65 mm pitch

APPLICATIONS

Digital still cameras

GENERAL DESCRIPTION

The AD9923 is a complete 36 MHz front end solution for digital still cameras and other CCD imaging applications. Similar to the AD9994 product, the AD9923 includes the analog front end and a fully programmable timing generator combined with a 15-channel vertical driver (V-driver). A *Precision Timing* core allows adjustment of high speed clocks with approximately 600 ps resolution at 36 MHz operation.

The on-chip V-driver supports up to 15 channels for use with 5-field, 10-phase CCDs.

The analog front end includes black level clamping, CDS, VGA, and a 12-bit ADC. The timing generator and V-driver provide all the necessary CCD clocks: RG, H-clocks, vertical clocks, sensor gate pulses, substrate clock, and substrate bias control. The internal registers are programmed using a 3-wire serial interface.

Packaged in an 8 mm × 8 mm CSPBGA, the AD9923 is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

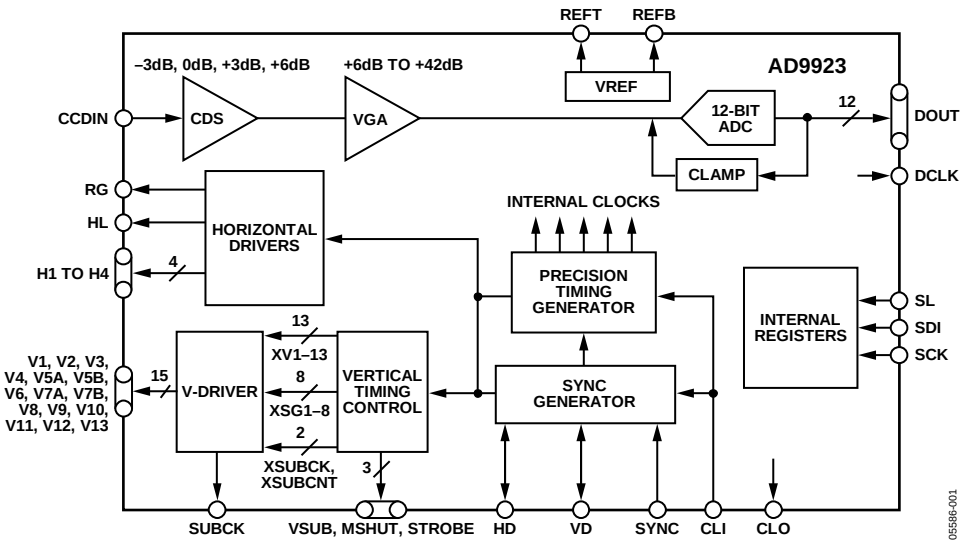

Figure 1.

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REVISION HISTORY

7/05—Revision 0: Initial Version

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SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
AFETG POWER SUPPLY VOLTAGES				
AVDD (AFE Analog Supply)	2.7	3.0	3.6	V
TCVDD (Timing Core Analog Supply)	2.7	3.0	3.6	V
RGVDD (RG Driver)	2.7	3.0	3.6	V
HVDD (HL, H1 to H4 Drivers)	2.7	3.0	3.6	V
DRVDD (Data Output Drivers)	2.7	3.0	3.6	V
DVDD (Digital)	2.7	3.0	3.6	V
V-DRIVER POWER SUPPLY VOLTAGES				
VDD1,VDD2 (V-Driver Logic)	+2.7	+3.0	+3.6	V
VH1, VH2 (V-Driver High Supply)	+11.5	+15.0	+16.5	V
VL1, VL2 (V-Driver Low Supply)	−8.5	−7.5	−5.5	V
VM1, VM2 (V-Driver Mid Supply)	−1.5	0.0	+1.5	V
VLL (SUBCK Low Supply)	−8.5	−7.5	−5.5	V
VMM (SUBCK Mid Supply)	−4.0	0.0	0.0	V
AFETG POWER DISSIPATION				
Total—36 MHz, 3.0 V Supply, 400 pF Total H-Load, 20 pF RG Load		335		mW
Standby 1 Mode		105		mW
Standby 2 Mode		1		mW
Standby 3 Mode		1		mW
Power from HVDD Only[1]		130		mW
Power from RGVDD Only		10		mW
Power from AVDD Only		75		mW
Power from TCVDD Only		40		mW
Power from DVDD Only		75		mW
Power from DRVDD Only		5		mW
V-DRIVER POWER DISSIPATION (VH = +15 V, VL = −7.5 V, VM = 0 V, VDD = 3.3 V, ALL V-DRIVER INPUTS TIED LOW)[2]				
VH1, VH2		5		mW
VL1, VL2		2.5		mW
VM1, VM2		0		mW
VDD1, VDD2		0.5		mW
MAXIMUM CLOCK RATE (CLI)	36			MHz

[1] The total power dissipated by the HVDD supply can be approximated using the equation

Total HVDD Power = [*CLOAD* × *HVDD* × *Pixel Frequency*] × *HVDD*

Reducing the H-load and/or using a lower HVDD supply reduces the power dissipation. CLOAD is the total capacitance seen by all H-outputs.

[2] V-driver power dissipation depends on the frequency of operation and the load they are driving. All inputs to the V-driver were tied low for the measurements in Table 1.

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DIGITAL SPECIFICATIONS

DRVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (POWERED by DVDD, DRVDD)					
High Level Output Voltage at I_{OH} = 2 mA	V_{OH}	VDD – 0.5			V
Low Level Output Voltage at I_{OL} = 2 mA	V_{OL}			0.5	V

H-DRIVER SPECIFICATIONS

HVDD = RGVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
RG and H-DRIVER OUTPUTS (RG, HL, and H1 to H4 POWERED by RGVDD, HVDD)				
High Level Output Voltage at Maximum Current	VDD – 0.5			V
Low Level Output Voltage at Maximum Current			0.5	V
Maximum Output Current (Programmable)	30			mA
Maximum Load Capacitance (for Each Output)	100			pF

VERTICAL DRIVER SPECIFICATIONS

VDD1, VDD2 = 3.3 V, VH1, VH2 = 15 V, VM1, VM2, VMM = 0 V, VL1, VL2, VLL = –7.5 V, 25°C.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
V-DRIVER OUTPUTS (SIMPLIFIED LOAD CONDITIONS, 3,000 pF to GROUND)					
Delay Time, VL to VM and VM to VH	t_{PLM}, t_{PMH}		35		ns
Delay Time, VM to VL and VH to VM	t_{PML}, t_{PHM}		35		ns
Rise Time, VL to VM	t_{RLM}		125		ns
Rise Time, VM to VH	t_{RMH}		260		ns
Fall Time, VM to VL	t_{FML}		220		ns
Fall Time, VH to VM	t_{FHM}		125		ns
Output Currents					
@ –7.25 V			10		mA
@ –0.25 V			–22		mA
@ +0.25 V			22		mA
@ +14.75 V			–10		mA
R_{ON}				35	Ω
SUBCK OUTPUT (SIMPLIFIED LOAD CONDITIONS, 1,000 pF to GROUND)					
Delay Time, VLL to VH	t_{PLH}		25		ns
Delay Time, VH to VLL	t_{PHL}		30		ns
Delay Time, VLL to VMM	t_{PLM}		25		ns
Delay Time, VMM to VH	t_{PMH}		25		ns
Delay Time, VH to VMM	t_{PHM}		30		ns
Delay Time, VMM to VLL	t_{PML}		25		ns
Rise Time, VLL to VH	t_{RLH}		40		ns

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Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, VLL to VMM	t_{RLM}		45		ns
Rise Time, VMM to VH	t_{RMH}		30		ns
Fall Time, VH to VLL	t_{FHL}		40		ns
Fall Time, VH to VMM	t_{FHM}		90		ns
Fall Time, VMM to VLL	t_{FML}		25		ns
Output Currents					
@ −7.25 V			20		mA
@ −0.25 V			12		mA
@ +0.25 V			12		mA
@ +14.75 V			20		mA
R_{ON}				15	Ω

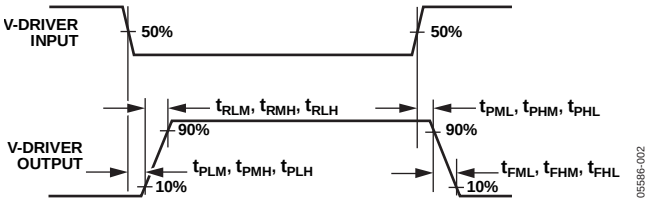

Figure 2. Definition of V-Driver Timing Specifications

ANALOG SPECIFICATIONS

AVDD = 3.0 V, f_{CLI} = 36 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS					Input characteristics definition[1]
Allowable CCD Reset Transient		0.5	1.2	V	
CDS Gain Accuracy					VGA gain = 6 dB (code 15, default value)
−3 dB CDS Gain	−3	−2.5	−2	dB	
0 dB CDS Gain (default)	0	+0.5	+1	dB	
+3 dB CDS Gain	+3	+3.5	+4	dB	
+6 dB CDS Gain	+5.5	+6	+6.5	dB	
Maximum Input Range Before Saturation					
0 dB CDS Gain (Default Setting)		1.0		V p-p	
−3 dB CDS Gain		1.4		V p-p	
+6 dB CDS Gain		0.5		V p-p	
Maximum CCD Black Pixel Amplitude					Positive offset definition
0 dB CDS Gain (Default)	−100		+200	mV	
+6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1,024		steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Minimum Gain (VGA Code 15)		6		dB	
Maximum Gain (VGA Code 1023)		42		dB	
BLACK LEVEL CLAMP					Measured at ADC output
Clamp Level Resolution		1,024		steps	
Minimum Clamp Level (Code 0)		0		LSB	
Maximum Clamp Level (Code 1023)		255		LSB	

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG-TO-DIGITAL CONVERTER (ADC)					
Resolution	12			bits	
Differential Nonlinearity (DNL)	−1.0	±0.5	+1.0	LSB	
No Missing Codes		Guaranteed			
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		2.0		V	
Reference Bottom Voltage (REFB)		1.0		V	
SYSTEM PERFORMANCE					Includes entire signal chain
Gain Accuracy					
Low Gain (VGA Code 15)	6.0	6.5	7.0	dB	Default CDS gain (0 dB)
Maximum Gain (VGA Code 1023)	42.0	42.5	43.0	dB	
Peak Nonlinearity, 500 mV Input Signal		0.1		%	12 dB gain applied
Total Output Noise		1.0		LSB rms	AC-grounded input, 6 dB gain applied
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply

[1] Input signal characteristics are defined as shown in Figure 3.

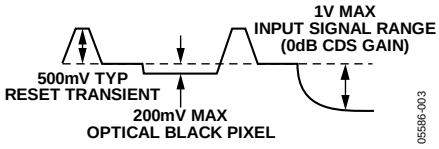

Figure 3. Signal Characteristics

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = DRVDD = 3.0 V, f_{CLI} = 36 MHz, unless otherwise noted.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK, CLI					
CLI Clock Period	t_{CONV}	27.8			ns
CLI High/Low Pulse Width		11.2	13.9	16.6	ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		6		ns
AFE CLPOB Pulse Width[1, 2]		2	20		pixels
AFE SAMPLE LOCATION[1]					
SHP Sample Edge to SHD Sample Edge	t_{S1}	11.6	13.9		ns
DATA OUTPUTS					
Output Delay from DCLK Rising Edge[1]	t_{OD}		8		ns
Inhibited Area for DOUTPHASE Edge Location		SHD		SHD + 11	edge location
Pipeline Delay from SHP/SHD Sampling to DOUT		16			cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	36			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t_{DV}	10			ns

[1] Parameter is programmable.
[2] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

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ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	To	Rating
AVDD	AVSS	−0.3 V to +3.9 V
TCVDD	TCVSS	−0.3 V to +3.9 V
HVDD	HVSS	−0.3 V to +3.9 V
RGVDD	RGVSS	−0.3 V to +3.9 V
DVDD	DVSS	−0.3 V to +3.9 V
DRVDD	DRVSS	−0.3 V to +3.9 V
VDD1	VSS1	−0.3 V to +6 V
VDD2	VSS2	−0.3 V to +6 V
VH1	VL1	−0.3 V to +25 V
VH2	VL1	−0.3 V to +25 V
VH1	VSS1	−0.3 V to +17 V
VH2	VSS1	−0.3 V to +17 V
VL1	VSS1	−17 V to +0.3 V
VL2	VSS1	−17 V to +0.3 V
VM1	VSS1	−6 V to +6 V
VM2	VSS1	−6 V to +6 V
VLL	VSS1	−17 V to +0.3 V
VMM	VSS1	−6 V to +0.3 V
V5V	VSS1	−0.3 V to +6 V
V1 to V15	VSS1	VL − 0.3 V to VH + 0.3 V
RG Output	RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H4 Output	HVSS	−0.3 V to HVDD + 0.3 V
Digital Outputs	DVSS	−0.3 V to DVDD + 0.3 V
Digital Inputs	DVSS	−0.3 V to DVDD + 0.3 V
SCK, SL, SDATA	DVSS	−0.3 V to DVDD + 0.3 V
REFT/REFB, CCDIN	AVSS	−0.3 V to AVDD + 0.3 V
Junction Temperature		150°C
Lead Temperature, 10 sec		350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

Thermal Resistance

CSP_BGA package: θ_{JA} = 40.3°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

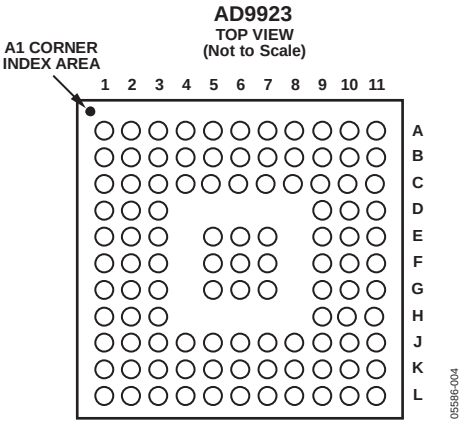

Figure 4. 105-Lead CSPBGA Package Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A7	AVDD	P	Analog Supply for AFE.
A1, A4, B2, B3, B4, B5, B6, B7	AVSS	P	Analog Ground for AFE.
B8	TCVDD	P	Analog Supply for Timing Core.
B9	TCVSS	P	Analog Ground for Timing Core.
E1	DVDD1	P	Digital Logic Power Supply 1.
F2	DVSS1	P	Digital Logic Ground 1.
K8, L7, L8	DVDD2	P	Digital Logic Power Supply 2.
K9	DVSS2	P	Digital Logic Ground 2.
D9	HVDD	P	H1 to H4, HL Driver Supply.
D10	HVSS	P	H1 to H4, HL Driver Ground.
B10	RGVDD	P	RG Driver Supply.
A10	RGVSS	P	RG Driver Ground.
L4	DRVDD	P	Data Output Driver Supply.
L5	DRVSS	P	Data Output Driver Ground.
J4	VDD1	P	V-Driver Logic Supply 1.
K5	VSS1	P	V-Driver Logic Ground 1.
L10	VDD2	P	V-Driver Logic Supply 2.
K10	VSS2	P	V-Driver Logic Ground 2.
F9	VH1	P	V-Driver High Supply 1.
D1	VH2	P	V-Driver High Supply 2.
E9	VL1	P	V-Driver Low Supply 1.
C1	VL2	P	V-Driver Low Supply 2.
C9	VM1	P	V-Driver Mid Supply 1.
D3	VM2	P	V-Driver Mid Supply 2.
F3	VLL	P	SUBCK Driver Low Supply.
E3	VMM	P	SUBCK Driver Mid Supply.
A6	CCDIN	AI	CCD Signal Input.
A5	CCDGND	AI	CCD Signal Ground.
A3	REFT	AO	Voltage Reference Top Bypass.
A2	REFB	AO	Voltage Reference Bottom Bypass.
C3	SL	DI	3-Wire Serial Load Pulse.
C2	SCK	DI	3-Wire Serial Clock.
B1	SDI	DI	3-Wire Serial Data Input.
G7	SYNC	DI	External System Synchronization Input.
E5	RSTB	DI	Reset Bar, Active Low Pulse.

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Pin No.	Mnemonic	Type[1]	Description
A8	CLI	DI	Reference Clock Input.
A9	CLO	DO	Clock Output for Crystal.
F11	H1	DO	CCD Horizontal Clock 1.
E11	H2	DO	CCD Horizontal Clock 2.
D11	H3	DO	CCD Horizontal Clock 3.
C11	H4	DO	CCD Horizontal Clock 4.
B11	HL	DO	CCD Last Horizontal Clock.
C10	RG	DO	CCD Reset Gate Clock.
K6	VSUB	DO	CCD Substrate Bias.
F5	MSHUT	DO	Mechanical Shutter Pulse.
G5	STROBE	DO	Strobe Pulse.
G6	SUBCK	DO	CCD Substrate Clock (E Shutter).
F1	DCLK	DO	Data Clock Output.
G1	D0	DO	Data Output (LSB).
H3	D1	DO	Data Output.
H2	D2	DO	Data Output.
H1	D3	DO	Data Output.
J3	D4	DO	Data Output.
J2	D5	DO	Data Output.
J1	D6	DO	Data Output.
K3	D7	DO	Data Output.
K2	D8	DO	Data Output.
K1	D9	DO	Data Output.
L3	D10	DO	Data Output.
L2	D11	DO	Data Output (MSB).
D2	VD	DIO	Vertical Sync Pulse. Input in slave mode, output in master mode.
E2	HD	DIO	Horizontal Sync Pulse. Input in slave mode, output in master mode.
C8	V1	VO3	CCD Vertical Transfer Clock.
G10	V2	VO2	CCD Vertical Transfer Clock.
E7	V3	VO3	CCD Vertical Transfer Clock.
G9	V4	VO2	CCD Vertical Transfer Clock.
C4	V5A	VO3	CCD Vertical Transfer Clock.
C5	V5B	VO3	CCD Vertical Transfer Clock.
F10	V6	VO2	CCD Vertical Transfer Clock.
C6	V7A	VO3	CCD Vertical Transfer Clock.
C7	V7B	VO3	CCD Vertical Transfer Clock.
G11	V8	VO2	CCD Vertical Transfer Clock.
H11	V9	VO2	CCD Vertical Transfer Clock.
H10	V10	VO2	CCD Vertical Transfer Clock.
F6	V11	VO3	CCD Vertical Transfer Clock.
F7	V12	VO3	CCD Vertical Transfer Clock.
E10	V13	VO2	CCD Vertical Transfer Clock.
K11	V5V	DI	Bias Voltage. Must be tied to +3 V signal through diode (See Figure 81).
J5	TEST0	DI	Test Input. Must be tied to VSS1 or VSS2.
J7	TEST1	DI	Test Input. Must be tied to VSS1 or VSS2.
K4	TEST2	DI	Test Input. Must be tied to VDD1 or VDD2.
J8	TEST3	DI	Test Input. Must be tied to VDD1 or VDD2.
A11, E6, H9, J6, J9, J10, J11, K7, L1, L6, L9, L11, G2, G3	NC		No Connect.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DIO = digital input/output, P = power, VO2 = vertical driver output 2-level, VO3 = vertical driver output 3-level.

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TYPICAL PERFORMANCE CHARACTERISTICS

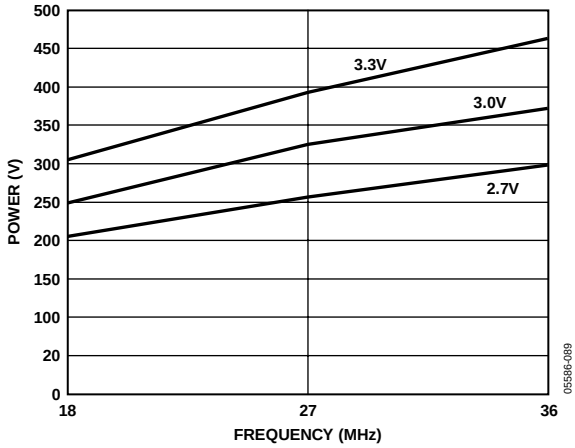

Figure 5. Power vs. Sample Rate

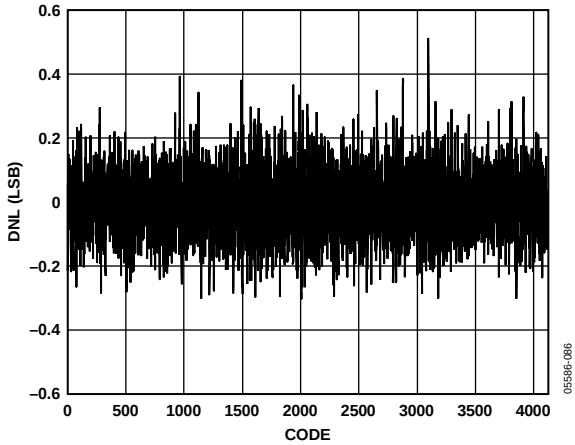

Figure 6. Typical DNL Performance

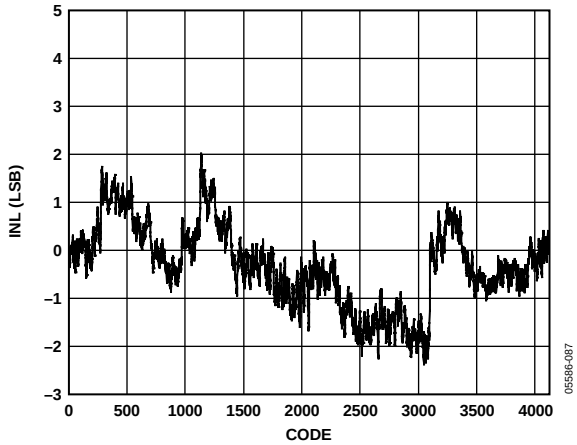

Figure 7. Typical INL Performance

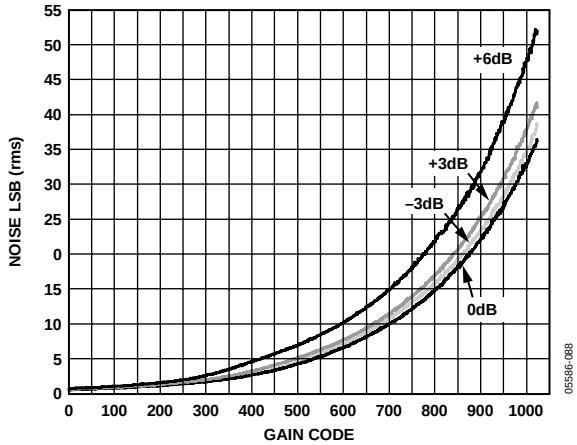

Figure 8. Output Noise vs. VGA Gain

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EQUIVALENT CIRCUITS

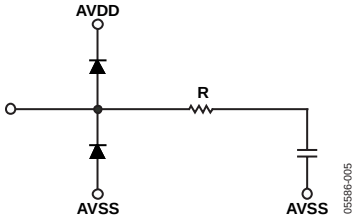

Figure 9. CCDIN, CCDGND

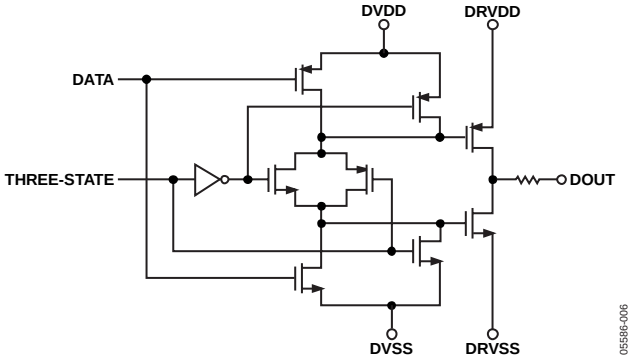

Figure 10. Digital Data Outputs

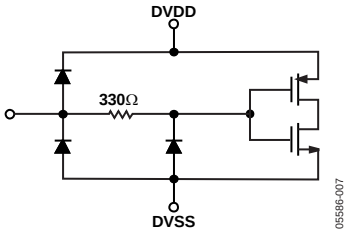

Figure 11. Digital Inputs

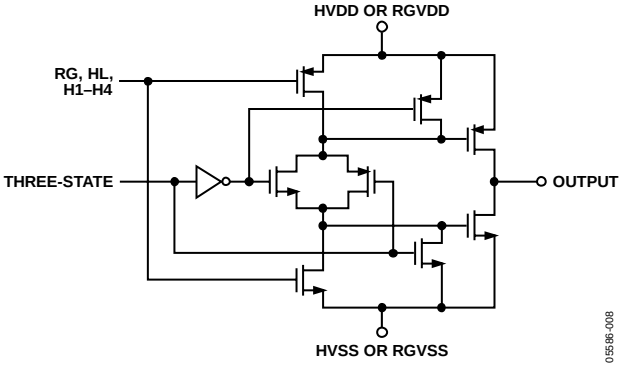

Figure 12. HL, H1 to H4 and RG Drivers

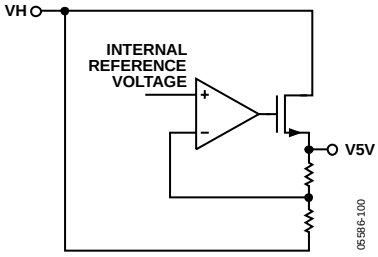

Figure 13. V5V

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TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4,096 codes, respectively, must be present over all operating conditions.

Integral Nonlinearity (INL)
The deviation of each code measured from a true straight line between the zero and full-scale values. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each output code to the true straight line.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the AD9923 output from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1.5 LSB beyond the last code transition. The deviation is measured from the middle of each output code to the true straight line. The error is expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately gained up to fill the full-scale range of the ADC.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB, and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage, using the relationship

$$1 \text{ LSB} = (\textit{ADC full scale}/2^n \text{ codes})$$

where *n* is the bit resolution of the ADC and *1 LSB* is 0.488 mV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in the data outputs for a given step change in the supply voltage.

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THEORY OF OPERATION

Figure 14 shows the typical system block diagram for the AD9923 in master mode. The CCD output is processed by the AD9923 AFE circuitry, which consists of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, CCD timing parameters are programmed into the AD9923 from the system microprocessor through the 3-wire serial interface. The AD9923 generates the CCD horizontal and vertical clocks and the internal AFE clocks from the system master clock, CLI, which is provided by the image processor or external crystal. External synchronization is provided by a sync pulse from the microprocessor, which resets internal counters and resyncs the VD and HD outputs.

Alternatively, the AD9923 can be operated in slave mode, in which the VD and HD are provided externally from the image processor. In this mode, the AD9923 timing is synchronized with VD and HD.

The H-drivers for HL, H1 to H4, and RG are included in the AD9923, allowing these clocks to be directly connected to the CCD. An H-driver voltage, HVDD, of up to 3.3 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9923 also includes programmable MSHUT and STROBE outputs, which can be used to trigger mechanical shutter and strobe (flash) circuitry.

Figure 15 and Figure 16 show the maximum horizontal and vertical counter dimensions for the AD9923. Internal horizontal and vertical clocking is controlled by these counters to specify line and pixel locations. The maximum HD length is 8192 pixels per line, and the maximum VD length is 4096 lines per field.

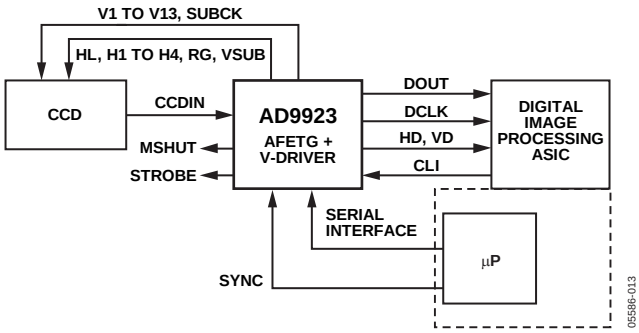

Figure 14. Typical System Block Diagram, Master Mode

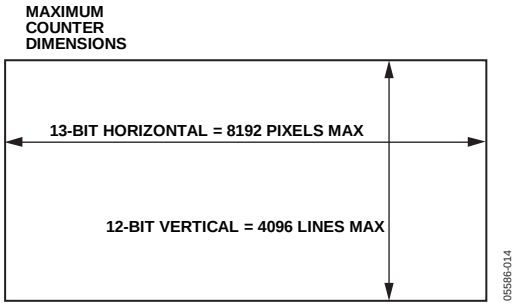

Figure 15. Vertical and Horizontal Counters

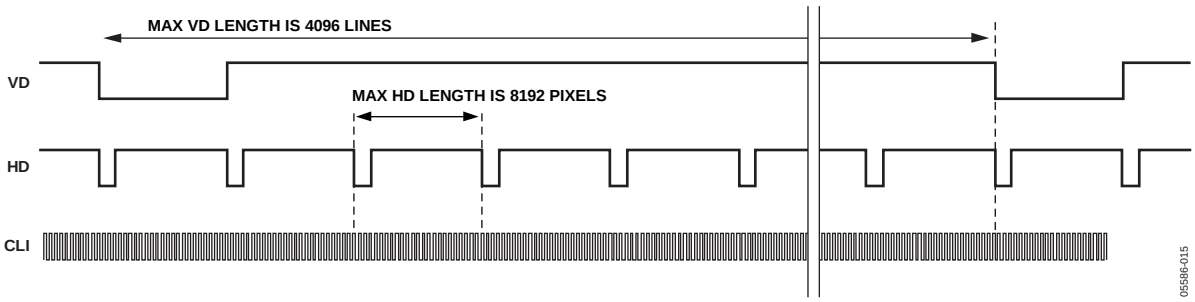

Figure 16. Maximum VD/HD Dimensions

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PRECISION TIMING
HIGH SPEED TIMING GENERATION

The AD9923 generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation for generating the timing used for both the CCD and the AFE. It consists of reset gate RG, horizontal drivers H1 to H4 and HL, and sample clocks SHP and SHD. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE-correlated double sampling.

The high speed timing of the AD9923 operates the same in master and slave modes. For more information on synchronization and pipeline delays, see the Power-Up and Synchronization in Slave Mode section.

Timing Resolution

The *Precision Timing* core uses a 1× master clock input (CLI) as a reference. The frequency of this clock should match the CCD pixel clock frequency. Figure 17 illustrates how the internal timing core divides the master clock period into 48 steps, or edge positions. Using a 36 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 0.6 ns. If a 1× system clock is not available, a 2× reference clock can be used by programming the CLIDIVIDE register (Address 0x30). The AD9923 then internally divides the CLI frequency by 2.

The AD9923 includes a master clock output, CLO, which is the inverse of CLI. This output is intended to be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9923. For more information on using a crystal, see Figure 79.

High Speed Clock Programmability

Figure 18 shows how the high speed clocks, RG, HL, H1 to H4, SHP, and SHD, are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. The horizontal clocks, HL, H1, and H3, have programmable rising and falling edges and polarity control. The H2 and H4 clocks are inverses of the H1 and H3 clocks, respectively. Table 9 summarizes the high speed timing registers and their parameters. Figure 19 shows the typical 2-phase, H-clock operation, in which H3 and H4 are programmed for the same edge location as H1 and H2.

The edge location registers are six bits wide, but there are only 48 valid edge locations available. Therefore, the register values are mapped into four quadrants, each of which contains 12 edge locations. Table 10 shows the correct register values for the corresponding edge locations. Figure 20 shows the default timing locations for high speed clock signals.

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9923 features on-chip output drivers for the RG and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG current can be adjusted for optimum rise/fall times in a particular load by using the H1 to H4, HL, and RGDRV registers (Address 0x36). The 3-bit drive setting for each output can be adjusted in 4.1 mA increments, with the minimum setting of 0 equal to 0 mA or three-state, and the maximum setting of 7 equal to 30.1 mA.

As shown in Figure 18, Figure 19, and Figure 20, the H2 and H4 outputs are inverses of H1 and H3 outputs, respectively. The H1/H2 crossover voltage is approximately 50% of the output swing. The crossover voltage is not programmable.

Digital Data Outputs

The AD9923 data output and DCLK phase are programmable using the DOUTPHASE register (Address 0x38, Bits[5:0]). Any edge from 0 to 47 can be programmed, as shown in Figure 21. Normally, the DOUT and DCLK signals track in phase, based on the DOUTPHASE register contents. The DCLK output phase can also be held fixed with respect to the data outputs by setting the DCLKMODE register to high (Address 0x38, Bit[8]). In this mode, the DCLK output remains at a fixed phase equal to a delayed version of CLI, and the data output phase remains programmable. For more detail, see the Analog Front End Description/Operation section.

There is a fixed output delay from the DCLK rising edge to the DOUT transition, called t_{OD}. This delay can be programmed to four values between 0 ns and 12 ns, using the DOUTDELAY register (Address 0x38, Bits[10:9]). The default value is 8 ns.

The pipeline delay through the AD9923 is shown in Figure 22. After the CCD input is sampled by SHD, there is a 16-cycle delay before the data is available.

Table 9. Timing Core Register Parameters for HL, H1 to H4, RG, SHP/SHD

Parameter	Length (Bits)	Range	Description
Polarity	1	High/low	Polarity control for HL, H1, H3, and RG (0 = no inversion, 1 = inversion)
Positive Edge	6	0 to 47 edge location	Positive edge location for HL, H1, H3, and RG (H2/H4 are inverses of H1/H3, respectively)
Negative Edge	6	0 to 47 edge location	Negative edge location for HL, H1, H3, and RG (H2/H4 are inverses of H1/H3, respectively)
Sampling Location	6	0 to 47 edge location	Sampling location for internal SHP and SHD signals
Drive Strength	3	0 to 7 current steps	Drive current for HL, H1 to H4, and RG outputs (4.1 mA per step)

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Table 10. *Precision Timing* Edge Locations

Quadrant	Edge Location (Decimal)	Register Value (Decimal)	Register Value (Binary)
I	0 to 11	0 to 11	000000 to 001011
II	12 to 23	16 to 27	010000 to 011011
III	24 to 35	32 to 43	100000 to 101011
IV	36 to 47	48 to 59	110000 to 111011

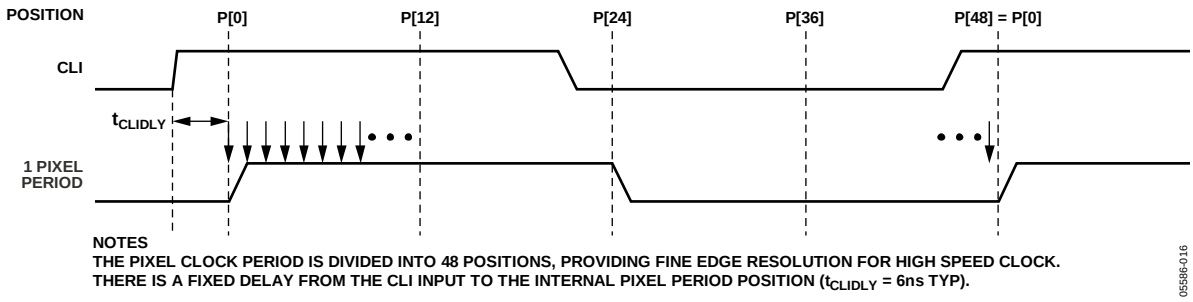

Figure 17. High Speed Clock Resolution from CLI Master Clock Input

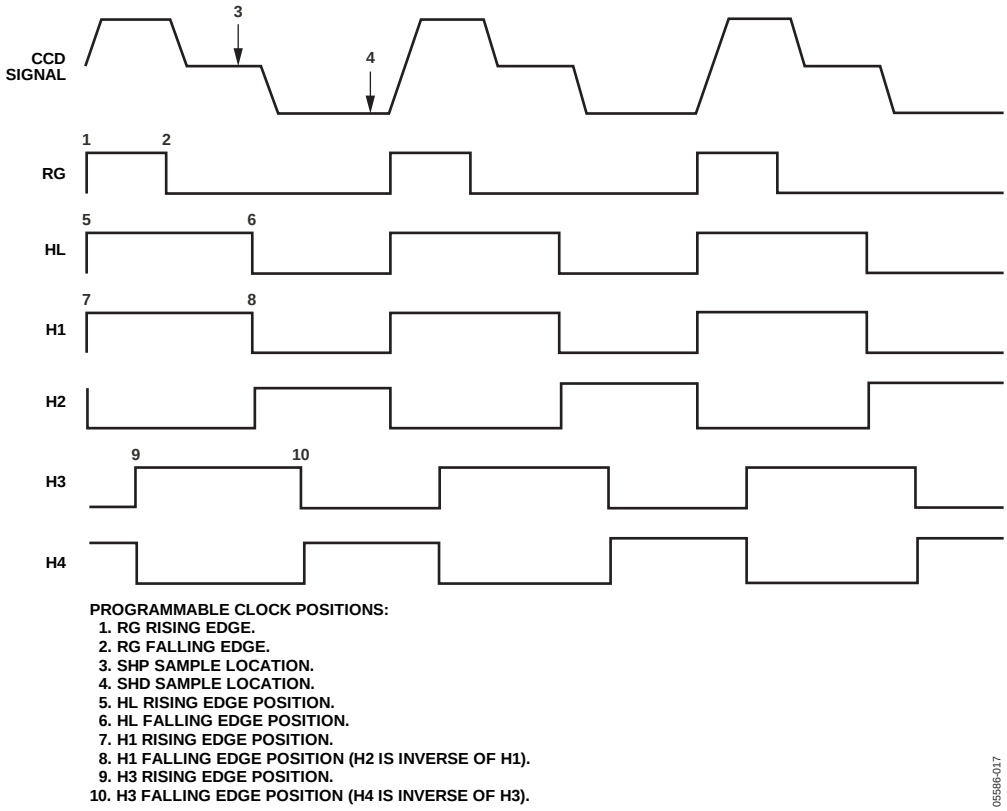

Figure 18. High Speed Clock Programmable Locations

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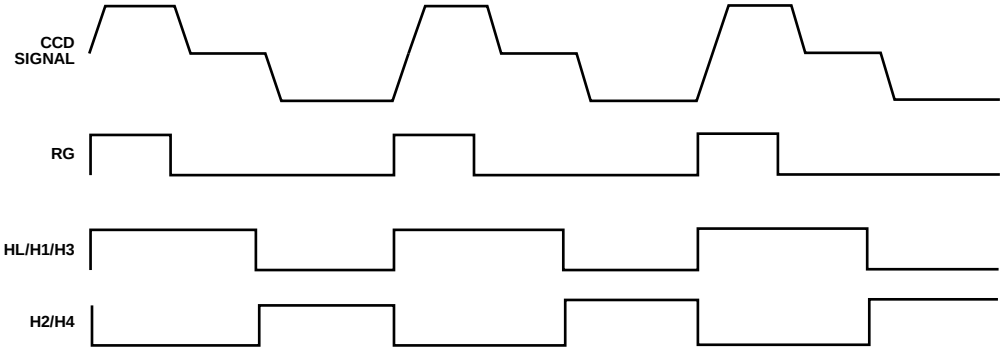
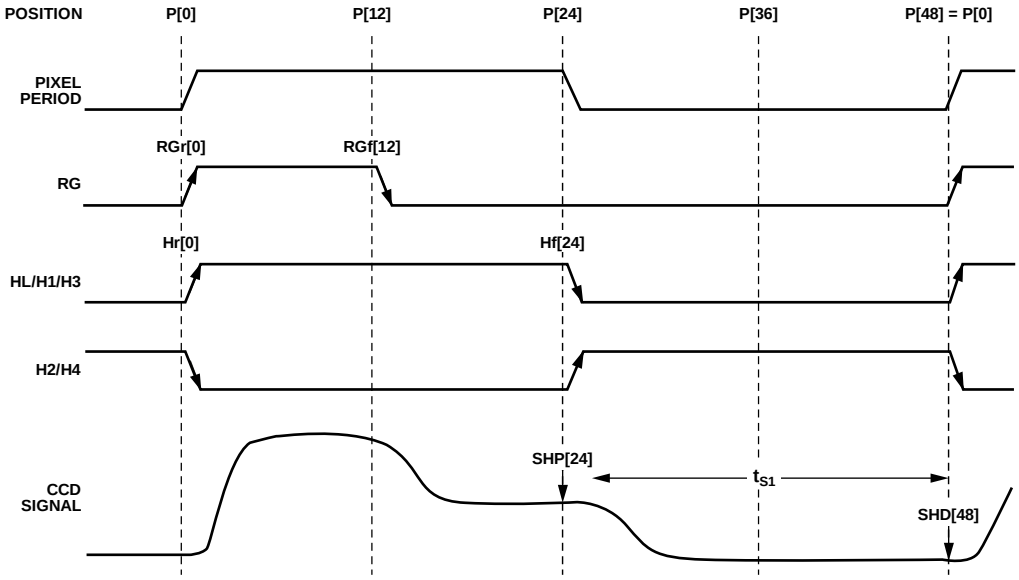


NOTES
1. USING THE SAME TOGGLE POSITIONS FOR H1 AND H3 GENERATES STANDARD 2-PHASE H-CLOCKING.

05586-018

Figure 19. 2-Phase H-Clock Operation



NOTES
1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 48 POSITIONS WITHIN ONE PIXEL PERIOD.
2. DEFAULT POSITIONS FOR EACH SIGNAL ARE SHOWN.

05586-019

Figure 20. High Speed Timing Default Locations

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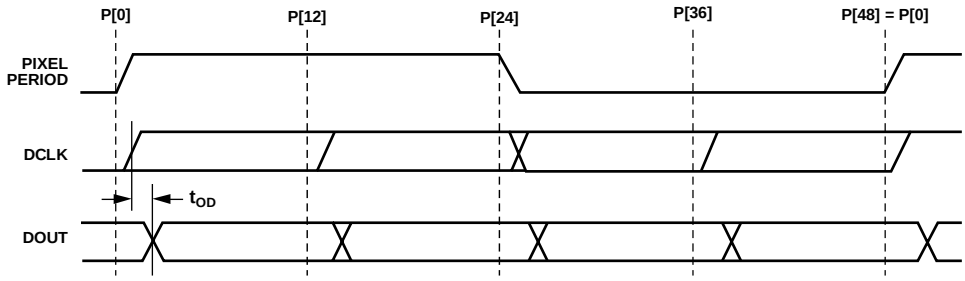
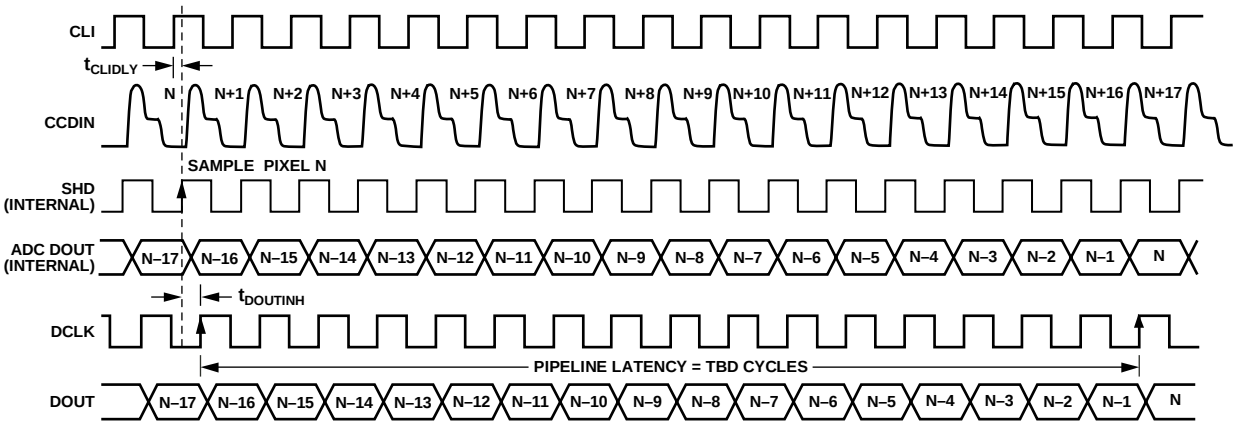


NOTES
1. DATA OUTPUT (DOUT) AND DCLK PHASE ARE ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
2. WITHIN 1 CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO 48 DIFFERENT LOCATIONS.
3. OUTPUT DELAY (t_{OD}) FROM DCLK RISING EDGE TO DOUT RISING EDGE IS PROGRAMMABLE.

05586-020

Figure 21. Digital Output Phase Adjustment



NOTES
1. TIMING VALUES SHOWN ARE SHDLOC = 0, WITH DCLKMODE = 0.
2. HIGHER VALUES OF SHD AND/OR DOUTPHASE SHIFT DOUT TRANSITION TO THE RIGHT WITH RESPECT TO CLI LOCATION.
3. INHIBIT TIME FOR DOUT PHASE IS DEFINED BY $t_{DOUTINH}$, WHICH IS EQUAL TO SHDLOC PLUS 11 EDGES. IT IS RECOMMENDED THAT THE 12 EDGE LOCATIONS FOLLOWING SHDLOC NOT BE USED FOR THE DOUTPHASE LOCATION.
4. RECOMMENDED VALUE FOR DOUT PHASE IS TO USE THE SHPLOC EDGE OR THE 11 EDGES FOLLOWING SHPLOC.
5. RECOMMENDED VALUE FOR t_{OD} (DOUT DLY) IS 4ns.
6. THE DOUT LATCH CAN BE BYPASSED USING REGISTER 0x01, BIT [1] = 1 SO THAT THE ADC DATA OUTPUTS APPEAR DIRECTLY AT THE DOUT PINS. THIS CONFIGURATION IS RECOMMENDED IF THE ADJUSTABLE DOUT PHASE IS NOT REQUIRED.

05586-021

Figure 22. Digital Data Output Pipeline Delay

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HORIZONTAL CLAMPING AND BLANKING

The AD9923 horizontal clamping and blanking pulses are fully programmable to suit a variety of applications. Individual controls are provided for CLPOB, PBLK, and HBLK during different regions of each field. This allows dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 23. These two signals are independently programmed using the registers in Table 11. SPOL is the start polarity for the signal, and TOG1 and TOG2 are the first and second toggle positions of the pulse. Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK can be programmed for each V-sequence. As described in the Vertical Timing Generation section, several V-sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK.

Figure 46 shows how the sequence change positions divide the readout field into regions. A different V-sequence can be assigned to each region, allowing the CLPOB and PBLK signals to change with each change in the vertical timing. Unused CLPOB and PBLK toggle positions should be set to 8191.

CLPOB and PBLK Masking Area

The AD9923 allows the CLPOB and/or PBLK signals to be disabled during certain lines in the field without changing the existing CLPOB and/or PBLK pattern settings.

To use CLPOB masking, the CLPMASKSTART and CLPMASKEND registers are programmed to specify the starting and ending lines in the field where the CLPOB patterns are ignored. There are three sets of CLPMASKSTART and CLPMASKEND registers, allowing up to three CLPOB masking areas to be created.

CLPOB masking registers are not specific to a given V-sequence; they are active for any existing field of timing. To disable the CLPOB masking feature, set these registers to the maximum value, 0xFFF (default value).

To use PBLK masking, the PBLKMASKSTART and PBLKMASKEND registers are programmed to specify the starting and ending lines in the field where the PBLK patterns are ignored. There are three sets of PBLKMASKSTART and PBLKMASKEND registers, allowing up to three PBLK masking areas to be created.

PBLK masking registers are not specific to a given V-sequence; they are active for any existing field of timing. To disable the PBLK masking feature, set these registers to the maximum value, 0xFFF (default value).

Table 11. CLPOB and PBLK Pattern Registers

Register	Length (Bits)	Range	Description
CLPOBPOL	1	High/low	Starting polarity of CLPOB for each V-sequence
PBLKPOL	1	High/low	Starting polarity of PBLK for each V-sequence
CLPOBTOG1	13	0 to 8191 pixel location	First CLPOB toggle position within the line for each V-sequence
CLPOBTOG2	13	0 to 8191 pixel location	Second CLPOB toggle position within the line for each V-sequence
PBLKTOG1	13	0 to 8191 pixel location	First PBLK toggle position within the line for each V-sequence
PBLKBTOG2	13	0 to 8191 pixel location	Second PBLK toggle position within the line for each V-sequence
CLPMASKSTART	12	0 to 4095 line location	CLPOB masking area—starting line within the field (maximum of three areas)
CLPMASKEND	12	0 to 4095 line location	CLPOB masking area—ending line within the field (maximum of three areas)
PBLKMASKSTART	12	0 to 4095 line location	PBLK masking area—starting line within the field (maximum of three areas)
PBLKMASKEND	12	0 to 4095 line location	PBLK masking area—ending line within the field (maximum of three areas)

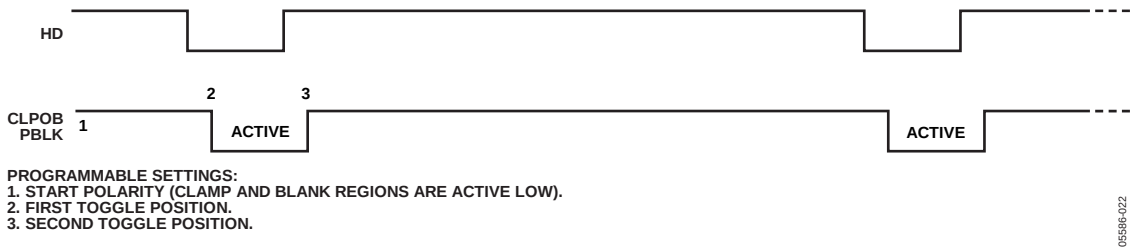

Figure 23. Clamp and Preblank Pulse Placement

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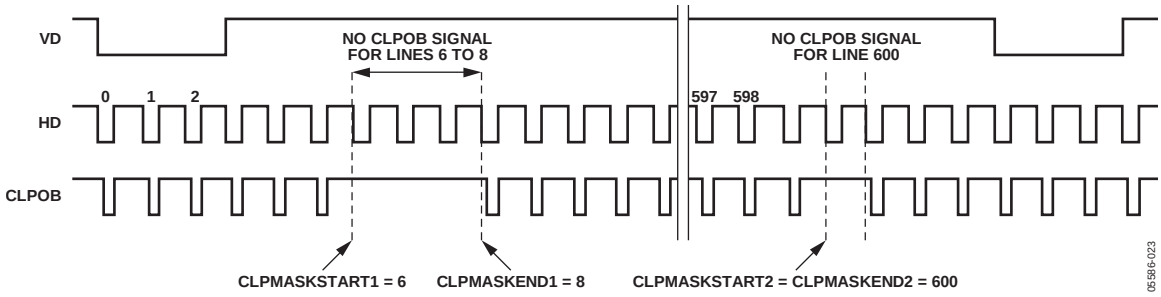

Figure 24. CLPOB Masking Example

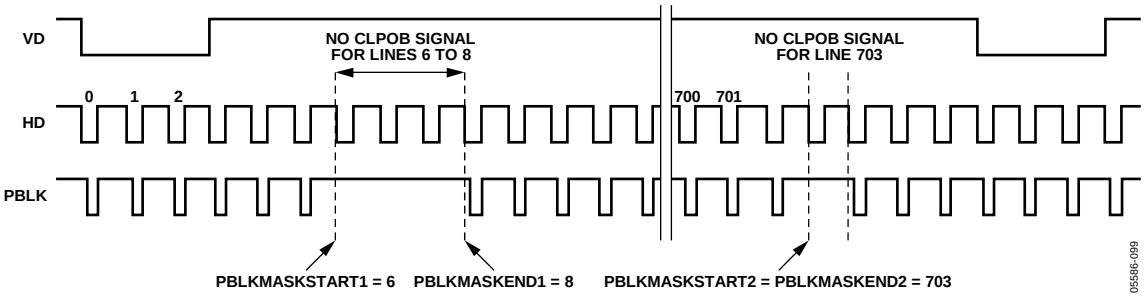

Figure 25. PBLK Masking Example

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Individual HBLK Patterns

The HBLK programmable timing shown in Figure 26 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions are used to designate the start and end positions of the blanking period. Additionally, there is a polarity control register, HBLKMASK, that designates the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK high sets H1 = H3 = low and H2 = H4 = high during blanking, as shown in Figure 27. As with CLPOB and PBLK registers, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.

Generating Special HBLK Patterns

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 28. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Table 12. HBLK Pattern Registers

Register	Length (Bits)	Range	Description
HBLKMASK	1	High/low	Masking polarity for H1, H3, HL (0 = mask low, 1 = mask high)
HBLKALT	3	0 to 7 alternation modes	Enables different odd/even alternation of HBLK toggle positions 0: disable alternation (HBLKTOGE1 to HBLKTOGE6 registers are used for each line) 1: TOGE1 and TOGE2 odd lines ,TOGE3 to TOGE6 even lines 2: TOGE1 and TOGE2 even lines, TOGE3 to TOGE6 odd lines 3: TOGE1 to TOGE6 even lines, TOGO1 to TOGE6 odd lines (freeze/resume not available) 4 to 7: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers are used for each line
HBLKTOGE1	13	0 to 4095 pixel location	HBLK first toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE2	13	0 to 4095 pixel location	HBLK second toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE3	13	0 to 4095 pixel location	HBLK third toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE4	13	0 to 4095 pixel location	HBLK fourth toggle position (for even lines only when HBLKALT = 3)
HBLKTOGE5	13	0 to 4095 pixel location	Fifth toggle position, even lines (HBLKSTART when HBLKALT = 4 to 7)
HBLKTOGE6	13	0 to 4095 pixel location	Sixth toggle position, even lines (HBLKEND when HBLKALT = 4 to 7)
HBLKLEN	13		HBLK pattern length, only used when HBLKALT = 4 to 7
HBLKREP	8		Number of HBLK pattern repetitions, only used when HBLKALT = 4 to 7
HBLKTOGO1	13	0 to 4095 pixel location	First toggle position for odd lines when HBLKALT = 3 (usually VREPA_3)
HBLKTOGO2	13	0 to 4095 pixel location	Second toggle position for odd lines when HBLKALT = 3 (usually VREPA_4)
HBLKTOGO3	13	0 to 4095 pixel location	Third toggle position for odd lines when HBLKALT = 3 (usually FREEZE1)
HBLKTOGO4	13	0 to 4095 pixel location	Fourth toggle position for odd lines when HBLKALT = 3 (usually RESUME1)
HBLKTOGO5	13	0 to 4095 pixel location	Fifth toggle position for odd lines when HBLKALT = 3 (usually FREEZE2)
HBLKTOGO6	13	0 to 4095 pixel location	Sixth toggle position for odd lines when HBLKALT = 3 (usually RESUME2)

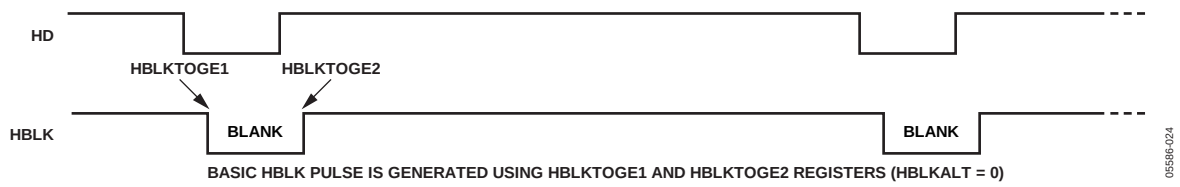

Figure 26. Typical Horizontal Blanking (HBLK) Pulse Placement

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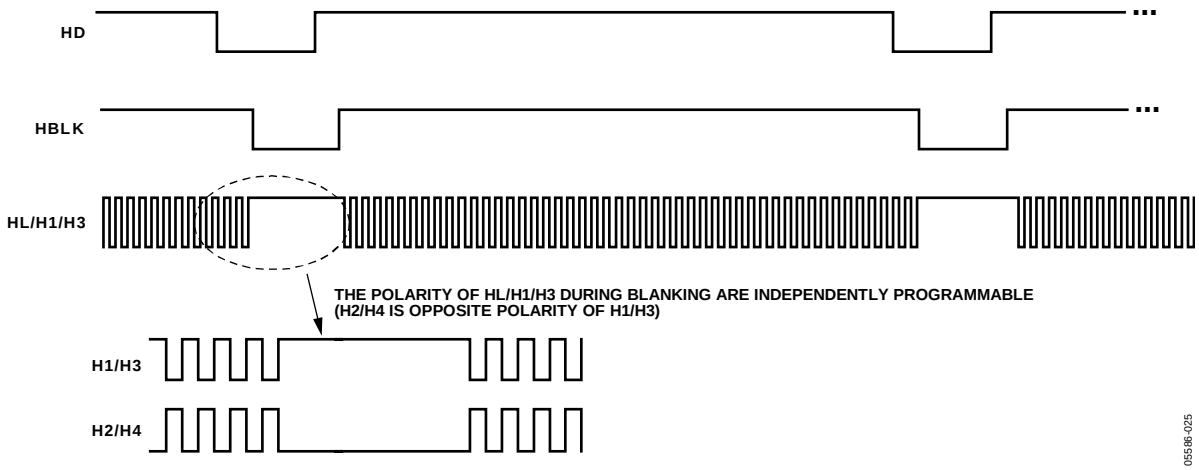

Figure 27. HBLK Masking Polarity Control

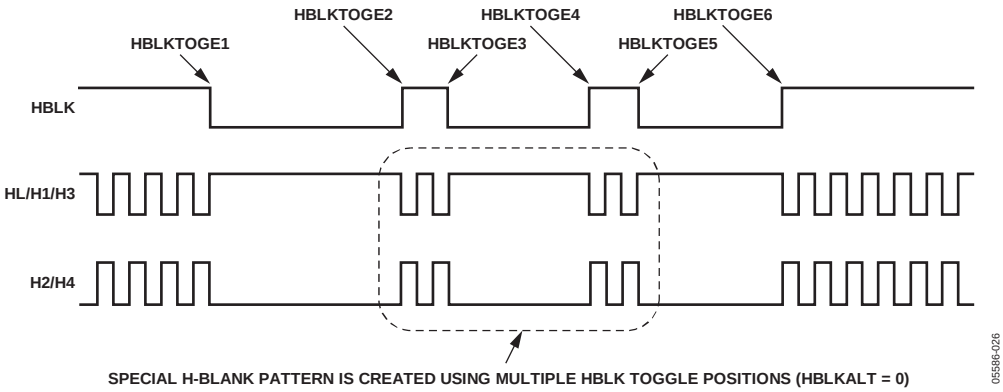

Figure 28. Using Multiple Toggle Positions for HBLK (HBLKALT = 0)

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Generating HBLK Line Alternation

The AD9923 can alternate different HBLK toggle positions on odd and even lines. This feature can be used in conjunction with V-pattern odd/even alternation, or on its own. When 1 is written to the HBLKALT register, HBLKTOGE1 and HBLKTOGE2 are used on odd lines, and HBLKTOGE3 to HBLKTOGE6 are used on even lines. Writing 2 to the HBLKALT register gives the opposite result: HBLKTOGE1 and HBLKTOGE2 are used on even lines, and HBLKTOGE3 to HBLKTOGE6 are used on odd lines. When 3 is written to the HBLKALT register, all six even toggle positions, HBLKTOGE1 to HBLKTOGE6, are used on even lines. There are also six additional toggle positions, HBLKTOGO1 to HBLKTOGE6, for odd lines. These registers are normally used for VPAT Group A, VPAT Group B, and freeze/resume functions, but when HBLKALT = 3, these registers become the odd line toggle positions for HBLK.

Another HBLK feature is enabled by writing 4 to 7 to HBLKALT. In these modes, the HBLK pattern is generated using a different set of registers—HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP—along with four toggle positions. This allows for multiple repeats of the HBLK signal, as shown in Figure 32.

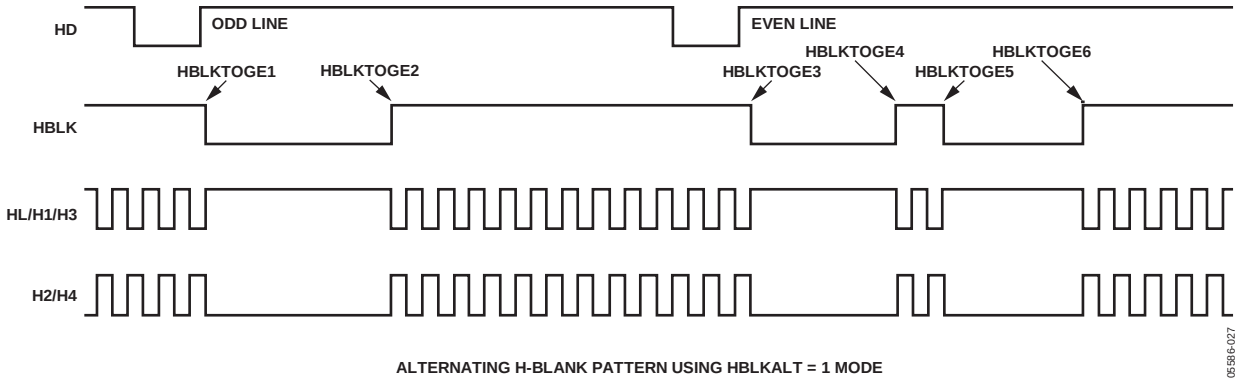

Figure 29. HBLK Odd/Even Alternation Using HBLKALT = 1

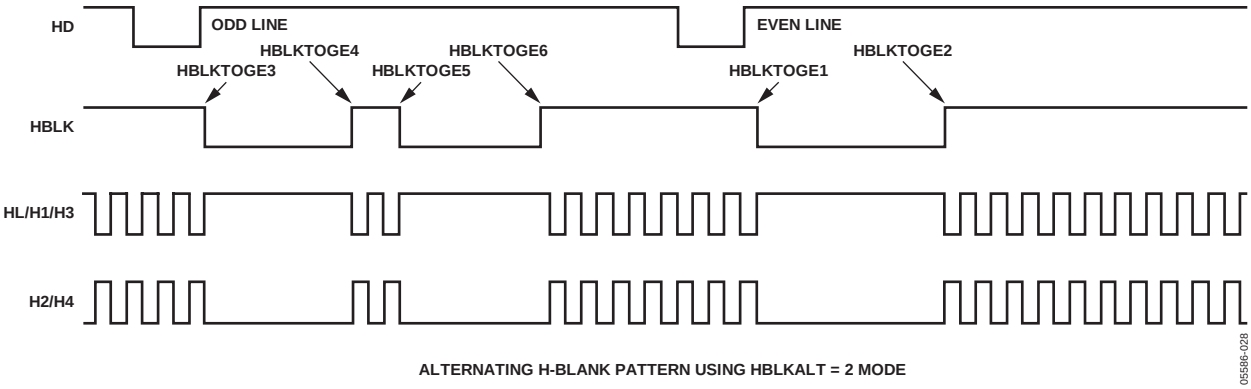

Figure 30. HBLK Odd/Even Alternation Using HBLKALT = 2

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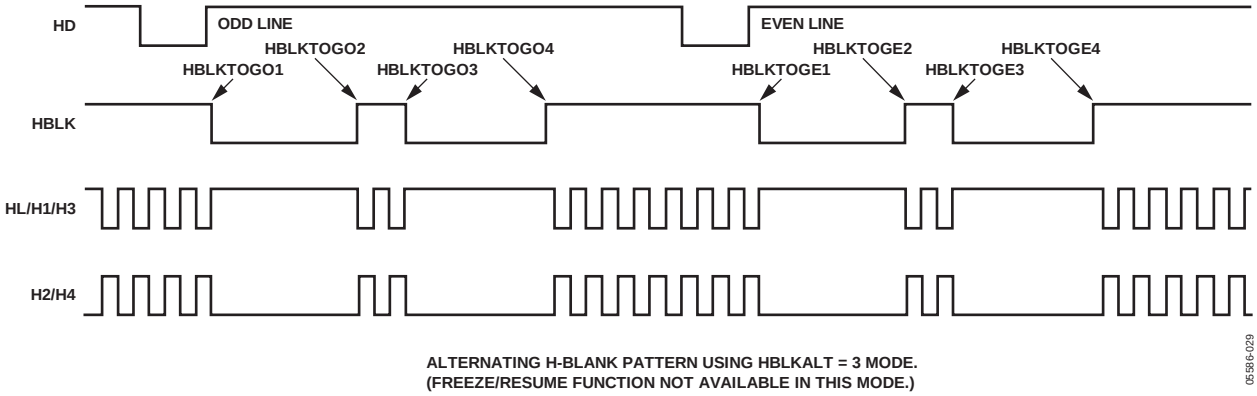

Figure 31. HBLK Odd/Even Alternation Using HBLKALT = 3

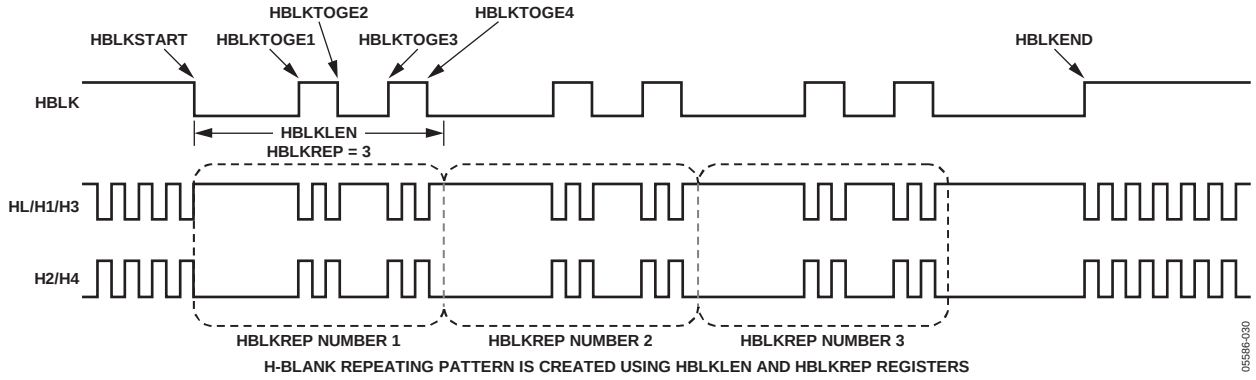

Figure 32. HBLK Repeating Pattern Using HBLKALT = 4 to 7

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Increasing H-Clock Width During HBLK

The AD9923 allows the H1 to H4 pulse width to be increased during the HBLK interval. The H-clock pulse width can increase by reducing the H-clock frequency (see Table 13).

The HBLKWIDTH register (Register 0x35, Bits[6:4]) is a 3-bit register that allows the H-clock frequency to be reduced by 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, or 1/14. The reduced frequency only occurs for H1 to H4 pulses that are located within the HBLK area.

Note: The AD9923 ignores the HBLKMASK polarity if HBLKWIDTH ≠ 0 and HBLKALT = 4 to 7. In this case, H1, H3, and HL masking polarities during the HBLK region are forced low and H2 and H4 masking polarities are forced high.

Table 13. HBLK Width Register

Register	Length (Bits)	Range	Description
HBLKWIDTH	3	1× to 1/14× pixel rate	Controls H1 to H4 width during HBLK as a fraction of pixel rate 0: same frequency as the pixel rate 1: 1/2 pixel frequency, that is, doubles the H1 to H4 pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency 6: 1/12 pixel frequency 7: 1/14 pixel frequency

Horizontal Timing Sequence Example

Figure 33 shows an example of a CCD layout. The horizontal register contains 28 dummy pixels that occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 OB pixels in the back.

Figure 34 shows the basic sequence layout to use during the effective pixel readout. The 48 OB pixels at the end of each line are used for CLPOB signals. PBLK is optional and often used to blank the digital outputs during the noneffective CCD pixels. HBLK is used during the vertical shift interval.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes can be used, such as adding a separate sequence to clamp during the entire line of OB pixels. This requires configuring a separate V-sequence for reading the OB lines.

The CLPMASKSTART and CLPMASKEND registers can be used to disable the CLPOB on a few lines without affecting the setup of the clamp sequences.

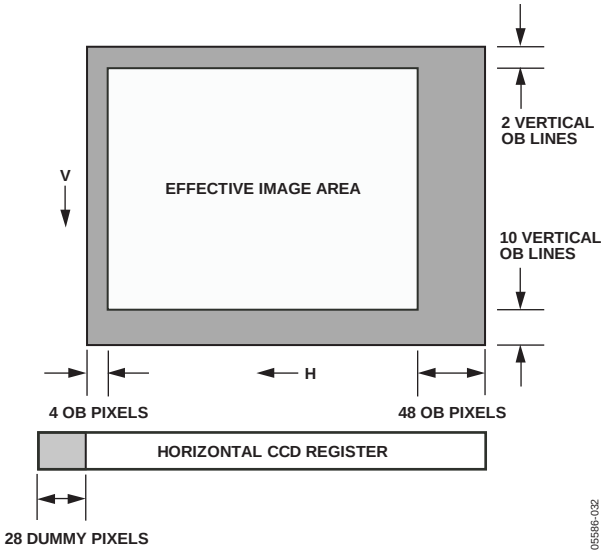

Figure 33. CCD Configuration Example

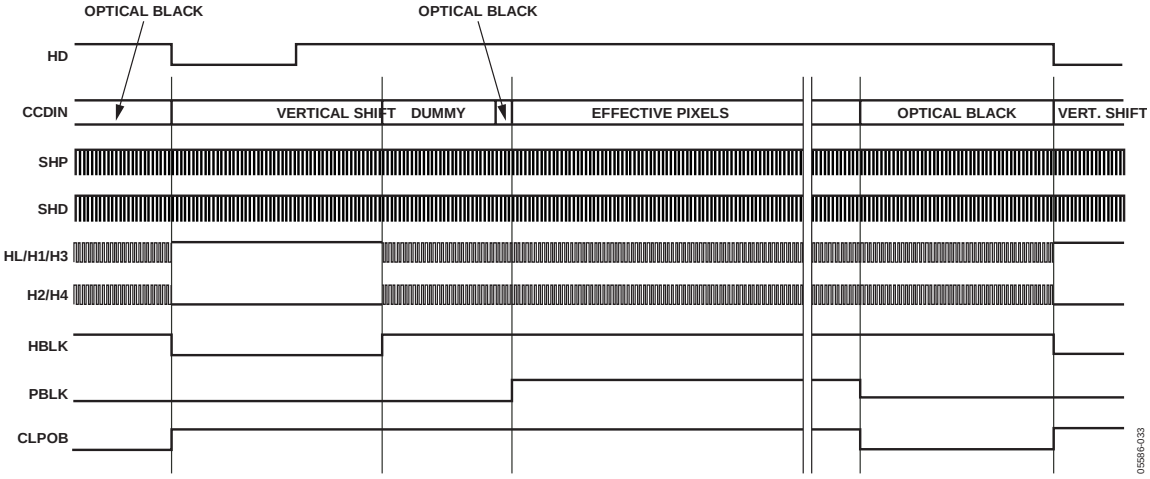

Figure 34. Horizontal Sequence Example

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VERTICAL TIMING GENERATION

The AD9923 provides a very flexible solution for generating vertical CCD timing; it can support multiple CCDs and different system architectures. The 13-phase vertical transfer clocks, XV1 to XV13, are used to shift lines of pixels into the horizontal output register of the CCD. The AD9923 allows these outputs to be individually programmed into various readout configurations, using a four-step process as shown in Figure 35.

1. Use the vertical pattern group registers to create the individual pulse patterns for XV1 to XV13.
2. Use the V-pattern groups to build the sequences and add more information.
3. Construct the readout for an entire field by dividing the field into regions and assigning a sequence to each region. Each field can contain up to nine regions to accommodate different steps, such as high speed line shifts and unique vertical line transfers, of the readout. The total number of V-patterns, V-sequences, and fields are programmable and limited by the number of registers. High speed line shifts and unique vertical transfers are examples of the different steps required for readout.
4. Use the MODE register to combine fields in any order for various readout configurations.

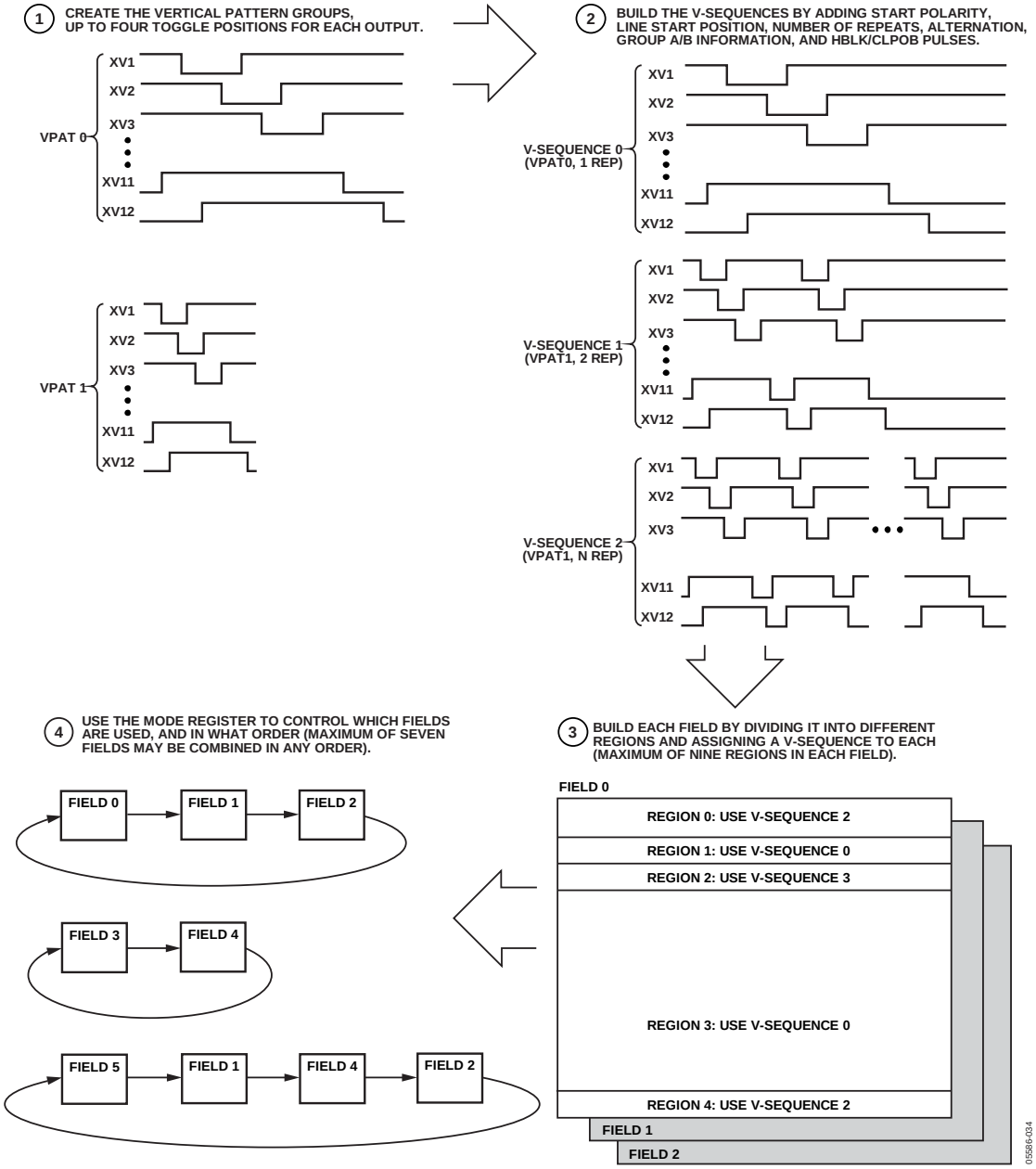

Figure 35. Summary of Vertical Timing Generation

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Vertical Pattern (VPAT) Groups

A vertical pattern (VPAT) group defines the individual pulse pattern for each XV1 to XV13 output signal. Table 14 summarizes the registers that are available for generating each VPAT group. The first, second, third, fourth, fifth, and sixth toggle positions (XVTOG1, XVTOG2, XVTOG3, XVTOG4, XVTOG5, XVTOG6) are the pixel locations where the pulse transitions. All toggle positions are 13-bit values that can be placed anywhere in the horizontal line.

More registers are included in the vertical sequence registers to specify the output pulses: XV1POL to XV13POL specifies the start polarity for each signal, VSTART specifies the start position of the VPAT group, and VLEN designates the total length of the VPAT group, which determines the number of pixels between each pattern repetition, if repetitions are used.

Toggle positions programmed to either Pixel 0 or Pixel 8191 are ignored. The toggle positions of unused XV-channels must be programmed to either Pixel 0 or Pixel 8191. This prevents unpredictable behavior, because the default values of the V-pattern group registers are unknown.

Table 14. Vertical Pattern Group Registers

Register	Length (Bits)	Range	Description
XVTOG1	13	0 to 8191 pixel location	First toggle position within line for each XV1 to XV12 output
XVTOG2	13	0 to 8191 pixel location	Second toggle position
XVTOG3	13	0 to 8191 pixel location	Third toggle position
XVTOG4	13	0 to 8191 pixel location	Fourth toggle position
XVTOG5	13	0 to 8191 pixel location	Fifth toggle position
XVTOG6	13	0 to 8191 pixel location	Sixth toggle position

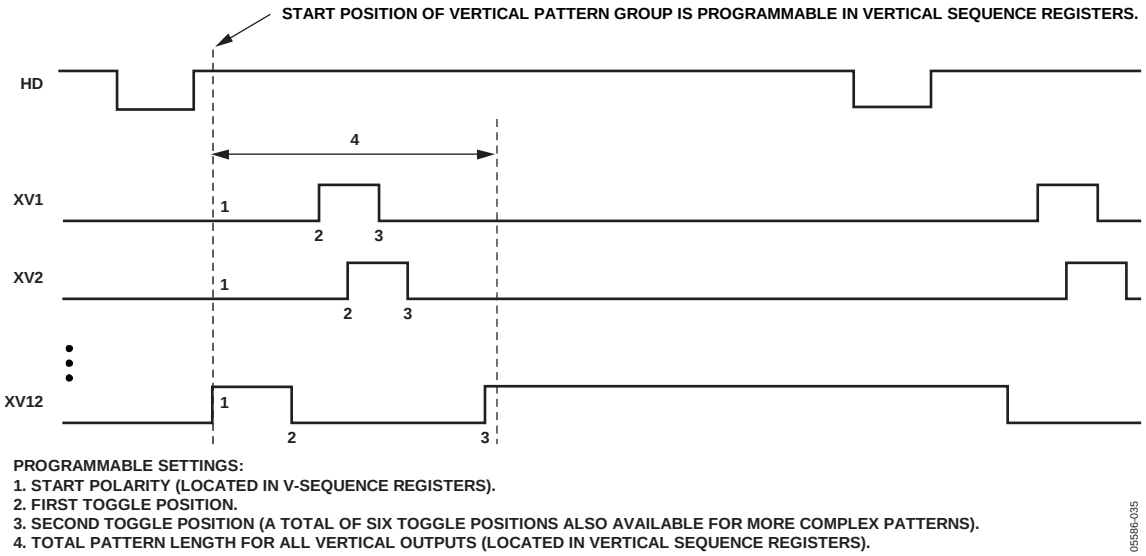

Figure 36. Vertical Pattern Group Programmability

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Vertical Sequences (VSEQ)

A vertical sequence (VSEQ) is created by selecting one of the V-pattern groups and adding repeats, a start position, and horizontal clamping and blanking information. Each VSEQ is programmed using the registers shown in Table 15. Figure 37 shows how each register is used to generate a V-sequence.

The VPATSELA and VPATSELB registers select which V-pattern group is used in a given V-sequence. Having two groups available allows each vertical output to be mapped to a different V-pattern group. The selected V-pattern group can have repetitions added for high speed line shifts or line binning by using the VREP registers for odd and even lines. Generally, the same number of repetitions is programmed into both registers. If a different number of repetitions is required on odd and even lines, separate values can be used for each register (see the Generating Line Alternation for V-Sequences and HBLK section). The VSTARTA and VSTARTB registers specify the pixel location where the V-pattern group starts. The VMASK register is used in conjunction with the FREEZE/RESUME registers to enable optional masking of the XV outputs. Either or both of the FREEZE1/RESUME1 and FREEZE2/RESUME2 registers can be enabled.

The line length (in pixels) is programmable using the HDLEN registers. Each V-sequence can have a different line length to accommodate various image readout techniques. The maximum number of pixels per line is 8192. Note that the last line of the field can be programmed separately using the HDLAST register, located in the field register (see Table 16).

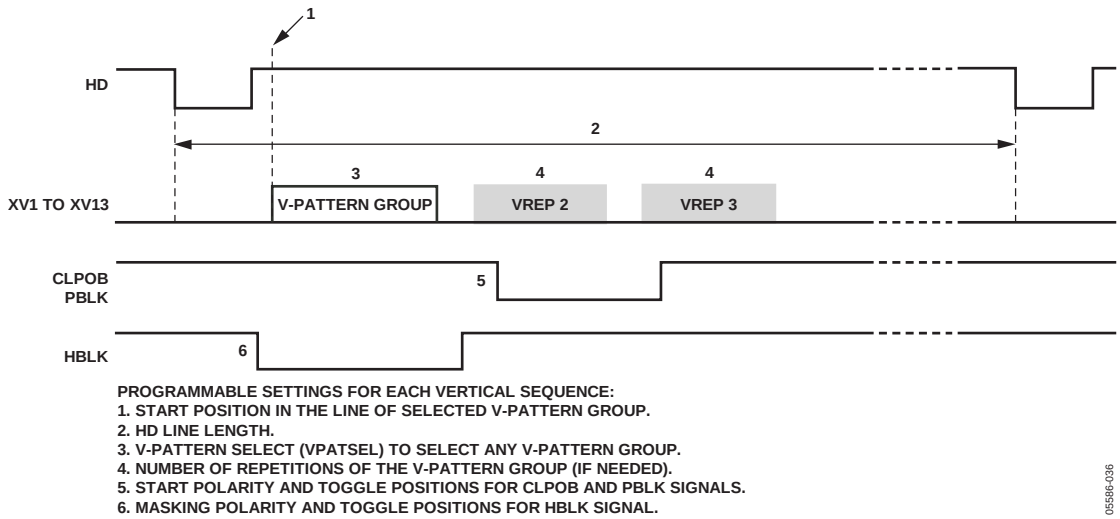

Figure 37. V-Sequence Programmability

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Table 15. V-Sequence Registers (See Table 11 and Table 12 for CLPOB, PBLK, and HBLK Registers.)

Register	Length (Bits)	Range	Description
HOLD	1	On/off	Use in conjunction with VMASK. 1 = hold instead of freeze/resume.
VMASK	2	0 to 3 mask mode	Enables the masking of XV1 to XV13 outputs at the locations specified by the FREEZE/RESUME registers. 0 = no mask. 1 = enable FREEZE1/RESUME1. 2 = enable FREEZE2/RESUME2. 3 = enable both FREEZE1/RESUME1 and FREEZE2/RESUME2.
HDLEN	13	0 to 8191 pixels	HD line length in each V-sequence.
XV1POL to XV13POL	1	High/low	Start polarity for each XV1 to XV13 output.
GROUPSEL	12	1b for each XV-output	Assigns each XV1 to XV13 output to either V-pattern Group A or V-pattern Group B. 0 = assigns to VPATSELA. 1 = assigns to VPATSELB.
TWO_GROUP	1	High/low	When high, all XV outputs combine Group A and Group B.
VPATSELA	5	0 to 31 V-pattern number	Selected V-pattern for Group A.
VPATSELB	5	0 to 31 V-pattern number	Selected V-pattern for Group B. If SPVTP_ENABLE = 1, VPATSELB is used for 2nd VTP inserted in SPVTP_ACTLINE.
VPATA_MODE	2	0 to 3 repetition mode	Selects alternation repetition mode for Group A only. 0 = disable alternation, use VREPA_1 for all lines. 1 = 2-line. Alternate VREPA_1 and VREPA_2 (same as odd/even). 2 = 3-line. Alternate VREPA_1, VREPA_2, and VREPA_3. 3 = 4-line. Alternate VREPA_1, VREPA_2, VREPA_3, and VREPA_4.
VSTARTA	13	0 to 8191 pixel location	Start position for the selected V-Pattern Group A.
VSTARTB	13	0 to 8191 pixel location	Start position for the selected V-Pattern Group B. If SPVTP_ENABLE = 1, VSTARTB is used for start position of VPATSELB in SPVTP_ACTLINE.
VLENA	13	0 to 8191 pixels	Length of selected V-Pattern Group A.
VLENB	13	0 to 8191 pixels	Length of selected V-Pattern Group B.
VREPB_ODD	12	0 to 4095 repeats	Number of repetitions for the V-Pattern Group B for odd lines. If no alternation is required for Group B, set VREPB_ODD equal to VREPB_EVEN.
VREPB_EVEN	12	0 to 4095 repeats	Number of repetitions for the V-Pattern Group B for even lines. If no alternation is required for Group B, set VREPB_EVEN equal to VREPB_ODD.
VREPA_1	12	0 to 4095 repeats	Number of repetitions for the V-Pattern Group A for first lines (odd).
VREPA_2	12	0 to 4095 repeats	Number of repetitions for the V-Pattern Group A for second lines (even).
VREPA_3	12	0 to 4095 repeats	Number of repetitions for the V-Pattern Group A for third lines.
VREPA_4	12	0 to 4095 repeats	Number of repetitions for the V-Pattern Group A for fourth lines.
FREEZE1	13	0 to 8191 pixel location	Pixel location where the XV outputs freeze or hold (see VMASK).
RESUME1	13	0 to 8191 pixel location	Pixel location where the XV outputs resume operation (see VMASK).
FREEZE2	13	0 to 8191 pixel location	Pixel location where the XV outputs freeze or hold (see VMASK).
RESUME2	13	0 to 8191 pixel location	Pixel location where the XV outputs resume operation (see VMASK).
SPVTP_ACTLINE	12	0 to 4095 line location	Active line for 2nd VTP insertion.
SPVTP_ENABLE	1	High/low	When high, 2nd VTP is inserted into SPVTP_ACTLINE.

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Group A/Group B Selection

The AD9923 has the flexibility to use two V-pattern groups in a vertical sequence. In general, all vertical outputs use the same V-pattern group during a sequence, but some outputs can be assigned to a different V-pattern group. This is useful during certain CCD readout modes.

The GROUPSEL register is used to select Group A or Group B for each XV output (the LSB is XV1, the MSB is XV13). Setting each bit to 0 selects Group A; setting each bit to 1 selects Group B. If only a single V-pattern group is needed for the vertical outputs, Group A is used by default (GROUPSEL = 0), and the outputs use the V-pattern group specified by the VPATSELA register.

If Group B flexibility is needed, the outputs set to 1 in the GROUPSEL register use the V-pattern group selected by the VPATSELB register. For example, Figure 38 shows outputs XV12 and XV13 using a separate V-Pattern Group B to perform special CCD timing.

Another application of the Group A and Group B registers is to combine two VPAT groups for more complex patterns. This is achieved by setting the TWO_GROUP register to 1. Figure 39 shows an example of this timing. When TWO_GROUP = 1, the Group A and Group B toggle positions are both used. In addition, length, starting polarity, and number of repetitions are all determined by the appropriate registers for Group A when TWO_GROUP = 1. Figure 40 shows the more complex operation of combining Group A and Group B with repetition.

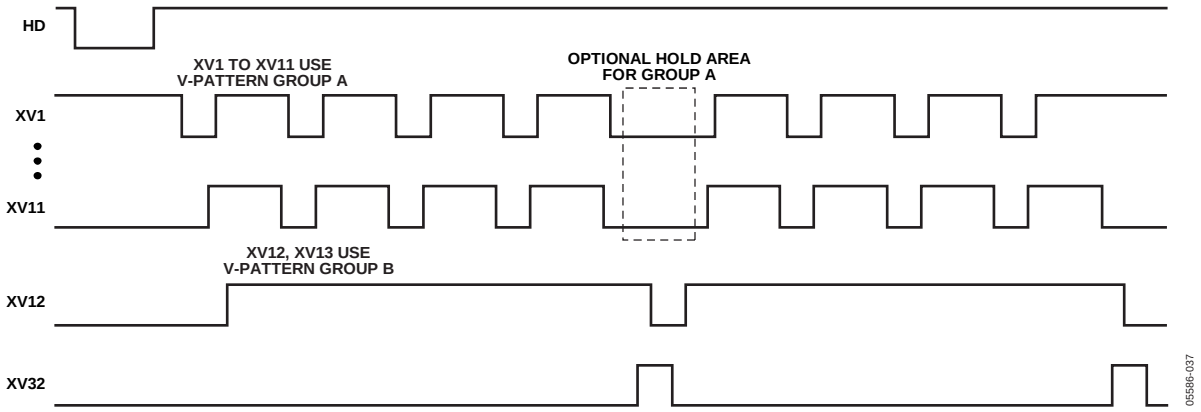

Figure 38. Using Separate Group A and Group B Patterns

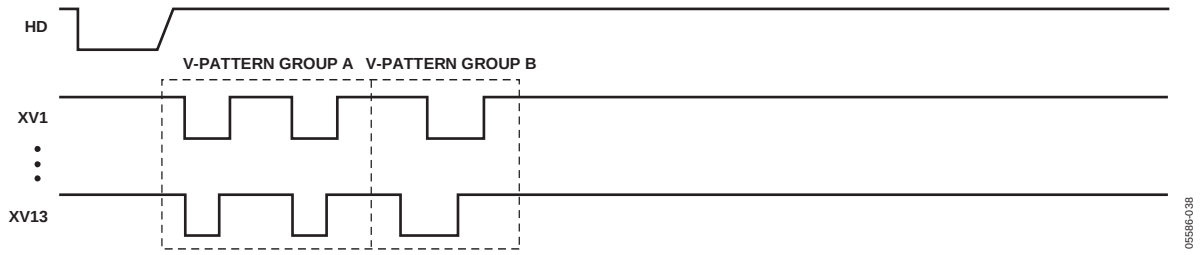

Figure 39. Combining Group A and Group B Patterns

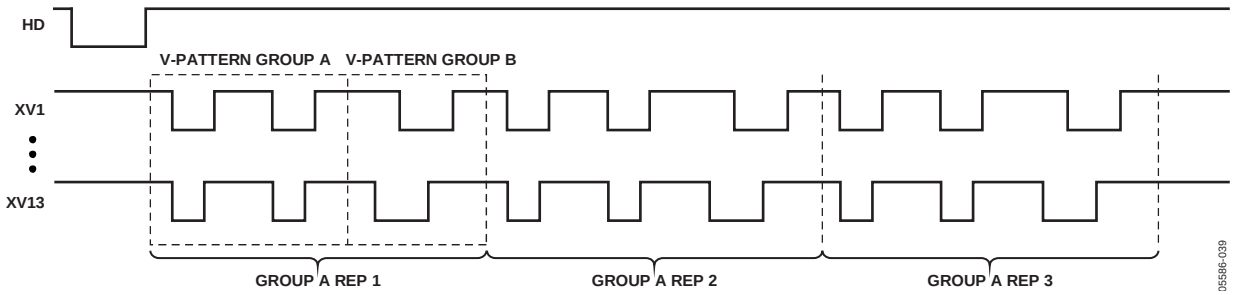

Figure 40. Combining Group A and Group B Patterns, with Repetition

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Generating Line Alternation for V-Sequences and HBLK

During low resolution readout, some CCDs require a different number of vertical clocks on alternate lines. The AD9923 can support such CCDs by using different VREP registers. This allows a different number of VPAT repetitions to be programmed on odd and even lines.

Note that only the number of repeats is different in odd and even lines, but the VPAT group remains the same. There are separate controls for the assigned Group A and Group B patterns. Both Group A and Group B can support odd and even line alternation. Group A uses the VREPA_1 and VREPA_2 registers; Group B uses the VREPB_ODD and VREPB_EVEN registers. Group A can also support 3-line and 4-line alternation by using the VREPA_3 and VREPA_4 registers.

Additionally, the HBLK signal can be alternated for odd and even lines. When the HBLKALT = 1, the HBLKTOGE1 and HBLKTOGE2 positions are used on odd lines, and the HBLKTOGE3 to HBLKTOGE6 positions are used on even lines. This allows the HBLK interval to be adjusted on odd and even lines if needed.

Figure 41 shows an example of simultaneous VPAT repetition alternation and HBLK alternation. Both types of alternation can be used separately.

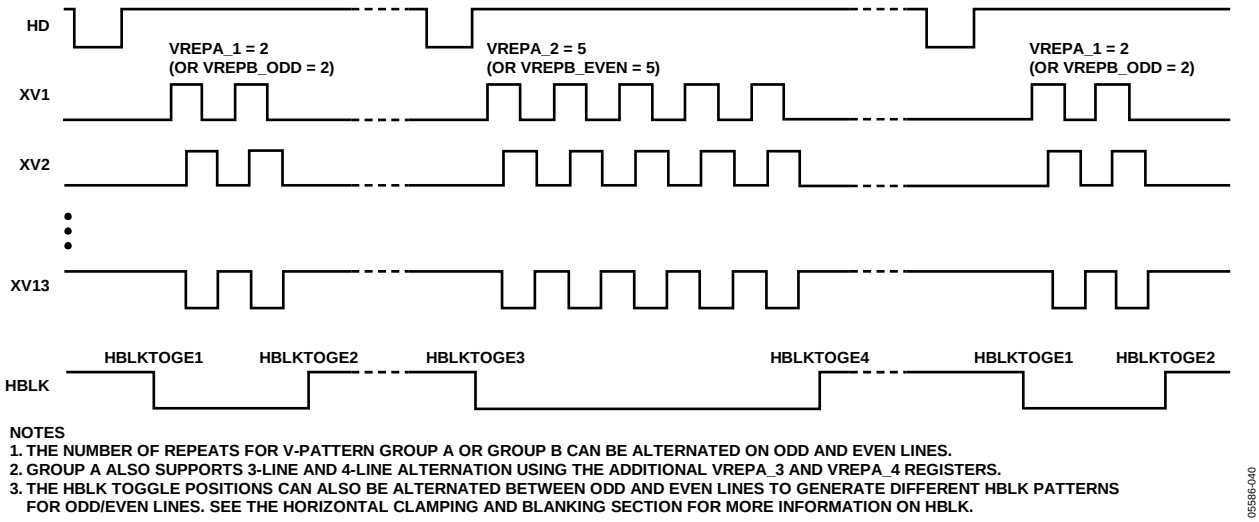

Figure 41. Odd/Even Line Alternation of VPAT Repetitions and HBLK Toggle Positions

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Masking Using Freeze/Resume Registers

As shown in Figure 42 and Figure 43, the FREEZE/RESUME registers are used to temporarily mask the XV outputs. The pixel locations to start (FREEZE) and end (RESUME) the masking create an area in which the vertical toggle positions are ignored. At the pixel location specified in the FREEZE register, the XV outputs are held static at their current dc state, high or low. The XV outputs are held until the pixel location specified by the RESUME register, at which point the signals continue with any remaining toggle positions.

Two sets of FREEZE/RESUME registers are provided, allowing the vertical outputs to be interrupted twice in the same line. The FREEZE and RESUME positions are enabled using the VMASK register.

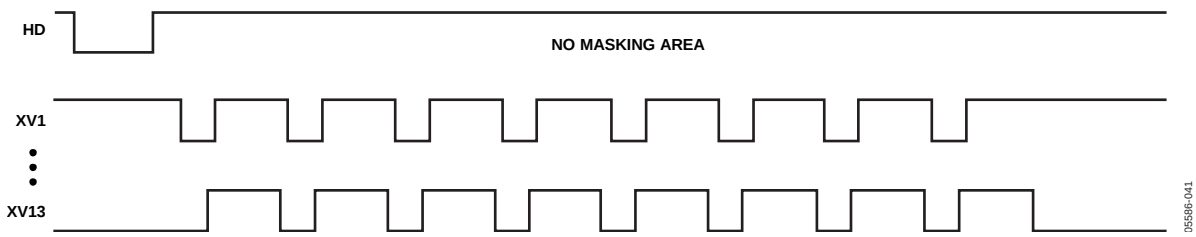

Figure 42. Not Using FREEZE/RESUME

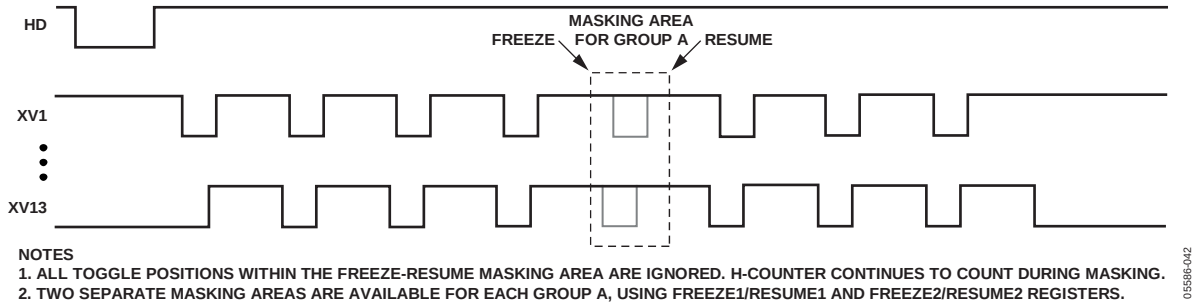

Figure 43. Using FREEZE/RESUME

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Hold Area Using FREEZE/RESUME Registers

The FREEZE/RESUME registers can also be used to create a hold area, in which the XV outputs are temporarily held and then later resume at the point where they were held. As shown in Figure 44, this is different than using the VMASK register, because the XV outputs continue from where they stopped, as opposed to having the pixel counter run continuously, with any toggle positions that fall between the FREEZE and RESUME locations being ignored.

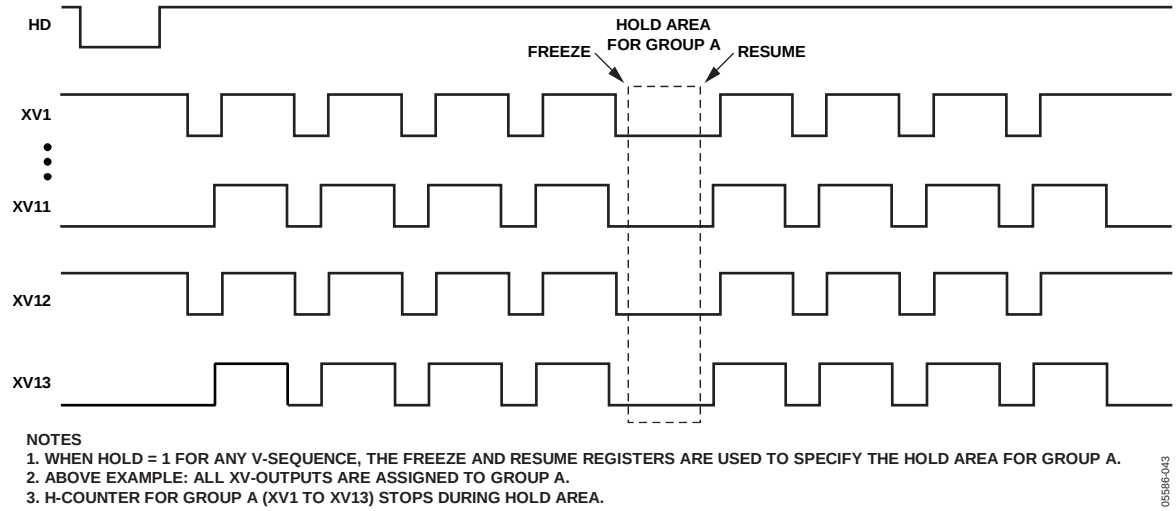

Figure 44. Hold Area for Group A

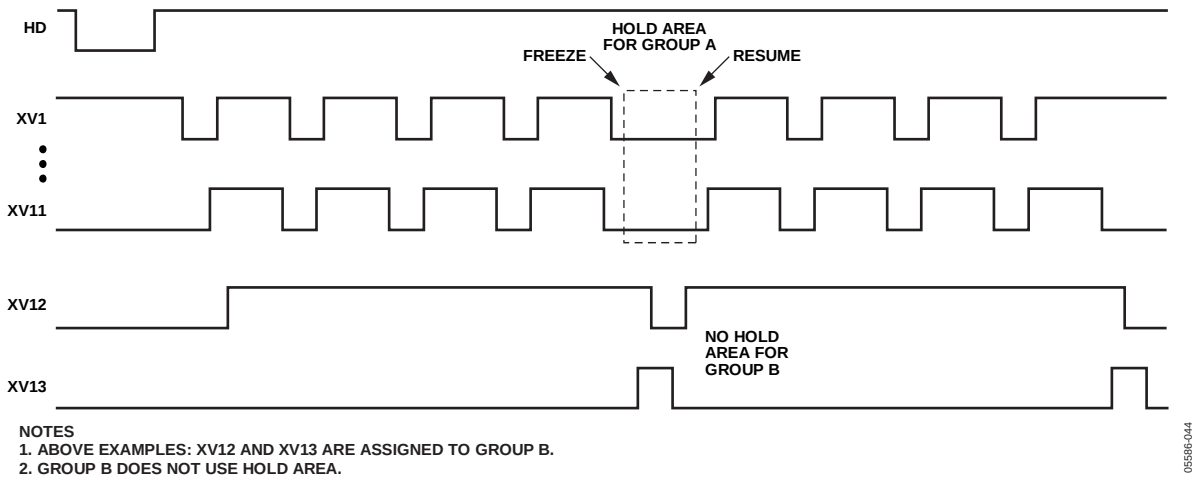

Figure 45. Group B Does Not Use Hold Area

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Complete Field: Combining V-Sequences

After the V-sequences are created, they are combined to create different readout fields. A field consists of up to seven regions. Within each region, a different V-sequence can be selected. Figure 46 shows how the sequence change position (SCP) registers designate the line boundary for each region and how the VSEQSEL registers select the V-sequence for each region. Registers to control the VSG outputs are also included in the field registers. Table 16 summarizes the registers used to create the different fields.

The VSEQSEL registers, one for each region, select which V-sequences are active during each region. The SWEEP registers can enable the sweep mode during any region.

The MULTI registers are used to enable the multiplier mode during any region. The SCP registers create the line boundaries for each region. The VDLEN register specifies the total number of lines in the field. The total number of pixels per line (HDLEN) is specified in the V-sequence registers, and the HDLAST register specifies the number of pixels in the last line of the field. The VPATSECOND register is used to add a second V-pattern group to the XV1 to X12 outputs during the sensor gate (VSG) line.

The SGMASK register is used to enable or disable each VSG output. There are two bits for each VSG output to enable separate masking during SGACTLINE1 and SGACTLINE2.

Setting a masking bit high disables, or masks, the output; setting it low enables the output. The SGPATSEL register assigns one of the eight SG patterns to each VSG output. Each SG pattern is created separately using the SG pattern registers. The SGACTLINE1 register specifies which line in the field contains the VSG outputs. The optional SGACTLINE2 register allows the same VSG pulses to repeat on a different line, although separate masking is available for SGACTLINE1 and SGACTLINE2.

Table 16. Field Registers

Register	Length (Bits)	Range	Description
VSEQSEL	5	0 to 31 V-sequence number	Selected V-sequence for each region in the field.
SWEEP	1	High/low	Enables sweep mode for each region when set high.
MULTI	1	High/low	Enables multiplier mode for each region when set high.
SCP	12	0 to 4095 line number	Sequence change position (SCP) for each region.
VDLEN	12	0 to 4095 lines	Total number of lines in each field.
HDLAST	13	0 to 8191 pixels	Length in pixels of the last HD line in each field.
VSTARTSECOND	13	0 to 8191 pixels	Start position of the second V-pattern group applied during VSG line.
VPATSECOND	5	0 to 31 V-pattern group number	Selected V-pattern group for the second pattern applied during VSG line.
SGMASK	16	High/low, each VSG	Set high to mask each VSG output. Two bits for each VSG output: one for SGLINE1, and one for SGLINE2. [0] Masking for VSG1 on SGLINE1. [1] Masking for VSG1 on SGLINE2 [2] Masking for VSG2 on SGLINE1. [3] Masking for VSG2 on SGLINE2. [15] Masking for VSG8 on SGLINE1. [16] Masking for VSG8 on SGLINE2.
SGPATSEL	24	0 to 7 pattern number, each VSG	Selects the VSG pattern number for each VSG output. VSG1[2:0], VSG2[5:3], VSG3[8:6], VSG4[11:9], VSG5[14:12], VSG6[17:15], VSG7[20:18], VSG8[23:21].
SGACTLINE1	12	0 to 4095 line number	Selects the line in the field where the VSG is active.
SGACTLINE2	12	0 to 4095 line number	Selects a second line in the field to repeat the VSG signals.

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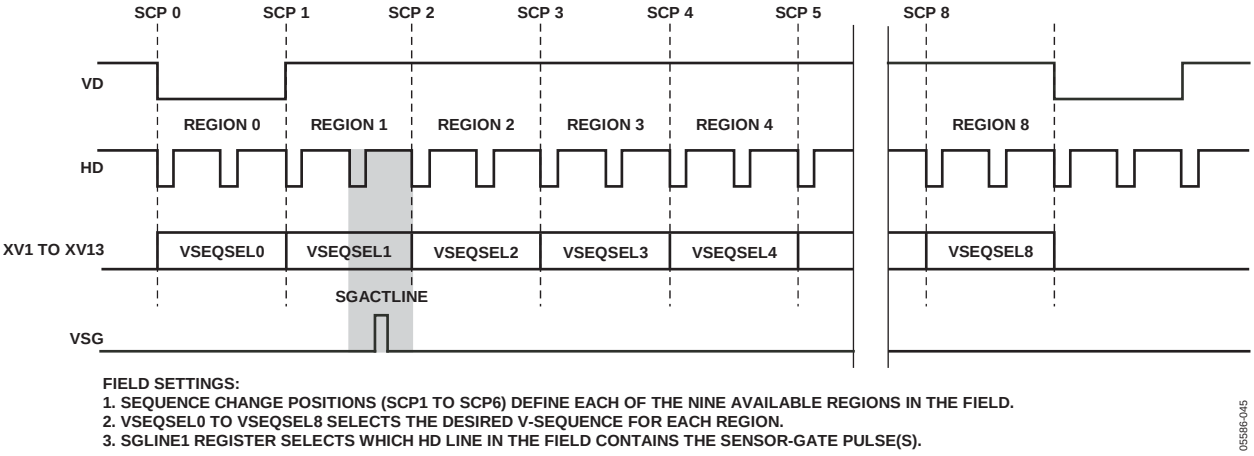

Figure 46. Complete Field Is Divided into Regions

Second V-Pattern Group During VSG Active Line and Special V-Pattern Insertion

Most CCDs require additional vertical timing during the sensor gate line. The AD9923 can output a second V-pattern group for XV1 to XV13 during the line when the VSG1 to VSG8 sensor gates are active. Figure 47 shows a typical VSG line, which includes two sets of V-pattern groups for XV1 to XV13. At the start of the VSG line, the V-pattern group is selected using the appropriate VSEQSEL register. The second V-pattern group, unique to the VSG line, is selected using the VPATSECOND register, located in the field registers. The start position of the second VPAT group uses the VSTARTSECOND register. For more information, see Table 16.

In addition to inserting a 2nd V-pattern into the VSG line, the AD9923 can insert a 2nd V-pattern into any other single line in each sequence. To enable this function in a particular sequence, set the SPXV_EN register in the appropriate set of sequence registers to 1. The SPXV_ACT register determines the active line for the special 2nd V-pattern. The VPATSELB and VSTARTB registers are used to control the V-pattern used and the starting pixel location of the special 2nd V-pattern. For more information, see Table 17.

To avoid undesired behavior, do not use the special 2nd V-pattern in the VSG line; use the existing VPATSECOND and VSTARTSECOND registers to insert a 2nd V-pattern into the VSG line. Also, since the special 2nd V-pattern insertion uses some of the Group B registers, the user cannot use the special 2nd V-pattern insertion function and Group B in the same sequence.

Table 17. Special 2nd V-Pattern Insertion

Register	Length (Bits)	Range	Description
SPXV_EN	1	0 or 1	0 = off, 1= enable special 2nd V-pattern insertion.
SPXV_ACT	12	Line 0 to 4095	Active line for special 2nd V-pattern insertion.
VPATSELB	5	0 to 31 V-pattern number	Selected V-pattern for special 2nd V-pattern insertion if SPXV_EN = 1.
VSTARTB	13	0 to 8191 pixel location	Start position for selected V-pattern for special 2nd V-pattern insertion if SPXV_EN = 1.

Sweep Mode Operation

The AD9923 contains an additional mode of vertical timing operation called sweep mode. This mode is used to generate a large number of repetitive pulses that span across multiple HD lines. Normally, the vertical timing of the AD9923 must be contained within one HD line length, but when sweep mode is enabled, the HD boundaries are ignored until the region is finished. This is useful, for example, in CCD readout operations. Depending on the vertical resolution of the CCD, up to 3,000 clock cycles, spanning across several HD line lengths, can be required to shift charge out of the vertical interline CCD registers. These registers must be free of all charge at the end of the image exposure before the image is transferred. This can be accomplished in sweep mode by quickly shifting out any charge using a long series of pulses from the XV1 to XV13 outputs. To enable sweep mode in any region, program the appropriate SWEEP register to high.

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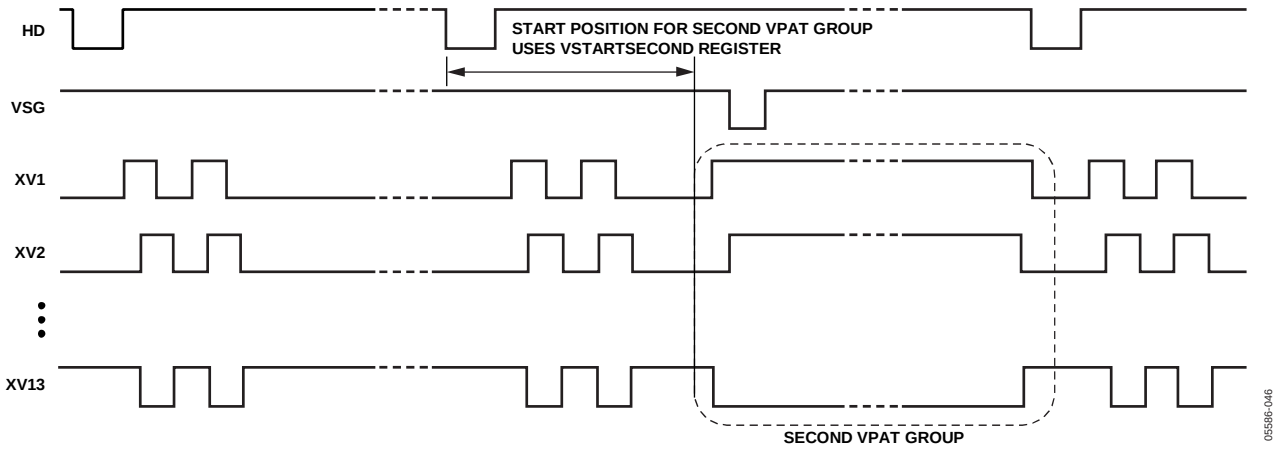

Figure 47. Example of Second VPAT Group During Sensor Gate Line

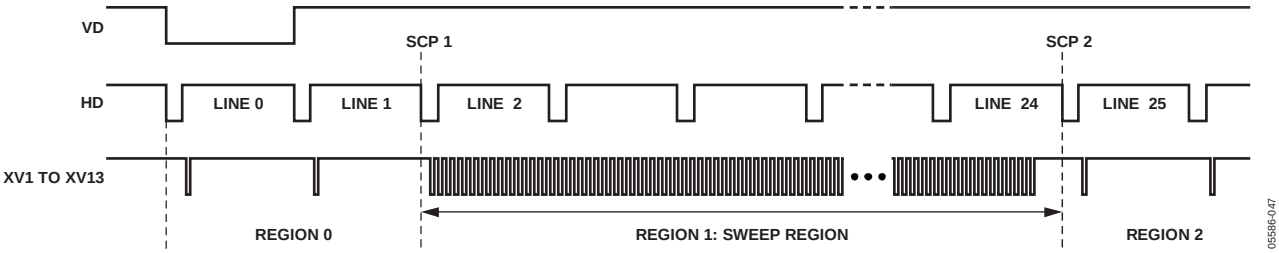

Figure 48. Example of Sweep Region for High Speed Vertical Shift

Figure 48 shows an example of sweep mode operation. The number of required vertical pulses depends on the vertical resolution of the CCD. The XV1 to XV13 output signals are generated using the V-pattern registers (shown in Table 14). A single pulse is created using the polarity and toggle position registers. The number of repetitions is then programmed to match the number of vertical shifts required by the CCD. Repetitions are programmed in the V-sequence registers using the VREP registers. This produces a pulse train of the appropriate length. Normally, the pulse train is truncated at the end of the HD line length, but with sweep mode enabled, the HD boundaries are ignored. In Figure 48, the sweep region occupies 23 HD lines. After the sweep mode region is complete, normal sequence operation resumes in the next region. When using sweep mode, set the region boundaries, using the sequence change position registers, to the appropriate lines to prevent the sweep operation from overlapping with the next V-sequence.

Multiplier Mode

To generate very wide vertical timing pulses, a vertical region can be configured into a multiplier region. This mode uses the V-pattern registers in a slightly different manner. Multiplier mode can be used to support unusual CCD timing requirements, such as vertical pulses that are wider than the 13-bit V-pattern toggle position counter.

The start polarity and toggle positions are used in the same manner as the standard VPAT group programming, but the VLEN register is used differently. Instead of using the pixel counter (HD counter) to specify the toggle position locations (XVTOG1, XVTOG2, XVTOG3, XVTOG4, XVTOG5, and XVTOG6) of the VPAT group, the VLEN value is multiplied by the XVTOG value to allow very long pulses to be generated. To calculate the exact toggle position, counted in pixels after the start position, use the following equation:

$$\textit{Multiplier Mode Toggle Position} = XVTOG \times VLEN$$

Because the XVTOG value is multiplied by VLEN value, the resolution of the toggle position placement is reduced.

If VLEN = 4, the toggle position accuracy is reduced to 4-pixel steps, instead of single pixel steps. Table 18 summarizes how the VPAT group registers are used in multiplier mode operation. In multiplier mode, the VREP registers should be programmed to the value of the highest toggle position.

The example shown in Figure 49 illustrates this operation. The first toggle position is 2, and the second toggle position is 9. In nonmultiplier mode, this causes the V-sequence to toggle at

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Pixel 2 and Pixel 9 within a single HD line. However, in multiplier mode the toggle positions are multiplied by VLEN = 4; therefore, the first toggle occurs at pixel count = 8, and the second toggle occurs at pixel count = 36. Sweep mode is also enabled to allow the toggle positions to cross the HD line boundaries.

Table 18. Multiplier Mode Register Parameters

Register	Length (Bits)	Range	Description
MULTI	1	High/low	High enables multiplier mode
XVPOL	1	High/low	Starting polarity of XV1 to XV13 signals in each VPAT group
XVTOG	13	0 to 8191 pixel location	Toggle positions for XV1 to XV13 signals in each VPAT group
VLEN	13	0 to 8191 pixels	Used as multiplier factor for toggle position counter
VREP	12	0 to 4095	VREPE/VREPO should be set to the value of the highest XVTOG value

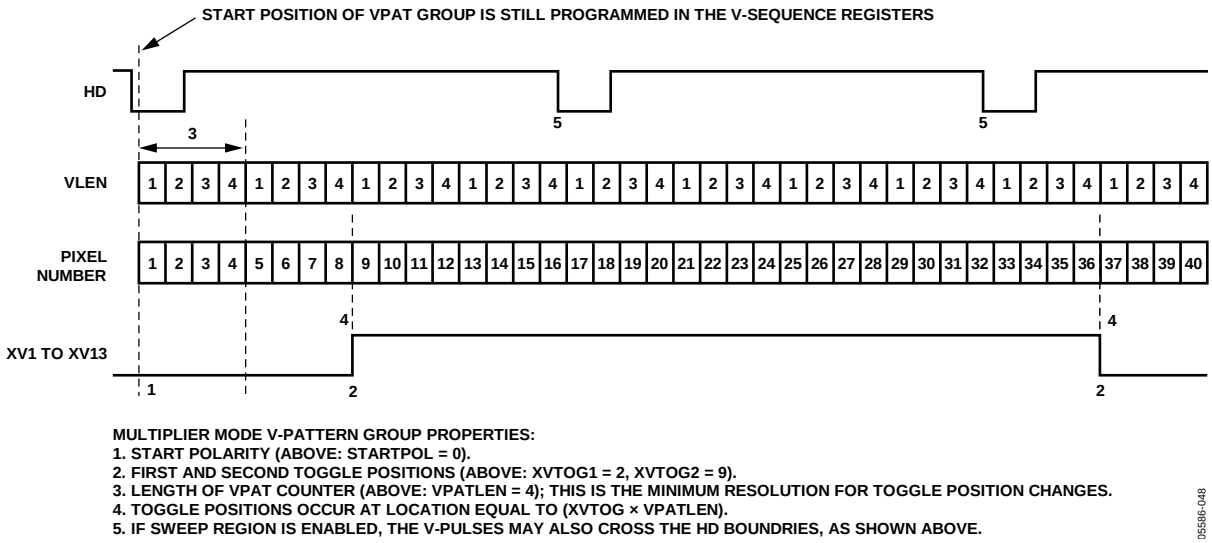

Figure 49. Example of Multiplier Region for Wide Vertical Pulse Timing

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Vertical Sensor Gate (Shift Gate) Patterns

In an interline CCD, the vertical sensor gates (VSG) are used to transfer the pixel charges from the light sensitive image area into the light shielded vertical registers. From the light shielded vertical registers, the image is then read line-by-line using the XV1 to XV13 vertical transfer pulses in conjunction with the high speed horizontal clocks.

Table 19 summarizes the VSG pattern registers. The AD9923 has eight VSG outputs, VSG1 to VSG8. Each output can be assigned to one of eight programmed patterns by using the SGPATSEL register. Each pattern is generated in a similar manner as the V-pattern groups, with a programmable start polarity (SGPOL), first toggle position (SGTOG1), and second toggle position (SGTOG2). The active line where the VSG1 to VSG8 pulses occur is programmable using the SGACTLINE1 and SGACTLINE2 registers. Additionally, any of the VSG1 to VSG8 pulses can be individually disabled using the SGMASK register. The individual masking allows all SG patterns to be preprogrammed, and the appropriate pulses for each field can be enabled separately. For maximum flexibility, the SGPATSEL, SGMASK, and SGACTLINE registers are separately programmable for each field. More detail is given in the Complete Field: Combining V-Sequences section.

Additionally, there is the SGMASK_BYP register (Address 0x59), which overrides SG masking in the field registers. The SGMASK_BYP register allows sensor gate masking to be changed without modifying the field register values. The SGMASK_BYP register is SCK updated; therefore, the new SG-masking values update immediately.

Table 19. VSG Pattern Registers[1]

Register	Length (Bits)	Range	Description
SGPOL	1	High/low	Sensor-gate starting polarity for SG patterns 0 to 7
SGTOG1	13	0 to 8191 pixel location	First toggle position for SG patterns 0 to 7
SGTOG2	13	0 to 8191 pixel location	Second toggle position for SG patterns 0 to 7
SGMASK_BYP	8	High/low for each VSG	SGMASK Bypass. This register overrides the SGMASK values in each Field register. One bit for each output, where Bit[0] is for VSG1 output and Bit[7] is for VSG8 output. 0 = active. 1 = mask output.
SGMASK_BYP_EN	1	0 or 1	1: Enables SGMASK bypass

[1] See field registers in Table 16.

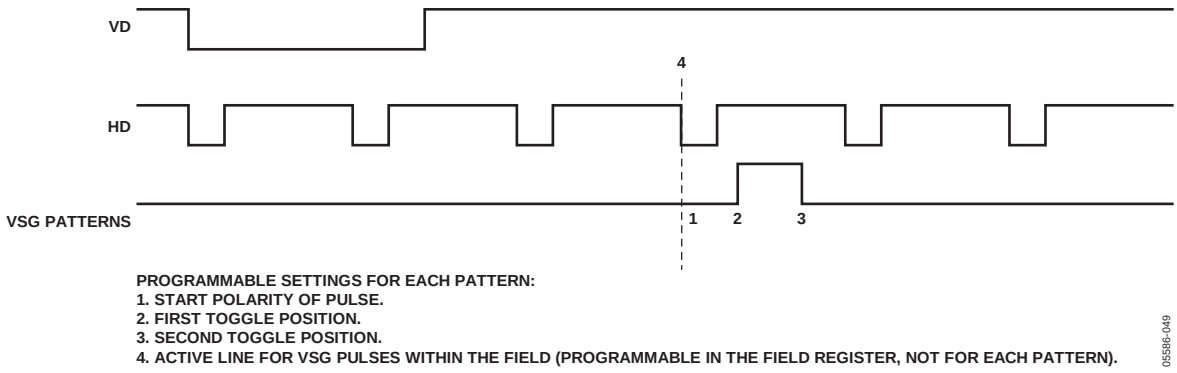

Figure 50. Vertical Sensor Gate Pulse Placement

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MODE Register

The MODE register is a single register that selects the field timing of the AD9923. Typically, all field, V-sequence, and V-pattern group information is programmed into the AD9923 at startup. During operation, the MODE register allows the user to select any combination of field timing to meet the current requirements of the system. Using the MODE register in conjunction with preprogrammed timing greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to rewrite the vertical timing information with each camera mode change.

A basic still camera application can require five fields of vertical timing—one for draft mode operation, one for autofocusing, and three for still image readout. The register timing information for the five fields is loaded at startup. Depending on how the camera is being used, the MODE register selects which field timing is active during camera operation.

Table 20 shows how the MODE register bits are used. Unlike other registers, the MODE register uses 10 address bits as data bits to increase the total register size to 38 bits. The address MSBs, A11 and A10, are 1 and 0, respectively, and are used to specify the MODE register write. The 3 MSBs, D37, D36, and D35, are used to specify the number of fields used. A value from 1 to 7 can be selected using these three bits. The remaining register bits are divided into 5-bit sections to select which programmed fields are used and in which order. Up to seven fields can be used in a single MODE write. The AD9923 starts with the field timing specified by the first field bit, and switches to the timing specified by the second field bit on the next VD, and so on.

After completing the number of fields specified in Bit D37 to Bit D35, the timing generator of the AD9923 repeats itself by starting at the first field. This continues until a new write to the MODE register occurs. Figure 51 shows MODE register settings for various field configurations.

Table 20. Mode Register Contents—VD Updated

Address	Data Bits	Default Value	Description
12b10_xx_xxxx_xxxx	[37:0]	0	A11, A10 must be set to 0x10; remaining A9:A0 bits used for D37:D28
	[37:35]		Number of fields (maximum of seven)
	[34:30]		Selected field for Field 7
	[29:25]		Selected field for Field 5
	[24:20]		Selected field for Field 6
	[19:15]		Selected field for Field 4
	[14:10]		Selected field for Field 3
	[9:5]		Selected field for Field 2
	[4:0]		Selected field for Field 1

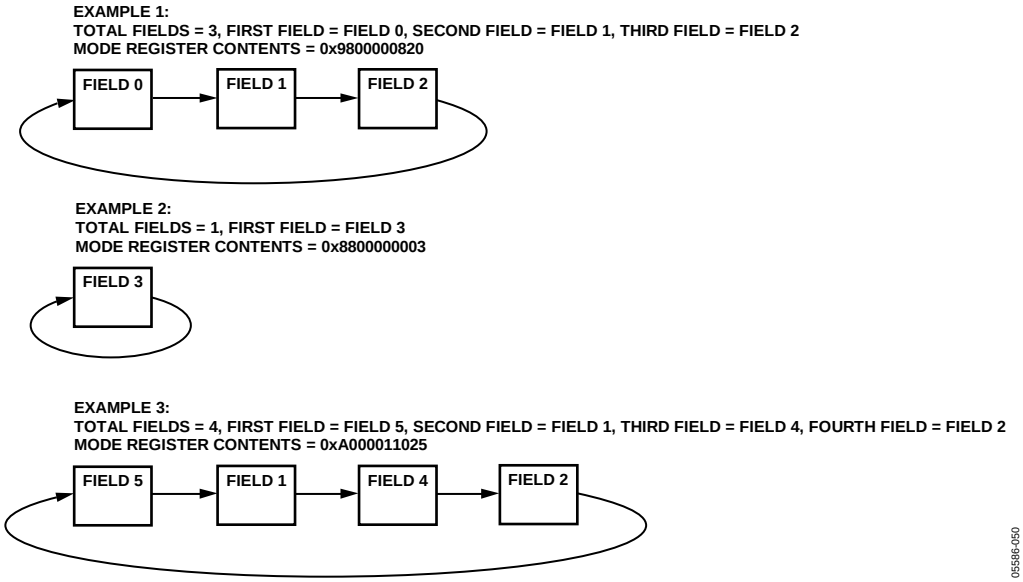

Figure 51. Using the Mode Register to Select Field Timing

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VERTICAL TIMING EXAMPLE

To better understand how the AD9923 vertical timing generation is used, consider the example CCD timing chart in Figure 52. It illustrates a CCD using a general 3-field readout technique. As described in the Complete Field: Combining V-Sequences section, each readout field should be divided into separate regions to perform each step of the readout. The sequence change position (SCP) registers determine the line boundaries for each region. Then, the VSEQSEL registers assign a V-sequence to each region. Each V-sequence contains specific timing information required for each region: XV1 to XV6 pulses (using VPAT groups), HBLK/CLPOB timing, and VSG patterns for the SG active lines.

The example shown in Figure 52 requires four regions, labeled Region 0, Region 1, Region 2, and Region 3, for each of the three fields. Because the AD9923 allows many individual fields to be programmed, Field 0, Field 1, and Field 2 can be created to meet the requirements of this timing example. In this example, the four regions for each field are very similar, but the individual registers for each field allow flexibility to accommodate more complex timing requirements.

Region 0 is a high speed vertical shift region. Sweep mode can be used to generate this timing operation, with the desired number of high speed vertical pulses needed to clear any charge from the vertical registers of the CCD.

Region 1 consists of two lines and uses standard, single-line, vertical-shift timing. The timing of this region is the same as the timing of Region 3.

Region 2 is the sensor gate line, where the VSG pulses transfer the image into the vertical CCD registers. This region might require use of the second V-pattern group for the SG active line.

Region 3 also uses the standard, single line, vertical shift timing, the same timing used in Region 1. In summary, four regions are required in each of the three fields.

The timing for Region 1 and Region 3 is essentially the same, reducing the complexity of the register programming. Other registers, such as the MODE register, shutter control registers (that is, TRIGGER, and the registers to control the SUBCK, VSUB, MSHUT, and STROBE outputs), and the AFE gain registers, VGAGAIN and CDSGAIN, must be used during the readout operation. These registers are explained in the MODE Register and Variable Gain Amplifier sections.

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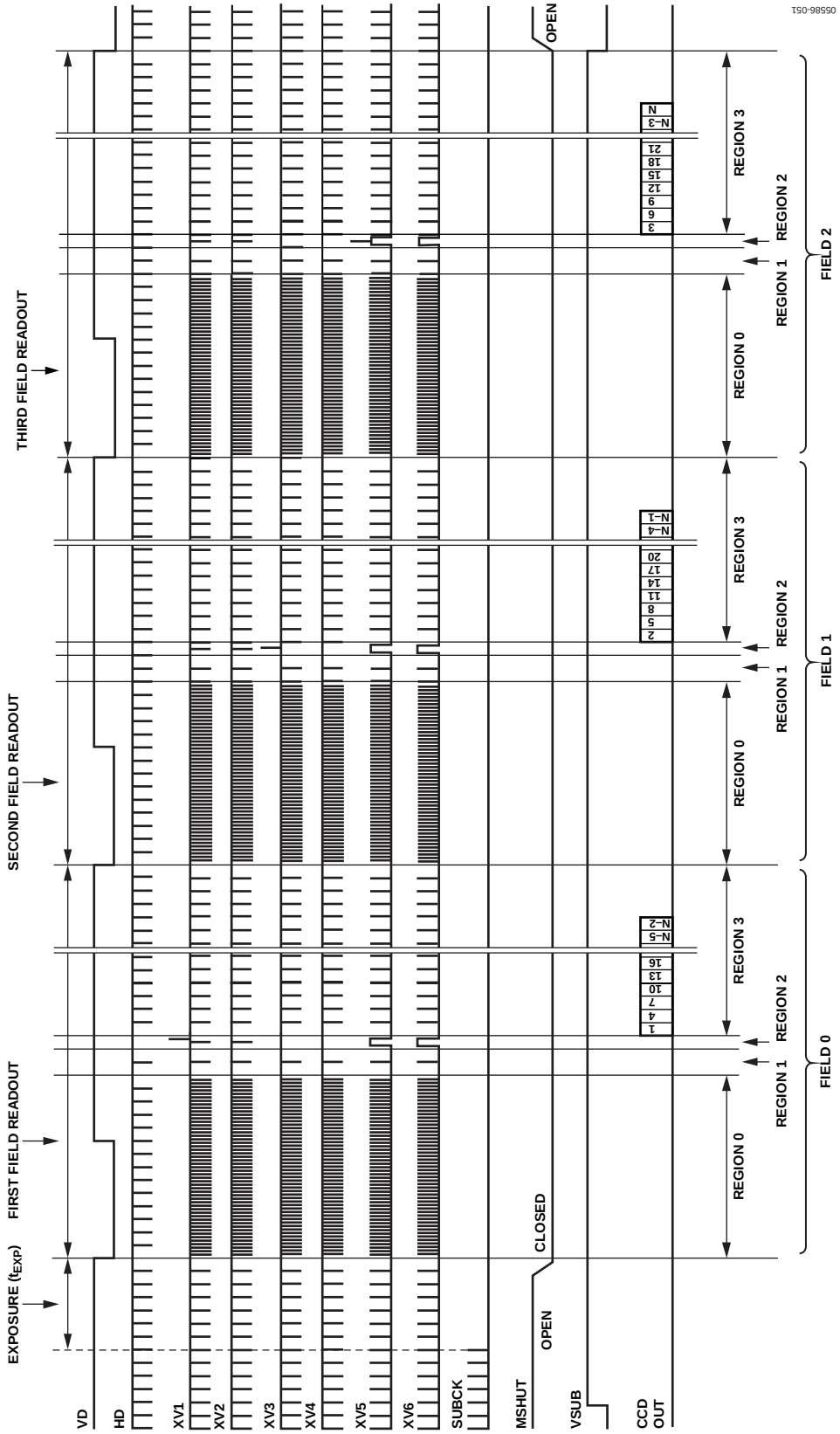

Figure 52. CCD Timing Example—Dividing Each Field into Regions

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VERTICAL DRIVER SIGNAL CONFIGURATION

As shown in Figure 53, XV1 to XV13, VSG1 to VSG8, and XSUBCK are outputs from the internal AD9923 timing generator, and V1 to V13 and SUBCK are the resulting outputs from the AD9923 vertical driver. The vertical driver mixes the XV and VSG pulses and amplifies them to the high voltages required for driving the CCD. Table 21 through Table 36 describe the output polarities for these signals vs. their input levels. Refer to these tables when determining the register settings for the desired output levels.

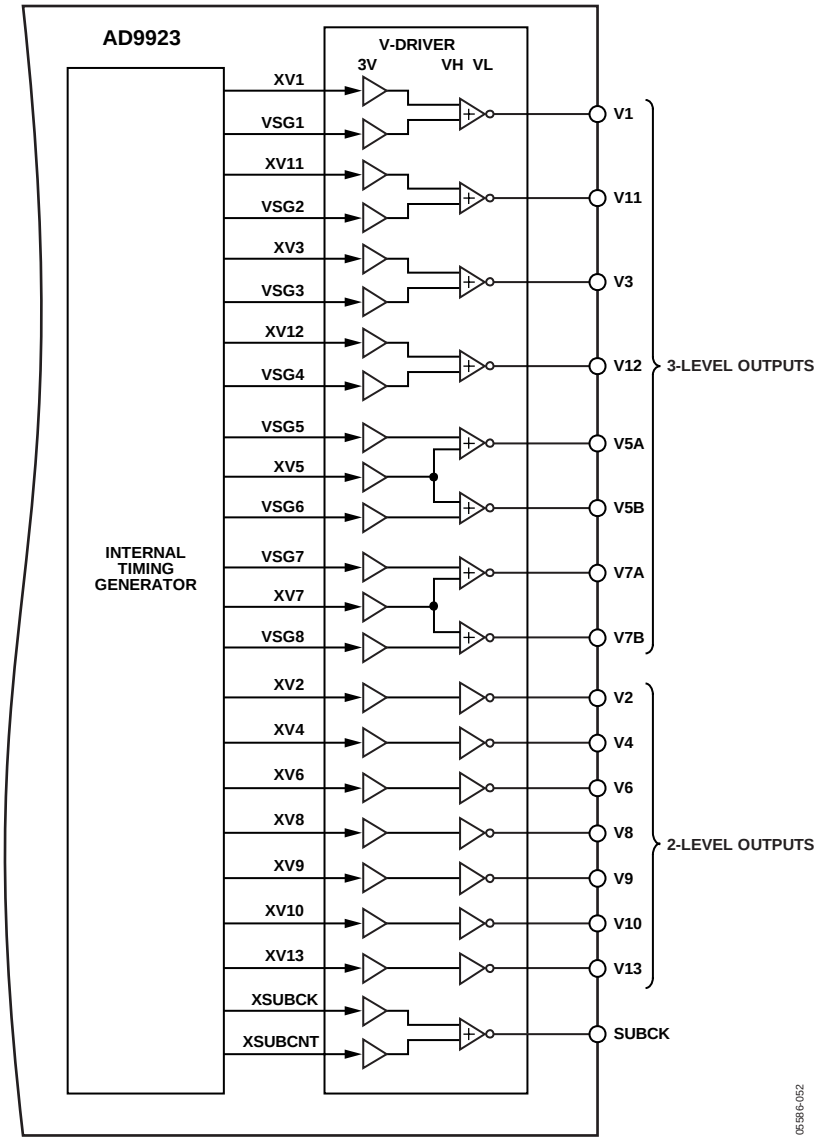

Figure 53. Internal Vertical Driver Input Signals

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Table 21. V1 Output Polarity

Vertical Driver Input		
XV1	VSG1	V1 Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 22. V3 Output Polarity

Vertical Driver Input		
XV3	VSG3	V3 Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 23. V5A Output Polarity

Vertical Driver Input		
XV5	VSG5	V5A Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 24. V5B Output Polarity

Vertical Driver Input		
XV5	VSG6	V5B Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 25. V7A Output Polarity

Vertical Driver Input		
XV7	VSG7	V7A Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 26. V7B Output Polarity

Vertical Driver Input		
XV7	VSG8	V7B Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 27. V11 Output Polarity

Vertical Driver Input		
XV11	VSG2	V11 Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 28. V12 Output Polarity

Vertical Driver Input		
XV12	VSG4	V12 Output
L	L	VH
L	H	VM
H	L	VL
H	H	VL

Table 29. V2 Output Polarity

Vertical Driver Input XV2	V2 Output
L	VM
H	VL

Table 30. V4 Output Polarity

Vertical Driver Input XV4	V4 Output
L	VM
H	VL

Table 31. V6 Output Polarity

Vertical Driver Input XV6	V6 Output
L	VM
H	VL

Table 32. V8 Output Polarity

Vertical Driver Input XV8	V8 Output
L	VM
H	VL

Table 33. V9 Output Polarity

Vertical Driver Input XV9	V9 Output
L	VM
H	VL

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Table 34. V10 Output Polarity

Vertical Driver Input XV10	V10 Output
L	VM
H	VL

Table 35. V13 Output Polarity

Vertical Driver Input XV13	V13 Output
L	VM
H	VL

Table 36. SUBCK Output Polarity

Vertical Driver Input		SUBCK Output
XSUBCK	XSUBCNT	
L	L	VH
L	H	VH
H	L	VMM
H	H	VLL

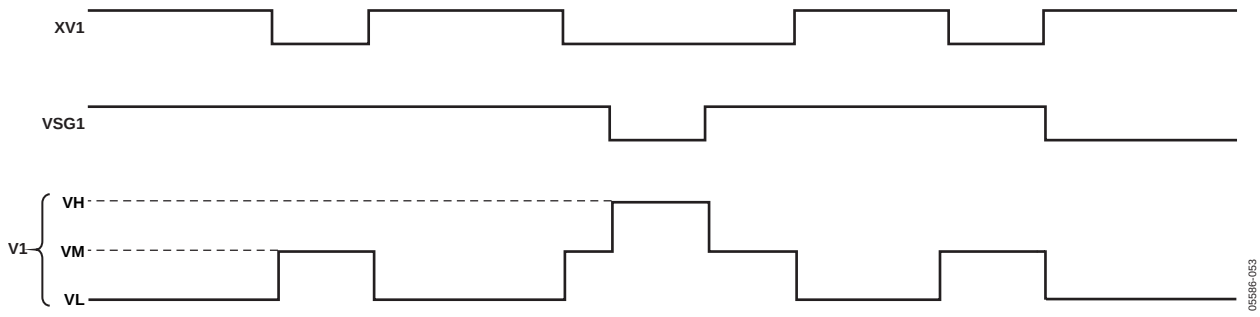

Figure 54. XV1, VSG1, and V1 Output Polarities

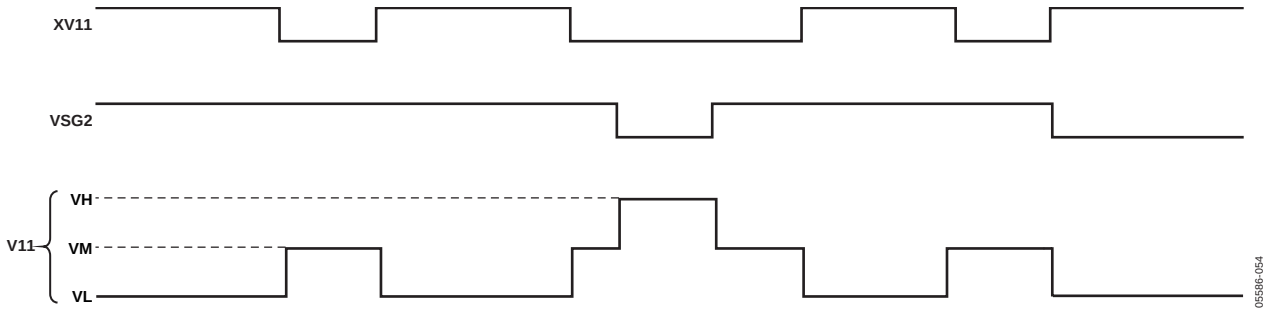

Figure 55. XV11, VSG2, and V11 Output Polarities

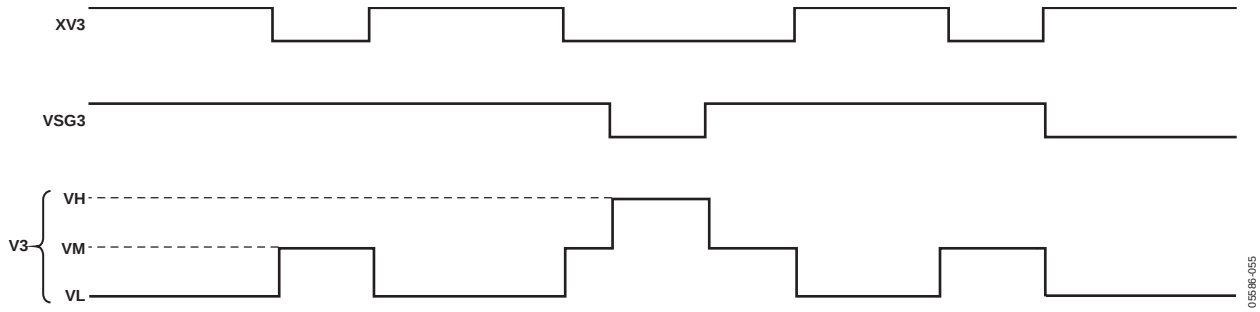

Figure 56. XV3, VSG3, and V3 Output Polarities

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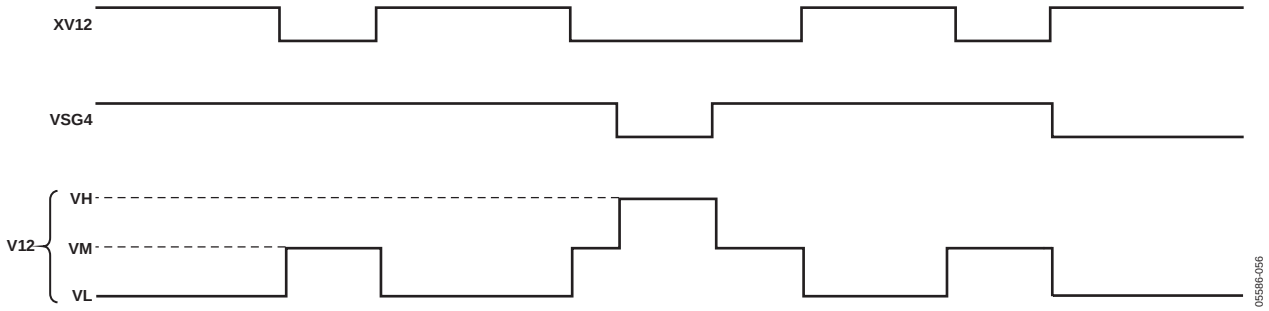

Figure 57. XV12, VSG4, and V12 Output Polarities

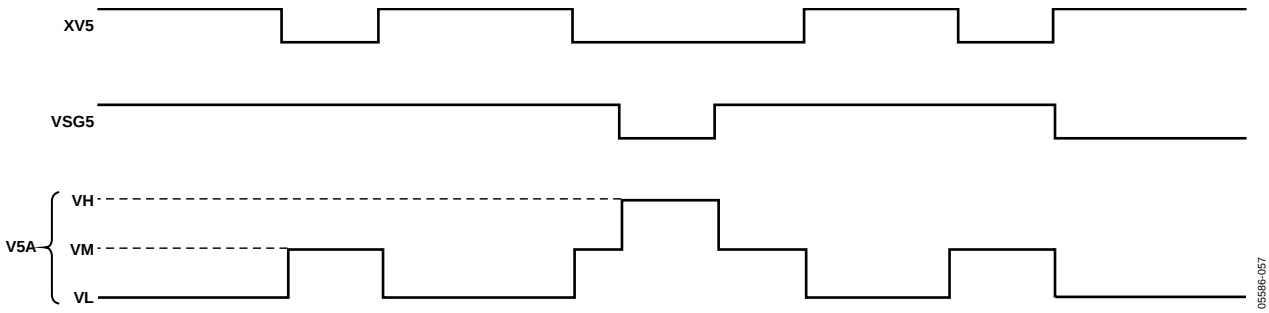

Figure 58. XV5, VSG5, and V5A Output Polarities

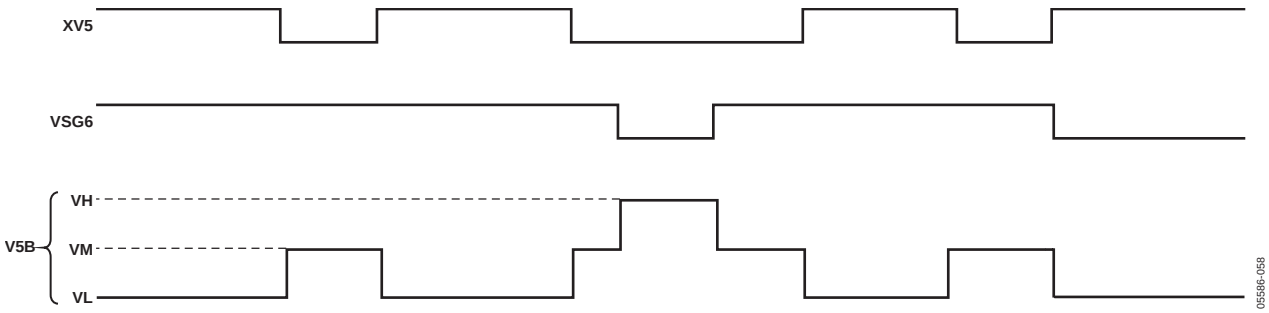

Figure 59. XV5, VSG6, and V5B Output Polarities

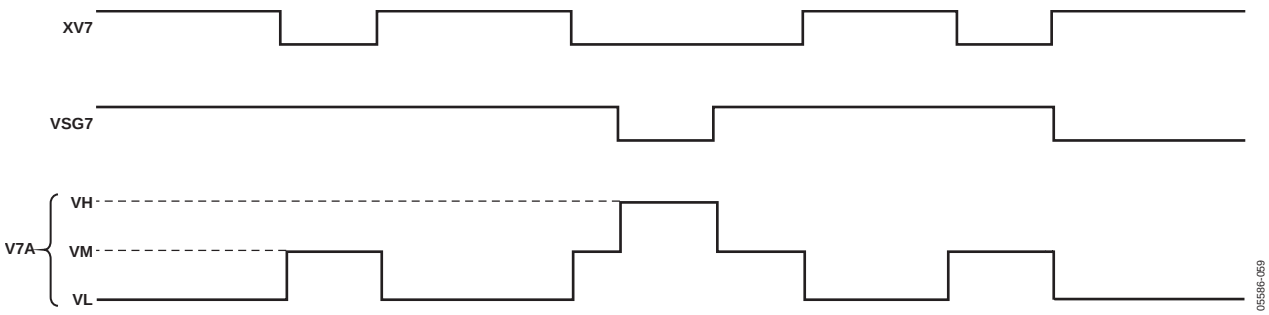

Figure 60. XV7, VSG7, and V7A Output Polarities

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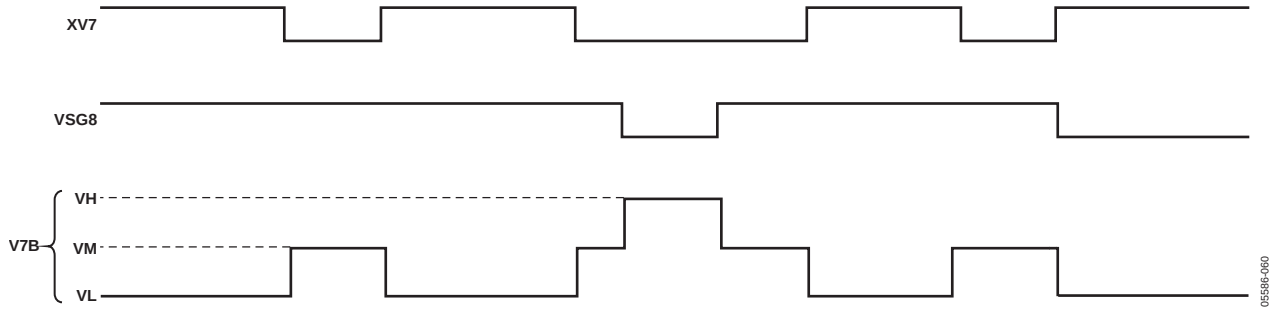

Figure 61. XV7, VSG8, and V7B Output Polarities

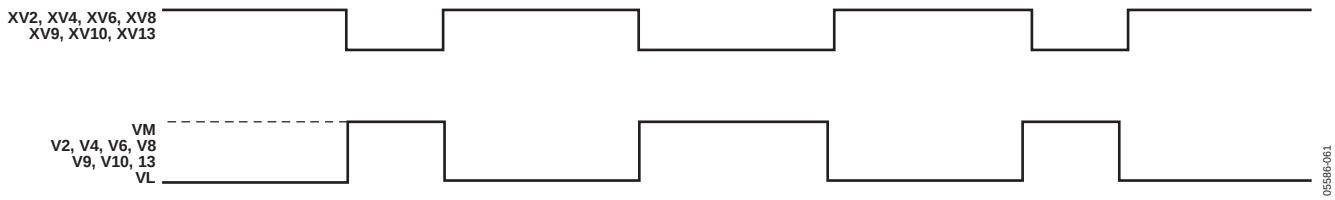

Figure 62. XV2, XV4, XV6, XV8, XV9, XV10, XV13 and V2, V4, V6, V8, V9, V10, V13 Output Polarities

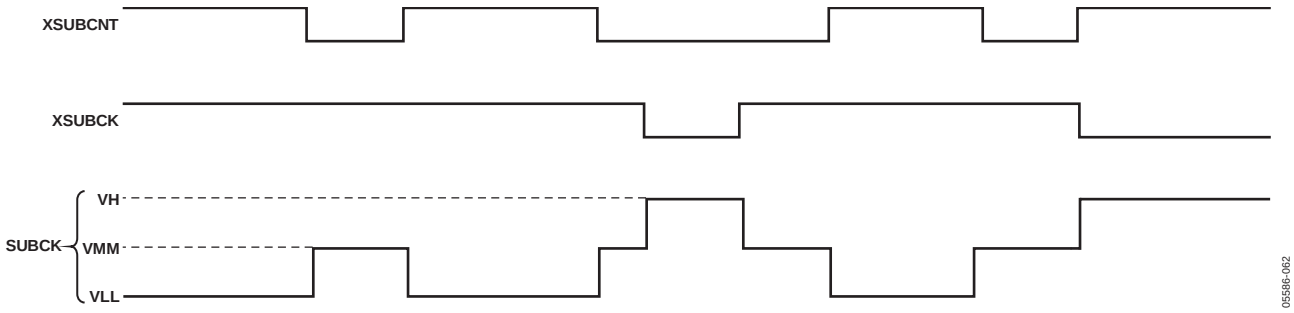

Figure 63. XSUBCK, XSUBCNT, and SUBCK Output Polarities

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SHUTTER TIMING CONTROL

The CCD image exposure time is controlled by the substrate clock signal (SUBCK), which pulses the CCD substrate to clear out accumulated charge. The AD9923 supports three types of electronic shuttering: normal, high precision, and low speed. Along with the SUBCK pulse placement, the AD9923 can accommodate different readout configurations to further suppress the SUBCK pulses during multiple field readouts. The AD9923 also provides programmable outputs to control an external mechanical shutter (MSHUT), strobe/flash (STROBE), and CCD bias select signal (VSUB). Up to four general shutter pulses (SHUT0 to SHUT3) and two VSUB pulses (VSUB0 and VSUB1) can be programmed and assigned to any of the three shutter output pins. The user can also combine the following shutter and VSUB pulses with a logic XOR operation to generate more complex timing (up to four toggle positions per line) for MSHUT, STROBE and VSUB: SHUT0 ^ VSUB0, SHUT0 ^ VSUB1, SHUT0 ^ SHUT1, and SHUT0 ^ SHUT2 ('^' indicates the logic XOR operation).

SUBCK: 3-Level Output

The AD9923 supports a 3-level output from the SUBCK buffer: VH, VMM, VLL. The VH power supply is shared with the V-driver outputs, but VMM and VLL are dedicated mid and low supplies for the SUBCK buffer. There are two inputs to the SUBCK buffer, XSUBCK and XSUBCNT. XSUBCNT is created by an internal multiplexer that selects from XV6, XV8, XV9, XV10, XV13, VSG1, VSG2, VSG3, VSG4, VSG5, VSG6, VSG7, VSG8, VSUB, MSHUT, and STROBE.

NOTE: The default value for the XSUBCNT_MUX register is 0 which assigns XV6 to XSUBCNT.

Table 37. XSUBCNT Multiplexer

Register	Length (Bits)	Range	Description
XSUBCNT_MUX	4	0 to 15	Selects internal signal to be used for XSUBCNT 0: XV6 1: XV8 2: XV9 3: XV10 4: VSG5 5: VSG6 6: VSG7 7: VSG8 8: VSG2 9: VSG3 10: VSG4 11: VSG1 12: XV13 13: VSUB 14: MSHUT 15: STROBE

SUBCK: Normal Operation

By default, the AD9923 operates in normal SUBCK configuration with the SUBCK signal pulsing in every VD field (see Figure 64). The SUBCK pulse occurs once per line, and the total number of repetitions within the field determines the exposure time. The SUBCK pulse polarity and toggle positions within a line are programmable, using the SUBCKPOL and SUBCK1TOG registers (see Table 38). The number of SUBCK pulses per field is programmed in the SUBCKNUM register (Address 0x64).

As shown in Figure 64, the SUBCK pulses always begin in the line following the SG-active line (specified in the SGACTLINE registers for each field). The SUBCKPOL, SUBCK1TOG, SUBCK2TOG, SUBCKNUM, and SUBCKSUPPRESS registers are updated at the start of the line after the sensor gate line, as described in the Serial Update section.

SUBCK: High Precision Operation

High precision shuttering is used in the same manner as normal shuttering, but an additional register is used to control the last SUBCK pulse. In this mode, the SUBCK pulses once per line, but the last SUBCK in the field has an additional SUBCK pulse, whose location is determined by the SUBCK2TOG register, as shown in Figure 65. Finer resolution of the exposure time is possible using this mode. Leaving the SUBCK2TOG register set to its maximum value (0xFFFFFF) disables the last SUBCK pulse (default setting).

SUBCK: Low Speed Operation

Normal and high precision shutter operations are used when the exposure time is less than one field long. For exposure times longer than one field interval, low speed shutter operation is used. The AD9923 uses a separate exposure counter to achieve long exposure times. The number of fields for the low speed shutter operation is specified in the EXPOSURENUM register (Address 0x63). As shown in Figure 66, this shutter mode suppresses the SUBCK and VSG outputs from 0 fields up to 4095 fields (VD periods). The VD and HD outputs can be suppressed during the exposure period by programming the VDHDOFF register to 1.

To generate a low speed shutter operation, trigger a long exposure by writing to the TRIGGER register, Bit D3. When this bit is set high, the AD9923 begins an exposure operation at the next VD edge. If a value greater than 0 is specified in the EXPOSURENUM register, the AD9923 suppresses the SUBCK output on subsequent fields.

If the exposure is generated using the TRIGGER register and the EXPOSURENUM register is set to 0, the behavior of the SUBCK is the same as during normal shutter or high precision shutter operations, in which the TRIGGER register is not used.

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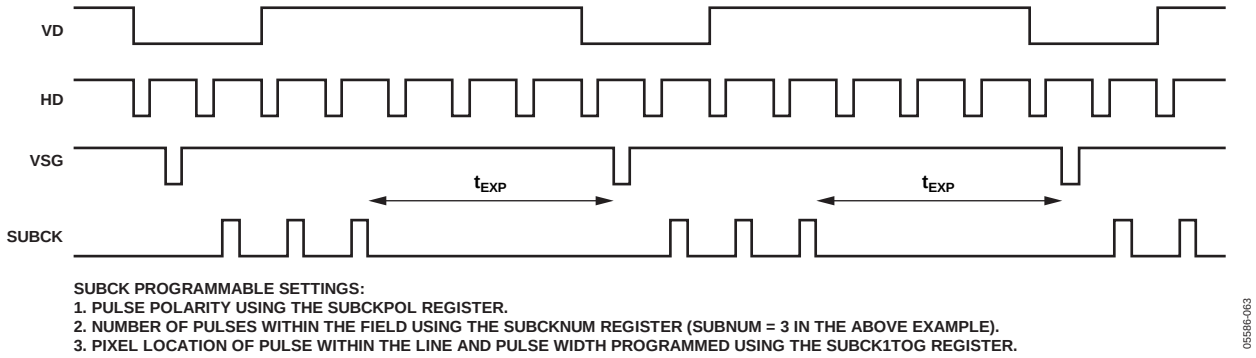

Figure 64. Normal Shutter Mode

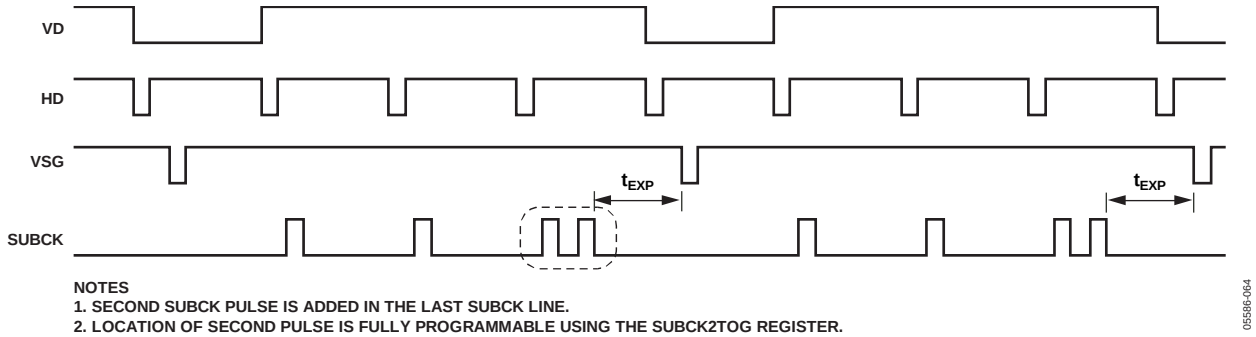

Figure 65. High Precision Shutter Mode

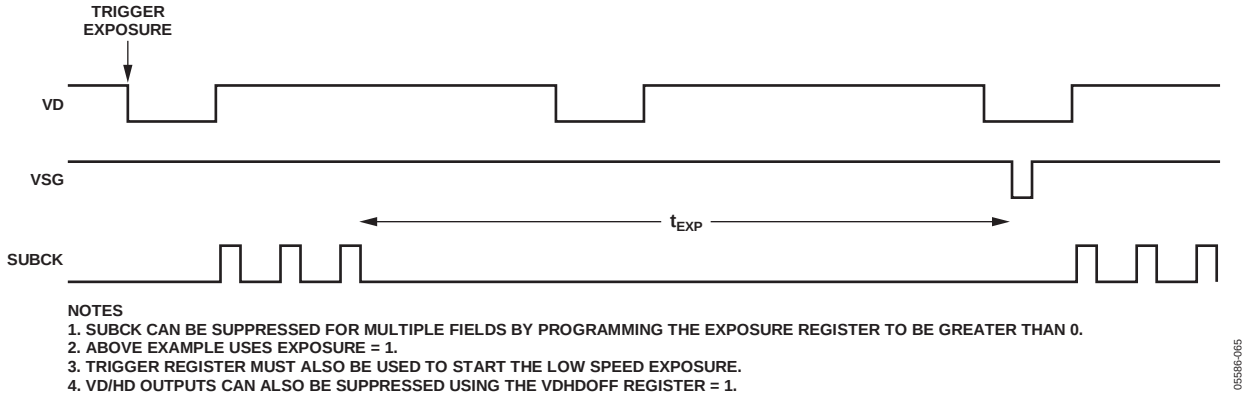

Figure 66. Low Speed Shutter Mode Using EXPOSURE Register

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SUBCK Suppression

Normally, the SUBCK begins pulsing on the line following the sensor gate line (VSG). Some CCDs require suppressing the SUBCK pulse for one or more lines following the VSG line. The SUBCKSUPPRESS register enables such suppression.

Readout After Exposure

After the exposure, the readout of the CCD data occurs, beginning with the sensor gate (VSG) operation. By default, the AD9923 generates VSG pulses in every field. When only a single exposure and readout frame are needed, as is the case in the CCD preview mode, the VSG and SUBCK pulses can operate in every field.

However, often during readout, the SUBCK output must be suppressed until the readout is complete. The READOUTNUM register specifies the number of additional fields after the exposure to continue the suppression of SUBCK. READOUTNUM can be programmed for 0 to 7 fields, and should be preprogrammed at startup, not at the same time as the exposure write. A typical interlaced CCD frame readout mode generally requires two fields of SUBCK suppression (READOUTNUM = 2) during readout. A 3-field, 6-phase CCD requires three fields of SUBCK suppression after the readout begins (READOUTNUM = 3).

If SUBCK output is required to initiate backup during the last field of readout, program the READOUTNUM register to one less than the total number of CCD readout fields. Like the exposure operation, the readout operation must be triggered using the TRIGGER register.

SUBCK Additional Masking

The SUBCKMASK register (Address 0x65), allows more complex SUBCK masking. It enables users to select the internal SHUT3 signal and create a custom SUBCK masking pattern that spans several fields.

When generating an exposure by using the TRIGGER register, as described above, the AD9923 outputs the SUBCK and VSG signals on every field by default. This works well for continuous, single field exposure and readout operations, such as those in the CCD live preview mode. However, if the CCD requires a longer exposure time, or if multiple readout fields are needed, the TRIGGER register is needed to initiate specific exposure and readout sequences.

Typically, the exposure and readout bits in the TRIGGER register are used together. This initiates a complete exposure-plus-readout operation. After the exposure, the readout occurs automatically. The values in the EXPOSURE and READOUTNUM registers determine the length of each operation.

It is possible to independently trigger the readout operation without triggering the exposure operation. This causes the readout to occur at the next VD, and the SUBCK output is suppressed according to the value set in the READOUTNUM register.

The TRIGGER register also controls the SHUT and VSUB signals. Each signal is individually controlled, but dependent on the triggering of the exposure and readout operations. See Figure 70 for a complete example of triggering the exposure and readout operations.

Alternatively, it is possible to manually control the exposure and readout operations by carefully updating the SUBCKSUPPRESS and VSG masking registers upon every VD field. As described in the following sections, it is possible to have partial or full manual control of the shutter signals. This allows greater flexibility in generating custom exposure/readout/shutter signal timing.

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Table 38. SUBCK and TRIGGER Register Parameters

Register	Length (Bits)	Range	Description
TRIGGER	8	On/off for eight signals	0: Triggers SHUT0, SHUT1, SHUT2, and SHUT3 signals. 1: Triggers SHUT1 signal. 2: Triggers SHUT2 signal. 3: Triggers SHUT3 signal. 4: Triggers VSUB0 signal. 5: Triggers VSUB1 signal. 6: Triggers EXPOSURE operation. 7: Triggers READOUT operation.
READOUTNUM	3	0 to 7 fields	Number of fields to suppress SUBCK after exposure.
EXPOSURENUM	12	0 to 4095 fields	Number of fields to suppress to SUBCK and VSG during exposure time (low speed shutter).
VDHDOFF	1	On/off	Disable VD/HD output during exposure. 1 = disable VD. 0 = enable VD.
SUBCKPOL[1]	1	High/low	SUBCK start polarity for SUBCK1 and SUBCK2.
SUBCK1TOG1[1]	12	0 to 4095 pixel locations	First toggle positions for first SUBCK pulse (normal shutter).
SUBCK1TOG2[1]	12	0 to 4095 pixel locations	Second toggle positions for first SUBCK pulse (normal shutter).
SUBCK2TOG1[1]	12	0 to 4095 pixel locations	First toggle positions for second SUBCK pulse in last line (high precision).
SUBCK2TOG2[1]	12	0 to 4095 pixel locations	Second toggle positions for second SUBCK pulse in last line (high precision).
SUBCKNUM[1]	12	1 to 4095 pulses	Total number of SUBCKs per field, at one pulse per line.
SUBCKSUPPRESS[1]	12	0 to 4095 pulses	Number of pulses, after the VSG line, to suppress SUBCK.
SUBCKMASK[1]	2	0 to 3 masking mode	Additional masking of SUBCK output. 0 = no additional mask. 1 = start mask at VD edge. 2 = use internal SHUT3 signal to mask.

[1] Register is not VD updated, but updated at the start of the line after the sensor gate line.

Shutter Outputs

The AD9923 contains three shutter output pins: VSUB, MSHUT, and STROBE. Internally, there are six possible shutter signals available: VSUB0, VSUB1, SHUT0, SHUT1, SHUT2, and SHUT3. Any of these signals, and the following combinations: SHUT0 ^ VSUB0, SHUT0 ^ VSUB1, SHUT0 ^ SHUT1, SHUT0 ^ SHUT2, can be mapped to any of the output pins using the VSUB_CTRL, MSHUT_CTRL, and STROBE_CTRL registers.

The VSUB signals behave differently than the SHUT signals, and are generally used for the VSUB output pin. If a more generic approach is desired for the shutter signals, the SHUT signals can be used for the VSUB output pin.

It is also possible to configure the SYNC pin as an output and send one of the internal shutter signals, or the combinations listed above, to the SYNC pin using the TESTO_CTRL register function. This provides the flexibility of outputting up to four shutter outputs if the external SYNC input function is not needed.

VSUB Signal Operation

The CCD readout bias (VSUB) can be programmed to accommodate different CCDs. Figure 67 shows two available modes. In Mode 0, VSUB goes active when the exposure begins during the field of the last SUBCK. The on position (rising edge in Figure 67) is programmable to any line within the field. VSUB remains active until the end of the image readout. In Mode 1, the VSUB is not activated until the start of the readout.

A function called VSUB_KEEPON is also available. When the appropriate VSUB_KEEPON bit is set high, the VSUB output remains active, even after the readout has finished. To disable the VSUB at a later time, set this bit back to low.

The AD9923 contains two programmable VSUB signals, VSUB0 and VSUB1. Either of these signals can be mapped to the VSUB output pin, the MSHUT pin, or the STROBE pin.

SHUT Signal Operation

SHUT signal operation is shown in Figure 68 through Figure 70. Table 39 shows the register parameters for controlling the SHUT signals. There are three different ways to use the SHUT signals: automatic trigger, single trigger, and manual control.

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Automatic Trigger

Generally, SHUT signals are triggered along with an exposure or readout operation, using the TRIGGER register. The SHUT_ON and SHUT_OFF positions are fully programmable to anywhere within the exposure period, using the field

(SHUT_ON_FD/SHUT_OFF_FD), line (SHUT_ON_LN/SHUT_OFF_LN), and pixel (SHUT_ON_PX/SHUT_OFF_PX) registers.

The field registers define the field in which the line and pixel values are used, with respect to the value of the exposure counter. The on and off positions can occur as soon as the field contains the last SUBCK (Exposure Field 0), or as late as the final exposure field before the readout begins. Separate field registers allow the on and off positions to occur in different exposure fields.

Single Trigger

SHUT signals can be triggered without triggering an exposure or readout operation. In this case, SHUT signals are triggered using the TRIGGER register, but the exposure bit is not triggered. Both the SHUT on and off positions occur in the next field, and the SHUT_ON_FD/SHUT_OFF_FD register values are ignored. Single trigger operation is useful if a pulse is required immediately in the next field without the occurrence of an exposure or readout operation. Also, single trigger operation is useful when the exposure or readout operation is manually generated without using the TRIGGER register, and the SUBCK and VSG masking are manually controlled.

Note that single trigger operation cannot occur if an exposure operation has been triggered. SHUT signals behave in automatic trigger mode if they and an exposure operation have been triggered.

Manual Control

Any SHUT signal can be controlled in manual control mode, instead of using the TRIGGER register to activate it. In this mode, the individual on and off lines and pixel positions are used separately, depending on the status of the manual signal control register. Note that only a single toggle position, either off or on, can be used in a VD interval.

As with single trigger operation, when manual control is enabled, the SHUT_ON_FD/SHUT_OFF_FD register values are ignored.

Because there is a separate bit to enable manual control on SHUT signals, this operation can be used regardless of the status of a triggered exposure operation.

Note that manual control can be used in conjunction with automatic or single trigger operations. If a SHUT signal is turned on using manual control, and then manual control is disabled, the SHUT signal remains on. If a subsequent trigger operation occurs, the on position toggle is ignored, because the signal is already on. In this case, only the off position can be triggered.

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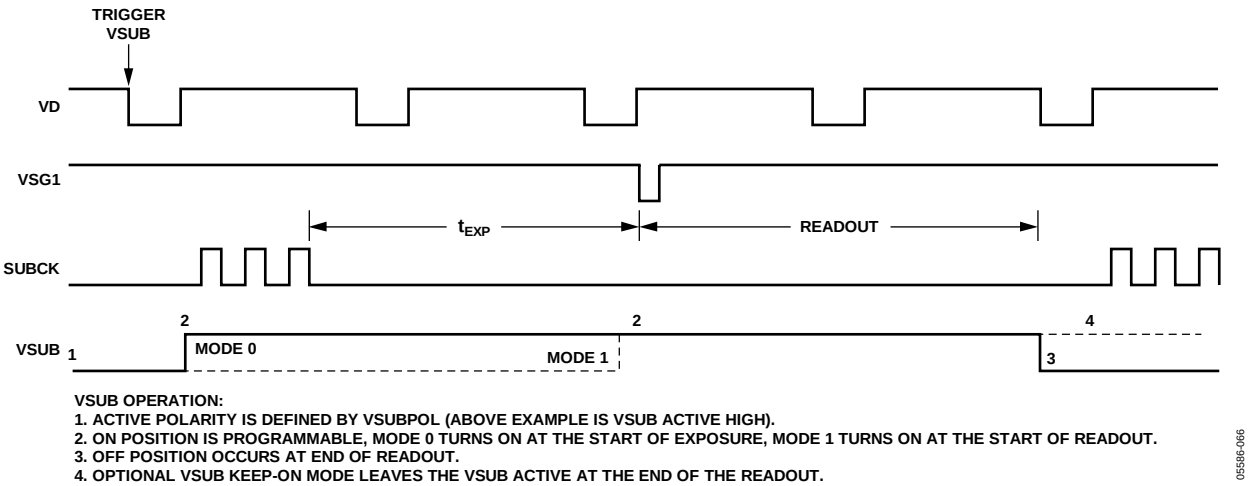

Figure 67. VSUB0, VSUB1 Signal Programmability

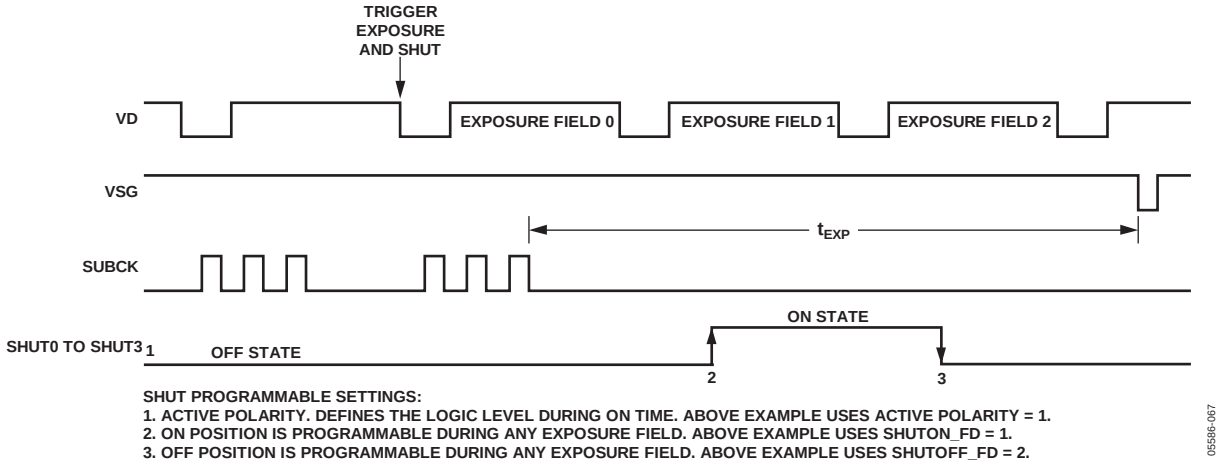

Figure 68. SHUT0 to SHUT3 Signal Programmability

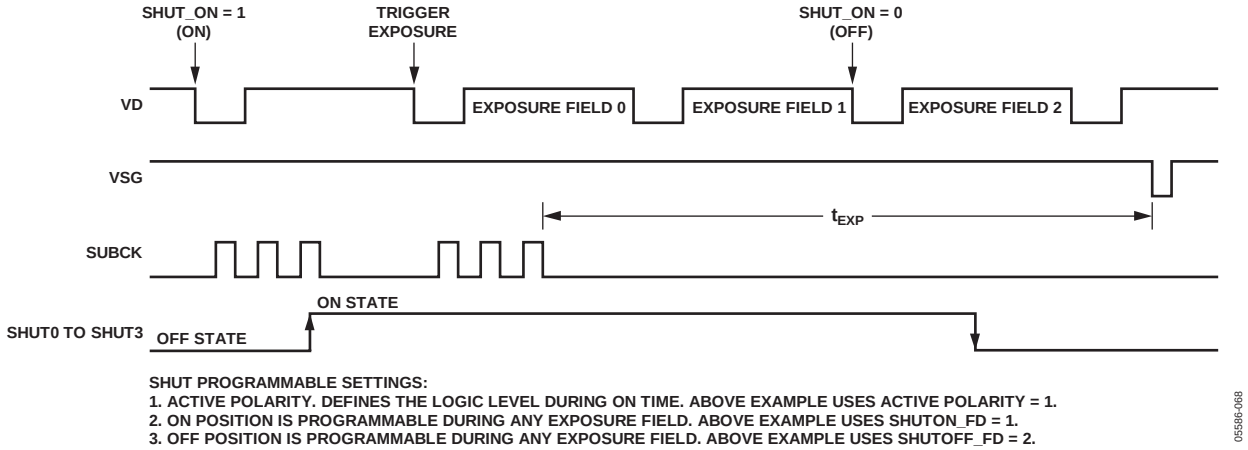

Figure 69. Manual Control of SHUT0 to SHUT3 Signals

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Table 39. VSUB0 to VSUB1 and SHUT0 to SHUT3 Register Parameters

Register	Length (Bits)	Range	Description
VSUB_CTRL	3	0 to 7	Selects which internal shutter signal is mapped to the VSUB pin. 0: SHUT0. 1: SHUT1. 2: SHUT2. 3: SHUT3. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output.
MSHUT_CTRL	3	0 to 7	Selects which internal shutter signal is mapped to the MSHUT pin. 0: SHUT0. 1: SHUT1. 2: SHUT2. 3: SHUT3. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output.
STROBE_CTRL	3	0 to 7	Selects which internal shutter signal is mapped to the STROBE pin. 0: SHUT0. 1: SHUT1. 2: SHUT2. 3: SHUT3. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output.
TESTO_CTRL	3	0 to 7	Selects which internal shutter signal is mapped to the TEST0 signal. 0: SHUT0. 1: SHUT1. 2: SHUT2. 3: SHUT3. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output.
VSUB0_MUX	1	High/low	0 = use VSUB0. 1= use SHUT0 ^ VSUB0.
VSUB1_MUX	1	High/low	0 = use VSUB1. 1= use SHUT0 ^ VSUB 1.
SHUT1_SHUT2_MUX	1	High/low	0 = use SHUT0 ^ SHUT1. 1 = use SHUT0 ^ SHUT2.
VSUB_MODE	1b	High/low	VSUB mode. See Figure 67. 0 = Mode 0. 1 = Mode 1.
VSUB_KEEPON	1	High/low	VSUB keep-on mode. VSUB stays active after readout when set high.
VSUB_ON	12	0 to 4095 line location	VSUB on position. Can turn on at any line in the field.
VSUBPOL	1	High/low	VSUB start polarity. When VSUB is triggered on.

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Register	Length (Bits)	Range	Description
SHUT_ON	1	On/off	SHUT manual control. 0 = SHUT off. 1 = SHUT on.
SHUTPOL	1	High/low	SHUT active polarity.
SHUT_MAN	1	Enable/disable	Enables SHUT manual control mode. 0 = disable. 1 = enable.
SHUT_ON_FD	12	0 to 4095 field location	Field location to switch on MSHUT. Inactive, or closed
SHUT_ON_LN	12	0 to 4095 line location	Line position to switch on MSHUT. Inactive, or closed.
SHUT_ON_PX	13	0 to 8191 pixel location	Pixel position to switch on MSHUT. Inactive, or closed.
SHUT_OFF_FD	12	0 to 4095 field location	Field location to switch off MSHUT. Inactive, or closed.
SHUT_OFF_LN	12	0 to 4095 line location	Line position to switch off MSHUT. Inactive, or closed.
SHUT_OFF_PX	13	0 to 8191 pixel location	Pixel position to switch off MSHUT. Inactive, or closed.

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EXAMPLE OF EXPOSURE AND READOUT OF INTERLACED FRAME

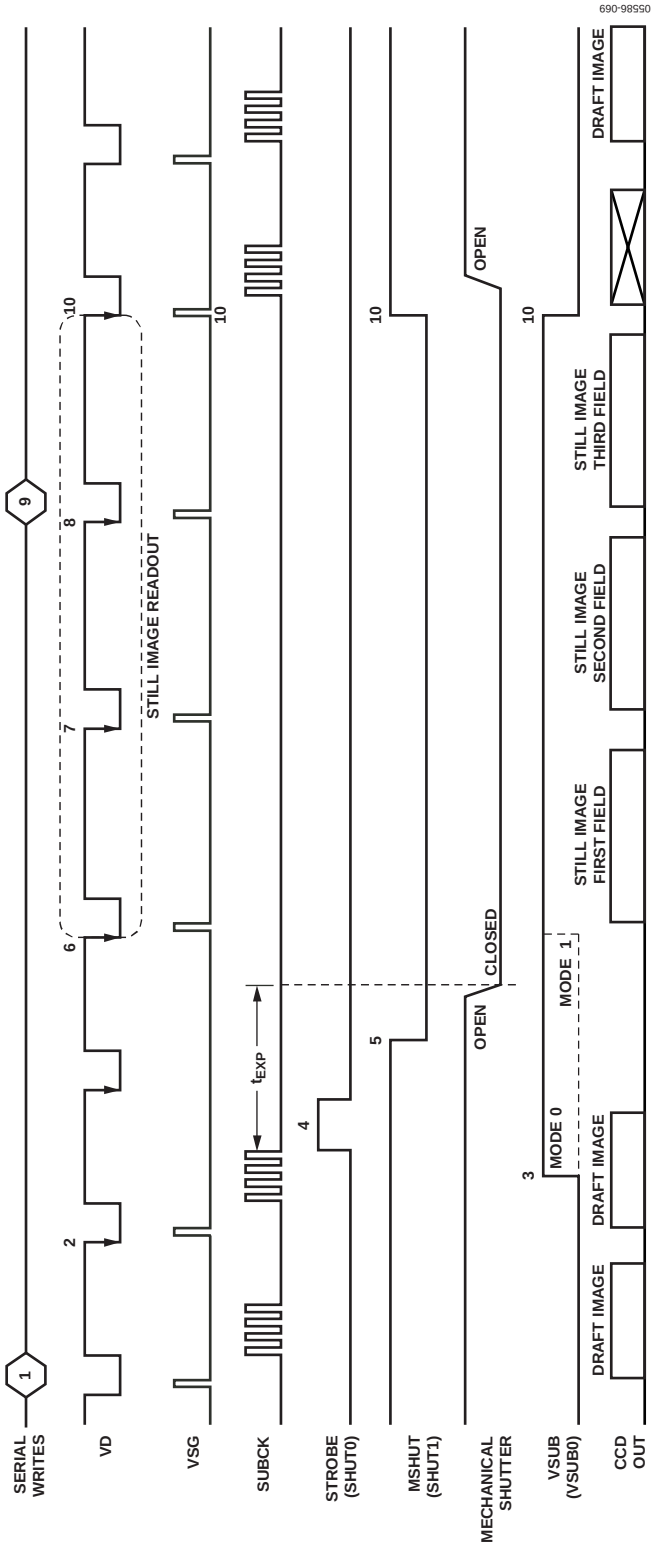

Figure 70. Example of Exposure and Still Image Readout Using Shutter Signals and Mode Register

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Explanation of Figure 70

The numbers in the Explanation of Figure 70 section correspond to the numbers embedded in Figure 70.

1. Write to the READOUTNUM register (Address 0x62) to specify the number of fields to suppress SUBCK during readout of CCD data. In this example, READOUTNUM = 3.

   Write to the EXPOSURENUM register (Address 0x63) to specify the number of fields to suppress SUBCK and VSG outputs during exposure. In this example, EXPOSURENUM = 1

   Write to the TRIGGER register (Address 0x61) to trigger the SHUT0 (STROBE), SHUT1 (MSHUT), and VSUB0 (VSUB) signals, and to start the exposure-plus-readout operation. To trigger these events (see Figure 70), set the register TRIGGER = 0xD3. Readout automatically occurs after the exposure period finishes.

   Write to the MODE register to configure the next five fields. The first two fields during exposure are the same as the current draft mode fields, and the next three fields are the still frame readout fields. The register settings for the draft mode field and the three readout fields are previously programmed.

2. VD/HD falling edge updates the serial writes from 1.

3. If VSUB0 MODE = 0 (Address 0x69), VSUB output turns on at the line specified in the VSUB0_ON register (Address 0x6A).

4. STROBE output turns on and off at the location specified in the SHUT0_ON/SHUT0_OFF registers (Address 0x6D/ Address 0x71).

5. MSHUT output turns off at the location specified in the SHUT1_OFF_FD, SHUT1_OFF_LN, and SHUT1_OFF_PX registers (Address 0x75 and Address 0x76). The SHUT1 on position is ignored, because the SHUT1 signal is already on from a previous manual operation (see Step 10).

6. The next VD falling edge automatically starts the first readout field.

7. The next VD falling edge automatically starts the second readout field.

8. The next VD falling edge automatically starts the third readout field.

9. Write to the MODE register to reconfigure the single draft mode field timing.

   Write a 1 to the SHUT1_MAN and SHUT1_ON registers (Address 0x72) to turn the MSHUT output back manually.

10. VD/HD falling edge updates the serial writes from 9. VSG outputs return to draft mode timing. SUBCK output resumes operation.

    MSHUT output returns to the on position (active, or open). Be sure to disable manual control of SHUT1 before another automatic trigger of the SHUT1 signal is needed.

    VSUB output returns to the off position (inactive).

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FG_TRIG OPERATION

The AD9923 contains one additional signal that can be used in conjunction with shutter operation or general system operation. The FG_TRIG signal is an internally generated pulse that can be output on the SYNC pins for shutter or other system functions. A unique feature of the FG_TRIG signal is that it is output with respect to the MODE register field status.

The FG_TRIG signal is generated using the SHUT1 start polarity and toggle position registers, programmable with line and pixel resolution. The field registers for SHUT1 are ignored because the field placement of the FG-TRIG pulse is matched to the field count specified by the MODE register operation. The FG_TRIGEN register contains a 3-bit value that specifies which field count contains the FG_TRIG pulse. Figure 71 shows how the FG_TRIG pulse is generated using these registers.

After the FG_TRIG signal is specified, it can be enabled using Bit 3 of the FG_TRIGEN register. The FG_TRIG signal is mapped to the SYNC output if the SYNC pin is configured as an output (SYNCENABLE = 0).

Table 40. FG_TRIG Operation Registers

Register	Address	Bit Location	Description
SYNCENABLE	0x12	[0]	0 = configures SYNC pin as an output. By default, the FG_TRIG signal is output on the SYNC pin. 1 = SYNC pin is an external synchronization input.
FG_TRIGEN	0xF1	[3:0]	[2:0] selects field count for pulse based on mode field counter. [3] = 1 to enable FG_TRIG signal output.
SHUT1POL	0x72	[1]	[1] FG_TRIG start polarity.
SHUT1_ON_LN	0x74	[11:0]	FG_TRIG first toggle, line location.
SHUT1_ON_PX	0x74	[25:13]	FG_TRIG first toggle, pixel location.
SHUT1_OFF_LN	0x76	[11:0]	FG_TRIG second toggle, line location.
SHUT1_OFF_PX	0x76	[25:13]	FG_TRIG second toggle, pixel location.

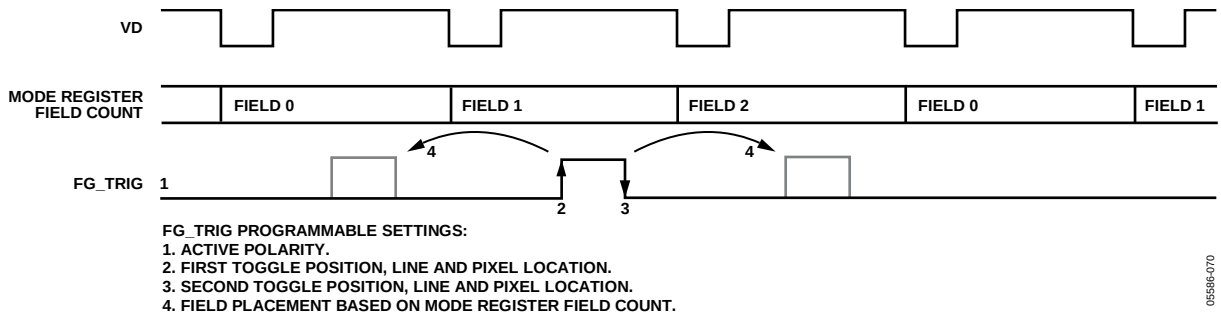

Figure 71. FG_TRIG Signal Generation

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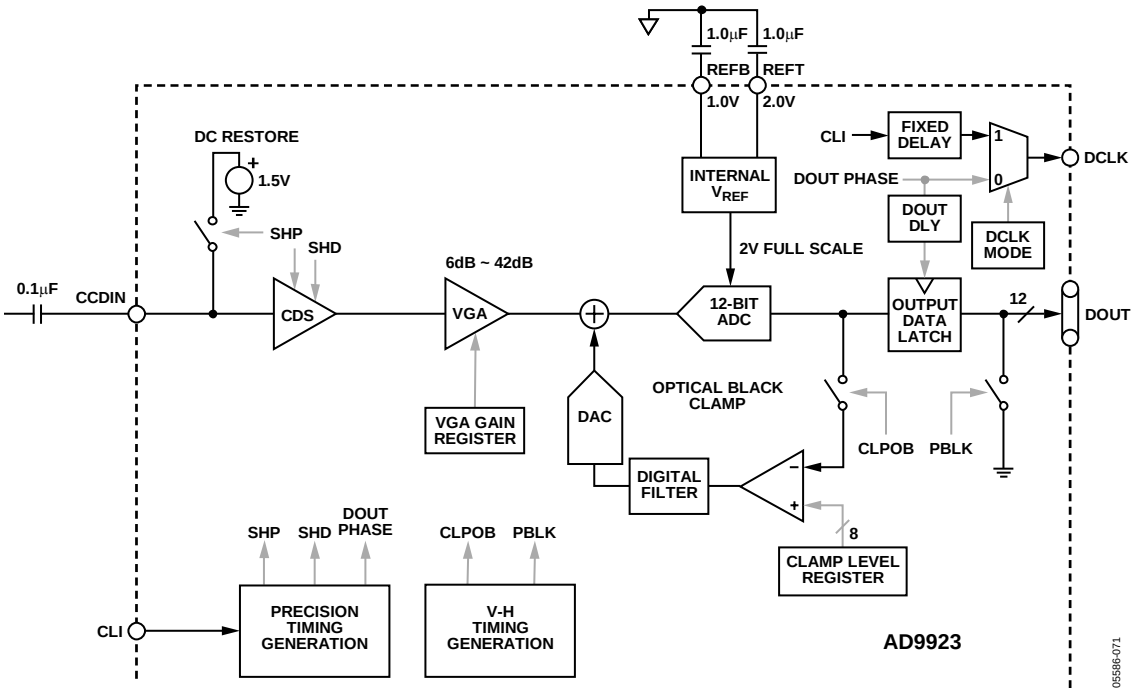

Figure 72. Analog Front End Functional Block Diagram

ANALOG FRONT END DESCRIPTION/OPERATION

The AD9923 signal processing chain is shown in Figure 72. Each step is essential to achieve a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.5 V so that it is compatible with the 3 V supply voltage of the AD9923.

Correlated Double Sampler

The CDS circuit samples each CCD pixel twice to extract video information and reject low frequency noise. The timing shown in Figure 20 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference and data levels of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC and SHDLOC registers located at Address 0x37. Placement of these clock signals is critical to achieve the best CCD performance.

The CDS gain can be set to −3 dB, 0 dB (default), +3 dB, or +6 dB in the CDSGAIN register, Address 0x04. The +3 dB and +6 dB settings improve noise performance, but reduce the input range (see Figure 8).

Variable Gain Amplifier

The VGA stage provides gain in the range of 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. A minimum gain of 6 dB is needed to match a 1 V input signal with an ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent range of gain is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain can be calculated for any gain register value using the following equation

$$Gain\ (\text{dB}) = (0.0351 \times Code) + 5.5\ \text{dB}$$

where the code range is 0 to 1023.

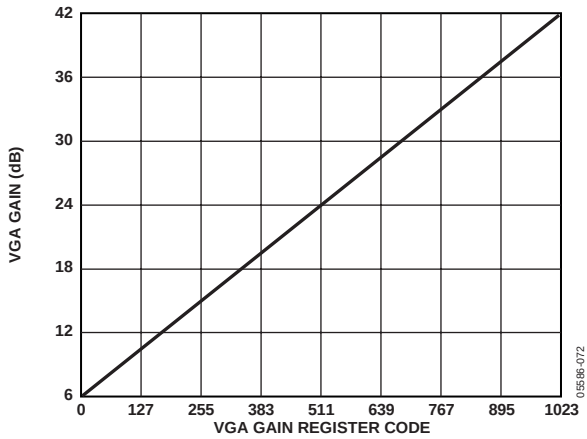

Figure 73. VGA Gain Curve

ADC

The AD9923 uses a high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 1 LSB. The ADC uses a 2 V input range. See Figure 6 and Figure 8 for typical linearity and noise performance plots.

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Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the CLAMPLEVEL register. The value can be programmed between 0 LSB and 255 LSB in 1,023 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during postprocessing, the AD9923 optical black clamping can be disabled using the CLPENABLE register (Address 0x00, Bit D2). Even though the loop is disabled, the CLAMPLEVEL register can still be used to provide programmable offset adjustment.

The CLPOB pulse should be placed during the CCD optical black pixels. It is recommended that the CLPOB pulse duration is at least 20 pixels wide to minimize clamping noise. Shorter pulse widths can be used, but clamping noise might increase, reducing the ability to track low frequency variations in the black level. See the Horizontal Clamping and Blanking section for timing examples.

Digital Data Outputs

The digital output data is latched using the DOUT PHASE register value, as shown in Figure 72. Output data timing is shown in Figure 21 and Figure 22. It is also possible to leave the output latches transparent, so that the data outputs from the ADC are immediately valid. Programming the DOUTLATCH register, Bit D1, to 1 sets the output latches transparent. The data outputs can also be disabled (three-stated) by setting the DOUTDISABLE Register 0x01, Bit D0, to 1.

The DCLK output can be used for external latching of the data outputs. By default, the DCLK output tracks the value of the DOUTPHASE register. By changing the DCLKMODE register, the DCLK output can be held at a fixed phase, and the DOUTPHASE register value is ignored.

To optimize the delay between the DCLK rising edge and the data output transition, the DOUTDELAY register is used. By default, there is approximately 8 ns of delay from the rising edge of DCLK to the transition of the data outputs. See the High Speed Timing Generation section for more information.

Switching the data outputs can couple noise into the analog signal path. To minimize switching noise, set the DOUTPHASE register to the same edge as the SHP sampling location, or up to 11 edges after the SHP sampling location. Other settings can produce good results, but require experimentation. It is recommended that the DOUTPHASE location not occur between the SHD sampling location and 11 edges after the SHD location. For example, if SHDLOC = 0, set DOUTPHASE to an edge location of 12 or greater. If adjustable phase is not required for the data outputs, the output latch can be left transparent using Register 0x01, Bit D1.

Data output coding is normally straight binary, but can be changed to gray coding by setting the GRAYEN Register 0x01, Bit D2, to 1.

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Recommended Power-Up Sequence for Master Mode

When the AD9923 is powered up, the following sequence is recommended (see Figure 74):

1. Turn on the power supplies for the AD9923, and start the master clock, CLI.
2. Reset the internal AD9923 registers by writing 1 to the SW_RST register (Address 0x10).
3. By default, all vertical outputs (XV, VSG, SUBCK) are low. If necessary, write to the STANDBY3POL Register 0xE2 to set different polarities for the vertical outputs to avoid damage to the V-driver and the CCD. See Table 43 for more information on polarities.
4. Bring the V5V pin high. V5V should be driven with a 3 V signal through a diode (see Figure 81). V5V must reach a minimum voltage of 2.3 V before continuing with the power-up sequence.
5. VH and VL, the V-driver supplies, can be powered up after completing Step 3 and Step 4. There are no restrictions on the order in which VH and VL are powered up.
6. Load the required registers to configure the required VPAT group, V-sequence, field timing information, high speed timing, horizontal timing, and shutter timing information.
7. To place the part into normal power operation, write 0x04 to the AFE STANDBY register (Bits[1:0], Address 0x00). If the CLO output is being used to drive a crystal, also power up the CLO oscillator by writing 1 to Register 0x16.
8. By default, the internal timing core is held in a reset state with TGCORE_RSTB register = 0. Write 1 to the TGCORE_RSTB register (Address 0x15) to start the internal timing core operation. If a 2× clock is used for the CLI input, set the CLIDIVIDE register (Address 0x30) to 1 before resetting the timing core.
9. Configure the AD9923 for master mode timing by writing 1 to the MASTER register (Address 0x20).
10. Write 1 to the OUTCONTROL register (Address 0x11). This allows the outputs to become active after the next SYNC rising edge.
11. Generate a SYNC event. If SYNC is high at power-up, bring SYNC input low for a minimum of 100 ns. Then, bring SYNC high. This causes the internal counters to reset and starts a VD/HD operation. The first VD/HD edge allows VD register updates to occur, including OUTCONTROL to enable all outputs. If an external SYNC pulse is not available, an internal SYNC pulse can be generated by writing to the SYNCPOL register, as described in the Generating Software Sync Without External Sync Signal section.

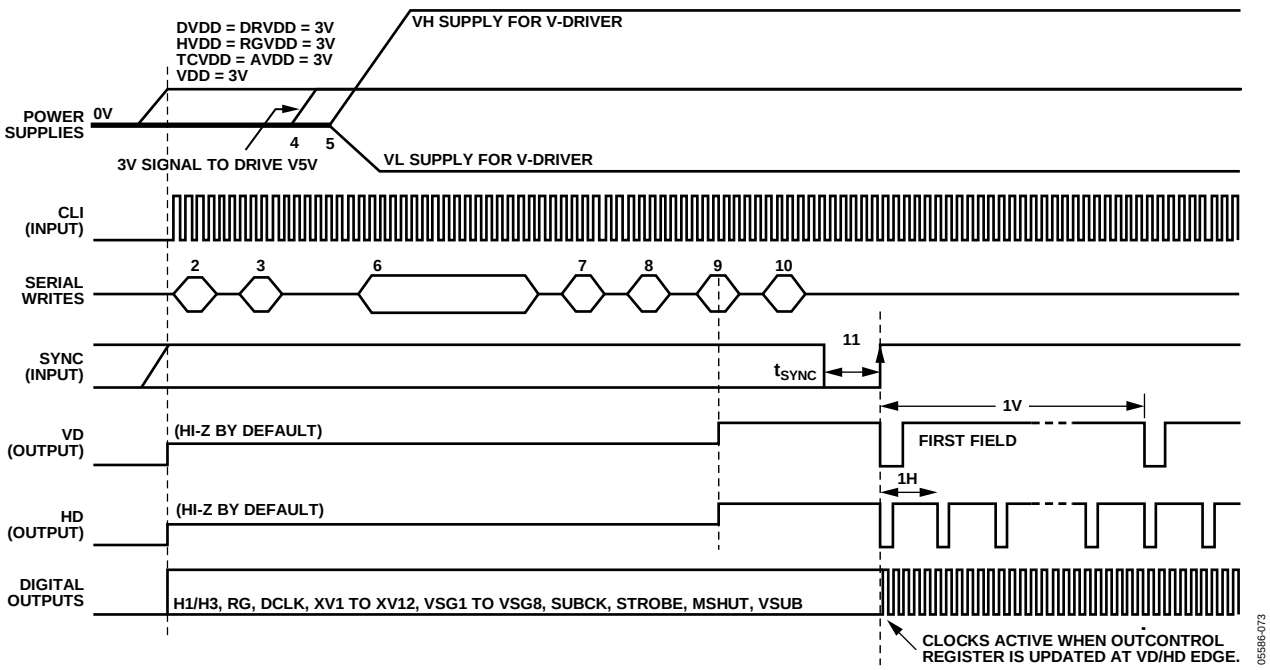

Figure 74. Recommended Power-Up Sequence and Synchronization, Master Mode

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Table 41. Power-Up Register Write Sequence

Register	Address	Data	Description
SW_RST	0x10	0x01	Resets all registers to default values
STANDBY3POL	0xE2	TBD	Standby 3 vertical and shutter output polarities
	0x20 to 0xFFF	TBD	Horizontal, vertical, shutter timing
STANDBY	0x00	0x04	Powers up the AFE
TEST3	0xEA	0x60	Set TEST3 register to recommended value
OSC_RST	0x16	0x01	Resets crystal oscillator circuit
TGCORE_RSTB	0x15	0x01	Resets internal timing core
MASTER	0x20	0x01	Configures master mode
OUTCONTROL	0x11	0x01	Enables all outputs after SYNC
SYNCPOL	0x13	0x01	SYNC active polarity (for software SYNC only)

Generating Software Sync Without External Sync Signal

If an external sync pulse is not available, it is possible to generate an internal sync pulse by writing to the SYNCPOL register (Address 0x13). If the software SYNC option is used, the SYNC input (Pin 35) should be low (VSS) during the power-up procedure. After the power-up procedure is complete, the SYNC pin can be used as an output by setting the SYNCENABLE register low (Address 0x12).

After power-up, follow Step 1 to Step 10 of the procedure in the Recommended Power-Up Sequence for Master Mode section. For Step 11, instead of using the external sync pulse, write 1 to the SYNCPOL register to generate an internal sync pulse and begin the timing operation.

SYNC During Master Mode Operation

The SYNC input can be used anytime during master mode operation to synchronize the AD9923 counters with external timing, as shown in Figure 75.

To suspend operation of the digital outputs during the SYNC operation, set the SYNCSUSPEND register (Address 0x14) to 1. If SYNCSUSPEND = 1, the polarities of the outputs are held at the same state as when OUTCONTROL = low, as shown in Table 42 and Table 43.

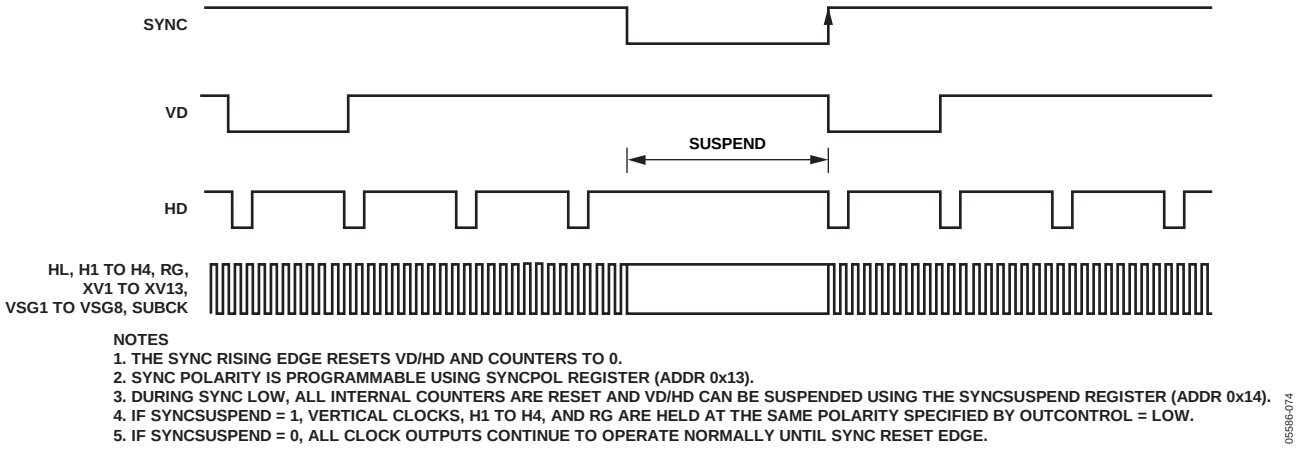

Figure 75. SYNC Timing to Synchronize AD9923 with External Timing

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Power-Up and Synchronization in Slave Mode

The power-up procedure for slave mode operation is the same as the procedure described for master mode operation, with two exceptions:

- Eliminate Step 8. Do not configure the part for master mode timing.
- No sync pulse is required in slave mode. Substitute Step 10 with starting the external VD and HD signals. This synchronizes the part, allows the register updates, and starts the timing operation.
- Note that DCLK will not begin to transition until Step 7 is complete.

When the AD9923 is used in slave mode, the VD/HD inputs synchronize the internal counters. After a falling edge of VD, there is a latency of 34 master clock edges (CLI) after the falling edge of HD until the internal H-counter is reset. The reset operation is shown in Figure 76.

Note: If SHDLOC is set so that the 3 ns minimum delay between the rising edge of SLI and the falling edge of the internal SHD signal is **NOT** met, the internal H-counter can reset after only 33 master clock edges (CLI).

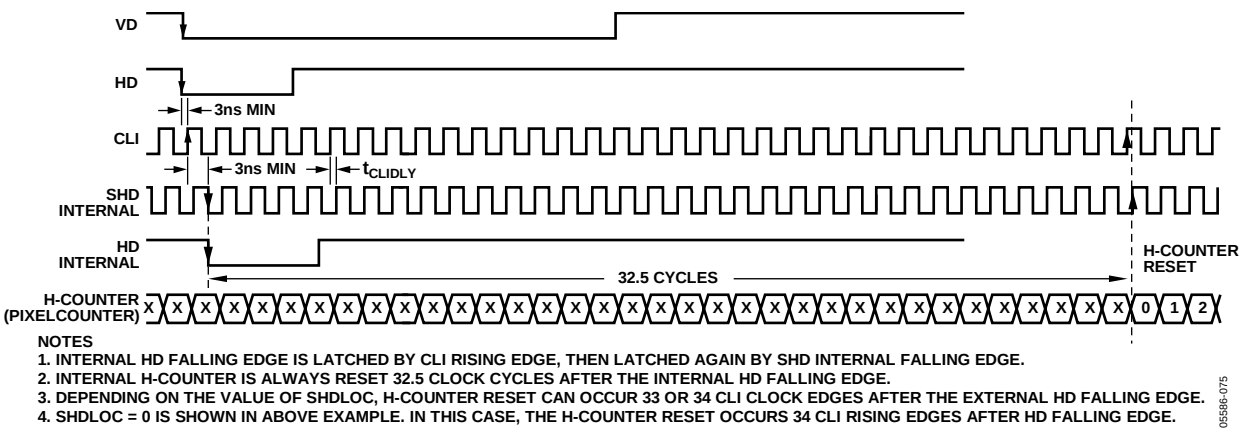

Figure 76. External VD/HD and Internal H-Counter Synchronization, Slave Mode

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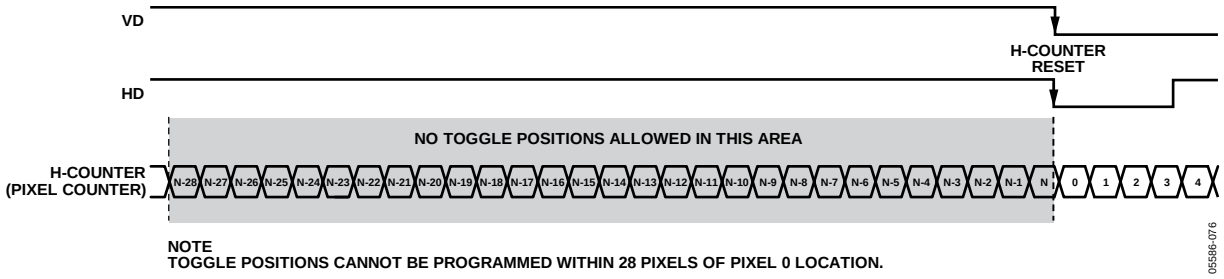

Figure 77. Toggle Position Inhibited Area—Master Mode

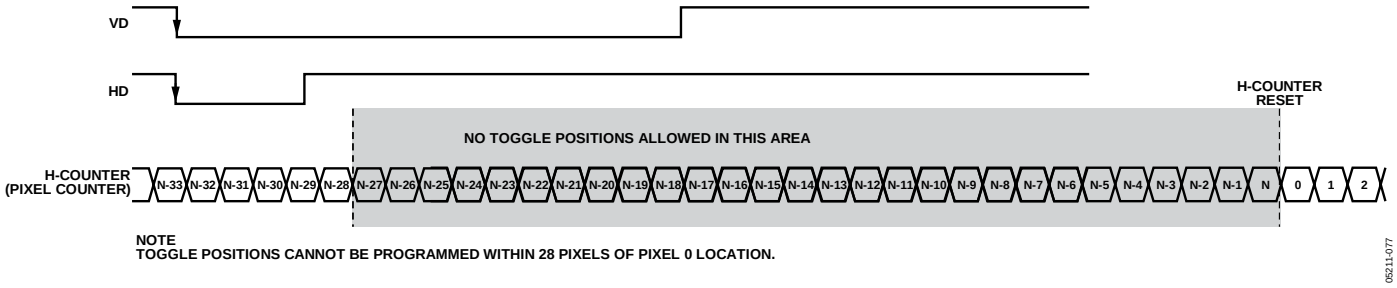

Figure 78. Toggle Position Inhibited Area—Slave Mode

Vertical Toggle Position Placement Near Counter Reset

One additional consideration during the reset of the internal counters is the vertical toggle position placement. Prior to the internal counters being reset, there is a region of 28 pixels during which no toggle positions can be programmed.

As shown in Figure 77, in master mode, the last 28 pixels before the HD falling edge should not be used for toggle position placement of the XV, VSG, SUBCK, HBLK, PBLK, or CLPOB pulses.

The next figure shows the same example for slave mode. The same restriction applies—the last 28 pixels before the counters are reset and cannot be used. However, the counter reset is delayed with respect to VD/HD placement; therefore, the inhibited area is different than it is in master mode.

It is also recommended that Pixel Location 0 is not used for toggle positions for the VSG and SUBCK pulses.

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STANDBY MODE OPERATION

The AD9923 contains three standby modes to optimize the overall power dissipation in various applications. Bits[1:0] of Register 0x00 control the power-down state of the device:

STANDBY[1:0] = 00 = normal operation (full power)

STANDBY[1:0] = 01 = Standby 1 mode

STANDBY[1:0] = 2 = Standby 2 mode

STANDBY[1:0] = 3 = Standby 3 mode (lowest power)

Table 42 and Table 43 summarize the operation of each power-down mode. Note that when OUTCONTROL = LO, it takes priority over the Standby 1 and Standby 2 modes in determining the digital output states, but Standby 3 mode takes priority over OUTCONTROL. Standby 3 has the lowest power consumption, and can shut down the crystal oscillator circuit between CLI and CLO. If CLI and CLO are being used with a crystal to generate the master clock, this circuit is powered down and there is no clock signal. When returning the device from Standby 3 mode to normal operation, reset the timing core at least 500 µs after writing to the OPRMODE register. This allows sufficient time for the crystal circuit to settle. The vertical and shutter outputs can be programmed to hold a specific value during the Standby 3 mode using Register 0xE2, as detailed in Table 43. The vertical outputs can be programmed to hold a specific value when OUTCONTROL = LO, or when in Standby 1 or Standby 2 mode, by using Register 0xF3. Please see the endnote references (Endnote 2 to Endnote 4) following Table 43 for the mapping of the bits in these registers to the various vertical and shutter outputs when the device is in one of the three standby modes, or when OUTCONTROL = LO. This feature is useful during power-up if different polarities are required by the V-driver and CCD to prevent damage.

Table 42. Standby Mode Operation

I/O Block	Standby 3 (default)[1, 2]	OUTCONTROL = LO[2]	Standby 2[3, 4]	Standby 1[3, 4]
AFE	Off	No change	Off	Only REFT, REFB on
Timing Core	Off	No change	Off	On
CLO Oscillator	Off	No change	On	On
CLO	HI	Running	Running	Running
HL	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
H1	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
H2	Hi-Z	HI	HI (4.3 mA)	HI (4.3 mA)
H3	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
H4	Hi-Z	HI	HI (4.3 mA)	HI (4.3 mA)
RG	Hi-Z	LO	LO (4.3 mA)	LO (4.3 mA)
VD	LO	$\overline{\text{VDHDPOL}}$ value	$\overline{\text{VDHDPOL}}$ value	Running
HD	LO	$\overline{\text{VDHDPOL}}$ value	$\overline{\text{VDHDPOL}}$ value	Running
DCLK	LO	Running	LO	Running
DOUT	LO	LO	LO	LO

[1] To exit Standby 3, write 00 to STANDBY (Bits[1:0], Address 0x00), then reset the timing core after 500 µs to guarantee proper settling of the oscillator.
[2] Standby 3 mode takes priority over OUTCONTROL for determining the output polarities.
[3] These polarities assume OUTCONTROL = HI, because OUTCONTROL = LO takes priority over Standby 1 and Standby 2.
[4] Standby 1 and Standby 2 set H and RG drive strength to their minimum values (4.3 mA).

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Table 43. Standby Mode Operation—Vertical and Shutter Outputs

Output	Standby 3 (default)[1, 2]	OUTCONTROL = LO	Standby 2[3, 4]	Standby 1[3, 4]
XV1	LO	LO	LO	LO
XV2	LO	LO	LO	LO
XV3	LO	LO	LO	LO
XV4	LO	LO	LO	LO
XV5	LO	LO	LO	LO
XV6	LO	LO	LO	LO
XV7	LO	LO	LO	LO
XV8	LO	LO	LO	LO
XV9	LO	LO	LO	LO
XV10	LO	LO	LO	LO
XV11	LO	LO	LO	LO
XV12	LO	LO	LO	LO
XV13	LO	HI	HI	HI
VSG1	LO	HI	HI	HI
VSG2	LO	HI	HI	HI
VSG3	LO	HI	HI	HI
VSG4	LO	HI	HI	HI
VSG5	LO	HI	HI	HI
VSG6	LO	HI	HI	HI
VSG7	LO	HI	HI	HI
VSG8	LO	HI	HI	HI
XSUBCK	LO	HI	HI	HI
VSUB[5]	LO	LO	LO	LO
MSHUT[5]	LO	LO	LO	LO
STROBE[5]	LO	LO	LO	LO

[1] Polarities for vertical and shutter outputs when the AD9923 is in Standby 3 mode are programmable using the STANDBY3POL register, Address 0xE2 (default register value = 0x000000).
[2] Bit assignments for the STANDBY3POL[23:0] register (Address 0xE2): (MSB) STROBE, MSHUT, VSUB, XSUBCK, VSG8, VSG7, VSG6, VSG3, VSG5, VSG4, VSG2, VSG1, XV13, XV12, XV11, XV10, XV9, XV8, XV7, XV6, XV5, XV4, XV3, XV2, and XV1 (LSB).
[3] Polarities for vertical outputs when the AD9923 is in Standby 1 and Standby 2, or OUTCONTROL = LO, are programmable using the STANDBY12POL register, Address 0xF3 (default register value = 0x3FE000)
[4] Bit assignments for the STANDBY12POL[20:0] register (Address 0xF3): (MSB) XSUBCK, VSG8, VSG7, VSG6, VSG3, VSG5, VSG4, VSG2, VSG1, XV13, XV12, XV11, XV10, XV9, XV8, XV7, XV6, XV5, XV4, XV3, XV2, and XV1 (LSB).
[5] VSUB, MSHUT, and STROBE polarities for Standby 1 and Standby 2 modes are controlled by STANDBY3POL.

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CIRCUIT LAYOUT INFORMATION

The AD9923 typical circuit connections are shown in Figure 81. The PCB layout is critical for achieving good image quality from the AD9923. All supply pins, particularly the pins for the AVDD, TCVDD, RGVDD, and HVDD supplies, must be decoupled to ground with good quality, high frequency chip capacitors. The decoupling capacitors should be as close as possible to the supply pins and have a very low impedance path to a continuous ground plane. There should be a bypass capacitor of at least 4.7 µF for each main supply—AVDD, HVDD, and DRVDD—but this is not necessary for each individual pin. In most applications, it is easier to share the supply for RGVDD and HVDD, which requires bypassing each supply pin separately. A separate 3 V supply can also be used for DRVDD, but it should still be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended.

The analog bypass pins (REFT and REFB) should be carefully decoupled to ground, as close as possible to their respective pins. The analog input (CCDIN) capacitor should also be located close to the pin.

The HL, H1 to H4, and RG traces should be designed to have low inductance to avoid excessive distortion of the signals. The complementary signals H1 and H2 should be routed as close together and as symmetrically as possible to minimize mutual inductance. The same should be done for the H3 and H4 signals. Heavier PCB traces are recommended because of the large transient current demand on HL and H1 to H4 by the CCD. If possible, physically locating the AD9923 closer to the CCD reduces the inductance on these lines. The routing path should be as direct as possible from the AD9923 to the CCD.

When powering up the V-driver of the AD9923, it is important to follow the following steps:

1. Connect VDD1, VDD2 to a +3 V supply and keep V5V low.
2. Perform any necessary writes to Register 0xE2.
3. Power-up the 3 V signal that drives the diode to V5V.
4. After V5V reaches a minimum voltage of 2.3 V, VH and VL can be powered on. There are no restrictions on the order in which VH and VL can be powered on.

A Schottky diode is recommended to drive the V5V pin to maximize the voltage on V5V prior to VH/VL powering on.

The AD9923 also contains an on-chip oscillator for driving an external crystal. The maximum crystal frequency that the AD9923 can support is 36 MHz. Figure 79 shows an example application using a typical 24 MHz crystal. For the exact values of the external resistors and capacitors, see the crystal manufacturer's data sheet.

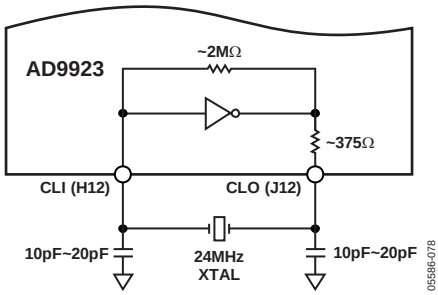

Figure 79. Crystal Driver Application

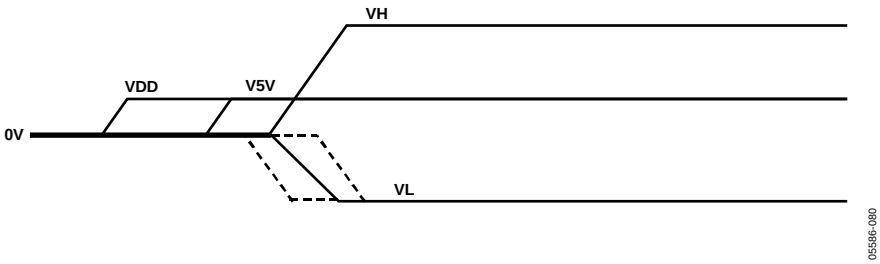

Figure 80. Suggested Power-Up Sequence for AD9923

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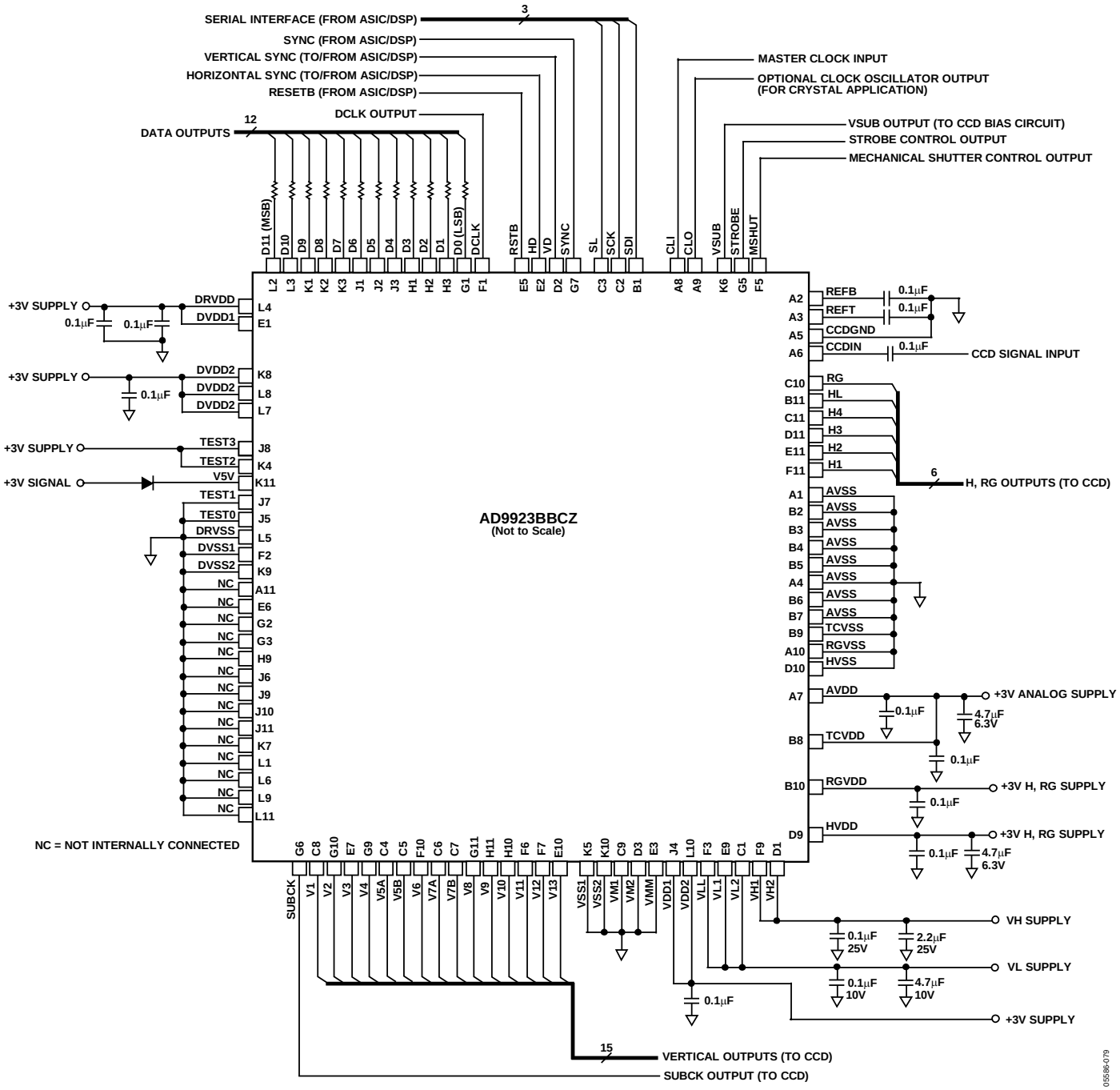

Figure 81. AD9923BBCZ Typical Circuit Configuration

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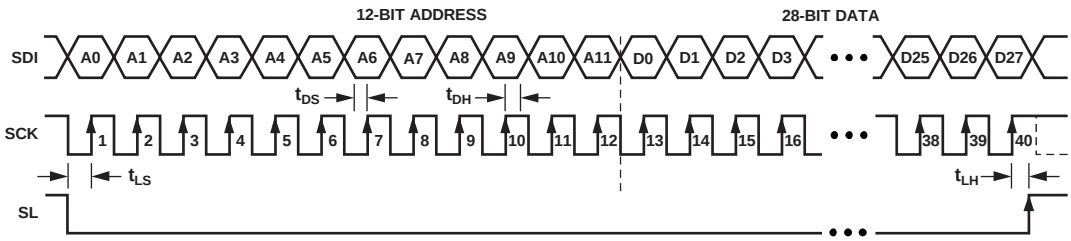
SERIAL INTERFACE TIMING

All of the AD9923 internal registers are accessed through a 3-wire serial interface. Each register consists of a 12-bit address and a 28-bit data-word. Both the address and data-word are written by starting with the LSB. To write to each register, a 40-bit operation is required, as shown in Figure 82. Although many data-words are fewer than 28 bits wide, all 28 bits must be written for each register. For example, if the data-word is only 20 bits wide, the upper 8 bits are don't cares and must be filled with 0s during the serial write operation. If fewer than 28 data bits are written, the register is not updated with new data.

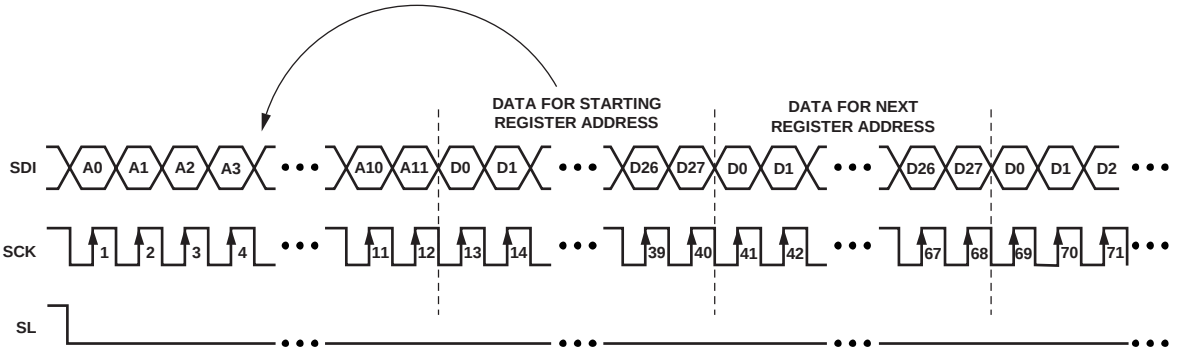
Figure 83 shows a more efficient way to write to the registers, using the AD9923 address auto-increment capability. Using this method, the lowest desired address is written first, followed by multiple 28-bit data-words. Each data-word is automatically written to the address of the next highest register. By eliminating the need to write each address, faster register loading is achieved. Continuous write operations can start with any register location.



NOTES
1. SDATA BITS ARE LATCHED ON SCK RISING EDGES. SCK MAY IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. ALL 40 BITS MUST BE WRITTEN: 12 BITS FOR ADDRESS AND 28 BITS FOR DATA-WORD.
3. IF THE DATA-WORD IS <28 BITS, 0s MUST BE USED TO COMPLETE THE 28-BIT DATA-WORD LENGTH.
4. NEW DATA VALUES ARE UPDATED IN THE SPECIFIED REGISTER LOCATION AT DIFFERENT TIMES, DEPENDING ON THE PARTICULAR REGISTER WRITTEN TO. SEE THE UPDATING OF NEW REGISTER VALUES SECTION FOR MORE INFORMATION.

05586-081

Figure 82. Serial Write Operation



NOTES
1. MULTIPLE SEQUENTIAL REGISTERS CAN BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 28-BIT DATA-WORDS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 28-BIT DATA-WORD (ALL 28 BITS MUST BE WRITTEN).
4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER IS LOADED.

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Figure 83. Continuous Serial Write Operation

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LAYOUT OF INTERNAL REGISTERS

The AD9923 address space is divided into two register areas, as illustrated in Figure 84. In the first area, Address 0x00 to Address 0x91 contain the registers for the AFE, miscellaneous functions, VD/HD parameters, timing core, CLPOB masking, SG patterns, shutter functions, and memory configuration. The second area of the address space, beginning at Address 0x400, consists of the registers for the V-pattern groups, V-sequences, and fields. This is a configurable set of registers; the user can decide how many V-pattern groups, V-sequences, and fields are used in a particular design. Therefore, the addresses for these registers vary, depending on the number of V-patterns and V-sequences chosen.

Register 0x90 (VPAT_NUM) and Register 0x91 (VSEQ_NUM) specify the total number of V-pattern groups and V-sequences used. The starting address for the V-pattern groups is 0x400. The starting address for a V-sequence is based on the number of V-pattern groups used, with each V-pattern group occupying 40 register addresses. The starting address for a field register depends on both the number of V-pattern groups and the number of V-sequences. Each V-sequence occupies 20 register addresses, and each field occupies 12 register addresses.

The starting address for a V-sequence is equal to 0x400 plus the number of V-pattern groups times 40. The starting address for a field is equal to the starting address of a V-sequence plus the number of V-sequences times 20. The VPAT, VSEQ, and field registers must occupy a continuous block of addresses.

Figure 85 shows an example with three V-pattern groups, four V-sequences, and two fields. The starting address for the V-pattern groups is 0x400. Because VPAT_NUM = 3, the V-pattern groups occupy 120 address locations. The start of the V-sequence register is 0x400 + 120 = 0x478. With VSEQ_NUM = 3, the V-sequences occupy 60 address locations. Therefore, the field registers begin at 0x448 + 60 = 0x4B4.

The AD9923 address space contains many unused addresses. Undefined addresses between Address 0x00 and Address 0x399 should not be written to, or the AD9923 might operate incorrectly. Continuous register writes should be performed carefully to avoid writing to undefined registers.

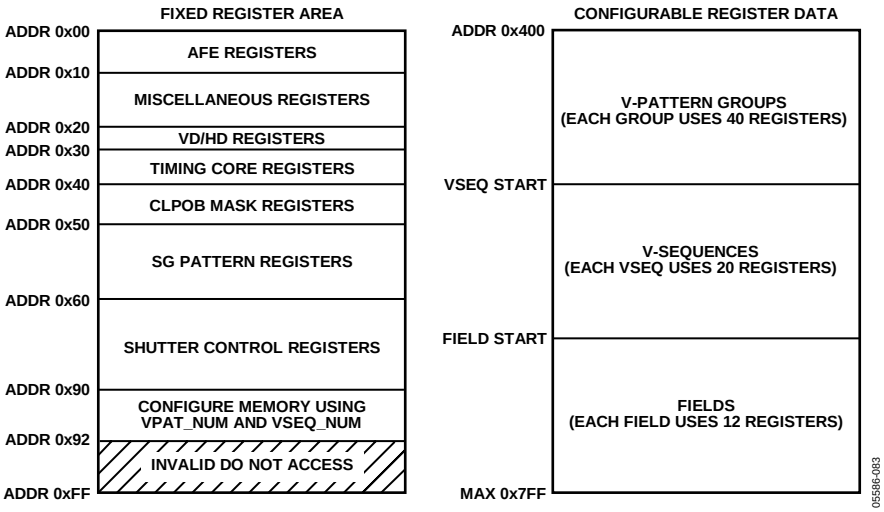

Figure 84. Layout of AD9923 Registers

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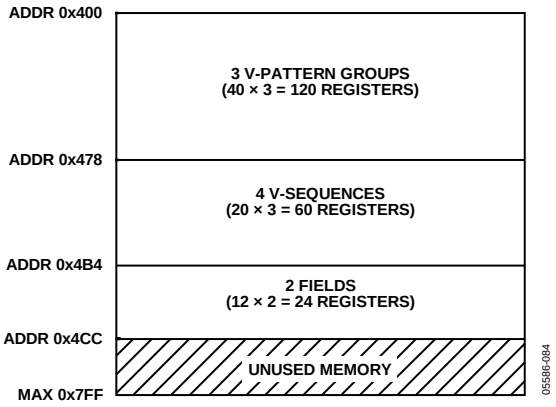

Figure 85. Example of Register Configuration

UPDATING NEW REGISTER VALUES

The AD9923 internal registers are updated at different times, depending on the particular register. Table 44 summarizes the four types of register updates. The register listing (Table 45 through Table 57) also contain a column with update type to identify when each register is updated:

- **SCK Updated**—Some registers are updated when the 28th data bit (D27) is written. These registers are used for functions, such as power-up and reset, that do not require gating with the next VD boundary.
- **VD Updated**—Many of the registers are updated at the next VD falling edge. By updating these values at the next VD edge, the current field is not corrupted, and the new register values are applied to the next field. The VD update can be further delayed, past the VD falling edge, by using the UPDATE register (Address 0x18). This delays the VD-updated register updates to any desired HD line in the field. Note that the field registers are not affected by the UPDATE register.
- **SG Updated**—A few shutter registers are updated at the HD falling edge at the end of an SG active line. These registers control the SUBCK signal; therefore, the SUBCK output is not updated until the SG line is complete.
- **SCP Updated**—All V-pattern and V-sequence registers are updated at the next SCP where they will be used. For example, in Figure 86, this field has selected Region 1 to use V-Sequence 3 for the vertical outputs; therefore, a write to a V-Sequence 3 or V-pattern group register, which is referenced by V-Sequence 3, is updated at SCP 1. If there are multiple writes to the same register, only the last one before SCP1 is updated. Likewise, a register write to a V-Sequence 5 register is updated at SCP 2, and a register write to a V-Sequence 8 register is updated at SCP 3.

Table 44. Register Update Locations

Update Type	Description
SCK	Register is immediately updated when the 28th data bit (D27) is written.
VD	Register is updated at the VD falling edge. VD-updated registers can be delayed further by using the UPDATE register at Address 0x18. Field registers are not affected by the UPDATE register.
SG	Register is updated at the HD falling edge at the end of the SG-active line.
SCP	Register is updated at the next SCP when the register is used.

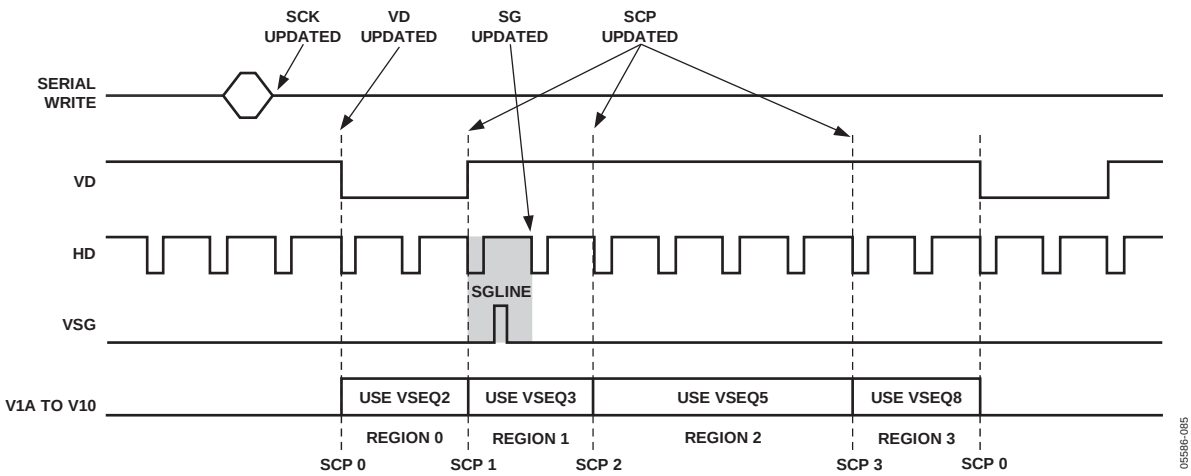

Figure 86. Register Update Locations (See Table 44 for Definitions)

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COMPLETE REGISTER LISTING

When an address contains less than 28 data bits, all remaining bits must be written as 0s.

Table 45. AFE Registers

Address	Data Bits	Default Value	Update Type	Name	Description
00	[1:0]	3	SCK	STANDBY	Standby modes. 0: normal operation. 1: Standby 1 mode. 2: Standby 2 mode. 3: Standby 3 mode.
	[2]	1		CLPENABLE	0: disable OB clamp. 1: enable OB clamp.
	[3]	0		CLPSPEED	0: select normal OB clamp settling. 1: select fast OB clamp settling.
	[4]	0		FASTUPDATE	0: ignore VGA update. 1: very fast clamping when VGA is updated.
	[5]	0		PBLK_LVL	0: blank data outputs to 0 during PBLK. 1: blank data outputs to programmed clamp level during PBLK.
	[6]	0		DCBYP	0: enable input dc-restore circuit during PBLK. 1: disable input dc-restore circuit during PBLK.
	[14:11]	0		XSUBCNT_MUX	Selects which internal signal is used for the XSUBCNT signal. 0: assign XV6 to XSUBCNT. 1: assign XV8 to XSUBCNT. 2: assign XV9 to XSUBCNT. 3: assign XV10 to XSUBCNT. 4: assign VSG5 to XSUBCNT. 5: assign VSG6 to XSUBCNT. 6: assign VSG7 to XSUBCNT. 7: assign VSG8 to XSUBCNT. 8: assign VSG2 to XSUBCNT. 9: assign VSG3 to XSUBCNT. 10: assign VSG4 to XSUBCNT. 11: assign VSG1 to XSUBCNT. 12: assign XV13 to XSUBCNT. 13: assign VSUB to XSUBCNT. 14: assign MSHUT to XSUBCNT. 15: assign STROBE to XSUBCNT.
01	[0]	0	SCK	DOUTDISABLE	0: data outputs are driven. 1: data outputs are three-stated.
	[1]	0		DOUTLATCH	0: latch data outputs using DOUT PHASE register setting. 1: output latch is transparent.
	[2]	0		TEST	Set to 0.
	[3]	1		TEST	Set to 1.
04	[1:0]	1	VD	CDSGAIN	CDS gain setting. 0: −3 dB. 1: 0 dB. 2: +3 dB. 3: +6 dB.
05	[9:0]	F	VD	VGAGAIN	VGA gain. 6 dB to 42 dB. (0.035 dB per step).
06	[9:0]	1EC	VD	CLAMPLEVEL	Optical black clamp level. 0 LSB to 256 LSB. (0.25 LSB per step.)

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Table 46. Miscellaneous Registers

Address	Data Bits	Default Value	Update Type	Name	Description
10	[0]	0	SCK	SW_RST	Software reset. Bit resets to 0. 1: reset Register 0x00 to Register 0x91 to default values.
11	[0]	0	VD	OUTCONTROL	0: make all outputs dc inactive. 1: enable outputs at next VD edge.
12	[0] [7:1] [9:8]	1 0 0	SCK	SYNCENABLE TEST OUTPUTPBLK	0: configure Ball G7 as an output signal, determined by Register 0x12, Bits[9:8]. 1: external synchronization enable (configure Ball G7 as SYNC input). Test mode only. Must be set to 0. When SYNCENABLE = 0, selects which signal is output on the SYNC pin. 0: CLPOB. 1: PBLK. 2: GPO (from Register 0x1A). 3: TESTOUT (from shutter registers).
13	[0]	0	SCK	SYNCPOL	SYNC active polarity. 0: active low. 1: active high.
14	[0]	0	SCK	SYNCSUSPEND	Suspends clocks during SYNC active pulse. 0: don't suspend. 1: suspend.
15	[0]	0	SCK	TGCORE_RSTB	Timing core reset bar. 0: reset TG core. 1: resume operation.
16	[0]	0	SCK	OSC_RST	CLO oscillator reset. 0: oscillator in power-down state. 1: resume oscillator operation.
17	[7:0] [8]	0 0	SCK	TEST1 TEST2	Test mode only. Must be set to 0. Test mode only. Must be set to 0.
18	[11:0]	0	VD	UPDATE	Serial update line. Sets the HD line within the field to update the VD-updated registers.
19	[0]	0	SCK	PREVENTUP	Prevents the updating of the VD-updated registers. 0: normal update. 1: prevent update of VD-updated registers.
1A	[0]	0	VD	GPO	General-purpose output (GPO) value when SYNCENABLE = 0 and OUTPUTPBLK = 2. 0: GPO is low at next VD edge. 1: GPO is high at next VD edge.

Table 47. VD/HD Registers

Address	Data Bits	Default Value	Update Type	Name	Description
20	[0]	0	SCK	MASTER	VD/HD master or slave mode. 0: slave mode. 1: master mode.
21	[0]	0	SCK	VDHDPOL	VD/HD active polarity. 0 = low. 1 = high.
22	[12:0] [24:13]	0 0	VD	HDRISE VDRISE	Rising edge location for HD. Rising edge location for VD.

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Table 48. Timing Core Registers

Address	Data Bits	Default Value	Update Type	Name	Description
30	[0]	0	SCK	CLIDIVIDE	Divide CLI input frequency by 2. 0: no divide. 1: divide by 2.
31	[5:0] [13:8] [16]	0 20 1	SCK	H1POSLOC H1NEGLOC H1H2POL	H1 rising edge location. H1 falling edge location. H1/H2 polarity control. 0: inverse of convention in Figure 18. 1: no inversion.
32	[5:0] [13:8] [16]	0 20 1	SCK	H3POSLOC H3NEGLOC H3H4POL	H3 rising edge location. H3 falling edge location. H3/H4 polarity control. 0: inverse of convention in Figure 18. 1: no inversion.
33	[5:0] [13:8] [16]	0 20 1	SCK	HLPOSLOC HLNEGLOC HLPOL	HL rising edge location. HL falling edge location. HL polarity control. 0: inverse of convention in Figure 18. 1: no inversion.
34	[5:0] [13:8] [16]	0 10 1	SCK	RGPOSLOC RGNEGLOC RGPOL	RG rising edge location. RG falling edge location. RG polarity control. 0: inverse of convention in Figure 18. 1: no inversion.
35	[0] [1] [2] [3] [6:4]	0 0 0 0 0	SCK	H1H2RETIME H3H4RETIME HLRETIME HLHBLKEN HBLKWIDTH	Retime HBLK for H1/H2 to the internal H1 clock. The preferred setting is 1, which adds one cycle of delay to the HBLK toggle positions. 0: no retime. 1: retime. Retime HBLK for H3/H4 to the internal H3 clock. Retime HBLK for HL to the internal HL clock. Enable HBLK for HL output. 0: disable. 1: enable. Controls H1 to H4 width during HBLK as a fraction of pixel rate. 0: same frequency as pixel rate. 1: 1/2 pixel frequency, that is, it doubles the H1 to H4 pulse width. 2: 1/4 pixel frequency. 3: 1/6 pixel frequency. 4: 1/8 pixel frequency. 5: 1/10 pixel frequency. 6: 1/12 pixel frequency. 7: 1/14 pixel frequency.
36	[3:0]	1	SCK	H1DRV	H1 drive strength. 0: off. 1: 4.3 mA. 2: 8.6 mA. 3: 12.9 mA. 4: 17.2 mA. 5: 21.5 mA. 6: 25.8 mA. 7: 30.1 mA.

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Address	Data Bits	Default Value	Update Type	Name	Description
	[7:4]	1		H2DRV	H2 drive strength.
	[11:8]	1		H3DRV	H3 drive strength.
	[15:12]	1		H4DRV	H4 drive strength.
	[19:16]	1		HLDRV	HL drive strength.
	[23:20]	1		RGDRV	RG drive strength.
37	[7:0]	24	SCK	SHPLOC	SHP sample location.
	[15:8]	0		SHDLOC	SHD sample location.
38	[5:0]	0	SCK	DOUTPHASE	DOUT phase control.
	[7:6]	0		Unused	Must be set to 0.
	[8]	0		DCLKMODE	DCLK mode. 0: DCLK tracks DOUT phase, 1: DCLK phase is fixed.
	[10:9]	2		DOUTDELAY	Data output delay (t_{OD}) with respect to DCLK rising edge. 0: no delay. 1: ~4 ns. 2: ~8 ns. 3: ~12 ns.
	[11]	0		DCLKINV	Invert DCLK output. 0: no inversion. 1: inversion of DCLK.

Table 49. CLPOB and PBLK Masking Registers

Address	Data Bits	Default Value	Update	Name	Description
40	[11:0]	FFF	VD	CLPOBMASKSTART1	CLPOB Masking Start Line 1.
	[12]	0		Unused	Must be set to 0.
	[24:13]	FFF		CLPOBMASKEND1	CLPOB Masking End Line 1.
41	[11:0]	FFF	VD	CLPOBMASKSTART2	CLPOB Masking Start Line 2.
	[12]	0		Unused	Must be set to 0.
	[24:13]	FFF		CLPOBMASKEND2	CLPOB Masking End Line 2.
42	[11:0]	FFF	VD	CLPOBMASKSTART3	CLPOB Masking Start Line 3.
	[12]	0		Unused	Must be set to 0.
	[24:13]	FFF		CLPOBMASKEND3	CLPOB Masking End Line 3.
43	[11:0]	FFF	VD	PBLKMASKSTART1	PBLK Masking Start Line 1.
	[12]	0		Unused	Must be set to 0.
	[24:13	FFF		PBLKMASKEND1	PBLK Masking End Line 1.
44	[11:0]	FFF	VD	PBLKMASKSTART12	PBLK Masking Start Line 2.
	[12]	0		Unused	Must be set to 0.
	[24:13]	FFF		PBLKMASKEND2	PBLK Masking End Line 2.
45	[11:0]	FFF	VD	PBLKMASKSTART3	PBLK Masking Start Line 3.
	[12]	0		Unused	Must be set to 0.
	[24:13]	FFF		PBLKMASKEND3	PBLK Masking End Line 3.

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Table 50. SG Pattern Registers

Address	Data Bits	Default Value	Update Type	Name	Description
50	[0]	1	VD	SGPOL_0	Start polarity for SGPattern 0. 0: low, 1: high.
	[1]	1		SGPOL_1	Start polarity for SGPattern 1.
	[2]	1		SGPOL_2	Start polarity for SGPattern 2.
	[3]	1		SGPOL_3	Start polarity for SGPattern 3.
	[4]	1		SGPOL_4	Start polarity for SGPattern 4.
	[5]	1		SGPOL_5	Start polarity for SGPattern 5.
	[6]	1		SGPOL_6	Start polarity for SGPattern 6.
	[7]	1		SGPOL_7	Start polarity for SGPattern 7.
51	[12:0]	1FFF	VD	SGTOG1_0	Pattern 0. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_0	Pattern 0. Toggle Position 2.
52	[12:0]	1FFF	VD	SGTOG1_1	Pattern 1. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_1	Pattern 1. Toggle Position 2.
53	[12:0]	1FFF	VD	SGTOG1_2	Pattern 2. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_2	Pattern 2. Toggle Position 2.
54	[12:0]	1FFF	VD	SGTOG1_3	Pattern 3. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_3	Pattern 3. Toggle Position 2.
55	[12:0]	1FFF	VD	SGTOG1_4	Pattern 4. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_4	Pattern 4. Toggle Position 2.
56	[12:0]	1FFF	VD	SGTOG1_5	Pattern 5. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_5	Pattern 5. Toggle Position 2.
57	[12:0]	1FFF	VD	SGTOG1_6	Pattern 6. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_6	Pattern 6. Toggle Position 2.
58	[12:0]	1FFF	VD	SGTOG1_7	Pattern 7. Toggle Position 1.
	[25:13]	1FFF		SGTOG2_7	Pattern 7. Toggle Position 2.
59	[7:0]	0	SCK	SGMASK_BYP	SGMASK override. These values override the VSG mask value located in the field registers.
	[8]	0	SCK	SGMASK_BYP_EN	SGMASK override enable. Must be set to 1 to enable override.

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Table 51. Shutter Control Registers

Address	Data Bits	Default Value	Update Type	Name	Description
60	[2:0]	0	VD	VSUB_CTRL	Selects which internal signal is used for the VSUB output pin. 0: use SHUT0 parameters (Registers 0x06D to 0x071). 1: use SHUT1 parameters (Registers 0x072 to 0x076). 2: use SHUT2 parameters (Registers 0x077 to 0x07B). 3: use SHUT3 parameters (Registers 0x07C to 0x080). 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output. See Register 0xEB, Bits [15,13:12] for VSUB0_MUX, VSUB1_MUX, and SHUT1_SHUT2_MUX.
	[5:3]	0		MHSUT_CTRL	Selects which internal signal is used for the MSHUT output pin. 0: use SHUT0 parameters. 1: use SHUT1 parameters. 2: use SHUT2 parameters. 3: use SHUT3 parameters. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output. See Register 0xEB, Bits [15,13:12] for VSUB0_MUX, VSUB1_MUX, and SHUT1_SHUT2_MUX.
	[8:6]	0		STROBE_CTRL	Selects which internal signal is used for the STROBE output pin. 0: use SHUT0 parameters. 1: use SHUT1 parameters. 2: use SHUT2 parameters. 3: use SHUT3 parameters. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output. See Register 0xEB, Bits [15,13:12] for VSUB0_MUX, VSUB1_MUX, and SHUT1_SHUT2_MUX.
	[11:9]	0		TESTO_CTRL	Selects which internal signal is used for the TESTO signal. 0: use SHUT0 parameters. 1: use SHUT1 parameters. 2: use SHUT2 parameters. 3: use SHUT3 parameters. 4: use VSUB0_MUX output. 5: use VSUB1_MUX output. 6: invalid setting. 7: use SHUT1_SHUT2_MUX output. See Register 0xEB, Bits [15,13:12] for VSUB0_MUX, VSUB1_MUX, and SHUT1_SHUT2_MUX.
61	[7:0]	0	VD	TRIGGER	Trigger for exposure/readout operation. Set bits high to trigger. [0]: SHUT0, SHUT1, SHUT2, and SHUT3. [1]: SHUT1. [2]: SHUT2. [3]: SHUT3. [4]: VSUB0. [5]: VSUB1. [6]: EXPOSURE.

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Address	Data Bits	Default Value	Update Type	Name	Description
					[7]: READOUT Note that if EXPOSURE and READOUT are triggered together, READOUT occurs immediately after the exposure is complete.
62	[2:0]	2	VD	READOUTNUM	Number of fields to suppress the SUBCK pulses during READOUT.
63	[11:0] [12]	0 0	VD	EXPOSURENUM VDHDOFF	Number of fields to suppress the SUBCK and VSG pulses during exposure. Disable VD and HD during exposure. 0: enable. 1: disable.
64	[11:0] [23:12]	0 0	SG	SUBSUPPRESS SUBCKNUM	Number of SUBCK pulses to suppress after VSG line. Number of SUBCK pulses per field.
65	[1:0]	0	SG	SUBCKMASK	Additional masking of SUBCK output 0: no mask. 1: begin mask on VD edge. 2: mask using internal SHUT3 signal. 3: same as 1 and 2 (1 has priority).
66	[0]	1	SG	SUBCKPOL	SUBCK pulse start polarity.
67	[12:0] [25:13]	1FFF 1FFF	SG	SUBCK1TOG1 SUBCK1TOG2	First SUBCK Pulse Toggle Position 1. First SUBCK Pulse Toggle Position 2.
68	[12:0] [25:13]	1FFF 1FFF	SG	SUBCK2TOG1 SUBCK2TOG2	Second SUBCK Pulse Toggle Position 1. Second SUBCK Pulse Toggle Position 2.
69	[0] [1]	0 0	VD	VSUB0_MODE VSUB0_KEEPON	VSUB0 readout mode. 0: Mode 0. 1: Mode 1. VSUB0 keep-on mode. 0: turn VUB0 off after READOUT or at next VD, 1: keep VSUB0 active beyond READOUT, until reset to 0.
6A	[11:0] [12] [13]	0 0 1	VD	VSUB0_ON Unused VSUB0POL	VSUB0 on position. Must be set to 0. VSUB0 start polarity.
6B	[0] [1]	0 0	VD	VSUB1_MODE VSUB1_KEEPON	VSUB1 readout mode. 0: Mode 0. 1: Mode 1. VSUB1 keep on mode. 1: keep VSUB1 active beyond readout.
6C	[11:0] [12] [13]	0 0 1	VD	VSUB1_ON Unused VSUB1POL	VSUB1 on position. Must be set to 0. VSUB1 start polarity.
6D	[0] [1] [2]	0 1 0	VD	SHUT0_ON SHUT0POL SHUT0_MAN	SHUT0 manual control of signal. 0: off. 1: on. SHUT0 active polarity. 1 = on state produces high output. SHUT0 manual control enable. 0: disable. 1: enable manual control.
6E	[11:0]	0	VD	SHUT0_ON_FD	SHUT0 field on position. Ignored during manual or nonshutter mode.
6F	[11:0] [12] [25:13]	0 0 0	VD VD	SHUT0_ON_LN Unused SHUT0_ON_PX	SHUT0 line on position. Must be set to 0. SHUT0 pixel on position.
70	[11:0]	0	VD	SHUT0_OFF_FD	SHUT0 field off position. Ignored during manual or nonshutter mode.

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Address	Data Bits	Default Value	Update Type	Name	Description
71	[11:0]	0	VD	SHUT0_OFF_LN	SHUT0 line off position.
	[12]	0		Unused	Must be set to 0.
	[25:13]	0	VD	HUT0_OFF_PX	SHUT0 pixel off position.
72	[0]	0	VD	SHUT1_ON	SHUT1 manual control of signal. 0: off. 1: on.
	[1]	1		SHUT1POL	SHUT1 active polarity. 1 = on state produces high output.
	[2]	0		SHUT1_MAN	SHUT1 manual control enable. 0: disable. 1: enable manual control.
73	[11:0]	0	VD	SHUT1_ON_FD	SHUT1 field on position. Ignored during manual or nonshutter mode.
74	[11:0]	0	VD	SHUT1_ON_LN	SHUT1 line on position.
	[12]	0		Unused	Must be set to 0.
	[25:13]	0	VD	SHUT1_ON_PX	SHUT1 pixel on position.
75	[11:0]	0	VD	SHUT1_OFF_FD	SHUT1 field off position. Ignored during manual or nonshutter mode.
76	[11:0]	0	VD	SHUT1_OFF_LN	SHUT1 line off position.
	[12]	0		Unused	Must be set to 0.
	[25:13]	0	VD	SHUT1_OFF_PX	SHUT1 pixel off position.
77	[0]	0	VD	SHUT2_ON	SHUT2 manual control of signal. 0: off. 1: on.
	[1]	1		SHUT2POL	SHUT2 active polarity. 1 = on state produces high output.
	[2]	0		SHUT2_MAN	SHUT2 manual control enable. 0: disable. 1: enable manual control.
78	[11:0]	0	VD	SHUT2_ON_FD	SHUT2 field on position. Ignored during manual or nonshutter mode.
79	[11:0]	0	VD	SHUT2_ON_LN	SHUT2 line on position.
	[12]	0		Unused	Must be set to 0.
	[25:3]	0	VD	SHUT2_ON_PX	SHUT2 pixel on position.
7A	[11:0]	0	VD	SHUT2_OFF_FD	SHUT2 field off position. Ignored during manual or nonshutter mode.
7B	[11:0]	0	VD	SHUT2_OFF_LN	SHUT2 line off position.
	[12]	0		Unused	Must be set to 0.
	[25:13]	0	VD	SHUT2_OFF_PX	SHUT2 pixel off position.
7C	[0]	0	VD	SHUT3_ON	SHUT3 manual control of signal. 0: off. 1: on.
	[1]	1		SHUT3POL	SHUT3 active polarity. 1 = on state produces high output.
	[2]	0		SHUT3_MAN	SHUT3 manual control enable. 0: disable. 1: enable manual control.
7D	[11:0]	0	VD	SHUT3_ON_FD	SHUT3 field on position. Ignored during manual or nonshutter mode.
7E	[11:0]	0	VD	SHUT3_ON_LN	SHUT3 line on position.
	[12]	0		Unused	Must be set to 0.
	[25:13]	0	VD	SHUT3_ON_PX	SHUT3 pixel on position.
7F	[11:0]	0	VD	SHUT3_OFF_FD	SHUT3 field off position. Ignored during manual or nonshutter mode.
80	[11:0]	0	VD	SHUT3_OFF_LN	SHUT3 line off position.
	[12]	0		Unused	Must be set to 0.
	[25:13]	0	VD	SHUT3_OFF_PX	SHUT3 pixel off position.

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Address	Data Bits	Default Value	Update Type	Name	Description
81	0	0	VD	SLOW_SHUT_EN	Slow shutter mode enable bit. 1: enable. 0: disable.
	[12:1]	0	VD	SLOW_SHUT_FD	Field for which slow shutter mode is active.

Table 52. Memory Configuration Registers

Address	Data Bits	Default Value	Update	Name	Description
90	[4:0]	0	VD	VPAT_NUM	Total number of V-pattern groups.
91	[4:0]	0	VD	VSEQ_NUM	Total number of V-sequences.

Table 53. Memory Configuration Registers

Address	Data Bits	Default Value	Update	Name	Description
E2	[24:0]	0	SCK	STANDBY3POL	Programmable polarities for vertical and shutter outputs during Standby 3. [0] = XV1 polarity. [1] = XV2 polarity. [2] = XV3 polarity. [3] = XV4 polarity. [4] = XV5 polarity. [5] = XV6 polarity. [6] = XV7 polarity. [7] = XV8 polarity. [8] = XV9 polarity. [9] = XV10 polarity. [10] = XV11 polarity. [11] = XV12 polarity. [12] = XV13 polarity. [13] = VSG1 polarity. [14] = VSG2 polarity. [15] = VSG3 polarity. [16] = VSG4 polarity. [17] = VSG5 polarity. [18] = VSG6 polarity. [19] = VSG7 polarity. [20] = VSG8 polarity. [21] = XSUBCK polarity. [22] = VSUB polarity. Note: controls polarity for Standby 1, Standby 2, and Standby 3. [23] = MSHUT polarity. Note: controls polarity for Standby 1, Standby 2, and Standby 3. [24] = STROBE polarity. Note: controls polarity for Standby 1, Standby 2, and Standby 3.
EA	[4:0]	0	SCK	TEST3	Test register.
EB	[11:0]	300	SCK	TEST4	Test register.
	[12]	0	SCK	VSUB0_MUX	0: Use VSUB0, 1: Use SHUT0 ^ VSUB0.
	[13]	0	SCK	VSUB1_MUX	0: Use VSUB1, 1: Use SHUT0 ^ VSUB1.
	[14]	0	SCK	TEST5	Test register. Set to 0.
	[15]	0	SCK	SHUT1_SHUT2_MUX	0: Use SHUT0 ^ SHUT1, 1: Use SHUT0 ^ SHUT2.

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Address	Data Bits	Default Value	Update	Name	Description
F1	[3:0]	0	SCK	FG_TRIGEN	FG_TRIG operation enable and field count selection. [2:0] Selects field count for pulse (based on mode field counter). [3] = 1 to enable FG_TRIG signal output.
F3	[21:0]	3FE000	SCK	STANDBY12POL	Programmable polarities for V-outputs and XSUBCK during Standby 1 and Standby 2. [0] = XV1 polarity. [1] = XV2 polarity. [2] = XV3 polarity. [3] = XV4 polarity.
					[4] = XV5 polarity. [5] = XV6 polarity. [6] = XV7 polarity. [7] = XV8 polarity. [8] = XV9 polarity. [9] = XV10 polarity. [10] = XV11 polarity. [11] = XV12 polarity. [12] = XV13 polarity. [13] = VSG1 polarity. [14] = VSG2 polarity. [15] = VSG3 polarity. [16] = VSG4 polarity. [17] = VSG5 polarity. [18] = VSG6 polarity. [19] = VSG7 polarity. [20] = VSG8 polarity. [21] = XSUBCK polarity.

Table 54. Mode Register: VD Updated

Address	Data Bits	Default Value	Description
12b10_xx_xxxx_xxxx	[37:0]	0	A11, A10 set to 10, remaining A9 to A0 bits used for D37:D28.
(Set A11, A10 = 10)	[37:35]		Number of fields (maximum of seven).
	[34:30]		Selected field for Field 7.
	[29:25]		Selected field for Field 6.
	[27:20]		Selected field for Field 5.
	[19:15]		Selected field for Field 4.
	[14:10]		Selected field for Field 3.
	[9:5]		Selected field for Field 2.
	[4:0]		Selected field for Field 1.

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Unused XV-channels must have toggle positions programmed to maximum values. For example, if XV1 to XV8 are used, XV9 to XV12 must have all toggle positions set to maximum values. This prevents unpredictable behavior, because default values are unknown.

Table 55. V-Pattern Group 0 (VPAT0) Registers

Address	Data Bits	Default Value	Update Type	Name	Description
00	[12:0]	X	SCP	XV1TOG1	XV1 Toggle Position 1.
	[25:13]	X		XV1TOG2	XV1 Toggle Position 2.
01	[12:0]	X	SCP	XV1TOG3	XV1 Toggle Position 3.
	[25:13]	X		XV1TOG4	XV1 Toggle Position 4.
02	[12:0]	X	SCP	XV2TOG1	XV2 Toggle Position 1.
	[25:13]	X		XV2TOG2	XV2 Toggle Position 2.
03	[12:0]	X	SCP	XV2TOG3	XV2 Toggle Position 3.
	[25:13]	X		XV2TOG4	XV2 Toggle Position 4.
04	[12:0]	X	SCP	XV3TOG1	XV3 Toggle Position 1.
	[25:13]	X		XV3TOG2	XV3 Toggle Position 2.
05	[12:0]	X	SCP	XV3TOG3	XV3 Toggle Position 3.
	[25:13]	X		XV3TOG4	XV3 Toggle Position 4.
06	[12:0]	X	SCP	XV4TOG1	XV4 Toggle Position 1.
	[25:13]	X		XV4TOG2	XV4 Toggle Position 2.
07	[12:0]	X	SCP	XV4TOG3	XV4 Toggle Position 3.
	[25:13]	X		XV4TOG4	XV4 Toggle Position 4.
08	[12:0]	X	SCP	XV5TOG1	XV5 Toggle Position 1.
	[25:13]	X		XV5TOG2	XV5 Toggle Position 2.
09	[12:0]	X	SCP	XV5TOG3	XV5 Toggle Position 3.
	[25:13]	X		XV5TOG4	XV5 Toggle Position 4.
0A	[12:0]	X	SCP	XV6TOG1	XV6 Toggle Position 1.
	[25:13]	X		XV6TOG2	XV6 Toggle Position 2.
0B	[12:0]	X	SCP	XV6TOG3	XV6 Toggle Position 3.
	[25:13]	X		XV6TOG4	XV6 Toggle Position 4.
0C	[12:0]	X	SCP	XV7TOG1	XV7 Toggle Position 1.
	[25:13]	X		XV7TOG2	XV7 Toggle Position 2.
0D	[12:0]	X	SCP	XV7TOG3	XV7 Toggle Position 3.
	[25:13]	X		XV7TOG4	XV7 Toggle Position 4.
0E	[12:0]	X	SCP	XV8TOG1	XV8 Toggle Position 1.
	[25:13]	X		XV8TOG2	XV8 Toggle Position 2.
0F	[12:0]	X	SCP	XV8TOG3	XV8 Toggle Position 3.
	[25:13]	X		XV8TOG4	XV8 Toggle Position 4.
10	[12:0]	X	SCP	XV9TOG1	XV9 Toggle Position 1.
	[25:13]	X		XV9TOG2	XV9 Toggle Position 2.
11	[12:0]	X	SCP	XV9TOG3	XV9 Toggle Position 3.
	[25:13]	X		XV9TOG4	XV9 Toggle Position 4.
12	[12:0]	X	SCP	XV10TOG1	XV10 Toggle Position 1.
	[25:13]	X		XV10TOG2	XV10 Toggle Position 2.
13	[12:0]	X	SCP	XV10TOG3	XV10 Toggle Position 3.
	[25:13]	X		XV10TOG4	XV10 Toggle Position 4.
14	[12:0]	X	SCP	XV11TOG1	XV11 Toggle Position 1.
	[25:13]	X		XV11TOG2	XV11 Toggle Position 2.
15	[12:0]	X	SCP	XV11TOG3	XV11 Toggle Position 3.
	[25:13]	X		XV11TOG4	XV11 Toggle Position 4.
16	[12:0]	X	SCP	XV12TOG1	XV12 Toggle Position 1.
	[25:13]	X		XV12TOG2	XV12 Toggle Position 2.
17	[12:0]	X	SCP	XV12TOG3	XV12 Toggle Position 3.
	[25:13]	X		XV12TOG4	XV12 Toggle Position 4.

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Address	Data Bits	Default Value	Update Type	Name	Description
18	[12:0]	X	SCP	XV1TOG5	XV1 Toggle Position 5.
	[25:13]	X		XV1TOG6	XV1 Toggle Position 6.
19	[12:0]	X	SCP	XV2TOG5	XV2 Toggle Position 5.
	[25:13]	X		XV2TOG6	XV2 Toggle Position 6.
1A	[12:0]	X	SCP	XV3TOG5	XV3 Toggle Position 5.
	[25:13]	X		XV3TOG6	XV3 Toggle Position 6.
1B	[12:0]	X	SCP	XV4TOG5	XV4 Toggle Position 5.
	[25:13]	X	SCP	XV4TOG6	XV4 Toggle Position 6.
1C	[12:0]	X	SCP	XV5TOG5	XV5 Toggle Position 5.
	[25:13]	X		XV5TOG6	XV5 Toggle Position 6.
1D	[12:0]	X	SCP	XV6TOG5	XV6 Toggle Position 5.
	[25:13]	X		XV6TOG6	XV6 Toggle Position 6.
1E	[12:0]	X	SCP	XV7TOG5	XV7 Toggle Position 5.
	[25:13]	X		XV7TOG6	XV7 Toggle Position 6.
1F	[12:0]	X	SCP	XV8TOG5	XV8 Toggle Position 5.
	[25:13]	X		XV8TOG6	XV8 Toggle Position 6.
20	[12:0]	X	SCP	XV9TOG5	XV9 Toggle Position 5.
	[25:13]	X		XV9TOG6	XV9 Toggle Position 6.
21	[12:0]	X	SCP	XV10TOG5	XV10 Toggle Position 5.
	[25:13]	X		XV10TOG6	XV10 Toggle Position 6.
22	[12:0]	X	SCP	XV11TOG5	XV11 Toggle Position 5.
	[25:13]	X		XV11TOG6	XV11 Toggle Position 6.
23	[12:0]	X	SCP	XV12TOG5	XV12 Toggle Position 5.
	[25:13]	X		XV12TOG6	XV12 Toggle Position 6.
24	[12:0]	X	SCP	XV13TOG1	XV13 Toggle Position 1.
	[25:13]	X		XV13TOG2	XV13 Toggle Position 2.
25	[12:0]	X	SCP	XV13TOG3	XV13 Toggle Position 3.
	[25:13]	X		XV13TOG4	XV13 Toggle Position 4.
26	[12:0]	X	SCP	XV13TOG5	XV13 Toggle Position 5.
	[25:13]	X		XV13TOG6	XV13 Toggle Position 6.
27	[25:0]	X	SCP	Unused	Must be set to 0.

Table 56. V-Sequence Registers

Address	Data Bits	Default Value	Update Type	Name	Description
00	[0]	X	SCP	CLPOBPOL	CLPOB start polarity.
	[1]	X		PBLKPOL	PBLK start polarity.
	[2]	X		HOLD	HOLD function.
	[4:3]	X		VMASK	Enable masking of V-outputs. 0: no mask. 1: enable Freeze1/Resume1. 2: enable Freeze2/Resume2. 3: enable both Freeze1/Resume1 and Freeze2/Resume2.
	[7:5]	X		HBLKALT	Enable HBLK alternation.
	[12:8]	X		Unused	Must be set to 0.
	[25:13]	X		HDLEN	HD line length (number of pixels in the line).
01	[0]	X	SCP	XV1POL	XV1 start polarity.
	[1]	X		XV2POL	XV2 start polarity.
	[2]	X		XV3POL	XV3 start polarity.
	[3]	X		XV4POL	XV4 start polarity.
	[4]	X		XV5POL	XV5 start polarity.

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Address	Data Bits	Default Value	Update Type	Name	Description
	[5]	X		XV6POL	XV6 start polarity.
	[6]	X		XV7POL	XV7 start polarity.
	[7]	X		XV8POL	XV8 start polarity.
	[8]	X		XV9POL	XV9 start polarity
	[9]	X		XV10POL	XV10 start polarity.
	[10]	X		XV11POL	XV11 start polarity
	[11]	X		XV12POL	XV12 start polarity.
	[12]	X		XV13POL	XV13 start polarity.
	[13]	X		XV1POL2	XV1 second polarity.
	[14]	X		XV2POL2	XV2 second polarity.
	[15]	X		XV3POL2	XV3 second polarity.
	[16]	X		XV4POL2	XV4 second polarity.
	[17]	X		XV5POL2	XV5 second polarity.
	[18]	X		XV6POL2	XV6 second polarity.
	[19]	X		XV7POL2	XV7 second polarity.
	[20]	X		XV8POL2	XV8 second polarity.
	[21]	X		XV9POL2	XV9 second polarity.
	[22]	X		XV10POL2	XV10 second polarity.
	[23]	X		XV11POL2	XV11 second polarity.
	[24]	X		XV12POL2	XV12 second polarity.
	[25]	X		XV13POL13	XV13 second polarity.
02	[12:0]	X	SCP	GROUPSEL	Select between Group A and Group B. 0: Group A, 1: Group B.
	[13]	X		TWO_GROUP	1: use all Group A and Group B toggle positions for single V-pattern.
	[18:14]	X		VPATSELB	Selected V-pattern Group B or Special V-pattern 2nd position.
	[23:19]	X		VPATSELA	Selected V-pattern Group A.
	[25:24]	X		VPATA_MODE	Number of alternation repeats. 0: disable alternation, use VREPA_1 for all lines. 1: 2-line alternation. 2: 3-line alternation. 3: 4-line alternation.
03	[12:0]	X	SCP	VSTARTB	Start position of selected V-pattern Group B, or start position of special V-pattern.
	[25:13]	X		VLENB	Length of selected V-pattern Group B.
04	[12:0]	X	SCP	VSTARTA	Start position of selected V-pattern Group A.
	[25:13]	X		VLENA	Length of selected V-pattern Group A.
05	[11:0]	X	SCP	VREPB_ODD	Number of repetitions for V-pattern Group B for odd lines.
	[12]	X		Unused	Must be set to 0.
	[24:13]	X		VREPB_EVEN	Number of repetitions for V-pattern Group B for even lines.
06	[11:0]	X	SCP	VREPA_1	Number of repetitions for V-pattern Group A for first lines.
	[12]	X		Unused	Must be set to 0.
	[24:13]	X		VREPA_2	Number of repetitions for V-pattern Group A for second lines.
07	[12:0]	X	SCP	VREPA_3	Number of repetitions for V-pattern Group A for third lines, or first HBLK toggle position for odd lines.
	[25:13]	X		VEPA_4	Number of repetitions for V-pattern Group A for fourth lines, or second HBLK toggle position for odd lines.
08	[12:0]	X	SCP	FREEZE1	Holds the XV1 to XV13 outputs at their current levels, or third HBLK toggle position for odd lines.
	[25:13]	X		RESUME1	Resumes the operation of XV1 to XV13 outputs to finish the pattern, or fourth HBLK toggle position for odd lines.
09	[12:0]	X	SCP	FREEZE2	Holds the XV1 to XV13 outputs at their current levels, or fifth HBLK toggle position for odd lines.

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Address	Data Bits	Default Value	Update Type	Name	Description
	[25:13]	X		RESUME2	Resumes the operation of XV1 to XV13 outputs to finish the pattern, or sixth HBLK toggle position for odd lines.
0A	[12:0]	X	SCP	HBLKTOGE1	First HBLK toggle position for even lines.
	[25:13]	X		HBLKTOGE2	Second HBLK toggle position for even lines.
0B	[12:0]	X	SCP	HBLKTOGE3	Third HBLK toggle position for even lines.
	25:13]	X		HBLKTOGE4	Fourth HBLK toggle position for even lines.
0C	[12:0]	X	SCP	HBLKSTART	Start location for HBLK in Alternation Mode 4 to Alternation Mode 7, or fifth HBLK toggle position for even lines.
	[25:13]	X		HBLKEND	End location for HBLK in Alternation Mode 4 to Alternation Mode 7, or sixth HBLK toggle position for even lines.
0D	[12:0]	X	SCP	HBLKLEN	HBLK length in HBLK Alternation Mode 4 to Alternation Mode 7.
	[20:13]	X		HBLKREP	Number of HBLK repetitions in HBLK Alternation Mode 4 to Alternation Mode 7.
	[21]	X		HBLKMASK_H1	Masking polarity for H1 during HBLK.
	[22]	X		HBLKMASK_H3	Masking polarity for H3 during HBLK.
	[23]	X		HBLKMASK_HL	Masking polarity for HL during HBLK.
0E	[12:0]	X	SCP	CLPOBTOG1	CLPOB Toggle Position 1.
	[125:13]	X		CLPOBTOG2	CLPOB Toggle Position 2.
0F	[12:0]	X	SCP	PBLKTOG1	PBLK Toggle Position 1.
	[25:13]	X		PBLKTOG2	PBLK Toggle Position 2.
10	[25:0]	X	SCP	UNUSED	Must be set to 0.
11	[11:0]	X	SCP	SPXV_ACT	Special XV pattern active line.
	[12]	X		UNUSED	Must be set to 0.
	[13]	X		SPXV_EN	Special XV pattern enable (active HI).
12	[25:0]	X	SCP	UNUSED	Must be set to 0.
13	[25:0]	X	SCP	UNUSED	Must be set to 0.

Table 57: Field Registers

Address	Data Bits	Default Value	Update Type	Name	Description
00	[4:0]	X	VD	SEQ0	Selected V-sequence for first region in the field.
	[9:5]	X		SEQ1	Selected V-sequence for second region in the field.
	[14:10]	X		SEQ2	Selected V-sequence for third region in the field .
	[19:15]	X		SEQ3	Selected V-sequence for fourth region in the field.
	[24:20]	X		SEQ4	Selected V-sequence for fifth region in the field.
01	[4:0]	X	VD	SEQ5	Selected V-sequence for sixth region in the field.
	[9:5]	X		SEQ6	Selected V-sequence for seventh region in the field.
	[14:10]	X		SEQ7	Selected V-sequence for eighth region in the field.
	[19:15]	X		SEQ8	Selected V-sequence for ninth region in the field.
02	[1:0]	X	VD	MULT_SWEEP0	Enables multiplier mode and/or sweep mode for Region 0. 0: multiplier off/sweep off. 1: multiplier off/sweep on. 2: multiplier on/sweep off. 3: multiplier on/sweep on.
	[3:2]	X		MULT_SWEEP1	Enables multiplier mode and/or sweep mode for Region 1.
	[5:4]	X		MULT_SWEEP2	Enables multiplier mode and/or sweep mode for Region 2.
	[7:6]	X		MULT_SWEEP3	Enables multiplier mode and/or sweep mode for Region 3.
	[9:8]	X		MULT_SWEEP4	Enables multiplier mode and/or sweep mode for Region 4.
	[11:10]	X		MULT_SWEEP5	Enables multiplier mode and/or sweep mode for Region 5.
	[13:12]	X		MULT_SWEEP6	Enables multiplier mode and/or sweep mode for Region 6.
	[15:14]	XX		MULT_SWEEP7	Enables multiplier mode and/or sweep mode for Region 7.
	[17:16]	X		MULT_SWEEP8	Enables multiplier mode and/or sweep mode for Region 8.

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Address	Data Bits	Default Value	Update Type	Name	Description
03	[11:0]	X	VD	SCP0	V-Sequence Change Position 0.
	[12]	X		Unused	Must be set to 0.
	[24:13]	X		SCP1	V-Sequence Change Position 1.
04	[11:0]	X	VD	SCP2	V-Sequence Change Position 2.
	[24:13]	X		Unused	Must be set to 0.
	[24:13]	X		SCP3	V-Sequence Change Position 3.
05	[11:0]	X	VD	SCP4	V-Sequence Change Position 4.
	[12]	X		Unused	Must be set to 0.
	[24:13]	X		SCP5	V-Sequence Change Position 5.
06	[11:0]	X	VD	SCP6	V-Sequence Change Position 6.
	[12]	X		Unused	Must be set to 0.
	[24:13]	X		SCP7	V-Sequence Change Position 7.
07	[11:0]	X	VD	SCP8	V-Sequence Change Position 8.
	[12]]	X		Unused	Must be set to 0.
	[24:13]	X		VDLEN	VD field length (number of lines in the field).
08	[12:0]	X	VD	HDLAST	HD last line length. Line length of last line in the field.
	[25:13]	X		VSTARTSECOND	Start position for second V-pattern on SG active line.
09	[4:0]	X	VD	VPATSECOND	Selected second V-pattern group for SG active line.
	[20:5]	X		SGMASK	Masking of VSG outputs during SG active line.
0A	[23:0]	X	VD	SGPATSEL	Selection of VSG patterns for each VSG output.
0B	[11:0]	X	VD	SGACTLINE1	SG Active Line 1.
	[12]	X		Unused	Must be set to 0.
	[24:13]	X		SGACTLINE2	SG Active Line 2.

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OUTLINE DIMENSIONS

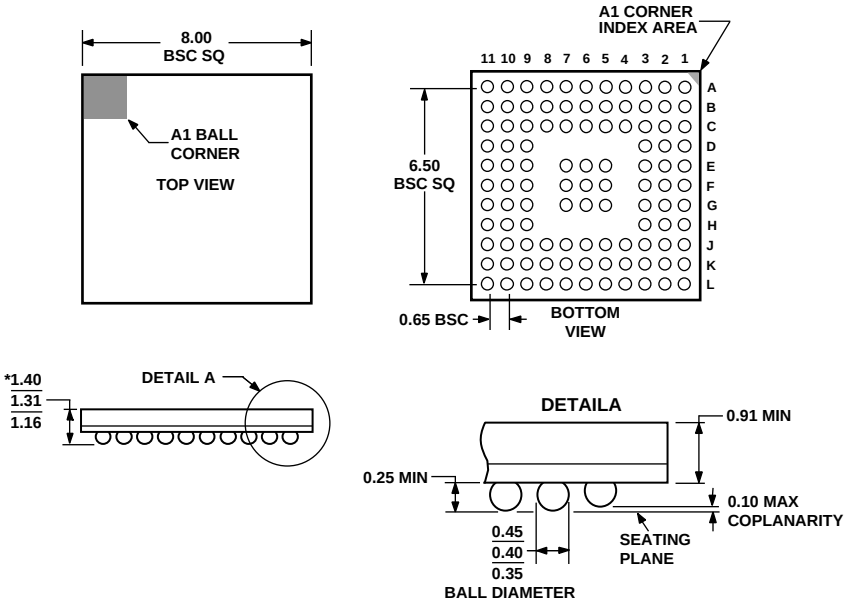

Figure 87. 105-Lead Chip Scale Package Ball Grid Array [CSP_BGA] (BC-105)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9923BBCZ	−25°C to + 85°C	105-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-105
AD9923BBCZRL	−25°C to + 85°C	105-Lead Chip Scale Package Ball Grid Array [CSP_BGA]	BC-105

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