SIEMENS

SIMATIC

S7-1200 G2 Programmable Logic Controller

System Manual

V1.0 01/2025
A5E52923928-AA

Legal information

Warning notice system

This manual contains notices you have to observe in order to ensure your personal safety, as well as to prevent damage to property. The notices referring to your personal safety are highlighted in the manual by a safety alert symbol, notices referring only to property damage have no safety alert symbol. These notices shown below are graded according to the degree of danger.

⚠ DANGER

indicates that death or severe personal injury **will** result if proper precautions are not taken.

⚠ WARNING

indicates that death or severe personal injury **may** result if proper precautions are not taken.

⚠ CAUTION

indicates that minor personal injury can result if proper precautions are not taken.

NOTICE

indicates that property damage can result if proper precautions are not taken.

If more than one degree of danger is present, the warning notice representing the highest degree of danger will be used. A notice warning of injury to persons with a safety alert symbol may also include a warning relating to property damage.

Qualified Personnel

The product/system described in this documentation may be operated only by **personnel qualified** for the specific task in accordance with the relevant documentation, in particular its warning notices and safety instructions. Qualified personnel are those who, based on their training and experience, are capable of identifying risks and avoiding potential hazards when working with these products/systems.

Proper use of Siemens products

Note the following:

⚠ WARNING

Siemens products may only be used for the applications described in the catalog and in the relevant technical documentation. If products and components from other manufacturers are used, these must be recommended or approved by Siemens. Proper transport, storage, installation, assembly, commissioning, operation and maintenance are required to ensure that the products operate safely and without any problems. The permissible ambient conditions must be complied with. The information in the relevant documentation must be observed.

Trademarks

All names identified by ® are registered trademarks of Siemens Aktiengesellschaft. The remaining trademarks in this publication may be trademarks whose use by third parties for their own purposes could violate the rights of the owner.

Disclaimer of Liability

We have reviewed the contents of this publication to ensure consistency with the hardware and software described. Since variance cannot be precluded entirely, we cannot guarantee full consistency. However, the information in this publication is reviewed regularly and any necessary corrections are included in subsequent editions.

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Introduction

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1.1 General information

Purpose of the documentation

The S7-1200 G2 programmable logic controllers (PLCs) can control a variety of automation applications. Compact design, affordable price, and a powerful instruction set make the S7-1200 G2 CPU and modules a perfect solution for controlling a wide variety of applications. Together with the STEP 7 configuration and programming tool (Page 51), you have the flexibility you need to design your automation solutions.

This documentation provides information about the S7-1200 G2 CPU and modules. It contains information for engineers, programmers, installers, and electricians.

Required basic knowledge

To understand this documentation, you need a general knowledge of automation and programmable logic controllers.

Validity of the documentation

This documentation applies to the S7-1200 G2 CPU family and G2 modules.

Refer to the technical specifications (Page 229) for each CPU and module in the S7-1200 G2 family.

Conventions

STEP 7: In this documentation, "STEP 7" is used as a synonym for all versions of the configuration and programming software "STEP 7 (TIA Portal)".

Also observe notes marked as follows:

NOTE

A note contains important information on the product described in the documentation, on the handling of the product, or on the section of the documentation to which particular attention should be paid.

ID link for the digital nameplate

The ID link is a globally unique identifier according to IEC 61406-1, which you will find as a QR code on your product.

The figure shows an example of an ID link for the CPU 1212C AC/DC/RLY.

You can recognize the ID link by the frame with a black frame corner at the bottom right. The ID link takes you to the digital nameplate of your product.

Scan the QR code on the product or on the packaging label with a smartphone camera, barcode scanner, or reader app. Access the ID link.

In the digital nameplate, you can find product data, manuals, declarations of conformity, certificates and other helpful information about your product.

Industry Mall

The Industry Mall is the catalog and order system of Siemens AG for automation and drive solutions on the basis of Totally Integrated Automation (TIA) and Totally Integrated Power (TIP).

You can find catalogs for all automation and drive products on the Internet (https://mall.industry.siemens.com).

Certifications and approvals

Refer to the technical specifications (Page 229) for details on certifications and approvals.

Glossary

The definitions in the glossary provide an easy first reference for understanding the terms in this documentation.

1.2 Maintaining operational safety of your plant

NOTE

Operators of plants with safety-related features must meet operational safety requirements. Suppliers must also take measures when monitoring products.

To stay up-to-date on the latest operational safety requirements, visit the Siemens Industry Online Support (https://support.industry.siemens.com/) site and subscribe to email notifications:

1. Follow one of the links below:
   - SIMATIC S7-1200 G2/SIMATIC S7-1200 G2 F (https://support.industry.siemens.com/cs/us/en/ps/30068)
   - Distributed I/O (https://support.industry.siemens.com/cs/ww/en/ps/14029)
   - STEP 7 TIA Portal (https://support.industry.siemens.com/cs/ww/en/ps/14667)
2. To subscribe to notifications, select "email on update".

NOTE

To reduce the risks associated with malicious or counterfeit CPUs and modules, use only official sales channels, such as the following:

- Siemens Industry Mall
- Official Siemens distributors
- Country-specific official Siemens sales and distribution channels

NOTE

To reduce the risks associated with compromised CPU or module firmware, only download firmware from the Siemens Industry Online Support website and verify the file integrity against the associated published SHA checksum.

NOTE

To reduce the risk of physical tampering with critical industrial equipment, implement the measures defined in the Operational guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html).

NOTE

For additional security, the CPU uses firmware encryption. While encryption provides confidentiality of the firmware, the main purpose is to enhance the secure boot process.

1.3 S7-1200 G2 documentation guide

S7-1200 G2 and the TIA Portal provide a variety of documentation and other resources for finding the technical information that you require.

- The S7-1200 G2 Programmable Logic Controller System Manual provides specific information about the operation, programming, and the specifications for the complete S7-1200 G2 product family.

  The system manual is available on Siemens Industry Online Support (https://support.industry.siemens.com/) in multiple display formats and languages.
- The TIA Portal Information System provides access to the conceptual information and specific instructions that describe the operation and functionality of the programming package and basic operation of SIMATIC CPUs.
- You can also follow or join product discussions on the Service & Support technical forum (https://support.industry.siemens.com/tf/ww/en/?Language=en&siteid=csius&treeLang=en&groupid=4000002&extranet=standard&viewreg=WW&nodeid0=34612486). These forums allow you to interact with various product experts.
  - Forum for S7-1200 G2 (https://support.industry.siemens.com/tf/ww/en/threads/237?title=simatic-s7-1200&skip=0&take=10&orderBy=LastPostDate+desc)
  - Forum for TIA Portal (https://support.industry.siemens.com/tf/ww/en/threads/243?title=step-7-tia-portal&skip=0&take=10&orderBy=LastPostDate+desc)
- The SIMATIC Industrial Software SIMATIC Safety - Configuring and Programming Manual (http://support.automation.siemens.com/WW/view/en/54110126/0/en) provides information about configuring and programming fail-safe PLCs.

Contact your Siemens distributor or sales office for assistance in answering any technical questions, for training, or for ordering S7 products. Because sales representatives are technically trained and have knowledge about your operations, process and industry, as well as about the Siemens products that you are using, they can provide efficient answers to problems you might encounter.

System manual updates

When needed, changes and supplements to released system manuals are available in a system manual update document. These updates take precedence over the system manual. You can find the latest system manual updates on Siemens Industry Online Support (https://support.industry.siemens.com/)

1.4 SIMATIC Technical Documentation

Additional SIMATIC documents will complete your information. You can find these documents and their use at the following links and QR codes.

The Industry Online Support gives you the option to get information on all topics. Application examples support you in solving your automation tasks.

Overview of the SIMATIC Technical Documentation

Here you will find an overview of the SIMATIC documentation available in Siemens Industry Online Support:

Industry Online Support International (https://support.industry.siemens.com/cs/ww/en/view/109742705)

Watch this short video to find out where you can find the overview directly in Siemens Industry Online Support and how to use Siemens Industry Online Support on your mobile device:

Quick introduction to the technical documentation of automation products per video (https://support.industry.siemens.com/cs/us/en/view/109780491)

YouTube video: Siemens Automation Products - Technical Documentation at a Glance (https://youtu.be/TwLSxxRQQsA)

Retention of the documentation

Retain the documentation for later use.

For documentation provided in digital form:

1. Download the associated documentation after receiving your product and before initial installation/commissioning. Use the following download options:
   - Industry Online Support International: (https://support.industry.siemens.com)

     The article number is used to assign the documentation to the product. The article number is specified on the product and on the packaging label. Products with new, non-compatible functions are provided with a new article number and documentation.
   - ID link:

     Your product may have an ID link. The ID link is a QR code with a frame and a black frame corner at the bottom right. The ID link takes you to the digital nameplate of your product. Scan the QR code on the product or on the packaging label with a smartphone camera, barcode scanner, or reader app. Call up the ID link.
2. Retain this version of the documentation.

Updating the documentation

The documentation of the product is updated in digital form. In particular in the case of function extensions, the new performance features are provided in an updated version.

1. Download the current version as described above via the Industry Online Support or the ID link.
2. Also retain this version of the documentation.

mySupport

With "mySupport" you can get the most out of your Industry Online Support.

Registration	You must register once to use the full functionality of "mySupport". After registration, you can create filters, favorites and tabs in your personal workspace.
Support requests	Your data is already filled out in support requests, and you can get an overview of your current requests at any time.
Documentation	In the Documentation area you can build your personal library.
Favorites	You can use the "Add to mySupport favorites" to flag especially interesting or frequently needed content. Under "Favorites", you will find a list of your flagged entries.
Recently viewed articles	The most recently viewed pages in mySupport are available under "Recently viewed articles".
CAx data	The CAx data area gives you access to the latest product data for your CAx or CAe system. You configure your own download package with a few clicks: • Product images, 2D dimension drawings, 3D models, internal circuit diagrams, EPLAN macro files • Manuals, characteristics, operating manuals, certificates • Product master data

You can find "mySupport" on the Internet. (https://support.industry.siemens.com/My/ww/en)

Application examples

The application examples support you with various tools and examples for solving your automation tasks. Solutions are shown in interplay with multiple components in the system - separated from the focus on individual products.

You can find the application examples on the Internet.
(https://support.industry.siemens.com/cs/ww/en/ps/ae)

1.5 Tool Support

Tools

The tools described below support you in all steps: from planning, over commissioning, all the way to analysis of your system.

TIA Selection Tool

The TIA Selection Tool tool supports you in the selection, configuration, and ordering of devices for Totally Integrated Automation (TIA).

As successor of the SIMATIC Selection Tools , the TIA Selection Tool assembles the already known configurators for automation technology into a single tool.

With the TIA Selection Tool , you can generate a complete order list from your product selection or product configuration.

You can find the TIA Selection Tool on the Internet.
(https://support.industry.siemens.com/cs/us/en/view/109767888)

SINETPLAN

SINETPLAN, the Siemens Network Planner, supports you in planning automation systems and networks based on PROFINET. The tool facilitates professional and predictive dimensioning of your PROFINET installation as early as in the planning stage. In addition, SINETPLAN supports you during network optimization and helps you to exploit network resources optimally and to plan reserves. This helps to prevent problems in commissioning or failures during productive operation even in advance of a planned operation. This increases the availability of the production plant and helps improve operational safety.

The advantages at a glance

- Network optimization thanks to port-specific calculation of the network load
- Increased production availability thanks to online scan and verification of existing systems
- Transparency before commissioning through importing and simulation of existing STEP 7 projects
- Efficiency through securing existing investments in the long term and the optimal use of resources

You can find SINETPLAN on the Internet (https://new.siemens.com/global/en/products/automation/industrial-communication/profinet/sinetplan.html).

1.6 Cybersecurity information

Siemens provides products and solutions with industrial cybersecurity functions that support the secure operation of plants, systems, machines and networks.

In order to protect plants, systems, machines and networks against cyber threats, it is necessary to implement – and continuously maintain – a holistic, state-of-the-art industrial cybersecurity concept. Siemens' products and solutions constitute one element of such a concept.

Customers are responsible for preventing unauthorized access to their plants, systems, machines and networks. Such systems, machines and components should only be connected to an enterprise network or the internet if and to the extent such a connection is necessary and only when appropriate security measures (e.g. firewalls and/or network segmentation) are in place.

For additional information on industrial cybersecurity measures that may be implemented, please visit
https://www.siemens.com/cybersecurity-industry.

Siemens' products and solutions undergo continuous development to make them more secure. Siemens strongly recommends that product updates are applied as soon as they are available and that the latest product versions are used. Use of product versions that are no longer supported, and failure to apply the latest updates may increase customer's exposure to cyber threats.

To stay informed about product updates, subscribe to the Siemens Industrial Cybersecurity RSS Feed under
https://new.siemens.com/cert.

Product overview

2

2.1 Introducing the S7-1200 G2 PLC

The S7-1200 G2 PLC family is Generation 2 of the S7-1200 and offers a significantly narrower footprint than the first generation. The CPU and devices provide the flexibility and power to control a wide variety of automation applications. The configuration and programming software is STEP 7 within the TIA Portal framework. If you have used the STEP 7 configuration and programming software (Page 51) with other CPU families, take note of compatibility information (Page 121).

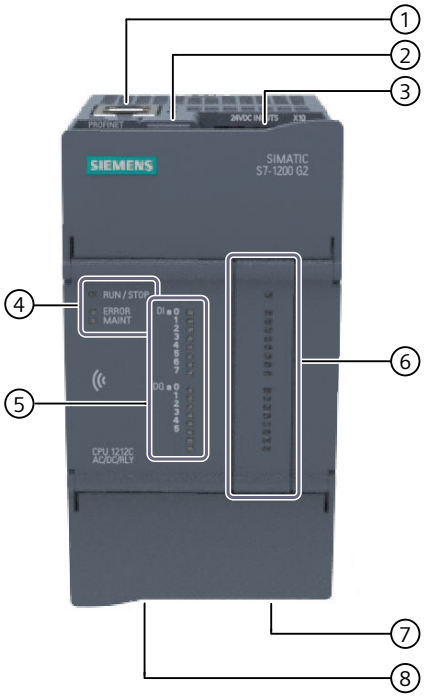
The CPU combines the following elements and more in a compact housing to create a powerful controller:

- A microprocessor
- An integrated power supply
- Input and output circuits
- Built-in PROFINET
- High-speed counters
- Standard and Advanced Motion Control

The S7-1200 G2 firmware adds new functionality and supports most of the previous S7-1200 functionality, with noted differences. (Page 20)

After you download your program, the CPU contains the logic required to monitor and control the devices in your application. The CPU monitors the inputs and changes the outputs according to the logic of your user program, which can include Boolean logic, counting, timing, complex math operations, motion control, and communications with other intelligent devices.

The CPU provides a built-in PROFINET interface with two ports for communication over a PROFINET network. You can connect additional Input, Output, and Communication modules (Page 19) to support larger automation applications.



① PROFINET interface with two ports (on the top of the CPU)
② Memory card slot (behind the door)
③ Removable input connector (behind the door)
④ Status LEDs for the CPU
⑤ Status LEDs for the on-board I/O
⑥ Optional plug-in expansion board
⑦ Removable output connector (behind the door, on the bottom of the CPU)
⑧ Power connector (behind the door, on the bottom of the CPU)

Several security features help protect access to both the CPU and the control program:

- Password protection that allows you to configure access to the CPU functions.
- "know-how protection" to hide the code within a specific block.
- Protection of confidential PLC configuration data
- Secure PG/PC and HMI communication
- Secure boot

You configure these security features in STEP 7. The TIA Portal Information System describes the types of security configurations.

For detailed information about a specific CPU or device, see the technical specifications (Page 229).

2.2 S7-1200 G2 modules and boards

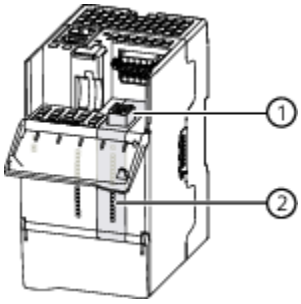
You can connect expansion boards and expansion modules to the CPU to increase its functionality. Four types are available: Communication boards (CBs), Signal boards (SBs), Communication modules (CMs), and Signal modules (SMs).

Communication boards (CBs) and Signal boards (SBs)

CBs and SBs are plug-in expansion boards. You can add CBs, such as the RS485, to increase the communication capability of a CPU. You can add SBs to increase the digital and analog I/O capability.

- The 1212 CPU supports one plug-in expansion board.
- The 1214 CPU supports two plug-in expansion boards.

In the following diagram, the plug-in expansion board is highlighted, and its key features are labeled:



① Removable communication port or I/O wiring connector

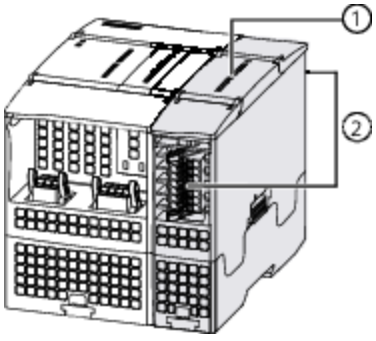
② Status LEDs

Communication modules (CMs)

CMs add communication options to the system, such as RS232/422/485 connectivity.

- CMs connect to the right side of a CPU or CM.
- All S7-1200 G2 CPUs support up to three CMs.

In the following diagram, the CM is highlighted, and its key features are labeled:



① Status LEDs

② Removable communication connector

Signal modules (SMs)

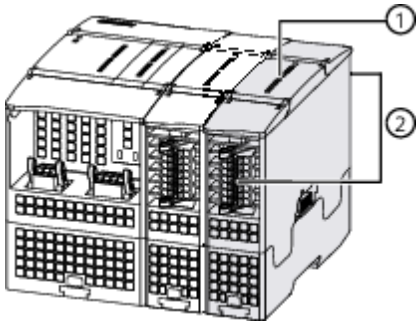
SMs add additional functionality to the system, such as digital and analog I/O capability. SMs connect to the right side of a CPU, CM, or SM.

- The 1212 CPU supports up to six expansion modules (CMs and SMs).
- The 1214 CPU supports up to ten expansion modules (CMs and SMs).

To determine the number of SMs you can use in a system, subtract the number of CMs from the maximum number of expansion modules supported.

For example, if you use three CMs with a 1212 CPU, you can use three SMs.

In the following diagram, the SM is highlighted, and its key features are labeled:



① Status LEDs
② Removable I/O wiring connector

2.3 Features

The S7-1200 G2 PLC (Page 17) provides the following features:

- Savings in Installation and wiring (Page 22) space
- Faster execution times
- Near field communication (NFC) (Page 188) application for mobile device access to the CPU
- Two expansion board slots (Page 19) for 1214 CPU models, one slot for 1212 CPU models
- Dual Ethernet ports for all CPU models
- Enhanced security
- 8 HSCs (High Speed Counters)
- 8 pulse generators for use as PTOs (Pulse Train Outputs) or for PWM (Pulse Width Modulation)
- Additional error OBs (Page 59)
- Standard motion control with advanced motion features (Page 197)
- Support for Real-Time PROFINET and Isochronous Real-Time PROFINET communication
- Support for Media Redundancy for Planned Duplication (MRPD) (Page 176) and Media Redundancy Protocol (MRP) (Page 176)
- Support for 31 PROFINET devices (Page 129)

- User-configurable alarms
- Web server (Page 195)
- Support for DHCP and DNS (Page 153)
- Work memory reporting as code work memory and data work memory
- Power budget calculation tool in TIA Portal
- 8MB of internal load memory
- 20KB of retentive memory
- System logging
- Support for users and roles
- SIMATIC Controller Profiling (https://support.industry.siemens.com/cs/ww/en/view/109750245)

Refer to the Technical Specifications (Page 229) for more information.

Differences from the S7-1200 family

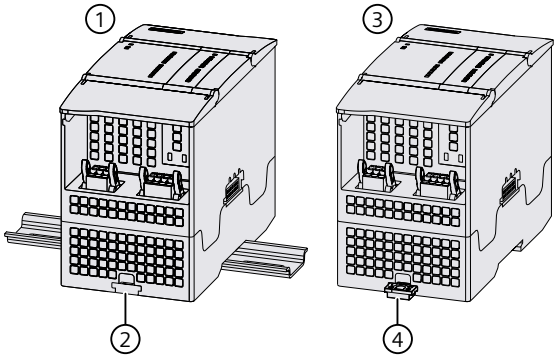
The S7-1200 G2 PLC (Page 17) provides features and differences from the S7-1200 PLC as described in Comparison to S7-1200 (Page 340).

Installation and wiring

3

3.1 Installation guidelines

You can install an S7-1200 G2 either on a standard DIN rail or on a panel, and you can orient the S7-1200 G2 either horizontally or vertically. The small size of the S7-1200 G2 allows you to make efficient use of space.



① DIN rail installation

② DIN rail clip in latched position

③ Panel installation

④ DIN rail clip in extended position for panel mounting

The S7-1200 G2 family provides a variety of expansion modules that you can use to increase the capabilities of the CPU with additional I/O or other communication protocols. For detailed information on a specific module, see the technical specifications (Page 229).

Electrical equipment standards classify the SIMATIC S7-1200 G2 system as Open Equipment. You must install the S7-1200 G2 in a housing, cabinet, or electric control room. Only allow authorized personnel access to the housing, cabinet, or electric control room.

Provide a dry environment for installation of the S7-1200 G2. SELV/PELV circuits provide protection against electric shock in dry locations.

Provide appropriate mechanical strength, flammability protection, and stability protection for open equipment in your location according to applicable electrical and building codes.

Conductive contamination due to dust, moisture, and airborne pollution can cause operational and electrical faults in the PLC.

If you locate the PLC in an area where conductive contamination might be present, protect the PLC in an enclosure with appropriate protection rating. IP54 is one rating for electronic equipment enclosures in dirty environments and might be appropriate for your application.

⚠ WARNING

Risks associated with improper installation

Improper installation of the S7-1200 G2 can result in electrical faults or unexpected operation of machinery.

You must follow all instructions for installation and maintenance of a proper operating environment to ensure that the equipment operates safely.

Electrical faults or unexpected machine operation can result in death, severe personal injury, and/or property damage.

Separating S7-1200 G2 devices from heat, high voltage, and electrical noise

When configuring the layout of S7-1200 G2 devices in a panel, always do the following:

- Separate the devices that generate high voltage and high electrical noise from the low-voltage, logic-type devices such as the S7-1200 G2.
- Place electronic-type devices in the cooler areas of the cabinet away from heat-generating devices to reduce exposure to high-temperatures and extend the operating life of the devices.
- Avoid placing low-voltage signal wires and communications cables in the same tray with AC power wiring and high-energy, rapidly-switched DC wiring when routing wiring for the devices.

Providing adequate clearance for cooling and wiring

The design of S7-1200 G2 devices provides for natural convection cooling. For proper cooling, allow at least 25 mm of clearance above, below, and on both sides of the system. Also, allow at least 25 mm of depth between the front of the modules and the inside of the enclosure.

⚠ CAUTION

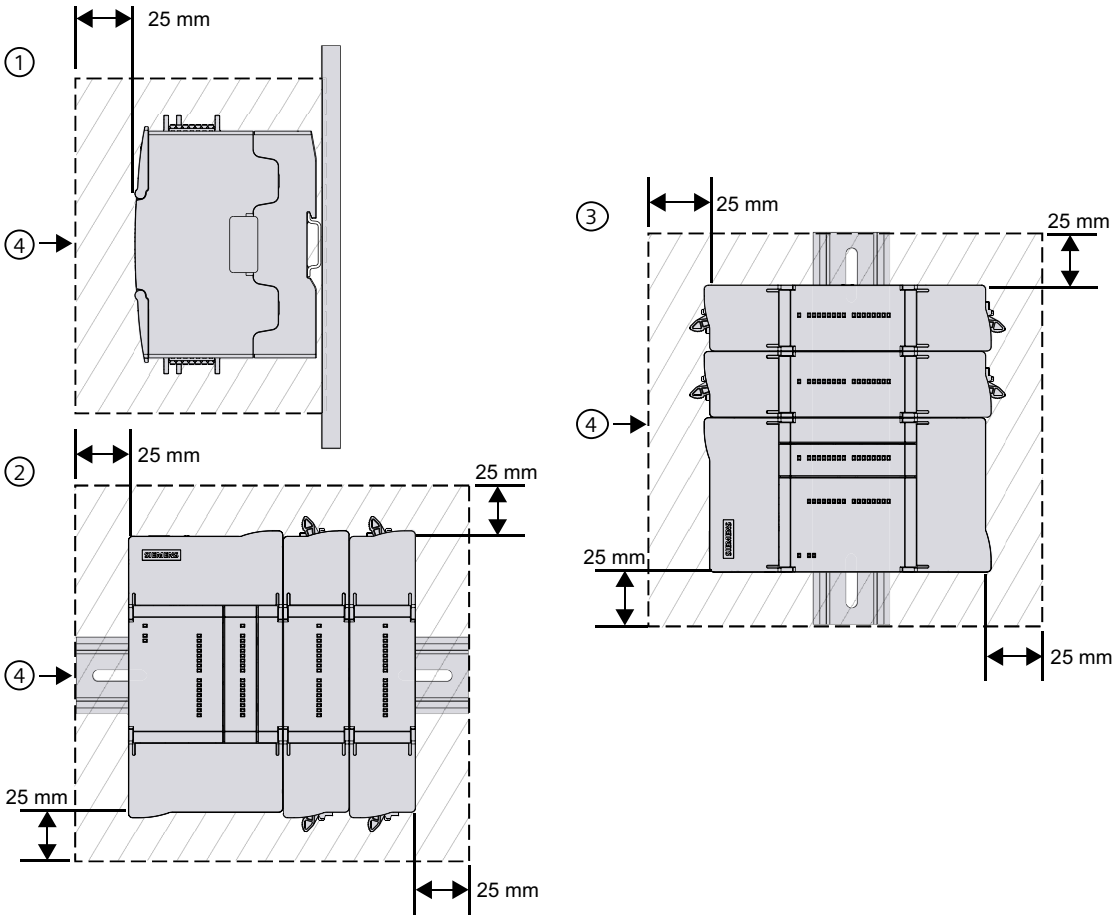
Effect of vertical mounting on allowable ambient temperature

Vertical mounting reduces the maximum allowable ambient temperature.

Orient a vertically mounted S7-1200 G2 system as shown in the following figure: the CPU, when vertically mounted, is at the bottom with its left side down. Ensure that the S7-1200 G2 system is mounted correctly.

Improper installation of a vertically mounted system can result in personal injury.

When planning your layout for the S7-1200 G2 system, allow enough clearance for the wiring and communications cable connections.



① Side view
② Horizontal installation
③ Vertical installation
④ Clearance area

3.2 Safety information

Before you install or remove any electrical device, ensure that the power to that equipment has been turned off. Also, ensure that the power to any related equipment has been turned off.

⚠ WARNING

Risk of electrocution when installing or removing devices

Installing or wiring the S7-1200 G2 or related equipment with power applied could cause electric shock or unexpected operation of equipment.

Always follow appropriate safety precautions and ensure that power is disabled to the S7-1200 G2 or related equipment before attempting to install or remove any devices.

Failure to disable all power to the S7-1200 G2 and related equipment during installation or removal procedures could result in death, severe personal injury, and/or property damage due to electric shock or unexpected equipment operation.

Always ensure that whenever you replace or install an S7-1200 G2 device you use the correct module or equivalent device.

Always be sure to follow the guidelines for grounding (Page 42).

⚠ WARNING

Risks associated with replacing S7-1200 G2 devices

Incorrect installation of an S7-1200 G2 module can cause the program in the S7-1200 G2 to function unpredictably.

Use the same model, orientation, and order when replacing an S7-1200 G2 device.

Failure to do so can cause unexpected equipment operation resulting in death, severe personal injury, and/or property damage.

⚠ WARNING

Installing or removing devices in a flammable or combustible atmosphere

Disconnecting equipment in a flammable or combustible atmosphere can cause a fire or an explosion.

Do not disconnect equipment in a flammable or combustible atmosphere; follow appropriate safety precautions when working in a flammable or combustible atmosphere.

A fire or explosion can result in death, serious injury, and/or property damage.

NOTICE

Risks associated with electrostatic discharge

Electrostatic discharge can damage the memory card or the receptacle on the CPU. If damaged, the receptacle or memory card can malfunction or become inoperable.

To protect the memory card and receptacle from electrostatic discharge, do the following:

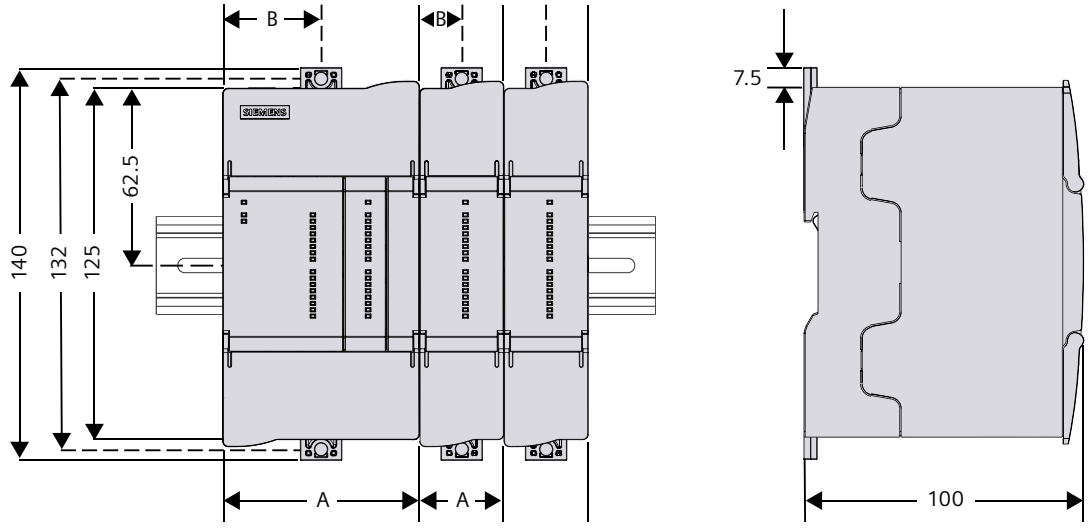
- Make contact with a grounded conductive pad or wear a grounded wrist strap when handling the memory card.
- Store the memory card in a conductive container.

Receptacle or memory card malfunction can result in property damage.

3.3 Mounting dimensions

Use the following mounting dimensions to ensure proper device installation. All mounting dimensions are shown in millimeters (mm).

CPU 1212C



CPU 1214C

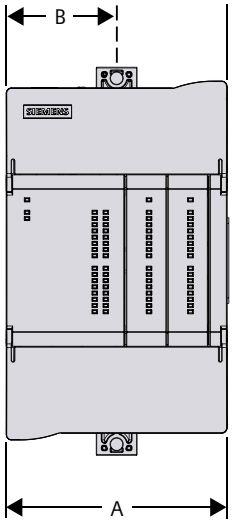


Table 3-1 Mounting dimensions (mm)

S7-1200 G2 Devices		**Width A (mm)**	**Width B (mm)**
CPU	CPU 1212C (AC/DC/Rly, DC/DC/Rly, and DC/DC/DC)	70	35
	CPU 1214C (AC/DC/Rly, DC/DC/Rly, and DC/DC/DC)	80	40
Fail-safe CPU	CPU 1212FC (DC/DC/Rly, and DC/DC/DC)	70	35
	CPU 1214FC (DC/DC/Rly, and DC/DC/DC)	80	40
Signal modules	SM 1221 (16 DI 24V)	30	15

S7-1200 G2 Devices		Width A (mm)	Width B (mm)
Signal modules	SM 1222 (16 DQ 24V and 16 Rly)	30	15
	SM 1223 (8 DI / 8 DQ and 8 DI / 8 Rly)	30	15
	SM 1231 (8 AI)	30	15
	SM1232 (8 AQ)	30	15
	SM 1233 (4 AI / 4 AQ)	30	15

Each CPU, SM, and CM supports mounting on either a DIN rail or on a panel. Use the DIN rail clips on the module to secure the device on the rail. These clips also snap into an extended position to provide screw mounting positions to mount the unit directly on a panel.

Always be sure to follow the guidelines for grounding (Page 42).

3.4 Providing power for the CPU

All S7-1200 G2 CPUs have an internal power supply that provides power to the CPU, any expansion modules or boards, and the 24 V DC Sensor power output.

You can connect any of the following to the CPU:

- Signal boards
- Communication modules
- Signal modules

Plug-in expansion boards, such as signal boards (SBs), install into the front of the CPU.

Communication modules (CM) and signal modules (SM) are installed to the right of the CPU. You can connect a CM to the right of a CPU or another CM. You can connect an SM to the right of a CPU, CM, or another SM.

The maximum number of expansion modules allowed for each CPU can be found in the Technical specifications (Page 229) under the CPU's General specifications and features.

For more information on expansion modules, see S7-1200 G2 modules (Page 19).

All S7-1200 G2 CPUs have a power budget calculator (Page 116) in the STEP 7 project. Select the CPU in Device view and navigate to the General tab > System power supply > Power segment overview to view the Power consumption per module and the Summary for the hardware configuration. When the chosen hardware configuration exceeds the available power budget, a compile warning is given.

Some of the 24 V DC power input ports in the PLC system are interconnected with a logic common circuit connecting multiple M terminals. The CPU 24 V DC power supply input, the SM relay coil power input, and a non-isolated analog power supply input are examples of circuits that are interconnected when designated as not isolated in the data sheets. All non-isolated M terminals must connect to the same external reference potential.

⚠ WARNING

Risks with connecting non-isolated M terminals to different reference potentials

Connecting non-isolated M terminals to different reference potentials causes unpredictable current flows. Unpredictable current flows can cause PLC damage or abnormal PLC and equipment operation.

Always ensure that all non-isolated M terminals in a PLC system are connected to the same reference potential.

PLC damage or abnormal PLC and equipment operation can cause death, severe personal injury, and/or property damage.

Each CPU supplies DC power:

- Each CPU has a 24 V DC sensor supply that can supply 24 V DC for local input points, for relay coils on the expansion modules, or for other requirements. If your 24 V DC power requirements exceed the budget of the sensor supply, you can add an external 24 V DC power supply to your system. You must manually connect the external 24 V DC supply to the input points or relay coils on the expansion modules.

⚠ WARNING

Risks with parallel connections

Connecting an external 24 V DC power supply in parallel with the CPU's DC sensor supply can result in a conflict between the two supplies as each seeks to establish its own preferred output voltage level.

When using the CPU's DC sensor supply in conjunction with an additional external 24 V DC power supply, they must not be wired in parallel.

Doing so could cause unpredictable operation of the PLC system, resulting in death, severe personal injury, and/or property damage.

Maximum applied voltage to S7-1200 G2 Fail-safe devices

When providing power for the S7-1200 G2 Fail-safe CPUs, you must observe the following:

- Operational voltage: The operational voltage of the fail-safe CPUs and fail-safe SMs is 20.4 V DC - 28.8 V DC. Design and testing assure operation of the unit to specifications. Defined transients from defined source impedances per EN 61000-4-2, 61000-4-4, and 61000-4-6, as specified in the data sheet for each product, can be imposed on this voltage without disrupting operation or causing damage. Sustained operation in the range of 28.8 - 35 V DC can result in unacceptable temperature rise and thermal damage, causing the product to become inoperable.
- Absolute maximum rating regarding supply voltage: The absolute maximum rating to prevent module damage and to ensure the functional safety of the modules is 35 V DC. The manufacturer must specify these power supplies to limit the output voltage to 35 V DC or less under fault conditions. Otherwise, you must supply external protection that reliably opens the circuit or limits the output voltage to less than 35 V DC to the fail-safe CPU and fail-safe SMs.

- Surge immunity (Page 229): Wiring systems subject to surges from lightning strike coupling must be equipped with external protection. This protection must be sufficient to clamp surge voltages and/or open the supply circuit to assure that the PLC system is not exposed to voltages greater than 35 V DC. You can find one specification for evaluation of protection from lightning type surges in EN 61000-4-5, with operational limits established by EN 61000-6-2. S7-1200 G2 DC Fail-safe CPUs and Fail-safe SMs require external protection to maintain safe operation when subject to surge voltages defined by this standard.

Requirements for power supplies in the event of voltage interruption

To ensure adherence to IEC 61131-2, only use power packs/power supply units with a main buffering time of at least 10 ms for DC power or 1/2 AC cycle. The port that powers the CPU meets IEC61131-2 rating of PS2 with an interruption time of 10 ms for DC power and 1/2 AC cycle for AC power. Observe the relevant requirement in your product standards (for example, 30 ms for Burner applications according to EN 298) regarding possible voltage interruptions. The latest information on PS components is available on the Internet (https://support.industry.siemens.com/).

⚠ WARNING

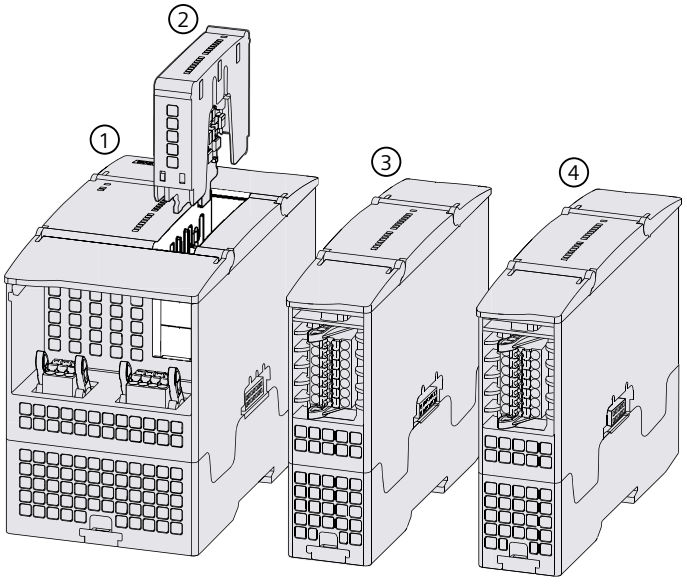
All power supply and fail-safe SM circuits must be connected together to a common voltage reference or must be isolated SELV circuits.

The power supply M terminals on the fail-safe CPU and the fail-safe SMs must be connected together or isolated as SELV. Failure to do so can result in unexpected machine or process operation.

Connecting all M terminals together or isolating with approved SELV isolation prevents unwanted current flows in the event of a single fault in the CPU to SM isolation boundary.

Unexpected machine or process operation can result in death or serious injury to personnel, and/or damage to equipment.

3.5 Expansion capability of the CPU



① Central processing unit (CPU)
② Expansion board
③ Communication module (CM), if used
④ Signal module (SM)

3.6 Installation and removal procedures

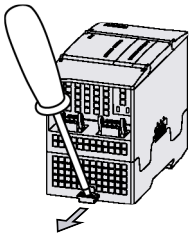
3.6.1 Installing and removing a CPU

You can install the S7-1200 G2 CPU on a DIN rail or a panel.

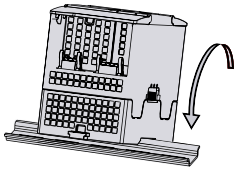
Installing the CPU on a DIN rail

To install the CPU on a DIN rail, follow these steps:

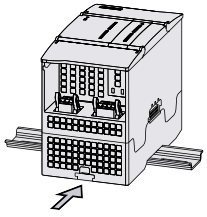
1. Install the DIN rail; secure the rail to the mounting panel every 75 mm.
2. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
3. Use an M3 screwdriver to extend the lower DIN rail clip on the CPU to allow it to fit over the rail.



4. Hook the CPU over the top of the DIN rail.
5. Rotate the CPU down into position on the rail.



6. Push in the lower DIN rail clip to secure it to the rail.



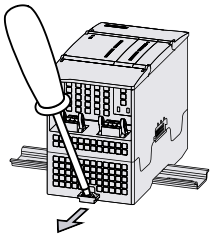
NOTE

Using DIN rail stops can be helpful if the CPU is in an environment with high vibration potential or if the CPU has been installed vertically. Use an end bracket (8WA1808 or 8WA1805) on the DIN rail to ensure that the modules remain connected.

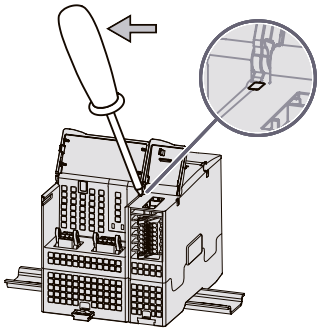
Removing the CPU from a DIN rail

To remove the CPU from a DIN rail, follow these steps:

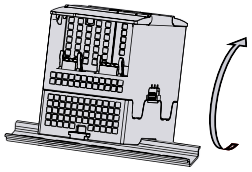
1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Disconnect the I/O connectors, wiring (Page 37), and cables from the CPU.
3. Use an M3 screwdriver to extend the lower DIN rail clip on the CPU to release it from the rail.



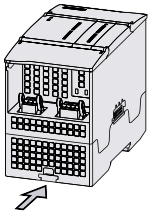
4. If the CPU is connected to an SM or CM, place an M3 screwdriver between the CPU and connected module; gently pry left to disconnect the CPU.



5. Rotate the CPU up and off the rail and remove the CPU from the system.



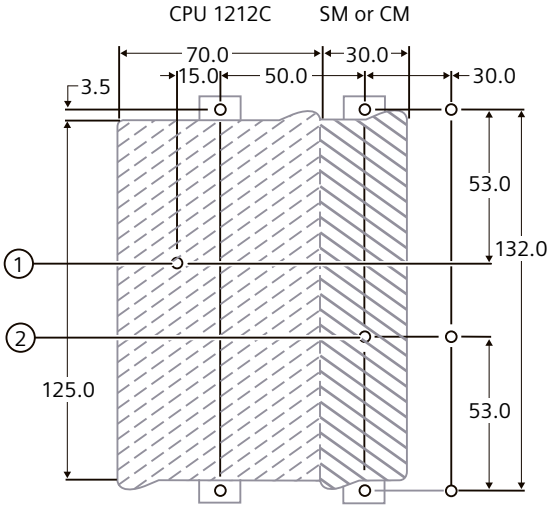
6. Push in the DIN rail clip to protect it from damage.

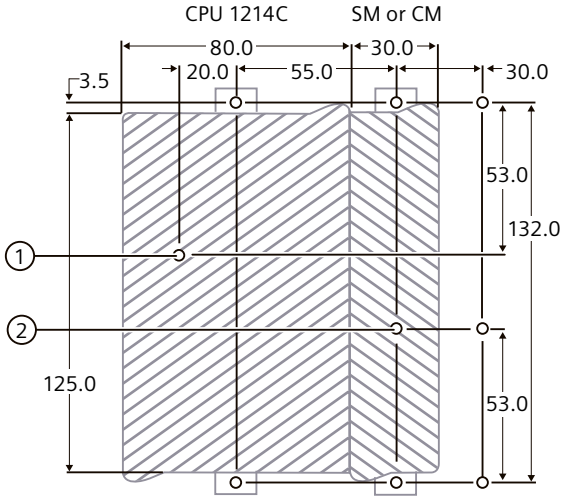


Installing the CPU on a panel

To install the CPU on a panel, follow these steps:

1. Locate, drill, and tap the mounting holes (M4), using the dimensions shown in the diagrams below.
2. Using the Guidelines for grounding (Page 42), install an M4 pan head stainless steel screw with a star washer into the panel at the grounding screw locations shown below.
3. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
4. Use a screwdriver to extend the upper and lower DIN rail clips on the CPU.
5. Secure the module to the panel, using a Pan Head M4 screw with spring and flat washer; apply the appropriate torque to compress the spring washer.





① CPU grounding screw

② SM or CM grounding screw

All measurements are shown in millimeters.

3.6.2 Installing and removing expansion modules

Installing and removing a CM or SM

You can connect a CM to a CPU or to another CM. Connect any CMs before installing any SMs. You can connect an SM to a CPU, CM, or SM.

Before you install or remove any electrical device, ensure that the power to that equipment has been turned off. Also, ensure that the power to any related equipment has been turned off.

⚠ WARNING

Installation or removal of S7-1200 G2 devices with power applied

Installation or removal of S7-1200 G2 or related equipment with the power applied can cause electric shock or unexpected operation of equipment.

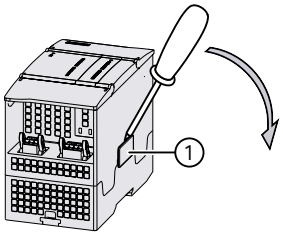
Always follow appropriate safety precautions and ensure that power to the S7-1200 G2 is disabled before attempting to install or remove S7-1200 G2 CPUs or related equipment.

Failure to disable all power to the S7-1200 G2 and related equipment during installation or removal procedures can result in death, severe personal injury and/or property damage due to electric shock or unexpected equipment operation.

Installing a CM or SM

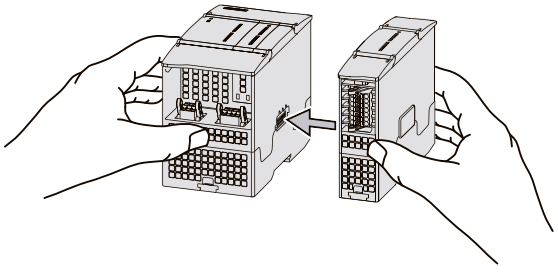
To install an CM or SM, follow these steps:

1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Remove the bus cover from the right side of the CPU or module. Insert a screwdriver into the slot above the bus cover, gently pry the cover loose, and remove it. Retain the cover for reuse.



① Bus cover

3. If you are installing the module on a DIN rail extend the lower DIN rail clip, hook the module over the top of the rail, and rotate the module down into place.
4. Align the bus connector and the posts of the module with the holes of the CPU or module, and firmly press the units together until the posts snap into place.



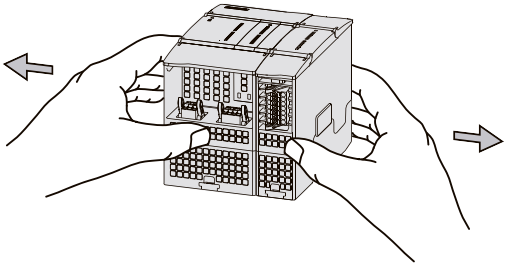
5. If you are DIN Rail mounting, push the lower DIN rail clip in to secure the module. If you are panel mounting, screw the module to the panel.

Removing a CM or SM

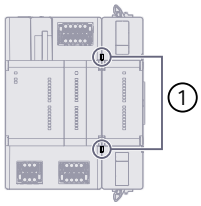
To remove an CM or SM, follow these steps:

1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Remove the I/O connectors and all wiring and cables from the module.
3. If the module is mounted on a DIN rail, use an M3 screwdriver to extend the lower DIN rail clip on the module. If the module is panel mounted, remove the mounting screws from the upper and lower DIN rail clips to release it from the panel.
   Note: In some cases, it may be necessary to loosen other devices mounted to the left or right to create room to disconnect the device you wish to remove.

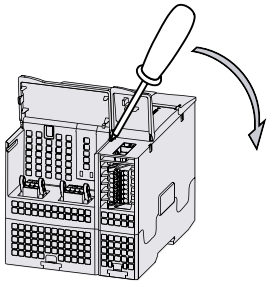
4. Separate the module from the CPU or module using one of the following methods:
   - Grasp the units and pull them apart.



   - Place an M3 screwdriver in the provided slot under the doors and pry the devices apart.



① Slots for screwdriver



5. Remove the module(s) from the DIN rail or panel; if removing a module(s) from a DIN rail, rotate it up and off the rail.
6. Push in the DIN rail clips on the modules you are removing to protect them from damage.

3.6.3 Installing and removing expansion boards

Installing or removing an SB

You can install one plug-in expansion board to CPU 1212 and two plug-in expansion boards of any type to CPU 1214.

Before you install or remove any electrical device, ensure that the power to that equipment has been turned off. Also, ensure that the power to any related equipment has been turned off.

⚠ WARNING

Installation or removal of S7-1200 G2 devices with power applied

Installation or removal of S7-1200 G2 or related equipment with the power applied can cause electric shock or unexpected operation of equipment.

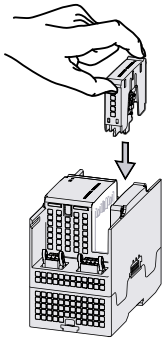
Always follow appropriate safety precautions and ensure that power to the S7-1200 G2 is disabled before attempting to install or remove S7-1200 G2 CPUs or related equipment.

Failure to disable all power to the S7-1200 G2 and related equipment during installation or removal procedures can result in death, severe personal injury and/or property damage due to electric shock or unexpected equipment operation.

Installing an SB

To install an SB, follow these steps:

1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Remove the upper and lower doors from the CPU.
3. Grasp the top and bottom of the existing blank board cover or plug-in expansion board, and pull away from the CPU to remove it. (If you are installing an SB into a newly purchased CPU, retain the preinstalled blank board cover after removing it from the CPU.)



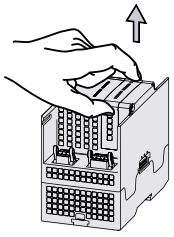
4. Insert the plug-in expansion board into the vacant slot and press down on it until it clicks into place.
5. Replace the upper and lower doors.

Removing an SB

To remove an SB, follow these steps:

1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Remove the upper and lower doors from the CPU.

3. Grasp the top and bottom of the plug-in expansion board and pull away from the CPU to remove it.



4. Insert the desired plug-in expansion board into the vacant slot and press down on it until it clicks into place. (If no SB is required, reinsert the blank board cover that came with the CPU.)
5. Replace the upper and lower doors.

⚠ WARNING

Risks associated with leaving a plug-in expansion board slot empty

Leaving a plug-in expansion board slot empty can expose the internal elements of the CPU to environmental contaminants like moisture, dust, or debris that can damage or shorten the lifespan of the CPU.

Do not leave a plug-in expansion board slot empty. If you are not installing a new SB, reinsert the blank board cover. (Blank board covers are preinstalled in the CPU at the time of purchase.)

Damage to the CPU can cause equipment malfunction. Equipment malfunction can potentially result in property damage, severe personal injury, or death.

3.6.4 Removing and installing terminal block connectors

Removing and installing a CPU, CM, or SM terminal block connector

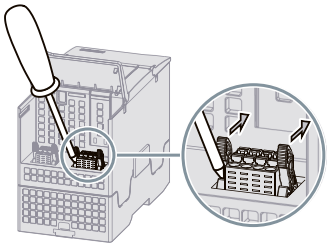
All S7-1200 G2 devices provide removable connectors to make connecting the wiring easy. For more information on how to wire connectors, see Wiring procedures (Page 44).

Removing a CPU, CM, or SM terminal block connector

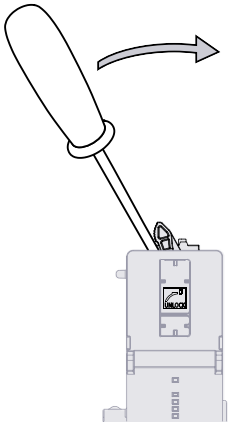
To remove an CPU, CM, or SM terminal block connector, follow these steps:

1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Use a screwdriver to release the terminal block connector levers or firmly press them in the direction shown below.

   CPU removal:



   CM or SM removal:



3. Grasp the connector and remove it from the CPU, CM, or SM.

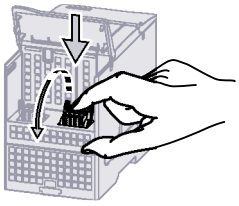
Installing a CPU, CM, or SM terminal block connector

To install an CPU, CM, or SM terminal block connector, follow these steps:

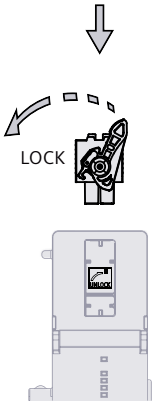
1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Align the terminal block connector with the pins on the unit; for the SM and CM you can use the symbol marked on the unit to identify proper orientation of the connector.

3. Press firmly down on the center of the terminal block connector until it snaps into place. (The levers will rotate and lock into place as you press down.)

   CPU installation:



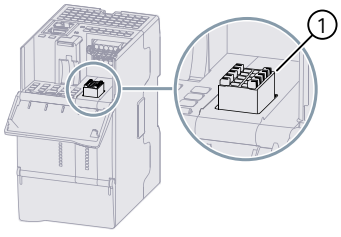
   CM or SM installation:



4. Make sure that the terminal block connector is properly aligned and in the locked position.

Removing and installing an SB terminal block connector

The terminal block connector for an SB is behind the top door of the CPU, as shown below.

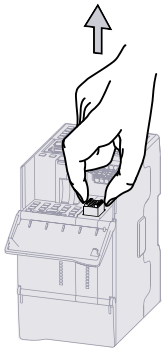


① SB terminal block connector

Removing an SB terminal block connector

To remove an SB terminal block connector, follow these steps:

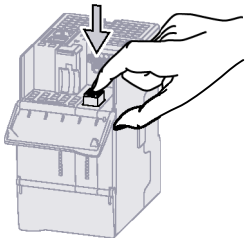
1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Firmly grasp the terminal block connector and pull away from the CPU.



Installing an SB terminal block connector

To install an SB terminal block connector, follow these steps:

1. Ensure that the CPU and all S7-1200 G2 equipment are powered down.
2. Align the terminal block connector with the pins on the unit.
3. Press down firmly on the center of the terminal block connector until it snaps into place.



3.7 Wiring guidelines and procedures

3.7.1 Safety considerations

Proper grounding and wiring of all electrical equipment are important to help ensure the optimum operation of your system and to provide additional electrical noise protection for your application and the S7-1200 G2. Refer to the technical specifications (Page 229) for the S7-1200 G2 wiring diagrams.

Prerequisites

Before grounding or installing wiring to any electrical device, ensure that the power to that device is off. Also, ensure that the power to any related equipment is off.

⚠ WARNING

Risk of electrocution when installing or removing devices

Installing or wiring the S7-1200 G2 or related equipment with power applied could cause electric shock or unexpected operation of equipment.

Always follow appropriate safety precautions and ensure that power is disabled to the S7-1200 G2 or related equipment before attempting to install or remove any devices.

Failure to disable all power to the S7-1200 G2 and related equipment during installation or removal procedures could result in death, severe personal injury, and/or property damage due to electric shock or unexpected equipment operation.

Always consider safety when designing the grounding and wiring for the S7-1200 G2 system. Follow all applicable electrical codes when wiring the S7-1200 G2 and related equipment. Install and operate all equipment according to all applicable national and local standards. Contact your local authorities to determine which codes and standards apply to your specific case.

⚠ WARNING

Risk of unexpected equipment operation

Control devices can fail in unsafe conditions, resulting in unexpected equipment operation.

Use an emergency stop function, electromechanical overrides, or other redundant safeguards that are independent of the S7-1200 G2.

Unexpected operation can result in death, severe personal injury and/or property damage.

3.7.2 Guidelines for isolation

S7-1200 G2 AC power supply boundaries and I/O boundaries to AC circuits provide safe separation between AC line voltages and low voltage circuits. These boundaries include double or reinforced insulation, or basic plus supplementary insulation, according to various standards. Components which cross these boundaries such as optical couplers, capacitors, transformers, and relays have been approved as providing safe separation. Only circuits rated for AC line voltage include safety isolation to other circuits. Isolation boundaries between 24 V DC circuits are functional only. Do not depend on these boundaries for safety.

The sensor supply output, communications circuits, and internal logic circuits of an S7-1200 G2 with included AC power supply are sourced as SELV (safety extra-low voltage) according to EN 61131-2.

To ensure safe operation, you must power the external connections to the following items from approved sources that meet the requirements of SELV/PELV, Class 2, Limited Voltage, or Limited Power according to various standards:

- Communications ports
- Analog circuits
- 24 V DC nominal power supply
- Digital I/O circuits

⚠ WARNING

Risk of electrocution with use of non-isolated or single insulation supplies

Using non-isolated or single insulation supplies can cause circuits that are normally safe to the touch, like communications circuits and low voltage sensor wiring, to carry hazardous levels of voltage.

Do not use non-isolated or single insulation supplies to supply low voltage circuits from an AC line.

Only use high voltage to low voltage power converters that are approved as sources of touch safe, limited voltage circuits.

Using non-isolated or single insulation supplies can cause unexpected electric shock resulting in death, severe personal injury, and/or property damage.

3.7.3 Guidelines for grounding

Ground all S7-1200 G2 and related equipment connections (common and ground) to a single point. Always connect this single point directly to the earth ground of the system.

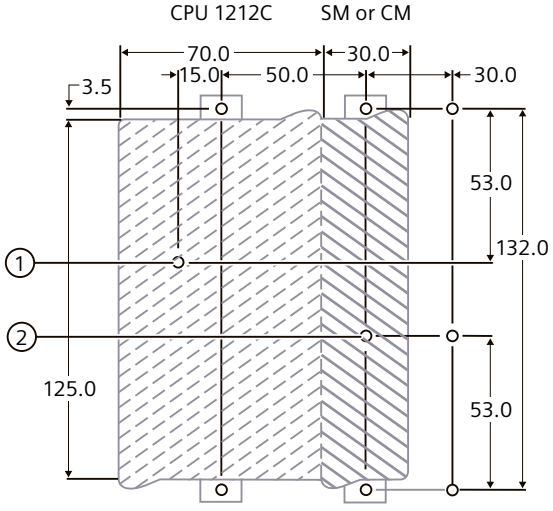
Use the shortest ground wire possible; use a large wire size, such as 2.5 mm^2 (14 AWG).

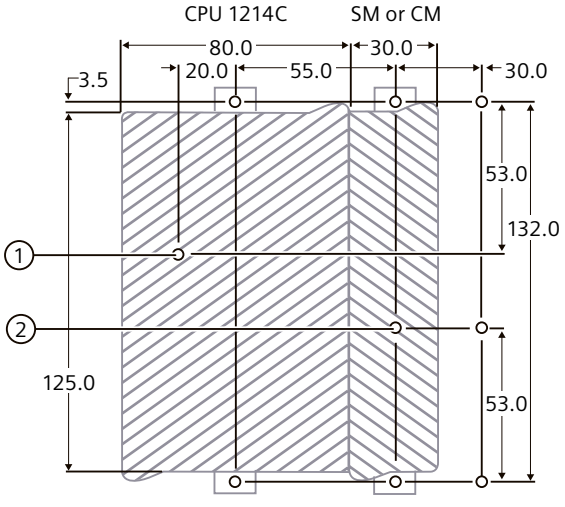
When using shielded cables, always connect the cable shields to the ground at both ends to reduce low and high frequency interference.

When locating grounds, consider safety-grounding requirements and the proper operation of protective interrupting devices.

When the S7-1200 G2 is mounted to a DIN rail, the units use a spring to make proper ground connection to the DIN rail. Ensure that the DIN rail is properly grounded to the system's single point ground.

When the S7-1200 G2 is mounted to a panel, it is required to place an M4 pan head stainless steel screw with a star washer into the panel at the locations shown below. This screw will allow the units ground spring to make proper electrical contact with the panel. Ensure that the panel is properly grounded to the system's single point ground.





① CPU grounding screw

② SM or CM grounding screw

All measurements are shown in millimeters.

3.7.4 Guidelines for wiring

When designing the wiring for the S7-1200 G2, provide a single disconnect switch that simultaneously removes power from the S7-1200 G2 CPU power supply, from all input circuits, and from all output circuits. Provide over-current protection, such as a fuse or circuit breaker, to limit fault currents on supply wiring. Consider providing additional protection by placing a fuse or other current limit in each output circuit.

Install appropriate surge suppression devices for any wiring that could be subject to lightning surges.

Avoid placing low-voltage signal wires and communications cables in the same wire tray with AC wires and high-energy, rapidly switched DC wires. Always route wires in pairs, with the neutral or common wire paired with the hot or signal-carrying wire.

Use the shortest wire possible and ensure that the wire is sized properly to carry the required current. Use properly sized copper ferrule sleeves to terminate the wire into the connector.

Use wire and cable with a temperature rating that is 45 °C higher than the ambient temperature around the S7-1200 G2. Use the specific electrical circuit ratings and the installation environment to determine what other types of wiring and materials are needed.

To reduce electrical noise, use shielded wires.

In addition to using shielded wires, you can do the following to further reduce electrical noise:

- Connect the shield to the ground at both ends of the cable.
- Ground other cable shields using clamps or copper tape around the shield to provide a high surface area connection to the grounding point.

When wiring input circuits that are powered by an external power supply, include an overcurrent protection device in that circuit. External protection is not necessary for circuits that are powered by the 24 V DC sensor supply from the S7-1200 G2 because the sensor supply is already current-limited.

All S7-1200 G2 modules have removable connectors for user wiring. To prevent loose connections, ensure that the connector is seated properly, locked in place, and that the wire is installed securely into the connector.

To help prevent unwanted current flows in your installation, the S7-1200 G2 provides isolation boundaries at certain points. When planning the wiring for the system, consider these isolation boundaries. Refer to the technical specifications (Page 229) for the amount of isolation provided and the location of the isolation boundaries. Circuits rated for AC line voltage include safety isolation to other circuits. Isolation boundaries between 24 V DC circuits are functional only; do not depend on these boundaries for safety.

A summary of Wiring rules for the S7-1200 G2 CPUs, CMs, SMs, and SBs is shown below:

Table 3-2 Wiring rules for S7-1200 G2 CPUs, CMs, SMs, and SBs

Wiring rules for...	**CPU, CM, and SM connector**	**SB connector**
Connection technology	**Push in**	**Push in**
Connectible conductor cross-sections for standard wires	0.2 mm^2 to 1.5 mm^2 (24 AWG to 16 AWG)	0.2 mm^2 to 0.8 mm^2 (24 AWG to 18 AWG)
Number of wires per connection	1 wire or combination of 2 wires in a double copper ferrule sleeve up to 1.5 mm^2 (total)	1 wire or combination of 2 wires up to 0.8 mm^2 (total)
Wire stripping length (Use copper ferrule sleeves for secure electric connection)	9 to 10 mm	7 mm

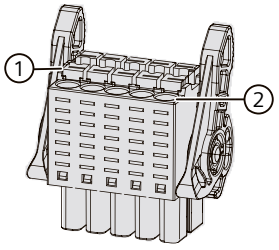
NOTE

Use copper ferrule sleeves on stranded conductors to reduce the risk of stray strands causing short circuits. Ferrules longer than the recommended strip length must include an insulating collar to prevent shorts due to side movement of conductors. Cross-sectional area limits for bare conductors also apply to ferrules.

3.7.5 Wiring and unwiring terminal block connectors

Removable terminal block connectors are used to wire S7-1200 G2 CPUs and modules.

All S7-1200 G2 removable terminal block connectors have the following parts:



① Spring release
② Push-in terminal

There are various types and sizes of terminal block connectors. For CPU, CM, and SM terminal block connectors, the color of the terminal block lock handle and spring release indicates the type of connector. For example, an orange handle and release indicates a high voltage connector. The color used on the connector matches the color of the terminal block header on the CPU or module.

For details on the terminal block connectors used in a specific CPU or module, refer to the wiring diagram of the device in the Technical specifications (Page 229). Information on terminal block spare kits can be found in Ordering information (Page 334).

NOTE

PLCs require correct wiring to ensure safety and proper operation.

When replacing the terminal block in your S7-1200 G2 CPU or module, it is important that you use the correct terminal block and correct wiring source for your module.

The G2 removable terminal block is designed to prevent you from accidentally placing a high voltage wired terminal block into a low voltage module, or from placing a special voltage wired terminal block into a normal voltage module.

Wiring rules

For wire size requirements and wire stripping length, refer to Wiring rules for S7-1200 G2 CPUs, SMs, and SBs (Page 43).

Solid or stranded wire can be used. Siemens recommends using ferrules with stranded wire.

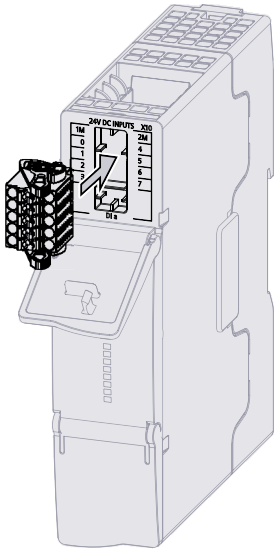
Wiring terminal block connectors

When wiring a removable terminal block connector, use a wire stripping tool to remove the plastic coating from the section of the wire that you are inserting into the connector.

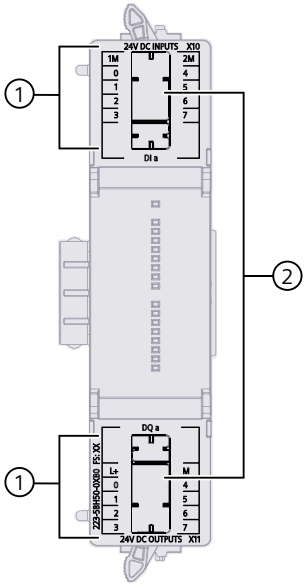
If using stranded wire, you might also need a 0.4 to 2.0 mm flat head screwdriver and a crimping tool.

To wire the removable terminal block connector of a CPU or expansion module, follow these steps:

1. Disconnect the CPU and all S7-1200 G2 equipment from electrical power.
2. Remove the terminal block connector from the CPU or module as described in Removing and installing S7-1200 G2 terminal block connectors (Page 37).
3. If wiring a CM or SM, place the terminal block connector into the wiring slot on the front of the module. (Skip this step if you are wiring a CPU or SB.)



Unlike the removable terminal block connectors on a CPU or SB, each expansion module has wiring slots with pin assignments located on the front of the module. Use these slots when wiring an expansion module.



① Pin assignments

② Wiring slots

4. Strip the end of the wire(s) to the length specified in Wiring rules for S7-1200 G2 CPUs, SMs, and SBs (Page 43).

NOTE

When using stranded wire, for best results, attach a ferrule to the end of the wire and crimp the end using a crimping tool. Do not attach a ferrule to solid wire. It is not necessary to use ferrules when using solid wire.

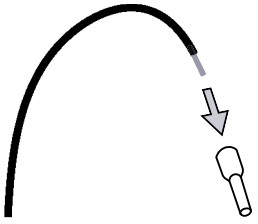
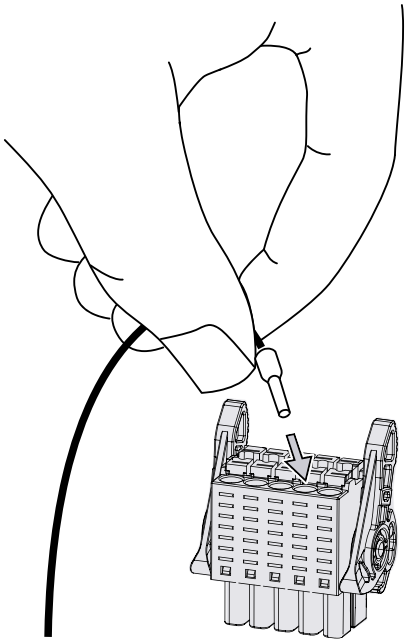
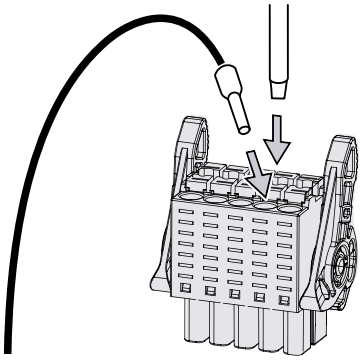


Figure 3-1 How to attach a ferrule to stranded wire

5. Use your hand to press the wire(s) into the push-in terminal,



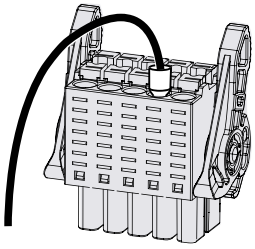
or use a 0.4 to 2.0 mm flathead screwdriver to press down on the spring release and insert the wire(s) into the push-in terminal.



NOTE

Pressing down on the spring release opens the teeth inside the connector and makes it easier to insert the wire. Once a wire is inserted into the push-in terminal, the teeth hold the wire in place.

6. Once all wires are inserted and secure, install the terminal block connector as described in Removing and installing S7-1200 G2 terminal block connectors (Page 37).

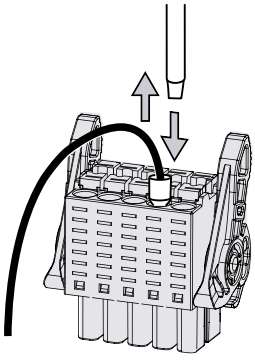


Unwiring terminal block connectors

Use a 0.4 to 2.0 mm flat head screwdriver to unwire the removable terminal block connector.

To unwire the removable terminal block connector of a CPU or expansion module, follow these steps:

1. Disconnect the CPU and all S7-1200 G2 equipment from electrical power.
2. Remove the terminal block connector from the CPU or module as described in Removing and installing S7-1200 G2 terminal block connectors (Page 37).
3. Using a 0.4 to 2.0 mm flathead screwdriver, press down on the spring release and remove the wire and ferrule from the push-in terminal.



3.7.6 Guidelines for inductive loads

Use suppressor circuits with inductive loads to limit the voltage rise when a control output turns off. Suppressor circuits protect your outputs from premature failure caused by the high voltage transient that occurs when current flow through an inductive load is interrupted.

In addition, suppressor circuits limit the electrical noise generated when switching inductive loads. High frequency noise from poorly suppressed inductive loads can disrupt the operation of the PLC. Placing an external suppressor circuit so that it is electrically across the load and physically located near the load is the most effective way to reduce electrical noise.

S7-1200 G2 DC outputs include internal suppressor circuits that are adequate for inductive loads in most applications. Internal protection is not provided for relay outputs because you can use S7-1200 G2 relay output contacts to switch either a DC or an AC load.

Consider using inductive loads with integrated suppression circuitry. However, for some applications, manufacturer-provided suppressor circuits are inadequate. You can use an additional suppressor circuit to further protect the PLC output.

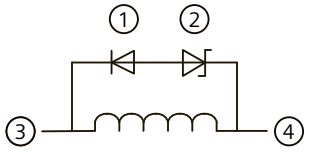
Consider using a metal oxide varistor (MOV), parallel RC circuit, or a combination of both for AC loads. A MOV suppressor with no parallel RC circuit often results in significant high frequency noise up to the clamp voltage.

A well-controlled turn-off transient will have a ring frequency of no more than 10 kHz, with less than 1 kHz preferred. Peak voltage for AC lines must be within +/- 1200 V of ground. Negative peak voltage for DC loads using the PLC internal suppression will be ~40 V below the 24 V DC supply voltage. External suppression must limit the transient to within 36 V of the supply to unload the internal suppression.

NOTE

The effectiveness of a suppressor circuit depends on the application; you must verify a suppressor circuit is suitable for your particular usage. Ensure that all components are correctly rated. Use an oscilloscope to observe the turn-off transient.

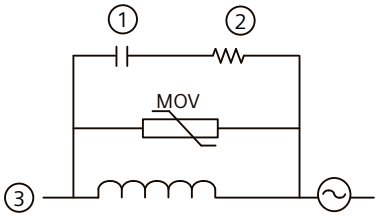
Typical suppressor circuit for DC or relay outputs that switch DC inductive loads



1. 1N4001 diode or equivalent
2. 8.2 V Zener (DC outputs), 36 V Zener (Relay outputs)
3. Output point
4. M, 24 V reference

In most applications, the addition of a diode (1) across a DC inductive load is suitable, but if your application requires faster turn-off times, then the addition of a zener diode (2) is recommended. Be sure to size your zener diode properly for the amount of current in your output circuit.

Typical suppressor circuit for relay outputs that switch AC inductive loads



1. See table for C value
2. See table for R value
3. Output point

Ensure that the working voltage of the metal oxide varistor (MOV) is at least 20% greater than the nominal line voltage.

Choose pulse-rated, non-inductive resistors, and capacitors recommended for pulse applications (typically metal film). Verify the components meet average power, peak power, and peak voltage requirements.

If you design your own suppressor circuit, the following table suggests resistor and capacitor values for a range of AC loads. These values are based on calculations with ideal component parameters. I rms in the table refers to the steady-state current of the load when fully ON.

Table 3-3 AC suppressor circuit resistor and capacitor values

Inductive load			**Suppressor values**		
I rms	230 V AC	120 V AC	Resistor		Capacitor
Amps	VA	VA	Ω	W (power rating)	nF
0.02	4.6	2.4	15000	0.1	15
0.05	11.5	6	5600	0.25	47
0.1	23	12	2700	0.5	100
0.2	46	24	1500	1	150
0.5	115	60	560	2.5	470
1	230	120	270	5	1000
2	460	240	150	10	1500

[2] **Conditions satisfied by the table values:**
Maximum turn-off transition step < 500 V
Resistor peak voltage < 500 V
Capacitor peak voltage < 1250 V
Suppressor current < 8% of load current (50 Hz)
Suppressor current < 11% of load current (60 Hz)
Capacitor dV/dt < 2 V/µs
Capacitor pulse dissipation : ∫(dv/dt) dt < 10000 V^2/µs
Resonant frequency < 300 Hz
Resistor power for 2 Hz max switching frequency
Power factor of 0.3 assumed for typical inductive load

3.7.7 Guidelines for lamp loads

Lamp loads, including LED lamp loads, are damaging to relay contacts because of the high turn-on surge current. This surge current will nominally be 10 to 15 times the steady state current for a Tungsten lamp. A replaceable interposing relay or surge limiter is recommended for lamp loads that will be switched a large number of times during the lifetime of the application.

3.8 Maintenance and repair

The components of the S7-1200 G2 automation system are maintenance-free.

NOTE

Only the manufacturer can carry out repairs to the components of the S7-1200 G2 automation system.

PLC concepts, configuration, and programming 4

4.1 TIA Portal

The Totally Integrated Automation Portal (TIA Portal) is an engineering framework for implementing automation solutions. The TIA Portal includes STEP 7 for PLC programming and configuration. You use STEP 7 to configure CPUs and modules (Page 107) and for programming your application logic (Page 122).

TIA Portal provides an extensive information system.

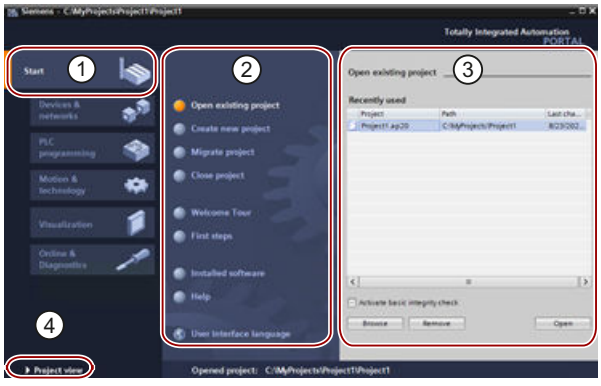
4.2 Different views in the TIA Portal

The TIA Portal provides two different views of the project that you use for your control application:

- Portal view: A task-oriented set of portals that are organized on the functionality of the tools
- Project view: A project-oriented view of the elements within the project

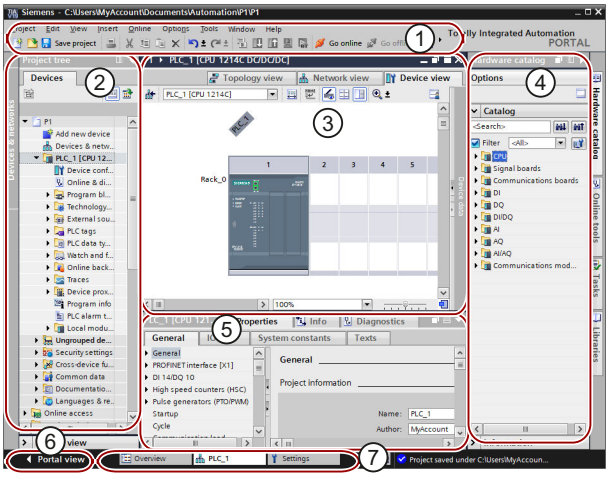
Choose which view helps you work most efficiently. With a single click, you can toggle between the Portal view and the Project view.

Portal view



① Portals for the different tasks
② Tasks for the selected portal
③ Selection panel for the selected action
④ Switch to Project view

Project view



① Menus and toolbar
② Project tree navigator
③ Work area
④ Task cards
⑤ Inspector window
⑥ Selector to change to the Portal view
⑦ Editor bar

With these components in one place, you have easy access to every aspect of your project. The work area consists of three tabbed views:

- Device view: Displays the device that you have added or selected and its associated modules
- Network view: Displays the CPUs and network connections in your network
- Topology view: Displays the PROFINET topology of the network including devices, passive components, ports, interconnections, and port diagnostics

Each view also enables you to perform configuration tasks. The inspector window shows the properties and information for the object that you have selected in the work area. As you select different objects, the inspector window displays the properties that you can configure. The inspector window includes tabs that allow you to see diagnostic information and other messages.

By showing all of the editors that are open, the editor bar helps you work more quickly and efficiently. To toggle between the open editors, simply click one of the open editors. You can also arrange two editors to appear together, arranged either vertically or horizontally. This feature allows you to drag and drop between editors.

4.3 Using the TIA Portal Information System

The TIA Portal Information System has extensive information about configuring and programming PLCs. In the TIA Portal Information System, refer to "Introduction to the TIA Portal > Help on the information system" for usage information.

When searching for information about the S7-1200 G2, note the following:

- When filtering a search on devices, S7-1200 G2 is not available as a device selection. Filtering by S7-1500 would be the closest match to S7-1200 G2 information.
- When using context-sensitive help in the TIA Portal, note that some objects offer an S7-1200 topic and others an S7-1500 topic. When offered a choice, S7-1500 would be the closest match.

This system manual for the S7-1200 G2 Programmable Logic Controller provides guidance in areas where the S7-1200 G2 differs from an S7-1200 or an S7-1500.

4.4 Program structure

4.4.1 Structure of a STEP 7 user program

The S7-1200 G2 CPU supports the following types of code blocks that allow you to create an efficient structure for your user program:

- Organization blocks (OBs) (Page 59) define the structure of the program. Some OBs run at startup. Some run continuously when the CPU is running your process. Some run under specific conditions.
- Data blocks (DBs) (Page 87) store data that can be used by the program blocks.
- Functions (FCs) and function blocks (FBs) contain the program code that corresponds to specific tasks. FCs and FBs can be called from an OB or from another FC or FB. Each FC or FB provides a set of input and output parameters for sharing data with the calling block. An FB also uses an associated data block (called an instance DB) to maintain the data values for that instance of the FB call. You can call an FB multiple times, each time with a unique instance DB. Calls to the same FB with different instance DBs do not affect the data values in any of the other instance DBs.

An S7-1200 G2 F-CPU supports the following types of code blocks that allow you to create an efficient structure for your safety program:

- Fail-safe organization blocks (F-OBs) define the structure of the safety program. The F-OB calls the main safety block in an F-Runtime Group (F-RTG); this group contains F-blocks that you create or that are inserted from the project or global libraries, as well as those which are added automatically by the safety program. You can manage F-RTGs in the Safety Administration Editor (SAE). There can be either one or two F-RTGs.
- Fail-safe data blocks (F-DBs) store data that can be used by the safety program blocks.
  - F-I/O data blocks are automatically generated by the safety program when you configure an F-I/O.
  - F-shared data blocks are data blocks that contain all data shared between the safety program and the F-subsystems.
  - F-runtime group information data blocks are created by the safety program when you create an F-runtime group. These blocks provide information on the F-runtime group and on the safety program.
- Fail-safe functions (F-FCs) and Fail-safe function blocks (F-FBs) contain the program code that corresponds specifically to safety tasks. F-FCs and F-FBs can be called from an F-OB or from another F-FC or F-FB. Each F-FC or F-FB contains instructions from either the project or global library and can call other created F-FBs or F-FCs to structure the user safety program.

NOTE

Integrated standard I/O channels not used for fail-safe I/O function

In your STEP 7 project, you can configure the integrated I/O of the F-CPU with standard code blocks, but these I/O are not safety I/O. You can only use F-I/O to accomplish safety tasks by configuring the fail-safe I/O channels with safety blocks.

To learn more about the code blocks which structure the safety program, refer to the "SIMATIC Safety - Configuring and Programming" manual (https://support.industry.siemens.com/cs/us/en/view/54110126).

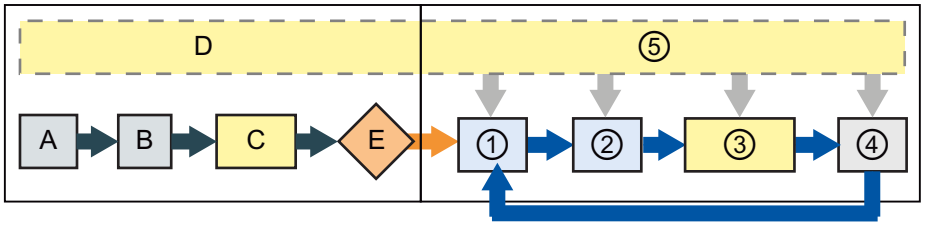
4.4.2 Execution of the user program

Execution of the user program begins with one or more optional startup OBs (Page 60) that execute once upon entering RUN mode. Execution then continues with configured program cycle OBs (Page 59) that execute cyclically. You can also associate an OB with an interrupt event, which can be either a standard event or an error event. These OBs execute whenever the corresponding standard or error event occurs.

Operating modes

The CPU has three modes of operation: STOP mode, STARTUP mode, and RUN mode. Status LEDs on the front of the CPU indicate the current mode of operation.

- In STOP mode, the CPU handles any communication requests (as appropriate) and performs self-diagnostics. The CPU does not execute the user program. Automatic updates of the process image do not occur. You can download a project to the CPU.
- In STARTUP and RUN modes, the CPU performs the tasks shown in the following figure:



STARTUP

A	Copies the state of the physical inputs to I memory
B	Initializes the Q output (image) memory area with either zero or the last value. Zeroes PN outputs
C	Initializes non-retentive M memory and data blocks to their initial value and enables configured cyclic interrupt and time of day events. Executes the startup OBs.
D	Stores any interrupt events into the queue to be processed after entering RUN mode
E	Enables the writing of Q memory to the physical outputs

RUN

①	Writes Q memory to the physical outputs
②	Copies the state of the physical inputs to I memory
③	Executes the program cycle OBs and updates the output values in the process image output area
④	Performs self-test diagnostics
⑤	Processes interrupts and communications during any part of the scan cycle

You can download some parts of a project in RUN mode (Page 215).

Restart of fail-safe system

The operating modes of the SIMATIC Safety system differ from those of the standard system only in terms of the restart characteristics.

When you switch a fail-safe CPU from STOP to RUN mode, the standard user program restarts in the usual way. When you restart the safety program, the fail-safe system initializes all data blocks with the F-Attribute with values from load memory. This is comparable to a cold restart.

Process image update and process image partitions

The CPU updates local digital and analog I/O points synchronously with the scan cycle using an internal memory area called the process image. The process image contains a snapshot of the physical inputs and outputs (the physical I/O points on the CPU, signal board, and signal modules).

You can configure I/O points to be updated in the process image every scan cycle or when a specific event interrupt occurs. You can also configure an I/O point to be excluded from process image updates. For example, your process might only need certain data values when an event such as a hardware interrupt occurs. By configuring the process image update for these I/O points to be associated with a partition that you assign to a hardware interrupt OB, you avoid having the CPU update data values unnecessarily every scan cycle when your process does not need a continual update.

For controlling whether your process updates I/O points automatically on every scan cycle, or upon the triggering of events, the S7-1200 G2 provides 32 process image partitions. The first process image partition, PIP0, is designated for I/O that is to be automatically updated every scan cycle, and is the default assignment. You can use the remaining partitions, PIP1 through PIP31, for assigning I/O process image updates to various interrupt events. You assign I/O to process image partitions in Device Configuration and you assign process image partitions to interrupt events when you create interrupt OBs (Page 59) or edit OB properties (Page 59).

By default, when you insert a module in the device view, STEP 7 sets its I/O process image update to "Automatic update". For I/O configured for "Automatic update", the CPU handles the data exchange between the module and the process image area automatically during every scan cycle.

To assign digital or analog points to a process image partition, or to exclude I/O points from process image updates, follow these steps:

1. View the Properties tab for the appropriate device in Device configuration.
2. Expand the selections under "General" as necessary to locate the desired I/O points.
3. Select "I/O addresses".
4. Optionally select a specific OB from the "Organization block" drop-down list.
5. From the "Process image" drop-down list, change "Automatic update" to a PIP from PIP1 through PIP31 or None. A selection of "None" means that you can only read from and write to this I/O using immediate instructions. To add the points back to the process image automatic update, change this selection back to "Automatic update".

You can immediately read physical input values and immediately write physical output values when an instruction executes. An immediate read accesses the current state of the physical input and does not update the process image input area, regardless of whether the point is configured to be stored in the process image. An immediate write to the physical output updates both the process image output area (if the point is configured to be stored in the process image) and the physical output point. Append the suffix ":P" to the I/O address if you want the program to immediately access I/O data directly from the physical point instead of using the process image.

NOTE

Use of process image partitions

If you assign I/O to one of the process image partitions PIP1 - PIP31, and do not assign an OB to that partition, then the CPU never updates that I/O to or from the process image. Assigning I/O to a PIP that does not have a corresponding OB assignment is the same as assigning the process image to "None". You can read the I/O directly from the physical I/O with an immediate read instruction, or write to the physical I/O with an immediate write instruction. The CPU does not update the process image.

The CPU supports distributed I/O for PROFINET (Page 135) networks.

4.4.3 Startup configuration and processing

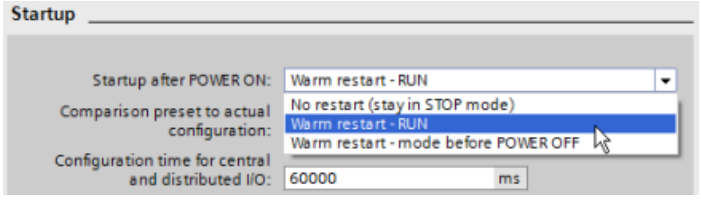
Startup configuration

The CPU supports a warm restart for entering the RUN mode. The CPU initializes all non-retentive system and user data at warm restart, and retains the values of all retentive user data.

Warm restart does not include a memory reset. A memory reset clears all work memory, clears retentive and non-retentive memory areas, copies load memory to work memory, and sets outputs to the configured "Reaction to CPU STOP". A memory reset does not clear the diagnostics buffer or the permanently saved values of the IP address.

You can configure the "startup after POWER ON" setting of the CPU. This configuration item appears under the "Device configuration" for the CPU under "Startup". Upon powering up, the CPU performs a sequence of power-up diagnostic checks and system initialization. During system initialization, the CPU deletes all non-retentive bit (M) memory and resets all non-retentive DB contents to the initial values from load memory. The CPU retains retentive bit (M) memory and retentive DB contents and then enters the appropriate operating mode. Certain detected errors prevent the CPU from entering the RUN mode. The CPU supports the following configuration choices:

- No restart (stay in STOP mode)
- Warm restart - RUN
- Warm restart - mode prior to POWER OFF



NOTICE

Risks associated with repairable faults

The CPU can enter STOP mode due to repairable faults, such as the following:

– Failure of a replaceable signal module

– Temporary faults, such as power line disturbance or erratic power up event

Such conditions can result in property damage.

If you have configured the CPU to "Warm restart - mode prior to POWER OFF", the CPU goes to the operating mode that the CPU was in prior to the loss of power or fault. If the CPU was in STOP mode at the time of power loss or fault, the CPU goes to STOP mode on power up. The CPU stays in STOP mode until the CPU receives a command to go to RUN mode. If the CPU was in RUN mode at the time of power loss or fault, the CPU goes to RUN mode on the next power up. The CPU goes to RUN mode providing the CPU detects no errors that would inhibit a transition to RUN mode.

Configure CPUs that you intend to operate independently of a STEP 7 connection to "Warm restart - RUN". This startup mode sets the CPU to return to RUN mode on the next power cycle.

Startup processing

See Execution of the user program (Page 54) for the processing sequence during startup.

Each startup OB includes startup information that helps you determine the validity of retentive data and the time-of-day clock. You can program instructions inside the startup OBs to examine these startup values and to take appropriate action.

The CPU also performs the following tasks during the startup processing:

- Interrupts are queued but not processed during the startup phase
- No cycle time monitoring is performed during the startup phase
- Configuration changes to HSC (high-speed counter), PTO (pulse train output), and PtP (point-to-point communication) modules can be made in startup
- Actual operation of HSC, PTO, and point-to-point communication modules only occurs in RUN

After the execution of the startup OBs finishes, the CPU goes to RUN mode and processes the control tasks in a continuous scan cycle.

Changing the operating mode

You can use the "STOP" or "RUN" commands (Page 188) from the online tools of the TIA Portal to change the current operating mode. You can also include an STP instruction in your program to change the CPU to STOP mode. Other tools provide a means to change the operating mode as well.

4.4.4 Processing the scan cycle in RUN mode

For each scan cycle, the CPU performs processing as described in Execution of the user program (Page 54).

The CPU handles interrupt events that are enabled according to priority in the order in which they occur. For interrupt events, the CPU reads the inputs, executes the OB, and then writes the outputs, using the associated process image partition (PIP), if applicable.

The system guarantees that the scan cycle will be completed in a time period called the maximum cycle time; otherwise a time error event is generated.

- Each scan cycle begins by retrieving the current values of the digital and analog outputs from the process image and then writing them to the physical outputs of the CPU, SB, and SM modules configured for automatic I/O update (default configuration). When a physical output is accessed by an instruction, both the output process image and the physical output itself are updated.
- The scan cycle continues by reading the current values of the digital and analog inputs from the CPU, SB, and SMs configured for automatic I/O update (default configuration), and then writing these values to the process image. When a physical input is accessed by an instruction, the value of the physical input is accessed by the instruction, but the input process image is not updated.
- After reading the inputs, the user program is executed from the first instruction through the end instruction. This includes all the program cycle OBs plus all their associated FCs and FBs. The program cycle OBs are executed in order according to the OB number with the lowest OB number executing first.

Communications processing occurs periodically throughout the scan, possibly interrupting user program execution (https://support.industry.siemens.com/cs/de/en/view/59193558/158758826123).

Self-diagnostic checks include periodic checks of the system and the I/O module status checks.

Interrupts can occur during any part of the scan cycle, and are event-driven. When an event occurs, the CPU interrupts the scan cycle and calls the OB that was configured to process that event. After the OB finishes processing the event, the CPU resumes execution of the user program at the point of interruption.

4.4.5 Organization blocks (OBs)

Organization blocks (OBs) control the execution of the user program.

The program cycle OB contains your main program. You can include more than one program cycle OB in your user program. During RUN mode, the program cycle OBs execute at the lowest priority level (Page 75) and can be interrupted by all other event types. The CPU executes the program cycle OBs in a continuous cycle known as the "program cycle" or "scan cycle". This cyclic processing is the normal type of processing used for programmable logic controllers. For many applications, the entire user program is located in a single program cycle OB.

Specific events in the CPU trigger the execution of other organization blocks. OBs cannot call each other. The startup OB runs when you start the CPU. It does not interrupt the program cycle OB. The CPU executes the startup OB before going to RUN mode.

Other OBs, called interrupt OBs, run when associated events or errors occur. These OBs interrupt the execution of the program cycle OBs.

An FC or FB cannot call an OB. Only an event such as a diagnostic interrupt or a time delay can start the execution of an OB. The CPU handles OBs according to their respective priority classes (Page 75), with higher priority OBs executing before lower priority OBs.

4.4.5.1 Program cycle OB

Program cycle OBs execute cyclically while the CPU is in RUN mode. The main block of the program is a program cycle OB. This is where you place the instructions that control your program and where you call additional user blocks. You can have multiple program cycle OBs, which the CPU executes in numerical order. Main (OB 1) is the default.

Program cycle events

The program cycle event happens once during each program cycle (or scan). During the program cycle, the CPU writes the outputs, reads the inputs and executes program cycle OBs. The program cycle event is required and is always enabled. You might have no program cycle OBs, or you might have multiple program cycle OBs. After the program cycle event occurs, the CPU executes the lowest numbered program cycle OB (usually "Main" OB 1). The CPU executes the other program cycle OBs sequentially (in numerical order) within the program cycle. Program execution is cyclical such that the program cycle event occurs at the following times:

- When the last startup OB finishes execution
- When the last program cycle OB finishes execution

You can delay the next program cycle after the program cycle OB finishes by configuring a minimum cycle time in the device configuration

Table 4-1 Start information for a program cycle OB

Input	Data type	Description
Initial_Call	Bool	True for initial call of the OB
Remanence	Bool	True if retentive data are available

4.4.5.2 Startup OB

Startup OBs execute one time when the operating mode of the CPU changes from STOP to RUN, including powering up in the RUN mode and in commanded STOP-to-RUN transitions. After completion, the main "Program cycle" begins executing. Refer to "Startup processing" in Startup configuration and processing (Page 57)

The Startup OBs support the following startup data bits:

Table 4-2 Startup locations supported by the startup OB

Input	Data Type	Description
LostRetentive	Bool	This bit is true if the retentive data storage areas have been lost
LostRTC	Bool	This bit is true if the time-of-day clock (Real time Clock) has been lost

4.4.5.3 Time delay interrupt OB

Time delay interrupt OBs execute after a time delay that you configure.

Time delay interrupt events

You configure time delay interrupt events to occur after a specified delay time has expired from the beginning of execution of the SRT_DINT instruction. You assign the delay time with the SRT_DINT instruction. The time delay events interrupt the program cycle to execute the corresponding time delay interrupt OB. You can attach only one time delay interrupt OB to a time delay event. The CPU supports 20 time delay events.

Table 4-3 Start information for a time delay interrupt OB

Input	Data type	Description
Sign	Word	Identifier passed to triggering call of SRT_DINT

4.4.5.4 Cyclic interrupt OB

Cyclic interrupt OBs execute at a specified interval. You can configure up to a total of 20 cyclic interrupt events, with one OB corresponding to each cyclic interrupt event.

Cyclic interrupt events

The cyclic interrupt events allow you to configure the execution of an interrupt OB at a configured cycle time. You configure the initial cycle time when you create the cyclic interrupt OB. A cyclic event interrupts the program cycle and executes the corresponding cyclic interrupt OB. Note that the cyclic interrupt event is at a higher priority class than the program cycle event.

You can attach only one cyclic interrupt OB to a cyclic event.

You can assign a phase shift to each cyclic interrupt so that the execution of cyclic interrupts can be offset from one another by the phase offset amount. For example, if you have a 5 ms cyclic event and a 10 ms cyclic event, every ten milliseconds both events occur at the same moment. If you phase shift the 5 ms event by 1 to 4 ms and the 10 ms event by 0 ms, then the two events do not occur at the same moment.

The default phase offset is 0. To change the initial phase shift, or to change the cyclic time for a cyclic event, follow these steps:

1. Right-click the cyclic interrupt OB in the project tree.
2. Select "Properties" from the context menu.
3. Click "Cyclic interrupt" from the "Cyclic interrupt [OB 30]" dialog, and enter the new initial values.

The maximum phase offset is 6000000 microseconds (6 seconds) or the maximum Cyclic time, whichever is smaller.

You can also query and change the cycle time and the phase shift from your program using the Query cyclic interrupt (QRY_CINT) and Set cyclic interrupt (SET_CINT) instructions. Cycle time and phase shift values set by the SET_CINT instruction do not persist through a power cycle or a transition to STOP mode; cycle time and phase shift values return to the initial values following a power cycle or a transition to STOP. The CPU supports a total of 20 cyclic interrupt events.

Table 4-4 Start information for cyclic interrupt OB

Name	Data type	Meaning
Initial_Call	BOOL	=TRUE in the first call of this OB • At the transition from STOP or HOLD to RUN • After reloading
Event_Count	INT	Number of discarded cyclic interrupt events since the last start of this OB

4.4.5.5 Hardware interrupt OB

Hardware interrupt OBs execute when the relevant hardware event occurs. A hardware interrupt OB interrupts normal cyclic program execution in reaction to a signal from a hardware event.

Hardware interrupt events

Changes in the hardware, such as a rising or falling edge on an input point, or an HSC (High Speed Counter) event trigger hardware interrupt events. The S7-1200 G2 supports hardware interrupt OBs to respond to hardware interrupt events.

You enable the hardware events in the device configuration, and assign an OB for an event in the device configuration or with an ATTACH instruction in the STEP 7 program. The CPU supports several hardware interrupt events. The CPU model and the number of input points determine the exact events that are available.

Limits on hardware interrupt events are as follows:

Edges:

- One for each CPU and SB digital input
- Additional hardware interrupt events are possible from distributed I/O depending on the device and submodules that you use.

HSC events:

- CV=PV: maximum of 8
- Direction changed: maximum of 8
- External reset: maximum of 8

Table 4-5 Start information for a hardware interrupt OB

Input	Data type	Description
LADDR	HW_IO	Hardware identifier of the module that triggered the hardware interrupt
USI	WORD	User structure identifier (16#0001 to 16#FFFF), reserved for future use
IChannel	USINT	Number of the channel that triggered the interrupt
EventType	BYTE	Identifier for the module-specific event type associated with the event triggering the interrupt, for example falling edge or rising edge.

Table 4-6 Bits in EventType based on module and process event

Module / Submodule	Value	Process event
Onboard I/O from CPU or SB	16#0	Rising edge
	16#1	Falling edge
HSC	16#0	HSC CV=RV1
	16#1	HSC direction changed
	16#2	HSC reset

4.4.5.6 Time error interrupt OB

If configured, the time error interrupt OB (OB 80) executes when either the scan cycle exceeds the maximum cycle time or a time error event occurs. If triggered, it executes, interrupting normal cyclic program execution or any event OB at priority 21 or lower.

The occurrence of either of these events generates a diagnostics buffer entry describing the event. The diagnostics buffer entry is generated regardless of the existence of the time error interrupt OB.

Time error interrupt events

The occurrence of any of several different time error conditions results in a time error event:

- Scan cycle exceeds maximum cycle time

  The "maximum cycle time exceeded" condition results if the program cycle does not complete within the specified maximum scan cycle time. See the topic Monitoring and configuring the cycle time (Page 78) for more information.
- CPU cannot start requested OB because a second time interrupt (cyclic or time-delay) starts before the CPU finishes execution of the first interrupt OB
- Queue overflow occurred

  The "queue overflow occurred" condition results if the interrupts are occurring faster than the CPU can process them. The CPU limits the number of pending (queued) events by using a different queue for each event type. If an event occurs when the corresponding queue is full, the CPU generates a time error event.

All time error events trigger the execution of the time error interrupt OB if it exists. If the time error interrupt OB does not exist, then the following conditions determine the CPU behavior:

- If a time error interrupt OB has never been downloaded to the CPU, the CPU ignores the first scan timeout condition and remains in RUN mode. If a second scan timeout condition occurs in the same program scan (two times the maximum cycle time value), the CPU generates a diagnostic buffer entry and transitions to STOP mode.
- If the time error interrupt OB has previously been downloaded, but has since been deleted, the CPU transitions to STOP mode if a time error event occurs, because the CPU cannot find the time error OB.

The user program can extend the program cycle execution time up to ten times the configured maximum cycle time by executing the RE_TRIGR instruction to restart the cycle time monitor. However, if two "maximum cycle time exceeded" conditions occur within the same program cycle without resetting the cycle timer, then the CPU transitions to STOP, regardless of whether the time error interrupt OB exists. See the topic Monitoring and configuring the cycle time (Page 78).

Time error interrupt OB includes start information that helps you determine which event and OB generated the time error. You can program instructions inside the OB to examine these start values and to take appropriate action.

Table 4-7 Start information for the time error OB (OB 80)

Input	Data type	Description
Fault_ID	BYTE	16#01 - maximum cycle time exceeded 16#02 - requested OB cannot be started 16#07 and 16#09 - queue overflow occurred
Csg_OBnr	OB_ANY	Number of the OB which was being executed when the error occurred
Csg_Prio	UINT	Priority of the OB causing the error

See topic Organization blocks (OBs) (Page 59) for instructions on adding OBs to your project.

4.4.5.7 Diagnostic error interrupt OB

The diagnostic error interrupt OB executes when the CPU detects a diagnostic error, or if a diagnostics-capable module recognizes an error and you have enabled the diagnostic error interrupt for the module. The diagnostic error interrupt OB interrupts the normal cyclic program execution. You can include an STP instruction in the diagnostic error interrupt OB to put the CPU in STOP mode if you desire your CPU to enter STOP mode upon receiving this type of error.

If you do not include a diagnostic error interrupt OB in your program, the CPU ignores the error and stays in RUN mode.

Diagnostic error events

PROFINET, local analog, and some local digital devices are capable of detecting and reporting diagnostic errors. The occurrence or removal of any of several different diagnostic error conditions results in a diagnostic error event. Standard CPUs and modules can generate the following diagnostic errors:

- No user power
- High limit exceeded
- Low limit exceeded
- Wire break
- Short circuit

Distributed devices can generate additional diagnostic errors.

Diagnostic error events trigger the execution of the diagnostic error interrupt OB (OB 82) if it exists. If it does not exist, then the CPU ignores the error.

See topic Organization blocks (OBs) (Page 59) for instructions on adding an OB to your project.

NOTE

Diagnostic errors for multi-channel local analog devices

The diagnostic error interrupt OB can process only one channel's diagnostic error at a time.

If two channels of a multi-channel device have an error, then the second error only triggers the diagnostic error interrupt OB under the following conditions: the first channel error clears, the execution of the diagnostic error interrupt OB that the first error triggered is complete, and the second error still exists.

The diagnostic error interrupt OB includes startup information that helps you determine whether the event is due to the occurrence or removal of an error, and the device and channel which reported the error. You can program instructions inside the diagnostic error interrupt OB to examine these startup values and to take appropriate action.

NOTE

If the outgoing event leaves the submodule with no pending diagnostics, the Diagnostic error OB start information references the submodule as a whole (16#8000), even if the source of the event was a specific channel.

Table 4-8 Startup information for the diagnostic error interrupt OB

Input	Data type	Description
IOstate	WORD	IO state of the device: • Bit 0 = 1 if the configuration is correct, and = 0 if the configuration is no longer correct. • Bit 4 = 1 if an error is present (such as a wire break). (Bit 4 = 0 if there is no error.) • Bit 5 = 1 if the configuration is **not** correct, and = 0 if the configuration is correct again. • Bit 7 = 1 if an I/O access error has occurred. Refer to LADDR for the hardware identifier of the I/O with the access error. (Bit 6 = 0 if there is no error.)
LADDR	HW_ANY	Hardware identifier of the device or functional unit that reported the error[1]
Channel	UINT	Channel number
MultiError	BOOL	TRUE if more than one error is present

[1] The LADDR input contains the hardware identifier of the device or functional unit which returned the error. The hardware identifier is assigned automatically when components are inserted in the device or network view and appears in the System constants tab of PLC tags. A name is also assigned automatically for the hardware identifier. These entries in the System constants tab of the PLC tags cannot be changed.

4.4.5.8 Pull or plug of modules OB

The "Pull or plug of modules" OB executes when a configured and non-disabled distributed I/O module or submodule generates an event related to inserting or removing a module.

Pull or plug of modules event

The following conditions generate a pull or plug of modules event:

- Someone removes or inserts a configured module
- A configured module is not physically present in an expansion rack
- An incompatible module is in an expansion rack that does not correspond to the configured module
- A compatible module for a configured module is in an expansion rack, but the configuration does not allow substitutes
- A module or submodule has parameterization errors

If you have not programmed this OB, the CPU remains in RUN mode when any of these conditions occur with a configured and non-disabled distributed I/O module.

Regardless of whether you have programmed this OB, the CPU changes to STOP mode when any of these conditions occur with a module in the local rack.

Table 4-9 Start information for pull or plug of modules OB

Input	Data type	Description
LADDR	HW_IO	Hardware identifier
Event_Class	Byte	16#38: module inserted 16#39: module removed
Fault_ID	Byte	Fault identifier For event class 16#38: • 54: Submodule inserted, which conforms to the parameterized submodule • 55: Submodule inserted, which does not conform to the submodule parameter assignment • 56: Submodule inserted, but error in module parameter assignment • 57: Submodule inserted, but with a fault or maintenance issue • 58: Submodule access error remedied For event class 16#39 • 51: Module removed • 54: Submodule removed

4.4.5.9 Rack or station failure OB

The "Rack or station failure" OB executes when the CPU detects the failure or communication loss of a distributed rack or station.

Rack or station failure event

The CPU generates a rack or station failure event when it detects one of the following:

- The failure of a PROFINET IO system (in the case of either an incoming or an outgoing event).
- The failure of an IO device (in the case of either an incoming or an outgoing event)
- Failure of some of the submodules of a PROFINET I-device

If you have not programmed this OB, the CPU remains in RUN mode when any of these conditions occur.

Table 4-10 Start information for rack or station failure OB

Input	Data type	Description
LADDR	HW_Device	Hardware identifier
Event_Class	Byte	16#38: outgoing event 16#39: incoming event
Fault_ID	Byte	Fault identifier

4.4.5.10 Time of day OB

Time of day OBs execute based on configured clock time conditions. The CPU supports up to 20 time of day OBs.

Time of day events

You can configure a time of day interrupt event to occur once on a specified date or time or cyclically with one of the following cycles:

- Every minute: The interrupt occurs every minute.
- Hourly: The interrupt occurs every hour.
- Daily: The interrupt occurs every day at a specified time (hour and minute).
- Weekly: The interrupt occurs every week at a specified time on a specified day of the week (for example, every Tuesday at 4:30 in the afternoon).
- Monthly: The interrupt occurs every month at a specified time on a specified day of the month. The day number must be between 1 and 28, inclusive.
- Every end of month: The interrupt occurs on the last day of every month at a specified time.
- Yearly: The interrupt occurs every year on the specified date (month and day). You cannot specify a date of February 29.

Table 4-11 Start information for a time of day event OB

Input	Data type	Description
CaughtUp	Bool	OB call is caught up because time was set forward
SecondTime	Bool	OB call is started a second time because time was set backward

4.4.5.11 Synchronous cycle OB

IRT (Isochronous Realtime) is a transmission method that can synchronize PROFINET devices with very high accuracy. You can operate I/O modules in distributed PROFINET I/O systems isochronously, for example, ET 200SP and ET 200MP distributed I/O systems. Both the I/O modules and the interface modules of the I/O systems must support isochronous mode.

The Synchronous cycle interrupt OB uses an isochronous mode interrupt to trigger the start of subprograms isochronously to the PROFINET send clock.

Refer to Cycle time and communication load (Page 80) for considerations of how higher priority OBs affect the main scan cycle.

Table 4-12 Start information for Synchronous cycle OB

Input	Data type	Meaning
Initial_Call	BOOL	TRUE = the first call of this OB during transition from STOP to RUN
PIP_Input	BOOL	Always FALSE. The program must call the SYNC_PI instruction to update the corresponding process image partition of the inputs.
PIP_Output	BOOL	Always FALSE. The program must call the SYNC_PO instruction to update the corresponding process image partition.
IO_System	USINT	Number of the distributed I/O system triggering the interrupt
Event_Count	INT	• = n: Number of lost cycles • = -1: An unknown number of cycles has been lost (for example, because cycle has changed)
SyncCycleTime	LTIME	Configured cycle time of the Synchronous cycle OB

4.4.5.12 Status OB

Status OBs execute if a PNIO slave triggers a status interrupt. This might be the case if a component (module or rack) of a PNIO slave changes its operating mode, for example from RUN to STOP.

Status events

For detailed information on events that trigger a status interrupt, refer to the manufacturer's documentation for the PNIO device.

Table 4-13 Start information for status OB

Input	Data type	Description
LADDR	HW_IO	Hardware identifier
Slot	UInt	Slot number
Specifier	Word	Alarm specifier

4.4.5.13 Update OB

Update OBs execute if a PNIO slave triggers an update interrupt.

Update events

For detailed information on events that trigger an update interrupt, refer to the manufacturer's documentation for the PNIO slave.

Table 4-14 Start information for update OB

Input	Data type	Description
LADDR	HW_IO	Hardware identifier
Slot	UInt	Slot number
Specifier	Word	Alarm specifier

4.4.5.14 Profile OB

Profile OBs execute if a DPV1 or PNIO slave triggers a profile-specific interrupt.

Profile events

For detailed information on events that trigger a profile interrupt, refer to the manufacturer's documentation for the DPV1 or PNIO slave.

Table 4-15 Start information for profile OB

Input	Data type	Description
LADDR	HW_IO	Hardware identifier
Slot	UInt	Slot number
Specifier	Word	Alarm specifier

4.4.5.15 MC-Servo and MC-Interpolator OB

STEP 7 creates the read-only MC-Servo and MC-Interpolator OBs automatically when you create a motion technology object and set the drive interface to be "Analog drive connection" or "PROFIDrive". You do not need to edit any OB properties or create this OB directly. The CPU uses these OBs for closed loop control. Refer to the STEP 7 Information System for further details.

The MC Servo OB uses a system-defined PIP with the name "PIP OB Servo".

Table 4-16 Start information for MC-Servo OB

Input	Data type	Description
Initial_Call	BOOL	TRUE indicates first call of this OB on transition from STOP to RUN
PIP_Input	BOOL	TRUE indicates the associated process image input is up to date.
PIP_Output	BOOL	TRUE indicates that the CPU transferred the associated process image output to the outputs in good time after the last cycle.
IO_System	USINT	Number of the distributed I/O system triggering the interrupt
Event_Count	INT	n: number of lost cycles -1: unknown number of cycles lost (for example, because cycle has changed)
Synchronous	BOOL	TRUE: The MC-Servo [OB91] is called synchronously with a bus system

Table 4-17 Start information for MC-Interpolator OB

Input	Data type	Description
Initial_Call	BOOL	TRUE indicates first call of this OB on transition from STOP to RUN
PIP_Input	BOOL	TRUE indicates the associated process image input is up to date.
PIP_Output	BOOL	TRUE indicates that the CPU transferred the associated process image output to the outputs in good time after the last cycle.
IO_System	USINT	Number of the distributed I/O system triggering the interrupt
Event_Count	INT	n: number of lost cycles -1: unknown number of cycles lost (for example, because cycle has changed)
Reduction	UInt	Reduction ratio of MC-Interpolator [OB92] to MC-Servo [OB91]

4.4.5.16 MC-PreInterpolator

The organization block MC_PreInterpolator [OB68] can be programmed and is called in the application cycle configured at the MC_Servo (Page 69). The MC_PreInterpolator is called directly before the MC_Interpolator .

Via the organization block, you can read out the configured application cycle.

Structure of the start information

Optimized start information:

Name	Data type	Meaning	
Initial_Call	BOOL	TRUE	In the first call of this OB after the CPU is switched on
PIP_Input	BOOL	TRUE	The associated process image input is up-to-date.
PIP_Output	BOOL	TRUE	The associated process image output was transferred to the outputs in time after the last cycle.
IO_System	USINT	Number of the distributed I/O system triggering the interrupt	
Event_Count	INT	n	Number of lost cycles
		-1	An unknown number of cycles has been lost, e.g. because the cycle has changed.
Reduction	UINT	Reduction ratio of MC_Interpolator to MC_Servo	
CycleTime	UDINT	Display of the application cycle configured for the MC_Interpolator in ns	

4.4.5.17 MC-PreServo

You can program the MC-PreServo OB to contain program logic for the STEP 7 program to execute directly before the MC-Servo OB executes.

MC-PreServo events

The MC-PreServo OB allows you to read out the configured application cycle information in microseconds.

Table 4-18 Start information for MC-PreServo OB

Input	Data type	Description
Initial_Call	BOOL	TRUE indicates first call of this OB on transition from STOP to RUN
PIP_Input	BOOL	TRUE indicates the associated process image input is up to date.
PIP_Output	BOOL	TRUE indicates that the CPU transferred the associated process image output to the outputs in good time after the last cycle.
IO_System	USINT	Number of the distributed I/O system triggering the interrupt
Event_Count	INT	n: number of lost cycles -1: unknown number of cycles lost (for example, because cycle has changed)
Synchronous	BOOL	Reserved
CycleTime	UDINT	Display of the application cycle configured for the MC-Servo OB in microseconds

4.4.5.18 MC-PostServo

You can program the MC-PostServo OB to contain program logic for the STEP 7 program to execute directly after the MC-Servo OB executes.

MC-PostServo events

The MC-PostServo OB allows you to read out the configured application cycle information in microseconds.

Table 4-19 Start information for MC-PostServo OB

Input	Data type	Description
Initial_Call	BOOL	TRUE indicates first call of this OB on transition from STOP to RUN
PIP_Input	BOOL	TRUE indicates the associated process image input is up to date.
PIP_Output	BOOL	TRUE indicates that the CPU transferred the associated process image output to the outputs in good time after the last cycle.
IO_System	USINT	Number of the distributed I/O system triggering the interrupt
Event_Count	INT	n: number of lost cycles -1: unknown number of cycles lost (for example, because cycle has changed)
Synchronous	BOOL	Reserved
CycleTime	UDINT	Display of the application cycle configured for the MC-Servo OB in microseconds

4.4.5.19 MC-LookAhead

STEP 7 creates the read-only MC_LookAhead OB automatically when you create a kinematics technology object. MC_LookAhead calculates the motion preparation of the kinematics technology object.

STEP 7 creates only one MC_LookAhead OB for all kinematics.

MC_LookAhead prepares the jobs of the job sequence in advance. In this way, less time is required for motion preparation in the MC_Interpolator organization block (Page 69) and you can set a shorter application cycle of the MC_Servo organization block (Page 69).

Downloading in RUN mode (Page 215) increases the CPU time required to prepare the motion jobs in the job sequence.

Block call and priority

MC_LookAhead is triggered by MC_Interpolator.

You configure the priority of the MC_LookAhead in the properties of the organization block under "General > Attributes > Priority". You can set values from 15 to 16 (default setting 15) for the priority. The priority of MC_LookAhead must be lower than the priority of MC_Interpolator.

Process response

Overflows can occur in the program scan cycle. Note the following response to overflows:

- The CPU tolerates a maximum of three consecutive MC_Interpolator overflows.
- The execution of an MC_Interpolator can only be interrupted by an MC_Servo call.

If more overflows or interruptions occur, the CPU transitions to STOP mode.

4.4.5.20 Programming error OB

The programming error OB executes if a programming error occurs during the processing of an instruction of the STEP 7 program. The programming error OB is processed according to its priority (Page 75).

You can handle programming errors locally using the GET_ERROR or GET_ERR_ID instructions within a program block. Otherwise, the CPU performs global error handling. With global error handling, a programming error event triggers the execution of the programming error OB, if it exists.

Table 4-20 Start information for the programming error OB

Name	Data type	Meaning
BlockNr	UINT	Number of the block in which the programming error occurred
Reaction	USINT	• 0: Ignore errors • 1: Replace incorrect value • 2: Skip command • 3: Programmed error handling, triggered by an array access with invalid index, for example, or by an error during parameter supply of an FC or FB
Fault_ID	BYTE	Error code (possible values: B#16#00, B#16#03, B#16#04, B#16#05, B#16#20, B#16#21, B#16#22, B#16#23, B#16#24, B#16#25, B#16#26, B#16#27, B#16#28, B#16#29, B#16#2C, B#16#30, B#16#31, B#16#32, B#16#33, B#16#34, B#16#35, B#16#38, B#16#39, B#16#3A, B#16#3B, B#16#3C, B#16#3D, B#16#3E, B#16#3F, B#16#50, B#16#51, B#16#75, B#16#76, B#16#A1, B#16#A2)
BlockType	USINT	Type of block in which the error occurred: • OB: 1 • FC: 2 • FB: 3 • SFC: 4 • SFB: 5 • DB: 6
Area	USINT	Area in which the incorrect access occurred: • Local data: B#16#40 to 4E, 86, 87, 8E, 8F, C0 to CE • Process image input: B#16#01 • Process image output: B#16#02 • Technology DB: B#16#04 • I: B#16#81 • Q: B#16#82 • M: B#16#83 • DB: B#16#84, 85, 8A, 8B
DBNr	DB_ANY	DB no. if AREA = DB or DI

Name	Data type	Meaning
Csg_OBNr	OB_ANY	OB number
Csg_Prio	USINT	OB priority
Width	USINT	Type of access during which the error occurred: • Bit: – B#16#00 for access to the standard memory area – B#16#01 for access to the optimized memory area • Byte: B#16#01 • Word: B#16#02 • DWord: B#16#03 • LWord: B#16#04

4.4.5.21 I/O access error OB

I/O access error OBs execute when the CPU executes an instruction that references I/O that does not exist.

You can handle I/O access errors locally using the GET_ERROR or GET_ERR_ID instructions within a program block. Otherwise, the CPU performs global error handling. With global error handling, an I/O access error event triggers the execution of the I/O access error OB, if it exists.

Table 4-21 Start information for the I/O access error OB

Name	Data type	Meaning
BlockNr	UINT	Number of the block in which the I/O access error occurred
Reaction	USINT	0: Ignore error, 1: Replace incorrect value, 2: Skip command
Fault_ID	BYTE	Error code: • B#16#42: I/O access error, reading • B#16#43: I/O access error, writing
BlockType	USINT	Type of block in which the error has occurred: • OB: 1 • FC: 2 • FB: 3 • SFC: 4 • SFB: 5 • DB: 6
Area	USINT	Identifier for the range in which the incorrect access occurred: • B#16#01: Direct access to input • B#16#02: Direct access to output • B#16#81: Access to process image input • B#16#82: Access to process image output
DBNr	DB_ANY	not user-relevant

Name	Data type	Meaning
Csg_OBNr	OB_ANY	OB number causing the I/O access error
Csg_Prio	USINT	OB priority that causes the I/O access error
Width	USINT	Type of access during which the error occurred: • Bit: B#16#00 • Byte: B#16#01 • Word: B#16#02 • DWord: B#16#03 • LWord: B#16#04

4.4.5.22 Event execution priorities and queuing

Events control CPU processing. An event triggers an interrupt OB to be executed. You can specify the interrupt OB for an event during the creation of the block, during the device configuration, or with an ATTACH or DETACH instruction. Some events happen on a regular basis like the program cycle or cyclic events. Other events happen only a single time, like the startup event and time delay events. Some events happen when the hardware triggers an event, such as an edge event on an input point or a high speed counter event. Events like the diagnostic error and time error event only happen when an error occurs. The event priorities and queues are used to determine the processing order for the event interrupt OBs.

The CPU processes events in order of priority where 1 is the lowest priority and 26 is the highest priority. You can assign a priority class to an OB in the attributes of the OB properties.

Interruptible OBs

OBs (Page 59) execute in priority order of the events that trigger them.

If an OB is executing and a higher priority event occurs before the OB completes its execution, the running OB is interrupted to allow the higher-priority event OB to run. The higher-priority event runs, and at its completion, the OB that was interrupted continues. When multiple events occur while an interruptible OB is executing, the CPU processes those events in priority order.

Consider the case where interrupt events trigger a cyclic OB and a time delay OB. In this example, the time delay OB (OB 201) has no process image partition assignment (Page 54) and executes at priority 4. The cyclic OB (OB 200) has a process image partition assignment of PIP1 and executes at priority 2. The following illustration shows interruptible OB execution mode:

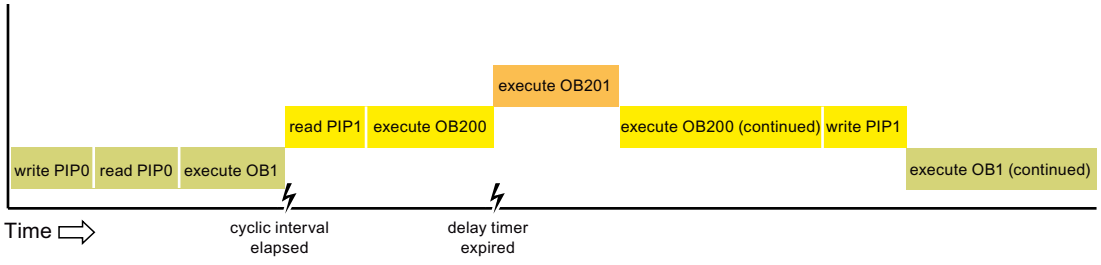
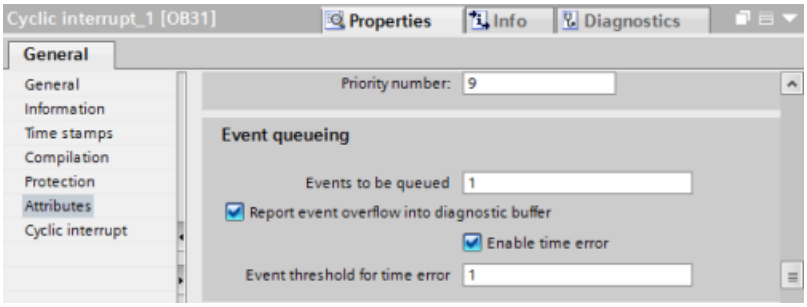


Figure 4-1 Interruptible OB execution

Understanding event execution priorities and queuing

The CPU limits the number of pending (queued) events from a single source, using a different queue for each event type. Upon reaching the limit of pending events for a given event type, the next event is lost. You can use a time error interrupt OB (Page 63) to respond to queue overflows.

Note that STEP 7 allows you to configure some specific event queueing parameters for the Cyclic interrupt OB and the Time of day OB.



For further information on CPU overload behavior and event queueing, refer to the "TIA Portal Information System > Editing devices and networks > Configuring devices and networks > Creating configurations > Configuring automation systems > Functional description of S7-1500 CPUs > Basics of program execution > CPU overload behavior" topic. The TIA Portal Information System does not have a specific S7-1200 G2 topic on overload behavior and event queueing.

Each CPU event has an associated priority. In general, the CPU services events in order of priority (highest priority first). The CPU services events of the same priority on a "first-come, first-served" basis.

Table 4-22 OB events

Event	Quantity allowed	Default OB priority
Program cycle	1 program cycle event[1] Multiple OBs allowed	1
Startup	1 startup event [1] Multiple OBs allowed	1
Time delay	Up to 20 time events 1 OB per event	OB 20: 3 OB 21: 4 OB 22: 5 OB 23: 6 OB 123 to OB 32767: 3
Cyclic interrupt	Up to 20 events 1 OB per event	8 to 17
Hardware interrupt	Up to 50 hardware interrupt events[2] 1 OB per event, but you can use the same OB for multiple events	16
Time error	1 event (only if configured)[3]	22
Diagnostic error	1 event (only if configured)	5
Pull or plug of modules	1 event	6
Rack or station failure	1 event	6
Synchronous cycle	1 event	21
Time of day	Up to 20 events	2
Status	1 event	4
Update	1 event	4
Profile	1 event	4
MC-Servo	1 event	26
MC-Interpolator	1 event	24
MC-PreServo	1 event	Same priority as MC-Servo
MC-PostServo	1 event	Same priority as MC-Servo
MC-PreInterpolator	1 event	Same priority as MC-Interpolator

Event	Quantity allowed	Default OB priority
MC-Lookahead	1 event	15
Programming error[4]	1 event	7
I/O access error[5]	1 event	7

1 The startup event and the program cycle event never occur at the same time because the startup event runs to completion before the program cycle event starts.

2 You can have more than 50 hardware interrupt event OBs if you use the DETACH and ATTACH instructions.

3 You can configure the CPU to stay in RUN if the scan cycle exceeds the maximum scan cycle time or you can use the RE_TRIGR instruction to reset the cycle time. However, the CPU goes to STOP mode the second time that one scan cycle exceeds the maximum scan cycle time.

4 Programming errors enable the program block to handle errors with GET_ERROR and GET_ERROR_ID within a program block. In the absence of these instructions, the CPU uses global error handling.

5 The CPU logs the first direct I/O read/write error in the diagnostics buffer and stays in RUN mode. You can access the error cause using the GET_ERROR_ID instruction.

In addition, the CPU recognizes other events that do not have associated OBs. The following table describes these events and the corresponding CPU actions:

Table 4-23 Additional events

Event	Description	CPU action
Max cycle time error	CPU exceeds the configured cycle time twice	The CPU logs the error in the diagnostics buffer and transitions to STOP mode.
Peripheral access error	I/O error during process image update	The CPU logs the first occurrence in the diagnostics buffer and stays in RUN mode.

Interrupt latency

The interrupt event latency (the time from notification of the CPU that an event has occurred until the CPU begins execution of the first instruction in the OB that services the event) is approximately 200 µsec, provided that a program cycle OB is the only event service routine active at the time of the interrupt event.

4.4.6 Monitoring and configuring the cycle time

The cycle time is the time that the CPU operating system requires to execute the cyclic phase of the RUN mode. The CPU provides two methods of monitoring the cycle time:

- Maximum scan cycle time
- Minimum scan cycle time

Scan cycle monitoring begins after the startup event is complete. Configuration for this feature appears under the "Device Configuration" for the CPU under "Cycle".

The CPU monitors the scan cycle. If the scan cycle time exceeds the configured maximum scan cycle time, the CPU generates an error and responds as follows:

- If the user program includes a time error interrupt OB (Page 63), then the CPU executes it.
- If the user program does not include a time error interrupt OB, then the time error event generates a diagnostic buffer entry. The CPU behavior is determined by the following:
  - If a time error interrupt OB has never been downloaded to the CPU, the CPU ignores the first scan timeout condition and remains in RUN mode. If a second scan timeout condition occurs in the same program scan (two times the maximum cycle time value), the CPU generates a diagnostic buffer entry and transitions to STOP mode.
  - If the time error interrupt OB has previously been downloaded, but has since been deleted, the CPU transitions to STOP mode if a time error event occurs, because the CPU cannot find the time error OB.

The RE_TRIGR instruction (re-trigger cycle time monitoring) allows you to reset the timer that measures the cycle time. If the elapsed time for the current program cycle execution is less than ten times the configured maximum scan cycle time, the RE_TRIGR instruction retriggers the cycle time monitoring and returns with ENO = TRUE. If not, the RE_TRIGR instruction does not retrigger the cycle time monitoring. It returns ENO = FALSE.

Typically, the scan cycle executes as fast as it can and the next scan cycle begins as soon as it completes. Depending upon the user program and communication tasks, the time period for a scan cycle can vary from scan to scan. To eliminate this variation, the CPU supports an optional minimum scan cycle time. By default, the minimum scan cycle time is enabled and is 1ms. When enabled, the CPU delays after the execution of the program cycle OBs until the minimum scan cycle time elapses before repeating the program cycle.

In the event that the CPU completes the normal scan cycle in less time than the specified minimum cycle time, the CPU spends the additional time of the scan cycle performing runtime diagnostics and/or processing communication requests (Page 80).

In the event that the CPU does not complete the scan cycle in the specified minimum cycle time, the CPU completes the scan normally (including communication processing) and does not create any system reaction as a result of exceeding the minimum scan time. The following table defines the ranges and defaults for the cycle time monitoring functions:

Table 4-24 Range for the cycle time

Cycle time	Range (ms)	Default
Maximum scan cycle time[1]	1 to 6000	150 ms
Minimum scan cycle time[2]	1 to maximum scan cycle time	1 ms

[1] The maximum scan cycle time is always enabled. Configure a cycle time between 1 ms to 6000 ms. The default is 150 ms.

[2] The minimum scan cycle time is 1 ms by default. If required, configure a cycle time between 1 ms and the maximum scan cycle time.

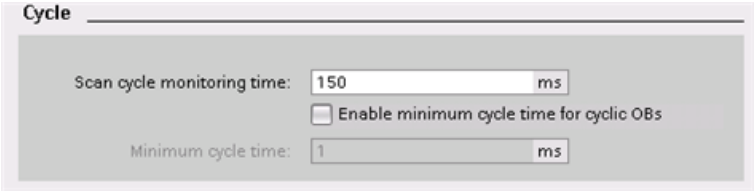
NOTE

To run as fast as possible, deselect "Enable minimum cycle time for cyclic OBs" under "Cycle > Cycle monitoring time [ms]" in Device configuration.

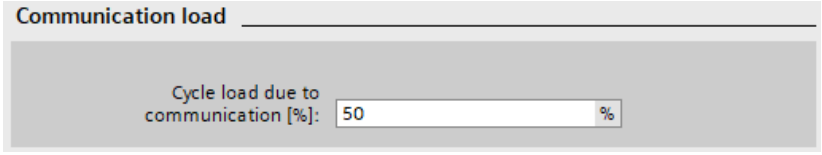
4.4.7 Cycle time and communication load

You use the CPU properties in the Device configuration to configure the following parameters:

- Cycle: You can enter a maximum scan cycle monitoring time. You can also enable and enter a minimum scan cycle time.



- Communication load: You can configure a percentage of the time to be dedicated for communication tasks.



NOTE

Communication impact on scan cycle

Using OBs with a higher priority than the main scan cycle can cause a performance strain on the execution cycle of the CPU. To mitigate this issue, reduce the Communication load from the default setting of 50% to a lower value. For more information about cycle and response times, see SIMATIC S7-1500, S7-1500R/H, ET 200SP, ET 200pro Cycle and response times (https://support.industry.siemens.com/cs/us/en/view/59193558/158758826123).

NOTE

Communication priority

Communication tasks have a priority of 15. CPU events with a priority of 16 or higher can interrupt communication processing. Interrupts from other events can negatively affect communication processing during the scan cycle. You can adjust the "Cycle load due to communication" percentage to increase the portion of the scan cycle dedicated to communication processing.

For more information about the scan cycle, see Execution of the user program (Page 54)

4.4.8 CPU memory

4.4.8.1 Memory management

The CPU provides the following memory areas to store the user program, data, and configuration:

- Load memory is non-volatile storage for the user program, data and configuration. When you download a project to the CPU, the CPU first stores the program in the Load memory area. This area is located either in a SIMATIC memory card (if present) or in the CPU. The CPU maintains this non-volatile memory area through a power loss. The memory card supports a larger storage space than that built-in to the CPU.
- Work memory is volatile storage for some elements of the user project while executing the user program. The CPU copies some elements of the project from load memory into work memory. This volatile area is lost when power is removed and is restored by the CPU when power is restored.
- Retentive memory is non-volatile storage for a limited quantity of work memory values. The CPU uses the retentive memory area to store the values of selected user memory locations during power loss. When a power down or power loss occurs, the CPU restores these retentive values upon power up.

The size of the user program, data, and configuration is limited by the available load memory and work memory in the CPU.

To display the memory usage for a compiled program block, right-click the block in the "Program blocks" folder in the STEP 7 project tree and select "Properties" from the context menu. The Compilation properties display the load memory and work memory for the compiled block.

To display the memory usage for the online CPU, double-click "Online and diagnostics" in STEP 7, expand "Diagnostics", and select "Memory".

Retentive memory

You can avoid data loss after power failure by marking certain data as retentive. The CPU allows you to configure the following data as retentive:

- Bit memory (M): You can define the size of retentive memory for bit memory in the PLC tag table or in the assignment list. Retentive bit memory always starts at MB0 and runs consecutively up through a specified number of bytes. Specify this value from the PLC tag table or in the assignment list by clicking the "Retain" toolbar icon. Enter the number of M bytes to retain starting at MB0.

  Note: You can display an assignment list for bit memory (M) by selecting the CPU in the project tree and selecting the **Tools > Assignment list** menu command.
- Tags of a function block (FB): If an FB is of type "Optimized block access", then the interface editor for this FB includes a "Retain" column. In this column, you can select either "Retain", "Non-retain", or "Set in IDB" individually for each tag. When you place such an FB in the program, the instance DB that corresponds to the FB includes this "Retain" column as well. You can only change the retentive state of a tag from within the instance DB interface editor if you selected "Set in IDB" (Set in instance data block) in the Retain selection for the tag in the optimized FB.

  If an FB is **not** of type "Optimized block access", then the interface editor for this FB does not include a "Retain" column. When you place such an FB in the program, the instance DB

that corresponds to the FB does, however, include a "Retain" column that is available for edit. In this case, selecting the "Retain" option for any tag results in the selection of **all** tags. Similarly, deselecting the option for any tag results in the deselection of **all** tags.

To view or modify whether an FB is optimized, open the properties of the FB and select the attributes.

- Tags of a global data block: If you select "Optimized block access" for the attributes in the properties of the data block, you can set each tag to be retentive or not. If you do not select "Optimized block access", then all of the data block tags have the same state. The tags are either all retentive or all non-retentive.

The technical specifications for the CPUs state the retentive data allocation. The STEP 7 project version can alter the amount of retentive memory. From the PLC tag table in STEP 7 or the assignment list, click the "Retain" toolbar icon to see how much memory is available.

4.4.8.2 Notes about retentive memory

NOTE

Downloading a program does not clear or make any changes to existing values in retentive memory. If you want to clear retentive memory before a download, then reset your CPU to factory settings prior to downloading the program.

NOTE

When power failure occurs, the CPU switches off power to all signal modules and signal boards. This ensures that the CPU has sufficient power to save retentive data to non-volatile memory.

4.4.8.3 System and clock memory

Use the CPU properties to enable bytes for "system memory" and "clock memory". Your program logic can reference the individual bits of these functions by their tag names.

The CPU initializes these bytes on the transition from STOP mode to STARTUP mode. The bits of the clock memory change synchronously to the CPU clock throughout the STARTUP and RUN modes.

⚠ WARNING

Risks with overwriting the system memory or clock memory bits

Overwriting the system memory or clock memory bits can corrupt the data in these functions and cause your user program to operate incorrectly. Because both the clock memory and system memory are unreserved in M memory, instructions or communications can write to these locations and corrupt the data.

Avoid writing data to these locations to ensure the proper operation of these functions, and always implement an emergency stop circuit for your process or machine.

Incorrect program operation can cause damage to equipment, severe injury, or death.

System memory

You can assign one byte in M memory for system memory. The byte of system memory provides the following four bits that can be referenced by your user program by the following tag names:

- First cycle: (Tag name "FirstScan") bit is set to1 for the duration of the first scan after the startup OB finishes. (After the execution of the first scan, the "first scan" bit is set to 0.)
- Diagnostics status changed: (Tag name: "DiagStatusUpdate") is set to 1 for one scan after the CPU logs a diagnostic event. Because the CPU does not set the "DiagStatusUpdate" bit until the end of the first execution of the program cycle OBs, your user program cannot detect if there has been a diagnostic change either during the execution of the startup OBs or the first execution of the program cycle OBs.
- Always 1 (high): (Tag name "AlwaysTRUE") bit is always set to 1.
- Always 0 (low): (Tag name "AlwaysFALSE") bit is always set to 0.

System memory bits have specific meanings, as shown in the table below:

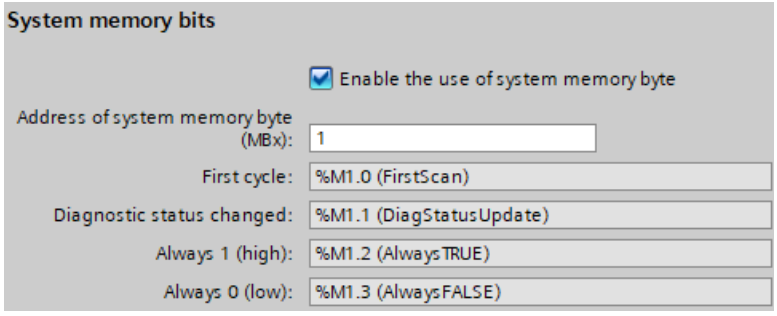


Table 4-25 System memory

7	6	5	4	3	2	1	0
Reserved Value 0				Always off Value 0	Always on Value 1	Diagnostic status indicator • 1: Change • 0: No change	First scan indicator • 1: First scan after startup • 0: Not first scan

Clock memory

You can assign one byte in M memory for clock memory. Each bit of the byte configured as clock memory generates a square wave pulse on the corresponding M memory bit. The byte of clock memory provides 8 different frequencies, from 0.5 Hz (slow) to 10 Hz (fast). You can use these bits as control bits, especially when combined with edge instructions, to trigger actions in the user program on a cyclic basis.

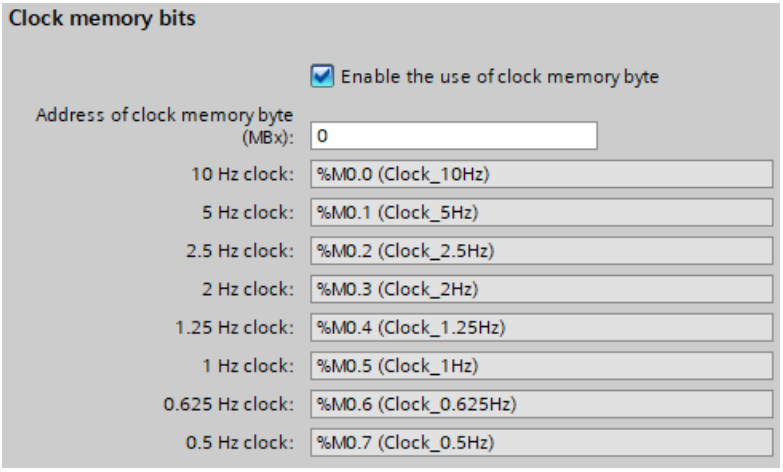


Table 4-26 Clock memory

Bit number	7	6	5	4	3	2	1	0
Period (s)	2.0	1.6	1.0	0.8	0.5	0.4	0.2	0.1
Frequency (Hz)	0.5	0.625	1	1.25	2	2.5	5	10

Because clock memory runs asynchronously to the CPU cycle, the status of the clock memory can change several times during a long cycle.

4.4.9 Diagnostics buffer

The CPU supports a diagnostics buffer that contains an entry for each diagnostic event. Each entry includes a date and time the event occurred, an event category, and an event description. The entries are displayed in chronological order, with the most recent event at the top. When the log is full (500 events), a new event replaces the oldest event in the log. If the CPU loses power, the diagnostics buffer retains the 100 most recent diagnostic events.

The following types of events are recorded in the diagnostics buffer:

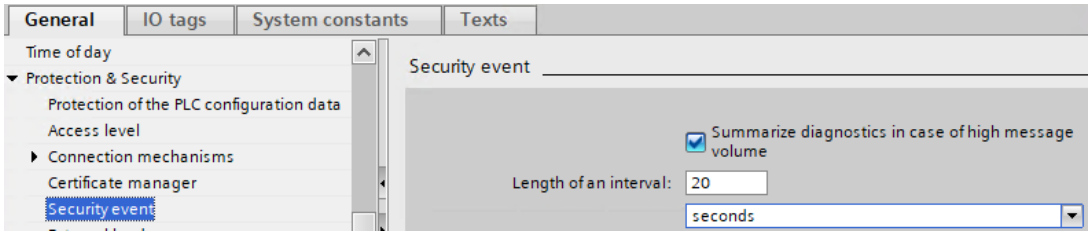
- Each system diagnostic event; for example, CPU errors and module errors
- Each state change of the CPU (each power up, each transition to STOP, each transition to RUN)
- Each user diagnostic alarm generated by the Gen_UsrMsg instruction.

To access the diagnostics buffer, you must be online. From the "Online & diagnostics (Page 206)" view, locate the diagnostics buffer under "Diagnostics > Diagnostics buffer".

Reducing the number of security diagnostic events

Some security events generate repeated entries in the diagnostics buffer. These messages can fill up the diagnostics buffer and potentially obscure other event messages. You can

configure the PLC to limit the number of diagnostic messages from security events. You make selections in the device configuration of the CPU based on the time interval in which you want to suppress recurring messages:



If you choose to summarize security events within a time interval, you have the choice of setting a time interval in seconds, minutes, or hours, and a numerical value in the range 1 .. 255.

If you choose to restrict security events, you will be restricting these types of events:

- Going online with the correct or incorrect password
- Manipulated communications data detected
- Manipulated data detected on memory card
- Manipulated firmware update file detected
- Changed protection level (access protection) downloaded to the CPU
- Password legitimization restricted or enabled (by instruction or CPU display)
- Online access denied due to the possible number of simultaneous access attempts being exceeded
- Timeout when an existing online connection is inactive
- Logging in to the Web server with the correct or incorrect password

4.4.10 Program alarms

The S7-1200 G2 allows you to create, edit, and monitor Program alarms in your STEP 7 project. These alarms deliver error messages or notifications about the PLC program running on your CPU.

From your STEP 7 project's Device configuration, select the "Diagnostics" tab and then select the "Alarm display" tab to view a log of Program alarms and their associated information. You can also configure Program alarms to display and be acknowledgeable in an HMI.

You can edit existing Program alarms in the Project tree under "PLC supervisions and alarms".

NOTE

The S7-1200 G2 CPU does not support supervisions.

See the following TIA Portal Information System topics for more detailed information on creating and editing Program alarms:

- "Creating and editing alarms (S7-1500)"
- "Program_Alarm: Generate program alarm with associated values (S7-1500)"
- "Program example for Get_Alarm & Ack_Alarms"

4.4.11 Time of day clock

The CPU supports a time-of-day clock. A super-capacitor supplies the energy required to keep the clock running during times when the CPU is powered down. The super-capacitor charges while the CPU has power. After the CPU has been powered up at least 24 hours, then the super-capacitor has sufficient charge to keep the clock running for typically 20 days.

STEP 7 sets the time-of-day clock to system time, which has a default value out of the box or following a factory reset. To utilize the time-of-day clock, you must set it. Timestamps such as those for diagnostics buffer entries, data log files, and data log entries, are based on the system time. You set the time of day from the "Set time of day" function (Page 206) in the "Online & diagnostics" view of the online CPU. STEP 7 then calculates the system time from the time you set plus or minus the Windows operating system offset from UTC (Coordinated Universal Time). Setting the time of day to the current local time produces a system time of UTC if your Windows operating system settings for time zone and daylight savings time correspond to your locale.

⚠ WARNING

Risk of attacker accessing your networks through open interfaces

If an attacker can access your networks through open interfaces, such as software like STEP 7, the SIMATIC Automation Tool, or through an HMI, the attacker can possibly disrupt control of your process by shifting the CPU system time.

The CPU supports "time of day" interrupts and clock instructions that depend upon accurate CPU system time. You must restrict access to the CPU by enabling access control and disabling the "Anonymous" user. Failure to do so can cause a security breach that allows an unknown user to disrupt control of your process by shifting the CPU system time.

Disruptions to process control can possibly cause death, severe injury, or property damage.

For security information and recommendations, see the "Operational Guidelines" white paper on the Siemens Industrial Cybersecurity Website.

STEP 7 includes instructions (Page 125) to read and write the system time (RD_SYS_T and WR_SYS_T), to read the local time (RD_LOC_T), and to set the time zone (SET_TIMEZONE). The RD_LOC_T instruction calculates local time using the time zone and daylight saving time offsets that you set in the "Time of day" configuration in the general properties of the CPU (Page 114). These settings enable you to set your time zone for local time, optionally enable daylight saving time, and specify the start and end dates and times for daylight saving time. You can also use the SET_TIMEZONE instructions to configure these settings.

NOTE

Time zone differences

If you set the time of day clock and the time zone of your programming device is different from the time zone you configured in the device configuration for your CPU (Page 114), then you might see unexpected timestamps for items such as the following:

- Diagnostic buffer entries
- Data log files
- Entries in data logs

See also

White papers and Guidelines: Operational guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html)

4.4.12 Data storage, memory areas, I/O and addressing

4.4.12.1 Accessing the data of the CPU

STEP 7 facilitates symbolic programming. You can create symbolic names or "tags" for I/O and memory. To use these tags in your user program, enter the tag name for the instruction parameter.

The CPU provides several options for storing data:

- Global memory: The CPU provides a variety of specialized memory areas, including inputs (I), outputs (Q) and memory (M). This memory is accessible by all code blocks without restriction.
- PLC tag table: You can enter symbolic names in the STEP 7 PLC tag table for specific memory locations. These tags are global to the STEP 7 program and allow programming with names that are meaningful for your application.
- Data block (DB): You can include DBs in your user program to store data for the code blocks. The data stored persists when the execution of the associated code block comes to an end. A "global" DB stores data that can be used by all code blocks, while an instance DB stores data for a specific FB and is structured by the parameters for the FB.
- Temp memory: Whenever the program calls a code block, the CPU allocates temporary, or local, memory (L) to be used during the execution of the block. When the execution of the code block finishes, the CPU reallocates the local memory for the execution of other code blocks.

Each memory location has a unique address. Your user program uses these addresses to access the information in the memory location. References to the input (I) or output (Q) memory areas, such as I0.3 or Q1.7, access the process image. To immediately access the physical input or output, append the reference with ":P" (such as I0.3:P, Q1.7:P, or "Stop:P").

You can force values (Page 215) for some memory areas. Some memory areas are retentive (Page 81) or optionally retentive.

Table 4-27 Memory areas

Memory area	Description	Force	Retentive
I Process image input I_:P [1] (Physical input)	Copied from physical inputs at the beginning of the scan cycle	No	No
	Immediate read of the physical input points on the CPU, SB, and SM	Yes	No
Q Process image output Q_:P [1] (Physical output)	Copied to physical outputs at the beginning of the scan cycle	No	No
	Immediate write to the physical output points on the CPU, SB, and SM	Yes	No

[1] To immediately access (read or write) the physical inputs and physical outputs, append a ":P" to the address or tag (such as I0.3:P, Q1.7:P, or "Stop:P").

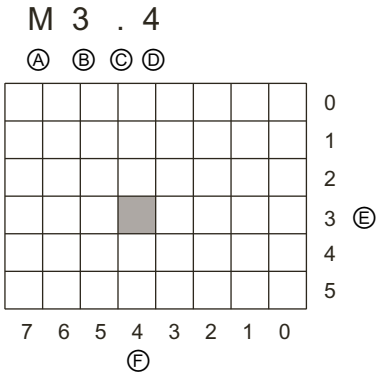
Memory area	Description	Force	Retentive
M Bit memory	Control and data memory	No	Yes (optional)
DB Data block	Data memory and also parameter memory for FBs	No	Yes (optional)
Temp memory	Temporary data for a block local to that block	No	No

[1] To immediately access (read or write) the physical inputs and physical outputs, append a ":P" to the address or tag (such as I0.3:P, Q1.7:P, or "Stop:P").

Each memory location has a unique address. Your user program uses these addresses to access the information in the memory location. The absolute address consists of the following elements:

- Memory area identifier (such as I, Q, or M)
- Size of the data to be accessed ("B' for Byte, "W" for Word, or "D" for DWord)
- Starting address of the data (such as byte 3 or word 3)

When accessing a bit in the address for a Boolean value, enter the memory area, the byte location, and the bit location for the data (such as I0.0, Q0.1, or M3.4).



A	Memory area identifier	E	Bytes of the memory area
B	Byte address: byte 3	F	Bits of the selected byte
C	Separator ("byte.bit")		
D	Bit location of the byte (bit 4 of 8)		

In the example, the memory area and byte address (M = bit memory area, and 3 = Byte 3) are followed by a period (".") to separate the bit address (bit 4).

4.4.12.2 Using absolute addressing to access CPU data

When using symbolic names for data (Page 87), you typically create tags either in the PLC tag table, a data block, or in the interface of an OB, FC, or FB. These tags include a name, data type, offset, and comment. Additionally, in a data block, you can specify a start value. You can use these tags when programming by entering the tag name at the instruction parameter.

Optionally, you can enter the absolute operand (memory area, size and offset) at the instruction parameter for most data types. The examples in the following sections show how to enter absolute operands. The % character is inserted automatically in front of the absolute

operand by the program editor. You can toggle the view in the program editor to one of these: symbolic, symbolic and absolute, or absolute.

You cannot use absolute addressing for the long data types (64-bit) such as LWORD, LINT, ULINT, LREAL, LTIME, LTOD, and LDT. You must use symbolic addressing for the long data types.

I (process image input): The CPU samples the peripheral (physical) input points just prior to the cyclic OB execution of each scan cycle (Page 54) and writes these values to the input process image. You can access the input process image as bits, bytes, words, or double words. Both read and write access is permitted, but typically, process image inputs are only read.

Table 4-28 Absolute addressing for I memory

Bit	I[byte address].[bit address]	I0.1
Byte, Word, or Double Word	I[size][starting byte address]	IB4, IW5, or ID12

By appending a ":P" to the address, you can immediately read the digital and analog inputs of the CPU, SB, SM or distributed module. The difference between an access using I_:P instead of I is that the data comes directly from the points being accessed rather than from the input process image. This I_:P access is referred to as an "immediate read" access because the data is retrieved immediately from the source instead of from a copy that was made the last time the input process image was updated.

Because the physical input points receive their values directly from the field devices connected to these points, you cannot write to these points. I_:P accesses are read-only, as opposed to I accesses which can be read or written to.

I_:P accesses are also restricted to the size of inputs supported by a single CPU, SB, or SM, rounded up to the nearest byte.

For example, if the inputs of a 4 DI / 4 DQ SB are configured to start at I4.0, then the input points can be accessed as I4.0:P, I4.1:P, I4.2:P, and I4.3:P or as IB4:P. Accesses to I4.4:P through I4.7:P are not rejected, but make no sense since these points are not used. Accesses to IW4:P and ID4:P are prohibited since they exceed the byte offset associated with the SB.

Accesses using I_:P do not affect the corresponding value stored in the input process image.

Table 4-29 Absolute addressing for I memory (immediate)

Bit	I[byte address].[bit address]:P	I0.1:P
Byte, Word, or Double word	I[size][starting byte address]:P	IB4:P, IW5:P, or ID12:P

Q (process image output): The CPU copies the values stored in the output process image to the physical output points. You can access the output process image in bits, bytes, words, or double words. Both read and write access is permitted for process image outputs.

Table 4-30 Absolute addressing for Q memory

Bit	Q[byte address].[bit address]	Q1.1
Byte, Word, or Double word	Q[size][starting byte address]	QB5, QW10, QD40

By appending a ":P" to the address, you can immediately write to the physical digital and analog outputs of the CPU, SB, SM or distributed module. The difference between an access using Q_:P instead of Q is that the data goes directly to the points being accessed in addition to the output process image (writes to both places). This Q_:P access is sometimes referred to

as an "immediate write" access because the data is sent immediately to the target point; the target point does not have to wait for the next update from the output process image.

Because the physical output points directly control field devices that are connected to these points, reading from these points is prohibited. That is, Q_:P accesses are write-only, as opposed to Q accesses which can be read or write.

Q_:P accesses are also restricted to the size of outputs supported by a single CPU, SB, or SM, rounded up to the nearest byte.

For example, if the outputs of a 4 DI / 4 DQ SB are configured to start at Q4.0, then the output points can be accessed as Q4.0:P, Q4.1:P, Q4.2:P, and Q4.3:P or as QB4:P. Accesses to Q4.4:P through Q4.7:P are not rejected, but make no sense since these points are not used. Accesses to QW4:P and QD4:P are prohibited since they exceed the byte offset associated with the SB.

Accesses using Q_:P affect both the physical output as well as the corresponding value stored in the output process image.

Table 4-31 Absolute addressing for Q memory (immediate)

Bit	Q[byte address].[bit address]:P	Q1.1:P
Byte, Word, or Double word	Q[size][starting byte address]:P	QB5:P, QW10:P or QD40:P

M (bit memory area): Use the bit memory area (M memory) for both control relays and data to store the intermediate status of an operation or other control information. You can access the bit memory area in bits, bytes, words, or double words. Both read and write access is permitted for M memory.

Table 4-32 Absolute addressing for M memory

Bit	M[byte address].[bit address]	M26.7
Byte, Word, or Double Word	M[size][starting byte address]	MB20, MW30, MD50

Temp (temporary memory): The CPU allocates the temp memory on an as-needed basis. The CPU allocates the temp memory for the code block and initializes the memory locations to 0 at the time when it starts the code block (for an OB) or calls the code block (for an FC or FB).

Temp memory is similar to M memory with one major exception: M memory has a "global" scope, and temp memory has a "local" scope:

- M memory: Any OB, FC, or FB can access the data in M memory, meaning that the data is available globally for all of the elements of the user program.
- Temp memory: The CPU restricts access to the data in temp memory to the OB, FC, or FB that created or declared the temp memory location. Temp memory locations remain local and different code blocks do not share temp memory, even when the code block calls another code block. For example: When an OB calls an FC, the FC cannot access the temp memory of the OB that called it.

The CPU limits memory as follows:

- 16 Kbytes temp (local) memory per block (OB/FB/FC)
- 64 Kbytes total temp (local) memory per event priority class.

You must consider each block's memory allocation and the nesting depth from the calling OB in planning memory usage.

You access temp memory by symbolic addressing only.

You can find out the amount of temp (local) memory that the blocks in your program use through the call structure in STEP 7. From the project tree select Program info and then select

the Call structure tab. You will see all of the OBs in your program and you can drill down to see the blocks that they call. For each block, you can see the local data allocation. You can also access the Call structure display from the STEP 7 **Tools > Call structure** menu command.

DB (data block): Use the DB memory for storing various types of data, including intermediate status of an operation or other control information parameters for FBs, and data structures required for many instructions such as timers and counters. You can access data block memory in bits, bytes, words, or double words. Both read and write access is permitted for read/write data blocks. Only read access is permitted for read-only data blocks.

Table 4-33 Absolute addressing for DB memory

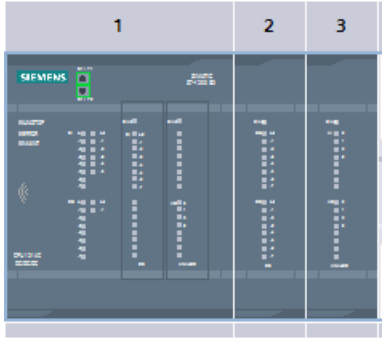
Bit	DB[data block number].DBX[byte address].[bit address]	DB1.DBX2.3
Byte, Word, or Double Word	DB[data block number].DB [size][starting byte address]	DB1.DBB4, DB10.DBW2, DB20.DBD8

NOTE

When you specify an absolute address in LAD or FBD, STEP 7 precedes this address with a "%" character to indicate that it is an absolute address. While programming, you can enter an absolute address either with or without the "%" character (for example %I0.0 or I.0). If omitted, STEP 7 supplies the "%" character.

In SCL, you must enter the "%" before the address to indicate that it is an absolute address. Without the "%", STEP 7 generates an undefined tag error at compile time

4.4.12.3 Addressing the local and expansion I/O



When you add a CPU and I/O boards or modules to your device configuration, STEP 7 automatically assigns input and output addresses. You can change the default addressing by selecting the address field in the device overview and entering new numbers.

- STEP 7 assigns digital inputs and outputs in groups of 8 points (1 byte), whether the module uses all the points or not.
- STEP 7 allocates analog inputs and outputs in groups of 4, where each analog point occupies 2 bytes.

The Device overview shows the I/O address assignments.

Device overview

...	Module	Slot	I address	Q address	Type
		0			
	G2_PLC_1	1			CPU 1214C DC/DC/DC
	DI 14/DQ 10_1	1 8	0...1	0...1	DI 14/DQ 10
	DI8 signal board (100 kHz)_1	1 9	4		DI8 signal board (100 kHz)
	AQ4 Signal board_1	1 10		80...87	AQ4 Signal board

		SM 1222 DQ16 x 24VDC_1	2		8...9	SM 1222 DQ16 x 24VDC
		SM 1233 AI4/AQ4_1	3	112...119	112...119	SM 1233 AI4/AQ4

This example represents the following configuration:

- CPU
- Signal board with 8 digital inputs
- Signal board with 4 analog outputs
- Signal module with 16 digital outputs
- Signal module with 4 analog inputs and 4 analog outputs

You can change I and Q addresses. STEP 7 assists you by preventing changes that are the wrong size or conflict with other addresses.

4.4.13 Processing of analog values

General purpose analog signal modules provide input signals or expect output values that represent either a voltage range or a current range. These ranges are as follows:

- Analog inputs: ±10 V, ±5 V, ±2.5 V, 0 to 20 mA, or 4 to 20 mA
- Analog outputs: ±10 V, 0 to 20 mA, or 4 to 20 mA

The values returned by the modules are integer values where 0 to 27648 represents the rated range for current, and -27648 to 27648 for voltage. Anything outside the range represents either an overflow or underflow. See the tables for analog input representation (Page 307) and analog output representation (Page 308) for details about the types of out-of-range values.

In your control program, you probably need to use these values in engineering units, for example to represent a volume, temperature, weight or other quantitative value. To do this for an analog input, you must first normalize the analog value to a real (floating point) value from 0.0 to 1.0. Then you must scale it to the minimum and maximum values of the engineering units that it represents. For values that are in engineering units that you need to convert to an analog output value, you first normalize the value in engineering units to a value between 0.0 and 1.0, and then scale it between 0 and 27648 or -27648 to 27648, depending on the range of the analog module. STEP 7 provides the NORM_X and SCALE_X instructions for this purpose. You can also use the CALCULATE instruction to scale the analog values.

Example: analog value processing

Consider, for example, an analog input that has a current range of 0 - 20 mA. The analog input module returns values in the range 0 to 27648 for measured values. For this example, consider that you are using this analog input value to measure a temperature range from 50 °C to 100 °C. A few sample values would have the following meanings:

Analog input value	Engineering units
0	50 °C
6192	62.5 °C
12384	75 °C
18576	87.5 °C
27648	100 °C

The calculation for determining engineering units from the analog input value in this example is as follows:

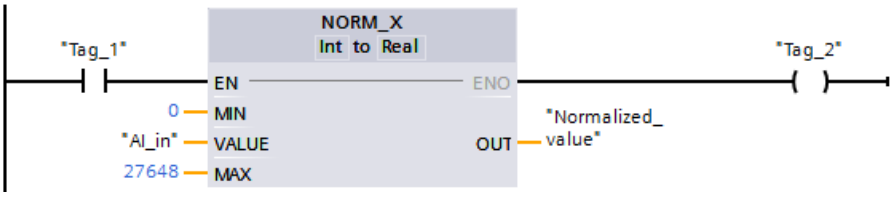
Engineering units value = 50 + (Analog input value) * (100 - 50) / (27648 - 0)

For the general case, the equation would be:

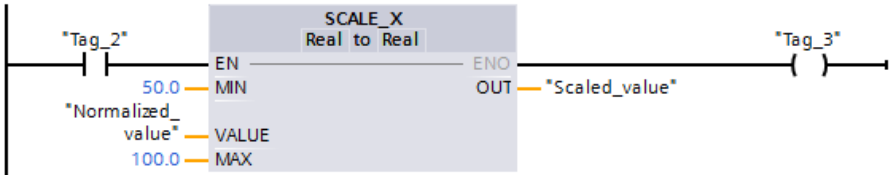
Engineering units value = (Low range of engineering units) +
(Analog input value) *
(High range of engineering units - Low range of engineering units) /
(Maximum analog input range - Minimum analog input range)

In PLC applications, the typical method is to normalize the analog input value to a floating point value between 0.0 and 1.0. Then, you would scale the resulting value to a floating point value in the range of your engineering units. For simplicity, the following LAD instructions use constant values for the ranges; you might actually choose to use tags:

Network 1



Network 2



4.4.14 Using a memory card

4.4.14.1 Memory cards

NOTE

The CPU supports SIMATIC memory cards (Page 333) for the following purposes:

- Empty memory card (Page 96)
- Transfer card (Page 96)
- Program card (Page 99)
- Firmware update card (Page 102)
- Card for protection of confidential PLC configuration data (Page 104)

You can use supported non-SIMATIC memory cards (Page 333) only for transferring the license conditions and copyrights OSS information (Page 106) to a memory card.

Transfer cards and program cards contain the code blocks, data blocks, technology objects, and the device configuration. Transfer cards and program cards do **not** contain, for example, force tables, watch tables, or PLC tag tables.

- Use a transfer card (Page 96) to copy a program to the internal load memory of the CPU without using STEP 7.
- Use an empty transfer card (Page 96) to recover a password-protected CPU when you have lost or forgotten the password (Page 106).
- Use a program card (Page 99) as external load memory for the CPU.

NOTE

Do not use the Windows formatter utility or any other formatting utility to reformat the memory card.

If a Siemens memory card is reformatted using the Microsoft Windows formatter utility, then the memory card will no longer be usable by any Siemens CPU.

4.4.14.2 Inserting a memory card in the CPU

NOTICE

Risks associated with electrostatic discharge

Electrostatic discharge can damage the memory card or the receptacle on the CPU. If damaged, the receptacle or memory card can malfunction or become inoperable.

To protect the memory card and receptacle from electrostatic discharge, do the following:

- Make contact with a grounded conductive pad or wear a grounded wrist strap when handling the memory card.
- Store the memory card in a conductive container.

Receptacle or memory card malfunction can result in property damage.

Check that the memory card is not write-protected. Slide the protection switch away from the "Lock" position.

The memory card is keyed for proper installation. Insert the memory card with the correct orientation.

If you insert a write-protected memory card into the CPU, STEP 7 displays a diagnostic message on the next power up, alerting you to that fact. The CPU powers up without failure, but instructions involving recipes or data logs, for example, return errors if the card is write-protected.

⚠ WARNING

Verify that the CPU is not running a process before inserting the memory card.

If you insert or remove a memory card of any type into a running CPU, the CPU restarts, resulting in diagnostic events, temporary loss of communication, and process disruption.

Before inserting or removing a memory card, always ensure that the CPU is not actively controlling a machine or process. Always install an emergency stop circuit for your application or process. Power off the CPU before inserting or removing a memory card.

Disruption of a running process can result in death, severe personal injury, and/or property damage.

NOTE

Do not insert program cards (Page 99) or transfer cards (Page 96) with S7-1200 projects into S7-1200 G2 CPUs.

S7-1200 projects are not compatible with version S7-1200 G2 CPUs. Inserting a memory card that is incompatible causes a CPU error.

If you do insert an invalid program card or transfer card, remove the card.

CPU behavior when you insert a memory card

When you insert a memory card in the CPU, the CPU performs the following steps:

1. Transitions to STOP mode (if not already in STOP mode) and restarts
2. Evaluates the card, and flashes the LEDs while evaluating
3. Performs actions based on the type of card:
   - Empty memory card (Page 96)
   - Transfer card (Page 96)
   - Program card (Page 99)
   - Firmware update card (Page 102)
   - Memory card for protecting confidential PLC configuration data (Page 104)
   - Memory card for copying license conditions and copyrights from the CPU (Page 106)

Procedure after card evaluation and processing

If the card is not an empty memory card (Page 96) or a program card (Page 99), power off the CPU and remove it.

After you remove the card, the CPU restarts and remains in STOP mode.

4.4.14.3 Empty memory card

An empty memory card does not have a job file (S7_JOB.S7S) or a SIMATIC folder (SIMATIC.S7S). The CPU behavior when you insert an empty memory card (Page 94) depends on the selection for "Disable copy from internal load memory to external load memory" in the "Protection & Security > External load memory" CPU properties (Page 114):

- If the check box is not selected, the CPU adds a job file. The CPU then copies internal load memory to external load memory (memory card) and erases internal load memory.
- If the check box is selected, the CPU does not create a program job file and it does not copy internal load memory to external load memory (memory card). It does not erase internal load memory.

If you insert a memory card that is not an empty memory card into the CPU, the configuration setting for "Disable copying from internal load memory to external load memory" has no effect on how the CPU evaluates the memory card.

4.4.14.4 Configuring the startup parameter of the CPU before copying the project to the memory card

When you copy a program to a transfer card or a program card, the program includes the startup parameter for the CPU (Page 114). Before copying the program to the memory card, always ensure that you have configured the operating mode for the CPU following a power-cycle. Select whether the CPU starts in STOP mode, RUN mode, or in the previous mode (prior to the power cycle).

4.4.14.5 Transfer card

NOTICE
Risks associated with electrostatic discharge Electrostatic discharge can damage the memory card or the receptacle on the CPU. If damaged, the receptacle or memory card can malfunction or become inoperable. To protect the memory card and receptacle from electrostatic discharge, do the following: • Make contact with a grounded conductive pad or wear a grounded wrist strap when handling the memory card. • Store the memory card in a conductive container. Receptacle or memory card malfunction can result in property damage.

Creating a transfer card

Configure the startup parameter of the CPU (Page 96) before copying a program to the transfer card.

To create a transfer card, follow these steps:

1. Insert an empty SIMATIC memory card that is not write-protected into an SD card reader/writer attached to your computer. (If the card is write-protected, slide the protection switch away from the "Lock" position.)

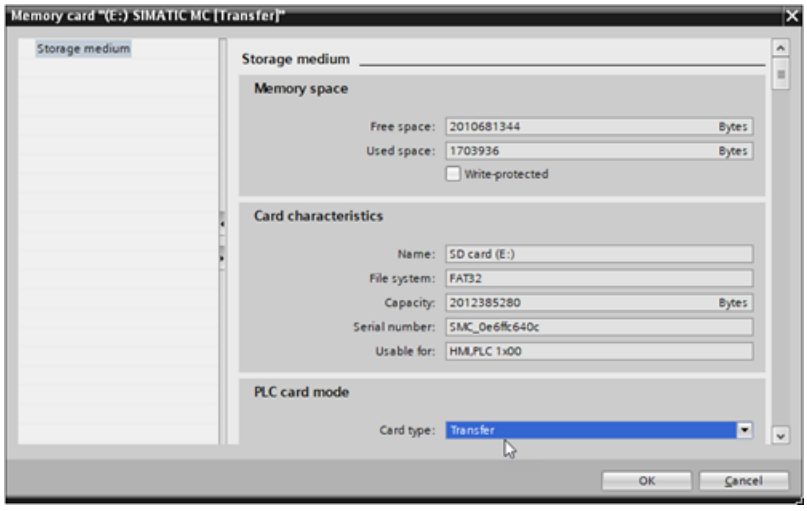
   If you are reusing a SIMATIC memory card that contains a user program, data logs, recipes, or a firmware update, you **must** delete the files before reusing the card. Use Windows File Explorer to display the contents of the memory card and delete the following files and folders if they exist:

   - S7_JOB.S7S
   - SIMATIC.S7S
   - FWUPDATE.S7S
   - DataLogs
   - Recipes
   - UserFiles

NOTICE
Do NOT delete the hidden files "__LOG__" and "crdinfo.bin" from the memory card. The "__LOG__" and "crdinfo.bin" files are required for the memory card. If you delete these files, you cannot use the memory card with the CPU.

2. In the Project tree (Project view), expand the "Card Reader/USB memory" folder and select your card reader. If you are creating an empty transfer card, you can go to Step 6.
3. Add the program by selecting the CPU in the Project tree and dragging the CPU to the memory card. Another method is to copy the CPU and paste it to the memory card. Copying the CPU to the memory card opens the "Load preview" dialog.
4. In the "Load preview" dialog, click the "Load" button to copy the CPU to the memory card.
5. When the dialog displays a message that the CPU (program) has been loaded without errors, click the "Finish" button.
6. Right-click the drive letter corresponding to the memory card and select "Properties" from the shortcut menu.

7. In the "Memory card" dialog, select "Transfer" from the "Card type" drop-down menu and click OK.



8. Remove the transfer card from the card reader.

Using a transfer card

WARNING

Risks when inserting a transfer card

Inserting a memory card causes the CPU to restart and evaluate the card, which can affect the operation of an online process or machine.

Before inserting a transfer card, ensure that the CPU is in STOP mode and your process is in a safe state.

Unexpected operation of a process or machine can result in death or injury to personnel and/or property damage.

To transfer the program to a CPU, insert the transfer card into the CPU (Page 94). At this point, the existing program is still in the CPU.

The CPU evaluates the memory card and copies the program to the internal load memory of the CPU.

When the MAINT LED flashes (yellow), the copy process is finished. Remove the transfer card.

The CPU then remains in STOP mode.

See also

Recovery from a lost password (Page 106)

4.4.14.6 Program card

NOTICE
Risks associated with electrostatic discharge Electrostatic discharge can damage the memory card or the receptacle on the CPU. If damaged, the receptacle or memory card can malfunction or become inoperable. To protect the memory card and receptacle from electrostatic discharge, do the following: • Make contact with a grounded conductive pad or wear a grounded wrist strap when handling the memory card. • Store the memory card in a conductive container. Receptacle or memory card malfunction can result in property damage.

Check that the memory card is not write-protected. Slide the protection switch away from the "Lock" position.

The memory card is keyed for proper installation. Insert the memory card with the correct orientation.

If you insert a write-protected memory card into the CPU, STEP 7 displays a diagnostic message on the next power up, alerting you to that fact. The CPU powers up without failure, but instructions involving recipes or data logs, for example, return errors if the card is write-protected.

Before you copy any program elements to the program card, delete any previously saved programs from the memory card.

Creating a program card

When used as a program card, the memory card is the external load memory of the CPU. If you remove the program card, the internal load memory of the CPU is empty. A program card includes the STEP 7 program and any data logs, recipes, or user files that belong to the program.

NOTE

If you insert an empty memory card into the CPU, the CPU copies the program and force values from internal memory to the memory card. After the copy has completed, the program in internal load memory is erased.

If you powered off the CPU before inserting the memory card, the CPU then goes to the configured startup mode (Page 96).

If you inserted the memory card without powering off, the CPU remains in STOP mode.

Always remember to configure the startup parameter of the CPU (Page 96) before copying a project to the program card. To create a program card, follow these steps:

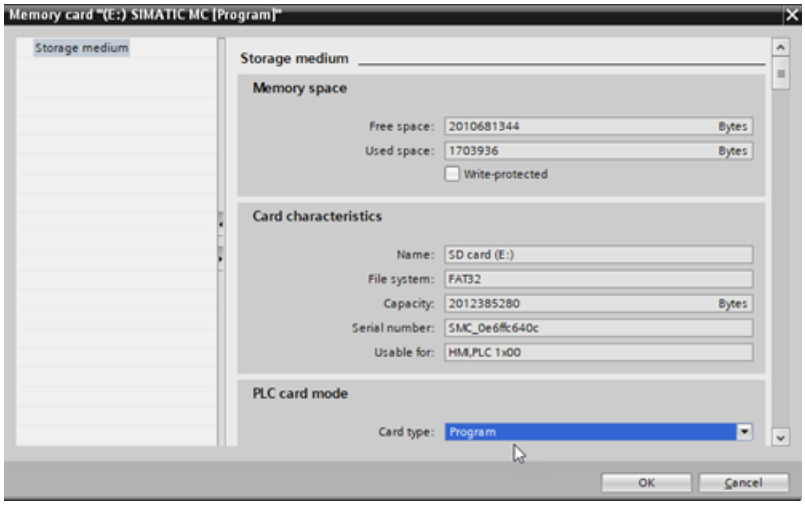
1. Insert an empty SIMATIC memory card that is not write-protected into an SD card reader/writer attached to your computer.

   If you are reusing a SIMATIC memory card that contains a user program, data logs, recipes, or a firmware update, you **must** delete the files before reusing the card. Use Windows File Explorer to display the contents of the memory card and delete the following files and folders if they exist:

   – S7_JOB.S7S
   – SIMATIC.S7S
   – FWUPDATE.S7S
   – DataLogs
   – Recipes
   – UserFiles

NOTICE
Do NOT delete the hidden files "__LOG__" and "crdinfo.bin" from the memory card. The "__LOG__" and "crdinfo.bin" files are required for the memory card. If you delete these files, you cannot use the memory card with the CPU.

2. In the Project tree (Project view), expand the "Card Reader/USB memory" folder and select the card reader.
3. Display the "Memory card" dialog by right-clicking the drive letter corresponding to the memory card in the card reader and selecting "Properties" from the context menu.
4. In the "Memory card" dialog, select "Program" from the Card type dropdown menu.



5. Add the program by selecting the CPU device (such as PLC_1 [CPU 1214C DC/DC/DC]) in the Project tree and dragging the CPU device to the memory card. (Another method is to copy the CPU device and paste it to the memory card.) Copying the CPU device to the memory card opens the "Load preview" dialog.

6. In the "Load preview" dialog, click the "Load" button to copy the CPU device to the memory card.
7. When the dialog displays a message that the download completed without errors, click the "Finish" button.

Using a program card as the load memory for a CPU

⚠ WARNING

Risks associated with inserting a program card

Use caution when inserting a program card while the CPU is in RUN mode. If you insert a program card into a CPU, the CPU restarts. Unexpected equipment operation can occur.

Ensure that the CPU is in STOP mode before inserting a program card.

Unexpected equipment operation can result in death, injury, and equipment damage.

To use a program card with a CPU, insert the program card (Page 94) into the CPU. The CPU evaluates the program card and erases the internal load memory of the CPU.

The program card must then remain in the CPU.

⚠ WARNING

Risks associated with removing a program card

If a program card is removed while the CPU is in RUN mode, the CPU restarts.

Use caution when removing a program card while the CPU is in RUN mode. Removing the program card removes the program from the CPU.

Unexpected equipment operation can occur resulting in death, injury, and equipment damage.

Service life of a SIMATIC memory card

The service life of a SIMATIC memory card depends on factors such as the following:

- Number of delete and write operations per memory block
- Number of bytes written
- External influences, such as ambient temperature

NOTE

Effect of write and delete operations on SIMATIC memory card service life

Write or delete operations, particularly repeated (cyclic) write/delete operations, reduce the service life of the SIMATIC memory card.

Cyclic execution of the following actions reduces the service life of the memory card depending on the number of write operations and data:

- Data Log Handling (for example, DataLogWrite)
- Recipe Handling (for example, RecipeExport)
- System Function Calls (SFCs) that write/delete to the file system (for example, WRIT_DBL, CREATE)
- System Function Blocks (SFBs) that write/delete to file system (for example, FileWriteC, FileDelete)
- Any other cyclic action that changes data on the persistent store (for example, Tracing, SET-TimeZone)

4.4.14.7 Firmware update card

You can use a SIMATIC memory card for performing a firmware update.

NOTE

You cannot update an S7-1200 CPU to S7-1200 G2 by firmware update.

Firmware updates are available on the Siemens Industry Online Support (https://support.industry.siemens.com/) Web site. From this Web site, navigate to "Downloads". From there, search for the specific type of module that you need to update.

Alternatively, you can access the downloads Web page (https://support.industry.siemens.com/cs/ww/en/ps/13639/dl) directly. Filter the downloads for S7-1200 G2 or a specific article number.

NOTICE

Risks associated with electrostatic discharge

Electrostatic discharge can damage the memory card or the receptacle on the CPU. If damaged, the receptacle or memory card can malfunction or become inoperable.

To protect the memory card and receptacle from electrostatic discharge, do the following:

- Make contact with a grounded conductive pad or wear a grounded wrist strap when handling the memory card.
- Store the memory card in a conductive container.

Receptacle or memory card malfunction can result in property damage.

You can also use one of these methods to perform a firmware update:

- Online and diagnostic tools of STEP 7 (Page 206)
- SIMATIC Automation Tool (https://support.industry.siemens.com/cs/ww/en/view/98161300)

Downloading and installing a firmware update

To download the firmware update to your memory card, follow these steps:

1. Insert an empty SIMATIC memory card that is not write-protected into an SD card reader/writer attached to your computer. If the card is write-protected, slide the protection switch away from the "Lock" position.

   You can reuse a SIMATIC memory card that contains a user program or another firmware update. To avoid any confusion, you should also delete files S7_JOB.S7S, SIMATIC.S7S, and FWUPDATE.S7S if they exist.

   NOTE

   Do NOT delete the hidden files "__LOG__" and "crdinfo.bin" from the memory card.

   The "__LOG__" and "crdinfo.bin" files are required for the memory card. If you delete these files, you cannot use the memory card with the CPU.

2. Select the zip file for the firmware update that corresponds to your module, and download it to your computer. Double-click the file, set the file destination path to be the root directory of the SIMATIC memory card, and start the extraction process. After the extraction is complete, the root directory (folder) of the memory card will contain a "FWUPDATE.S7S" directory and the "S7_JOB.S7S" file.

   NOTE

   Do not put multiple firmware updates for the same article number (MLFB) on your memory card. Putting multiple updates for the same article number on the memory card causes the firmware update to fail.

   You can put multiple firmware updates for different article (MLFB) numbers on a single memory card. This allows you to use a single memory card to update the firmware of multiple station hardware modules.

3. Safely eject the card from the card reader/writer.

Installing a firmware update

⚠ WARNING

Risks when installing firmware updates

Installing the firmware update causes the CPU to restart, which can affect the operation of an online process or machine.

Verify that the CPU is not actively running a process before installing the firmware update. Before inserting the memory card, always ensure that the CPU is offline and in a safe state.

Unexpected operation of a process or machine can result in death or injury to personnel and/or property damage.

To install the firmware update, insert the firmware update card into the CPU (Page 94).

After you insert the card, the firmware update starts. When the MAINT LED flashes (yellow), the firmware update has finished. Remove the firmware update card. A firmware update does not affect the STEP 7 program and device configuration.

During update, the firmware update procedure ignores UPD files that do not correspond to any station hardware modules. If you have multiple station hardware modules with the same article number (MLFB), the firmware update is installed on all of those modules. This allows you to create a master firmware update memory card to update all stations in your facility.

If you powered off the CPU before removing the memory card, the CPU then goes to the configured startup mode (Page 96).

If you removed the memory card without powering off, the CPU remains in STOP mode.

The Diagnostics buffer includes entries when firmware update attempts are made, whether successful or not. In the case of a failure, the Diagnostics buffer message provides an explanation for the failure. You can then easily scan the Diagnostics buffer for any unexpected anomalies.

4.4.14.8 Memory card for protecting confidential PLC configuration data

You can use a SIMATIC memory card to set or change the password for Protection of confidential PLC configuration data.

NOTICE
Risks associated with electrostatic discharge Electrostatic discharge can damage the memory card or the receptacle on the CPU. If damaged, the receptacle or memory card can malfunction or become inoperable. To protect the memory card and receptacle from electrostatic discharge, do the following: • Make contact with a grounded conductive pad or wear a grounded wrist strap when handling the memory card. • Store the memory card in a conductive container. Receptacle or memory card malfunction can result in property damage.

Risks associated with the decommissioning process

S7-1200 G2 CPUs do not support secure erasure of the memory card and internal flash. Therefore, during the decommissioning process, you must securely dispose of the CPU and memory card to prevent the loss of proprietary or confidential information.

How to create a memory card with the Protection of confidential PLC configuration data password

To create the memory card with this password, follow these steps:

1. Insert an empty SIMATIC memory card that is not write-protected into an SD card reader/writer attached to your computer. If the card is write-protected, slide the protection switch away from the "Lock" position.
   You can reuse a SIMATIC memory card that contains a user program or firmware update, but you must delete some of the files on the memory card. To reuse a memory card, you must delete the "S7_JOB.S7S" file before creating the Protection of confidential PLC configuration data file. Use Windows Explorer to display the contents of the memory card and to delete the "S7_JOB.S7S" file.

NOTICE
Do NOT delete the hidden files "__LOG__" and "crdinfo.bin" from the memory card. The "__LOG__" and "crdinfo.bin" files are required for the memory card. If you delete these files, you cannot use the memory card with the CPU.

2. Create a file on the root of the memory card called "S7_JOB.S7S". Open the file with a text editor and type the following: SET_PWD.
3. Create a folder on the root of the memory card called: SET_PWD.S7S.
4. Under the "SET_PWD.S7S" folder, create a text file called "PWD.TXT". The file must be named "PWD.TXT". Enter your Protection of confidential PLC configuration data password as the text contents of the file. The file must contain a single line of text representing the Protection of confidential PLC configuration data password. Follow the STEP 7 rules for passwords when creating the password, using these characters:
   - 0123456789
   - A...Z a...z
   - !#$%&()*+,-./:;<=>?@ [\]_{|}~^
5. To clear the Protection of confidential PLC configuration data password on the PLC, the file must be empty.
6. Safely eject the card from the card reader/writer.

How to set the Protection of confidential PLC configuration data password

To set the Protection of confidential PLC configuration data password, follow these steps:

1. Verify that the CPU is not actively running a process before setting the Protection of confidential PLC configuration data password.
2. Insert the memory card into the CPU (Page 94). The CPU evaluates the card and sets the Protection of confidential PLC configuration data password.
3. Remove the memory card. After the CPU restarts, it uses the new Protection of confidential PLC configuration data password.

If the existing program requires the Protection of confidential PLC configuration data password you set with the memory card, the PLC can go to RUN based on the project configuration.

If the existing user program requires a different Protection of confidential PLC configuration data password than what you set with the memory card, the program will not load after restarting. You must clear the existing program and download a program that uses the Protection of confidential PLC configuration data password that you set in the previous steps.

4.4.14.9 Recovery from a lost password

If you have lost the password for a password-protected CPU, use an empty transfer card (Page 96) to delete the password-protected program. The empty transfer card erases the internal load memory of the CPU. You can then download a new user program from STEP 7 to the CPU.

⚠ WARNING

Risks when inserting transfer cards

If you insert a transfer card in a running CPU, the CPU goes to STOP. Control devices can fail in an unsafe condition, resulting in unexpected operation of controlled equipment.

Verify that the CPU is not actively running a process before inserting the memory card. Before inserting a transfer card, always ensure that the CPU is in STOP mode and your process is in a safe state.

Such unexpected operations can result in death or serious injury to personnel, and/or damage to equipment

You must remove the transfer card before setting the CPU to RUN mode.

4.4.14.10 Memory card for copying license conditions and copyrights from the CPU

License conditions and copyright files for open-source and third-party software (OSS files) are embedded in the CPU firmware. You can copy them to a supported non-SIMATIC standard memory card (Page 333).

Copying license conditions and copyrights to a non-SIMATIC memory card

To copy the license conditions and copyright files to a supported non-SIMATIC standard memory card, insert a supported non-SIMATIC standard memory card (Page 94) into the CPU. The format of the memory card must be "FAT32" file system.

The CPU restarts and copies the license conditions and copyrights to the memory card. They are in a zip file in a folder named OSS at the root level of the memory card file system. You can remove the memory card.

4.5 Managing users and roles

With the TIA Portal you can perform user management and access control (UMAC). This allows you to create and manage users and roles in your project who are allowed to perform specific functions. You can assign roles with specific rights to each user. You can then assign runtime rights to your S7-1200 G2 PLC.

After adding users and making role assignments, you must load the configuration to the CPU(s) to activate UMAC. After you load the project to your S7-1200 G2 PLC, only authorized users can access various CPU functions (Page 206).

For more information, refer to "Managing users and roles" in the TIA Portal Information System.

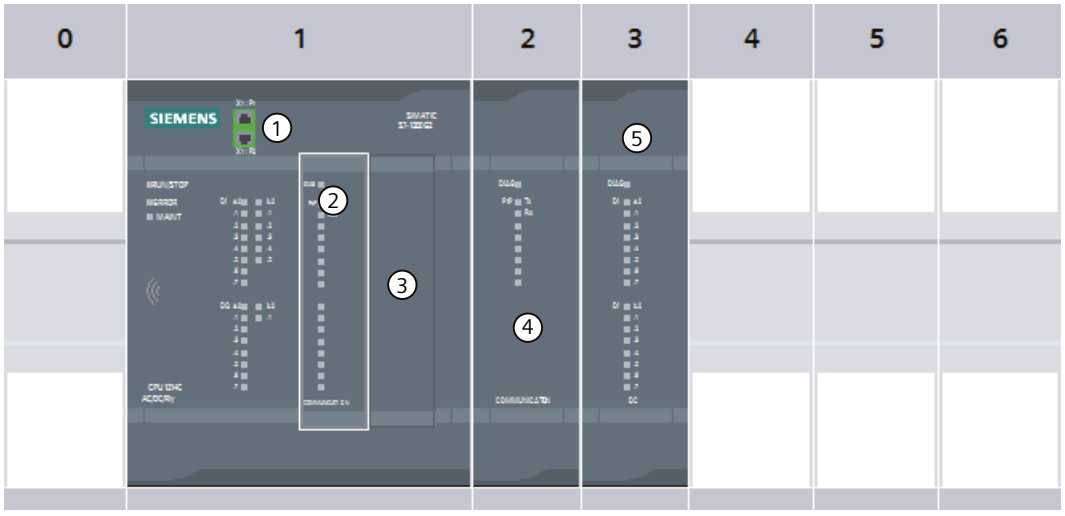
NOTE

S7-1200 G2 supports local user but not global users.

4.6 Device configuration

4.6.1 Overview

You create the device configuration for your PLC by adding a CPU and additional boards and modules to your project as needed.



① PROFINET port(s) of CPU (under door)

② Signal board (SB) or Communication board (CB)

③ CPU

④ Communication module (CM)

⑤ Signal module (SM) for digital or analog I/O

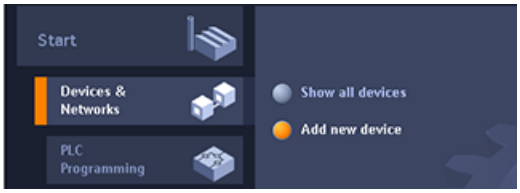
To learn more about the number of modules you can configure in your project, see Installing and removing expansion modules (Page 33).

Refer to Ordering Information (Page 332) for expansion boards and modules that are available.

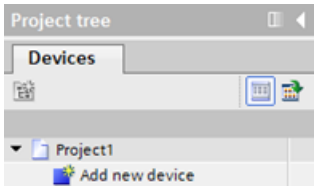
4.6.2 Inserting a CPU

You can insert a CPU into your project from either the Portal view or the Project view of STEP 7:

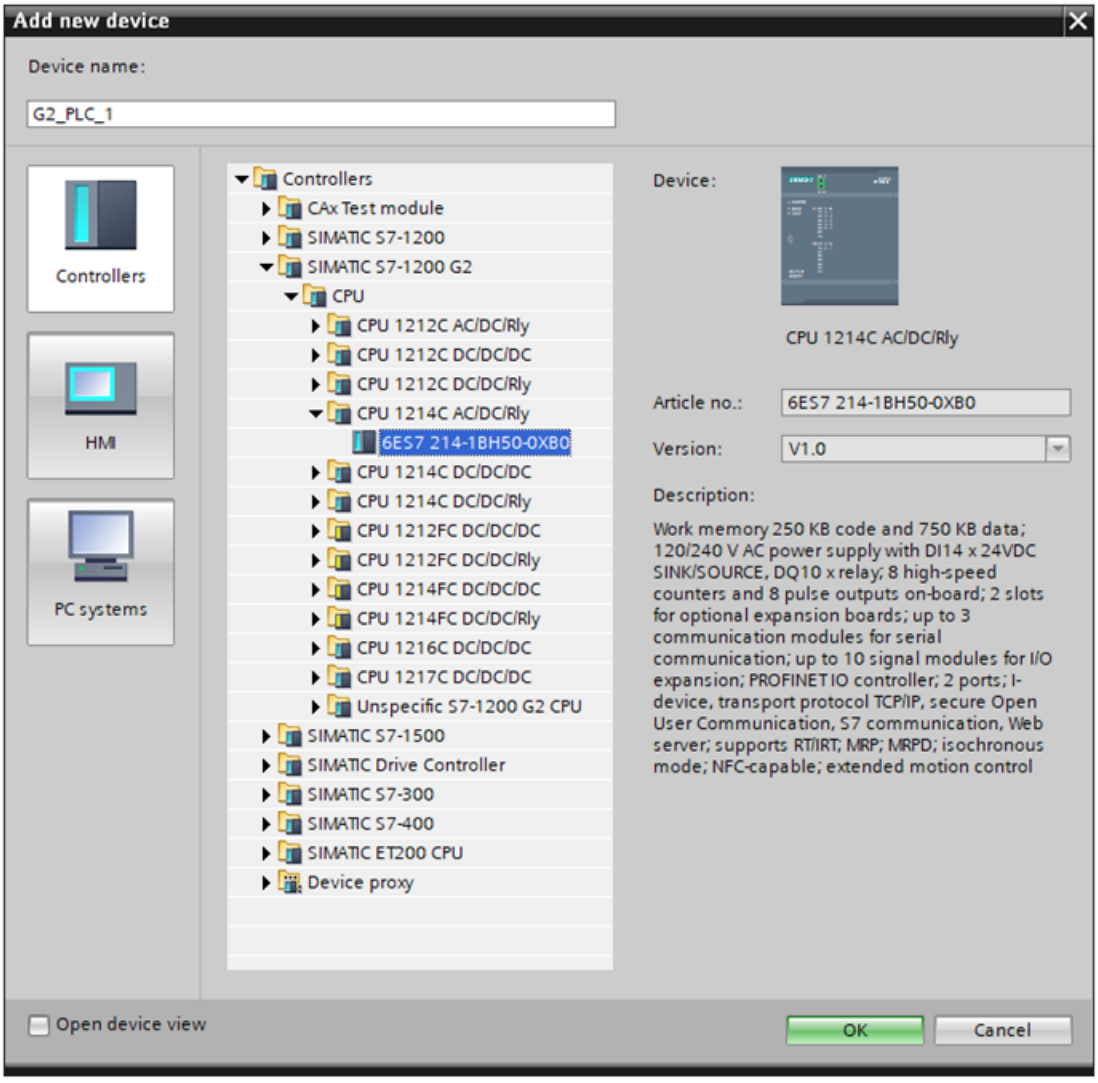
- In the Portal view, select "Devices & Networks" and click "Add new device".



- In the Project view, under the project name, double-click "Add new device".



From the "Add new device" dialog, select the correct Article Number and firmware version from the list.



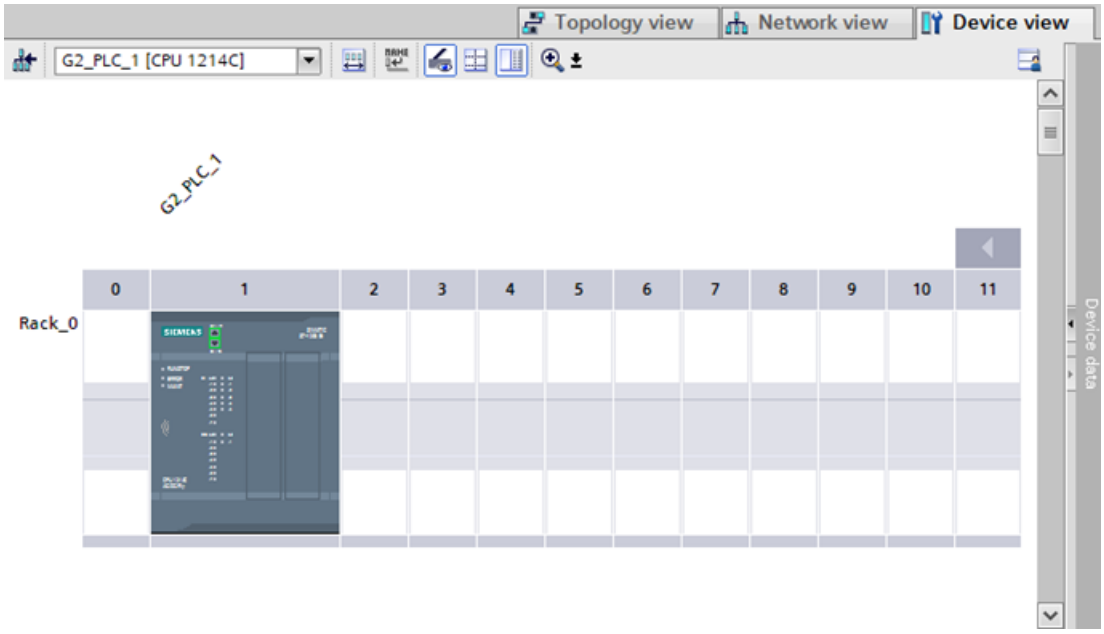
Configuring PLC security settings for your inserted CPU

When you insert an S7-1200 G2 CPU, STEP 7 launches the security wizard to help you set up your PLC security settings. Follow the steps in the wizard to set up your PLC security settings.

Refer to Protection & Security topics in the TIA Portal Information System to learn more about each configuration task and related security concepts.

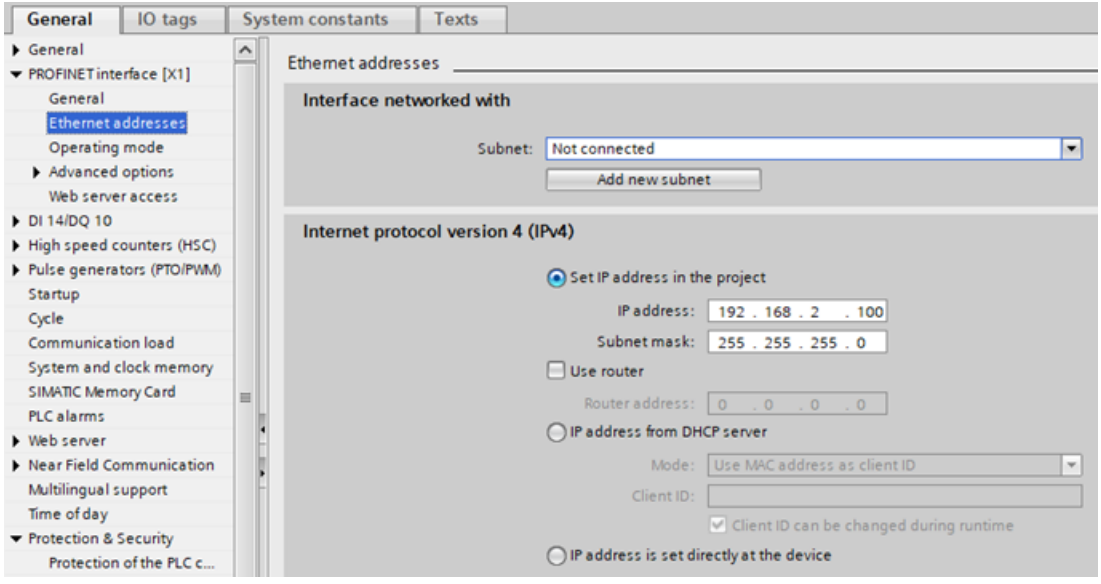
Device configuration for the inserted CPU

After you add a CPU, STEP 7 creates the rack and displays the CPU in the Device view:



Clicking the CPU in the Device view displays the CPU properties in the inspector window.

You can assign an IP address for the CPU during the device configuration. If your CPU is connected to a router on the network, select the checkbox next to "Use router" and enter the router's IP address.



4.6.3 Uploading the configuration of a connected CPU

STEP 7 provides two methods for uploading the hardware configuration of a connected CPU:

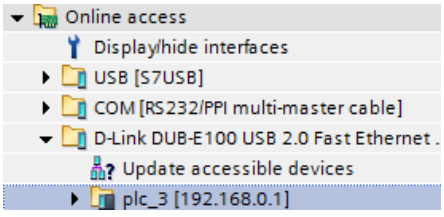
- Uploading the connected device as a new station
- Configuring an unspecified CPU and detecting the hardware configuration of the connected CPU

Note that the first method uploads both the hardware configuration and the software of the connected CPU.

Uploading a device as a new station

To upload a connected device as a new station, follow these steps:

1. Expand your communications interface from the "Online access" node of the project tree.



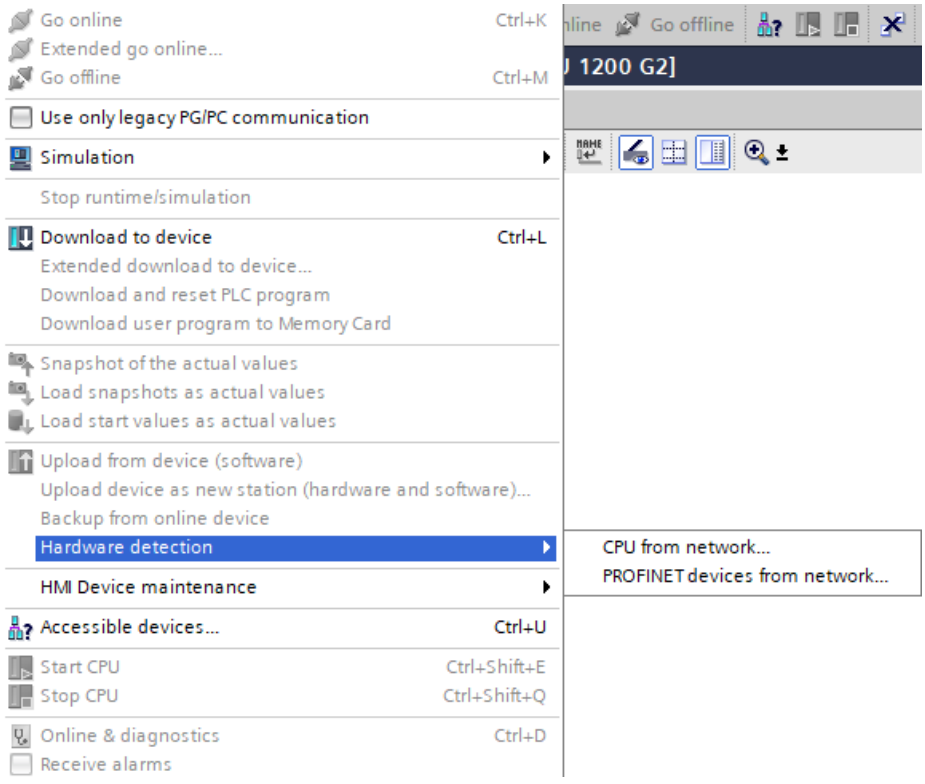
2. Double-click "Update accessible devices".
3. Select the PLC from the detected devices.
4. From the Online menu of STEP 7, select the "Upload device as new station (hardware and software)" menu command.

STEP 7 uploads both the hardware configuration and the program blocks.

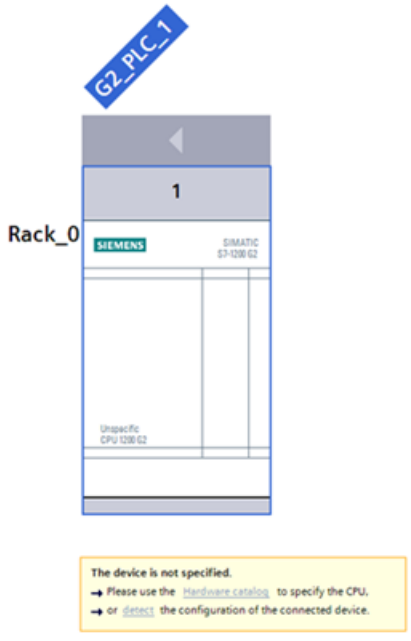
Detecting the hardware configuration of an unspecified CPU

If you are connected to a CPU, you can upload the configuration of that CPU, including any modules, to your project. Create a new project and use "Add new device (Page 113)" to add an "Unspecific S7-1200 G2 CPU".

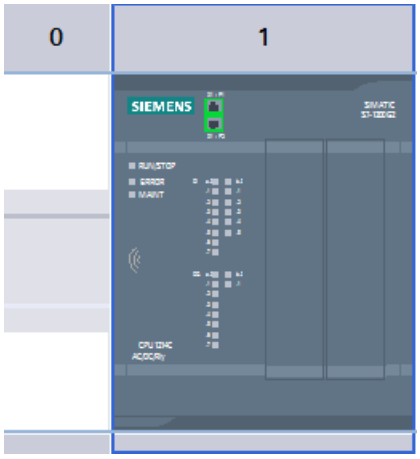
From the program editor, select the "Hardware detection" command from the "Online" menu.



From the device configuration, select "detect" in the box below the CPU. STEP 7 then detects the configuration of the PLC.



After you select the CPU from the online dialog and click Load, STEP 7 uploads the hardware configuration from the CPU, including any devices. You can then configure the parameters for the CPU and the modules (Page 114).



NOTE

Increased CPU Power-on time with missing/unplugged modules

Powering the CPU while it has missing or unplugged modules relative to your downloaded configuration causes an increased power-on time. During this period, the CPU and NFC functionality (Page 188) are unresponsive due to a longer CPU startup time. The length of the timeout for SBs is shorter than for CMs or SMs.

4.6.4 Adding modules to the configuration

Use the STEP 7 hardware catalog to add any of the following expansion modules or expansion boards to the CPU configuration:

- Signal modules (SM) provide additional digital or analog I/O points. These modules are connected to the right side of a CPU, CM, or SM.
- Signal boards (SB) provide additional I/O points for the CPU. The SB is installed on the front of the CPU.
- A Communication board (CB) provides an additional communication port (such as RS485). The CB is installed on the front of the CPU.
- A Communication module (CM) provides an additional communication port (such as RS232/RS485/RS422). This module is connected to the right side of a CPU or CM.

To learn more about possible configurations of expansion modules, see S7-1200 G2 Modules (Page 19).

To insert a module into the device configuration, select the device in the hardware catalog and either double-click or drag the device to the appropriate slot. You must download your device configuration to the CPU for the devices to be functional.

4.6.5 Configuring the operation of the CPU

STEP 7 enables you to configure your S7-1200 G2 CPU by editing the CPU properties listed below. You can change Startup behavior, modify the behavior of digital I/O, or enable security settings, in addition to other valuable functions.

To configure the operational parameters for the CPU, select the CPU in the Device view and use the "Properties" tab of the inspector window.

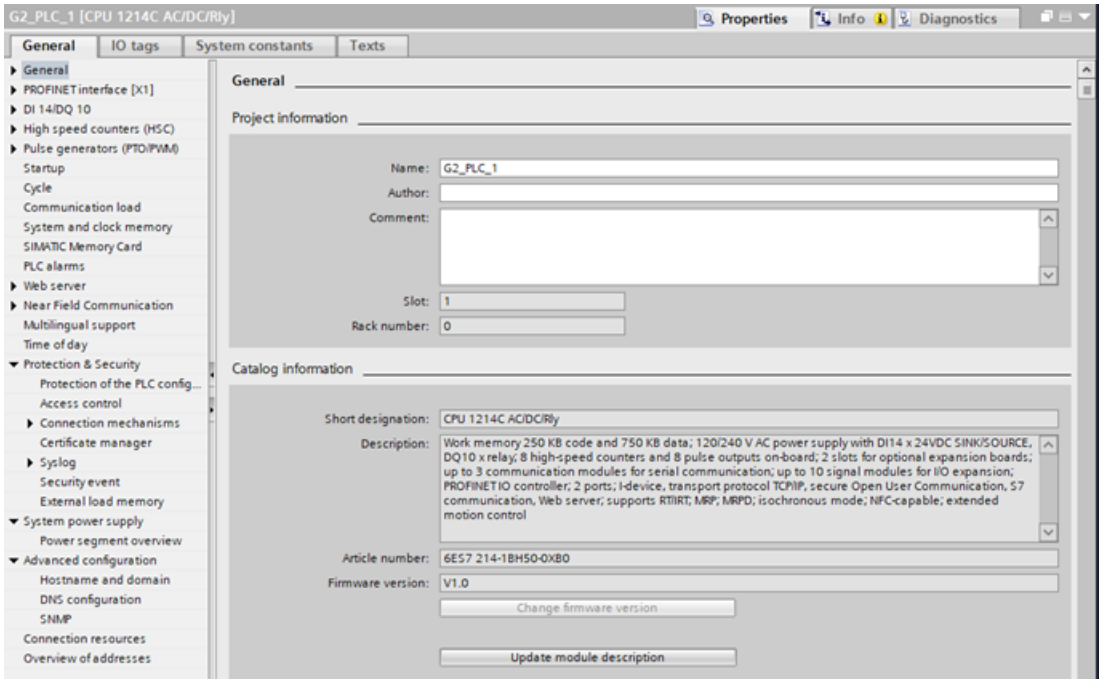


Table 4-34 CPU properties

Property	Description
General	Contains Project information, Catalog information, Identification & Maintenance, and Checksums.
PROFINET interface	Sets the IP address and Advanced PROFINET features.
DI and DQ	Configures the behavior of the local (onboard) digital I/O (for example, digital input filter times and digital output reaction to a CPU stop).
High-speed counters (Page 127) and pulse generators (Page 125)	Enables and configures the high-speed counters (HSC) and the pulse generators used for pulse train output (PTO) and pulse-width modulation (PWM). When you configure a digital output of the CPU or signal board (SB) as an HSC Compare output, or as a pulse output for use with PWM, PTO, or motion control instructions, that physical output is now controlled by the HSC or pulse-generator function. The corresponding process-image value is no longer written to that physical output; changes to the process image will be ignored by a physical output assigned to an HSC or pulse generator.
Startup (Page 57)	**Startup after POWER ON:** Selects the behavior of the CPU following an off-to-on transition, such as to start in STOP mode or to go to RUN mode after a warm restart.

[1] If you disable access control, every user has full access to the CPU without a password. You are essentially granting users "Full access (no protection)" (if using a standard CPU) or "Full access incl. fail-safe (no protection)" (if using an F-CPU). Users can access most CPU functions. Because of this, Siemens recommends disabling access control only during commissioning and that only authorized persons have access to the CPU during this phase.

Property	Description
Startup (Page 57)	**Comparison preset to actual configuration:** Specifies the startup characteristics of the CPU for situations in which the actual configuration of the S7-1200 G2 station does not correspond to the preset configuration: • Startup of the CPU only if compatible • Startup of the CPU even if mismatch A module in the configured slot must be compatible with the configured module. Compatible means that the module that is present matches the number of inputs and outputs and must match with respect to its electrical and functional properties. It may be more capable, but not less capable.
	Configuration time: Specifies a maximum amount of time (default: 60000 ms) in which the local I/O and distributed I/O must start up. (The CMs receive power and communication parameters from the CPU during startup. This assignment time allows time for the I/O connected to the CM to be brought online.) The CPU goes to RUN as soon as the local I/O and distributed I/O have started and are ready for operation, regardless of the assignment time. If the local I/O and distributed I/O have not been brought online within this time, the CPU still goes to RUN--without the local I/O and distributed I/O.
Cycle (Page 78)	Defines a maximum cycle time or a fixed minimum cycle time.
Communication load	Allocates a percentage of the CPU time to be dedicated to communication tasks.
System and clock memory (Page 82)	Enables a byte for "system memory" functions and enables a byte for "clock memory" functions (where each bit toggles on and off at a predefined frequency).
SIMATIC Memory Card	Allows you to configure the CPU to determine when the SD card has aged to a configured percentage value. You select "Aging of the SIMATIC Memory card" checkbox to configure the threshold value percentage. You can use the GetSMCInfo instruction to check the SIMATIC memory card against this configured value.
PLC alarms	Enables central alarm management, allowing the CPU to transfer alarm text to the HMI device.
Web server (Page 195)	Enables and configures the Web server feature.
Near Field Communication (Page 188)	Enables reading data from a supported CPU with the S7-1200 G2 NFC app.
Multilingual support	Assigns a project language for the device and the Web server to use for displaying diagnostics buffer entry texts for each of the possible Web server user interface display languages.
Time of day	Selects the time zone and configures daylight saving time. Allows for Time Synchronization across plant components.
Protection & Security	**Protection of the PLC configuration data**: Allows for password protection of confidential PLC configuration data.
	Access control: Allows for disabling or enabling access control and, optionally, access levels.[1]
	Connection mechanisms (Page 135): Permits access with PUT/GET communication from a remote partner when the Anonymous user is enabled. Allows for configuration of secure PG/HMI certificate-based communication.
	Certificate manager (Page 135): Enables certificate-based security settings for global or partner devices.
	Syslog: Allows for the logging and non-retentive storage of safety-related event messages.

[1] If you disable access control, every user has full access to the CPU without a password. You are essentially granting users "Full access (no protection)" (if using a standard CPU) or "Full access incl. fail-safe (no protection)" (if using an F-CPU). Users can access most CPU functions. Because of this, Siemens recommends disabling access control only during commissioning and that only authorized persons have access to the CPU during this phase.

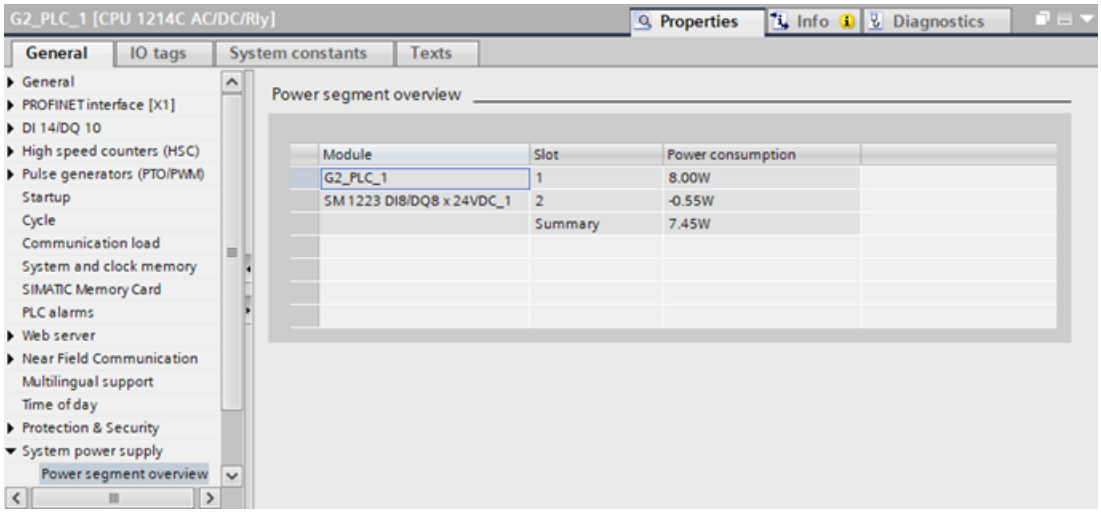
Property	Description
Protection & Security	**Security event**: Details important actions and events in the diagnostics buffer which can trigger group alarms.
	External load memory: Allows for the disabling of copying from internal to external load memory.
System power supply (Page 116)	Enables automatic calculation of power consumption by providing an overview of power segments representing each configured module.
Advanced configuration	Contains: • Hostname and domain - Assign the name or IP address of the host computer and activate the domain configuration in STEP 7. • DNS configuration (Page 129) - Configure the DNS server address. • SNMP (Page 129) - Activate SNMP (Simple Network Management Protocol).
Connection resources (Page 133)	Provides a summary of the communication connection resources that are available for the CPU and the number of connection resources that have been configured.
Overview of addresses	Provides a summary of the I/O addresses that have been configured for the CPU.

[1] If you disable access control, every user has full access to the CPU without a password. You are essentially granting users "Full access (no protection)" (if using a standard CPU) or "Full access incl. fail-safe (no protection)" (if using an F-CPU). Users can access most CPU functions. Because of this, Siemens recommends disabling access control only during commissioning and that only authorized persons have access to the CPU during this phase.

You can learn more about the above CPU properties by referring to the related device configuration topics in the TIA Portal Information System.

4.6.5.1 Configuring the system power supply

As you add modules to your configuration of the S7-1200 G2, TIA Portal automatically calculates your overall power consumption (Page 27). This enables you to anticipate the energy needs of a given physical device configuration.



You can configure the Sensor Supply wired interface to suit your application.

4.6.6 Configuring the parameters of the modules

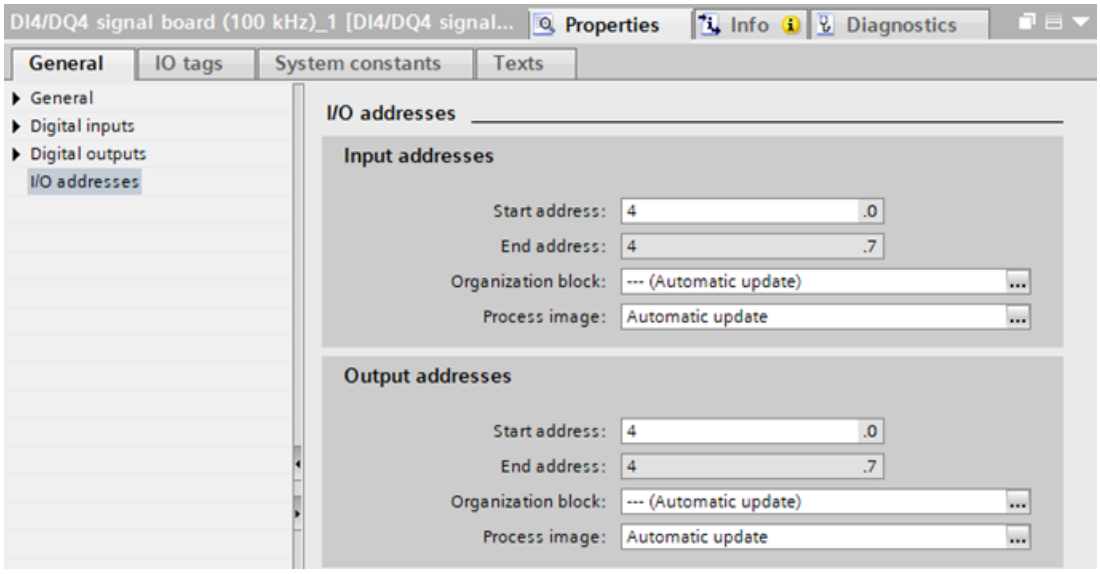
STEP 7 enables you to configure the inputs and outputs of devices connected to your S7-1200 G2 CPU on the network. You can assign values to both analog and digital I/O to accomplish tasks such as "pulse catch", to update process image partitions, or to monitor diagnostic functions.

To configure the operational parameters for the modules, select the module in the Device view and use the "Properties" tab of the inspector window.

Configuring a signal module (SM) or a signal board (SB)

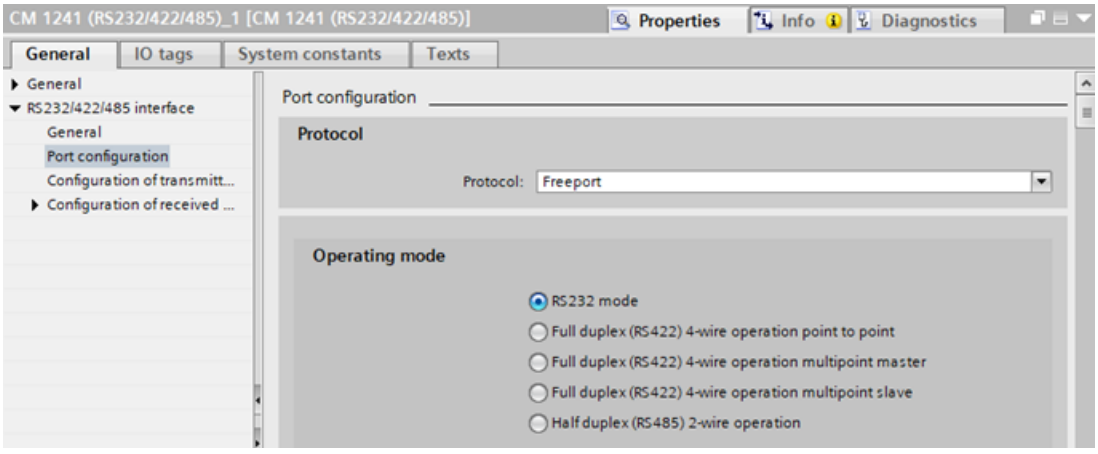
The device configuration for signal modules and signal boards provides the means to configure the following:

- Digital I/O: You can configure inputs for rising-edge detection or falling-edge detection (associating each with an event and hardware interrupt) or for "pulse catch" (to stay on after a momentary pulse) through the next update of the input process image. Outputs can use a freeze or substitute value.
- Analog I/O: For individual inputs, you can configure parameters such as measurement type (voltage or current), range, and smoothing, as well as enable underflow or overflow diagnostics. Analog outputs provide parameters such as output type (voltage or current) and for diagnostics, such as short circuit (for voltage outputs) or upper/lower limit diagnostics. You can configure the ranges of analog inputs and outputs in engineering units in your program logic.
- I/O addresses: You can configure the start address for the set of inputs and outputs of the module. You can also assign the inputs and outputs to a process image partition (PIP) or to automatically update, or to use no process image partition. See "Execution of the user program" (Page 54) for an explanation of the process image and process image partitions.



Configuring a communication module (CM)

You can configure the parameters for point-to-point communication modules (CMs) on the network.

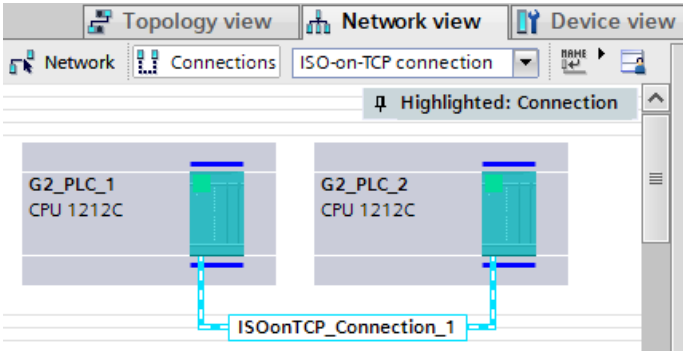


4.6.7 Configuring the CPU for communication

The S7-1200 G2 is designed to solve your communications and networking needs by supporting both simple and complex networks. The S7-1200 G2 also provides tools that allow you to communicate with other devices, which might use their own communications protocols.

Creating a network connection

Use the "Network view" of Device configuration to create the network connections (Page 136) between the devices in your project. After creating the network connection, use the "Properties" tab of the inspector window to configure the parameters of the network.



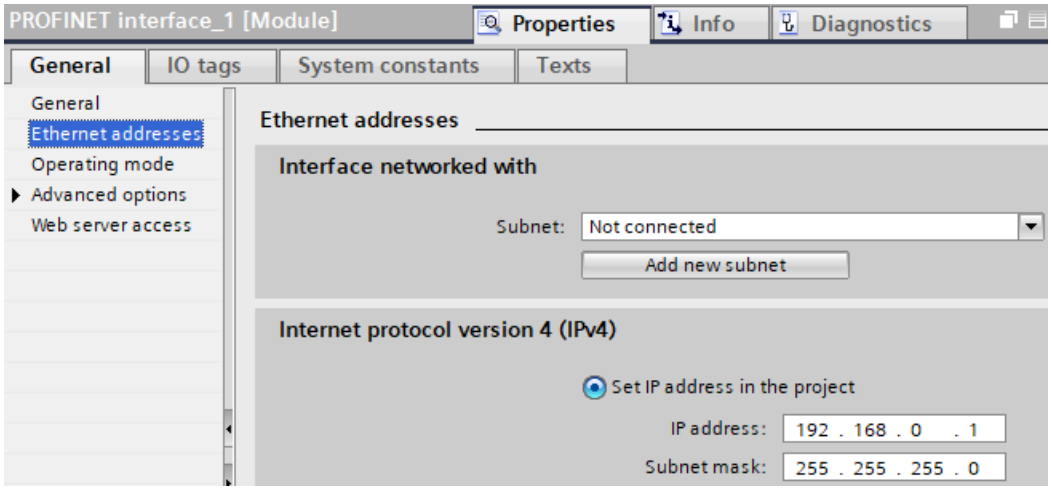
The S7-1200 G2 CPU supports the following connections:

- S7 connection (Page 179)
- ISO-on-TCP connection (Page 150)
- TCP connection (Page 149)
- UDP connection (Page 150)
- HMI connection (PLC to an HMI)

Assigning the IP address and Subnet

The S7-1200 G2 CPU does not have a pre-configured IP address. You must manually assign an IP address (Page 142) for the CPU in the Properties Tab under "General > Ethernet addresses".

To make a connection to your CPU, your chosen network interface and the CPU must be on the same class of network and on the same subnet. You can either set up your network interface to match the default IP address of the CPU, or you can change the IP address of the CPU to match the network class and subnet of your network interface.

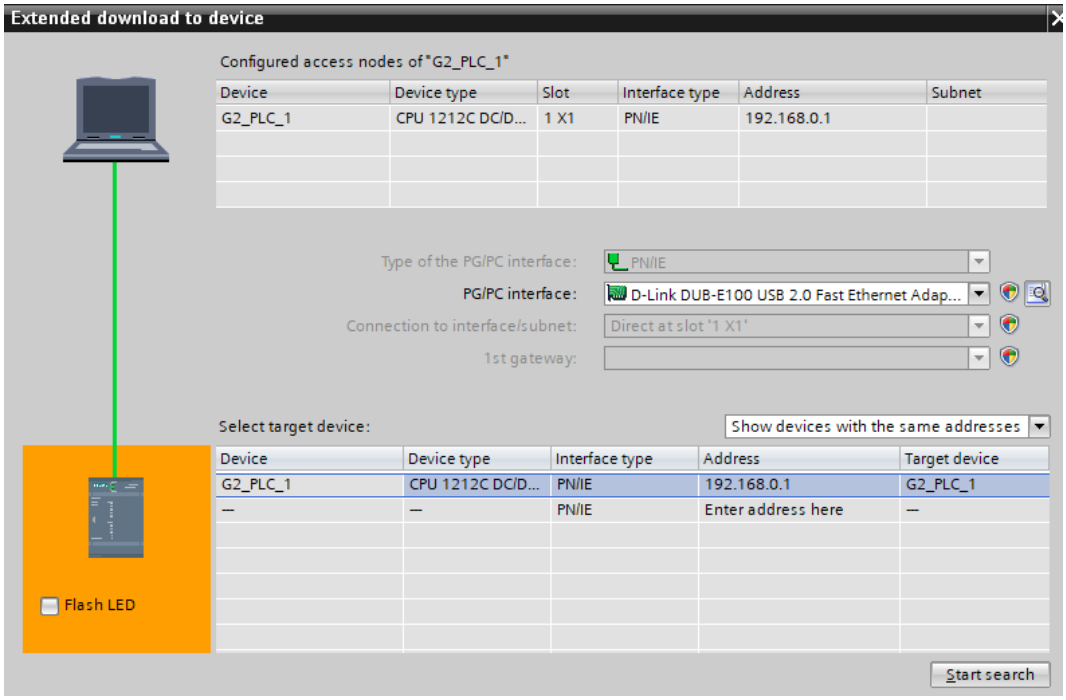


Configuring the Local/Partner connections

For the TCP, ISO-on-TCP, and UDP Ethernet protocols, use the "Properties" of the instruction (TSEND_C, TRCV_C, or TCON) to configure the "Local/Partner" connections (Page 137).

Downloading to the CPU

After configuration, download your STEP 7 project to the CPU to test the PROFINET network (Page 147). The download operation sets all IP addresses for devices configured as "Set IP address in the project".



4.6.8 Time synchronization

The objective of time synchronization of the time-of-day clocks is to have one master clock that synchronizes all other local clocks. The master clock synchronizes the local clocks initially and also periodically re-synchronizes the clocks to avoid the effects of drift over time.

In the case of the S7-1200 G2 and its local base components, only the CPU has time-of-day clocks that might need to be synchronized. You can configure the CPU's time-of-day clock to be synchronized to an external master clock. The external master clock might supply the time of day using an NTP server.

Setting the time-of-day clock

There are multiple ways to set the time-of-day clock in the S7-1200 G2 CPU:

- Using the NTP server (Page 148)
- Using STEP 7
- From the user program
- Using an HMI panel
- From the SIMATIC Automation Tool
- From the Web server

By default, time synchronization using the NTP server to change the CPU's clock is disabled.

You can select the update interval using the NTP server. The update interval of the NTP server is set to 10 seconds by default.

When you activate time synchronization in a module, STEP 7 prompts you to select the "CPU synchronizes the modules of the device", if you have not already selected the check box in the CPU's "Time synchronization" dialog. STEP 7 also warns you if you configured more than one master clock source for time synchronization.

⚠ WARNING

Risk of attacker accessing your networks through open interfaces

If an attacker can access your networks through open interfaces, such as software like STEP 7 or SAT, or through an HMI, the attacker can possibly disrupt control of your process by shifting the CPU system time.

The S7-1200 G2 CPU supports "time of day" interrupts and clock instructions that depend upon accurate CPU system time. You must restrict access to the CPU by enabling access control and disabling the "Anonymous" user. Failure to do so can cause a security breach that allows an unknown user to disrupt control of your process by shifting the CPU system time.

Disruptions to process control can possibly cause death, severe injury, or property damage.

For security information and recommendations, see the "Operational Guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html)" white paper on the Siemens Industrial Cybersecurity Website.

NOTE

Receiving time synchronizations for the CPU from more than one source could cause conflicting time updates. Time synchronizations from multiple sources could adversely affect instructions and events based on time of day.

4.7 Compatibility between STEP 7 versions and the S7-1200 G2 CPU

TIA Portal V20 and later supports configuration and programming of the S7-1200 G2 CPU. Older versions of the TIA Portal do not support the S7-1200 G2 family.

Working with an older project and adding S7-1200 G2 CPUs

You might want to add S7-1200 G2 CPUs to an existing application that uses other CPUs and that was created in an older version of the TIA Portal. To do this, you will need a TIA Portal V20 project.

You can open a project in TIA Portal V20 from a V13 SP2 or later project and upgrade the project to V20. The TIA Portal dialogs guide you in upgrading the project if it is possible. You can then add the S7-1200 G2 CPUs for your application and perform these tasks in the TIA Portal:

1. Configure the S7-1200 G2 devices.
2. Program the logic for the S7-1200 G2 CPUs.
3. Download the hardware configuration and software to the S7-1200 CPUs.

⚠ WARNING

Risks with editing and executing program logic from versions older than TIA Portal V13

Do not attempt to upgrade a project that is V13 or older to the current version by copying program logic from one CPU to an S7-1200 G2 CPU.

You must first open the V13 project in TIA Portal V13 SP2 and upgrade the project to V13 SP2. Then you can open the latest version of the TIA Portal and upgrade the project from V13 SP2 project to V20.

Executing STEP 7 program logic that you copied from an older version to a newer version can cause unpredictable program behavior and can result in death or severe personal injury.

Migrating program logic from an S7-1200 CPU to an S7-1200 G2 CPU

If you want to migrate existing program logic from an S7-1200 CPU to an S7-1200 G2 CPU, note that there is no device exchange from any type of CPU to an S7-1200 G2 CPU. Note also that the instruction set and library support in S7-1200 G2 has differences from other CPU families. To migrate program logic from an S7-1200 CPU to an S7-1200 G2 CPU, follow these steps:

1. Add an S7-1200 G2 CPU to the upgraded project that has S7-1200 CPUs and configure the device. Be sure to observe the Warning above when upgrading a project.
2. Copy the program blocks from the S7-1200 CPU to the program blocks of the S7-1200 G2 CPU.
3. Create and edit any PLC tag tables that you need.
4. Attempt to compile the program, choosing "rebuild all" for both hardware and software.
5. Resolve any memory and I/O addressing differences between the two CPUs. Resolve any instruction differences between the two CPUs. Continue resolving compiler errors until the program compiles.

4.8 Instruction set

4.8.1 Supported programming languages

STEP 7 provides the following standard programming languages for the S7-1200 G2:

- LAD (ladder logic) is a graphical programming language. The representation is based on circuit diagrams.
- FBD (Function Block Diagram) is a programming language that is based on the graphical logic symbols used in Boolean algebra.
- SCL (structured control language) is a text-based, high-level programming language.
- CEM (Cause-Effect-Matrix) for programming Function Blocks (FBs)

When you create a code block, you select the programming language for that block.

The STEP 7 program can utilize code blocks created in any or all of the programming languages.

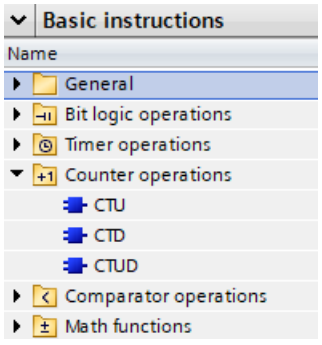
See the STEP 7 Information System for information on any of the programming languages.

4.8.2 Instructions for programming the PLC

STEP 7 provides instructions to program your S7-1200 G2 PLC. Categories and folders differ based on your programming language. The LAD Programming language presents instructions in the following main categories:

- Basic
- Extended
- Technology
- Communication
- Optional Packages

Folders under each main category list the instruction group as shown in the example below:



To find more information about each instruction and its use, follow these steps:

1. Open a program block to display the Instruction task card.
2. Expand an instruction group.
3. Do one of the following:
   - Select the individual instruction and press F1.
   - Hover over an individual instruction to reveal a TIA Portal tooltip. If you click the tooltip, or continue to hover over the instruction, a cascading tooltip provides a link to the corresponding instruction topic in the TIA Portal Information System.

You can access the TIA Portal Information System in one of the following ways:

- Select "Help" in the Portal view.
- Select the "Help > Show help" menu command in the Project view.

In the help Content tab, use the following path to access the instructions help: Programming a PLC > Instructions.

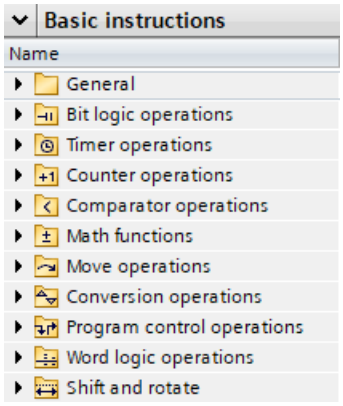
NOTE

Choosing an instruction by PLC family

If the TIA Portal Information System presents an instruction differently within the tooltips or table of contents based on PLC family, follow the S7-1500 option for the instruction topic.

4.8.3 Basic instructions

Basic Instructions are instructions that you use often and include the following folder groups:

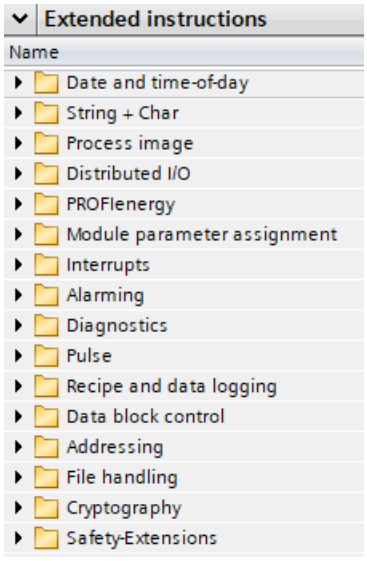


Instructions in these folders allow you to do the following:

- General - Add a network and connect network elements.
- Bit logic operations - Perform Boolean logic.
- Timer operations - Delay actions and measure elapsed time.
- Counter operations - Count internal program or external process events.
- Comparator operations - Compare two values or compare a value with a range and use the compare result in Boolean logic.
- Math functions - Perform calculations including integer and floating-point math.
- Move operations - Copy data elements to a new memory address and convert from one data type to another.
- Conversion operations - Convert from one data type to another, perform scaling, and round a floating-point number to the nearest integer.
- Program control operations - Control program sequence including jumps, retrigger cycle monitoring timer, and STOP the PLC.
- Word logic operations - Compare two values, bit by bit, using Boolean logic.
- Shift and rotate - Shift or rotate a value right or left by a specified number of bits.

4.8.4 Extended instructions

Extended instructions allow for more possibilities and include the following folder groups:



Instructions in these folders allow you to do the following:

- Date and time-of-day - Manipulate and compare time values. Set and read local time and system time.
- String + Char - Create, convert, and manipulate strings and characters. Search for, replace, insert, or append substrings.
- Process image - Update or synchronize the process image inputs or outputs.
- Distributed I/O - Exchange information with distributed I/O using read and write records.
- PROFIenergy - Activate or deactivate energy-saving states in lower-level PROFIenergy devices.
- Module parameter assignment - Read and write parameter records to modules.
- Interrupts - Control runtime aspects of interrupt events. Attach and detach OBs to interrupt events.
- Alarming - Generate program alarms and user diagnostic alarms.
- Diagnostics - Read status and diagnostic information. Generate diagnostic information for third-party components.
- Pulse - Control pulse width modulation (PWM) and pulse train output (PTO) functions.
- Recipe and data logging
  - Import and export recipes
  - Create, open, write, clear, close, and delete data logs (See "Working with data logs" below.)
- Data block control - Create a new data block in load or work memory. Transfer data between data blocks.

- Addressing - Convert module addresses among these options:
  - IO address
  - Hardware identifier
  - Slot
- File handling - Create a file on a memory card; write to and read from this file.
- Cryptography - Generate a random number. Perform encoding and decoding.
- Safety-Extensions - Acknowledge warning message about exceeding the F-cycle time.

Working with data logs

The TIA Portal Information System documents data logging at this path: Information System > Programming a PLC > Instructions > Instructions (S7-1200, S7-1500) > Extended instructions > Recipes and data logging > Data logging

In addition, be aware of this information when working with data logs:

NOTICE
Recommended frequency for write operations when using data logs When using data logs on memory cards, a high frequency of write operations can affect the S7-1200 system negatively. To ensure the overall performance and robustness of your system, limit write operations to every 200 ms or longer. Exceeding this limit can shorten the lifespan of the memory card or internal flash.

NOTE

Data log management

Keep no more than 1000 data logs in a file system. Exceeding this number can prevent the Web server from having enough CPU resources to display the data logs.

Manage your data logs to ensure that you only keep the number that you need to maintain, and do not exceed 1000 data logs.

NOTE

Editing data logs on the memory card

You can copy data logs from a memory card using a PC card reader. Do not change them or delete them using a PC card reader.

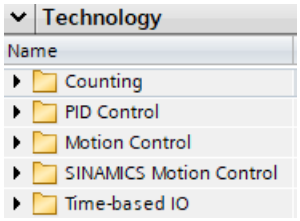
To delete, download, or display data logs use one of the following methods:

- SIMATIC Automation Tool
- DataLogDelete instruction
- Web API (Page 195) methods "DataLogs.DownloadAndClear", "Files.Browse", "Files.Download" and supporting code as documented for displaying data logs.

If you open the file system of the memory card in the File explorer, you run the risk of accidentally deleting or changing a data log or other system files, potentially damaging files or making the memory card unusable.

4.8.5 Technology instructions

Technology Instructions allow you to perform technological functions and include the following folder groups:

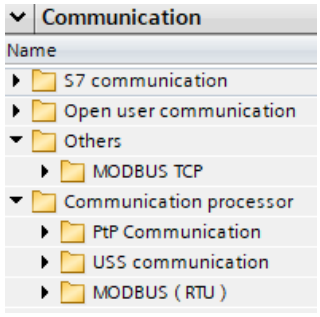


Instructions in these folders allow you to do the following:

- Counting - Control high-speed counter (HSC) functions such as counting and frequency measurement.
- PID Control - Control proportional-integral-derivative (PID) functions.
- Motion Control - Initiate absolute or relative moves. Perform homing and jog operations.
- SINAMICS Motion Control - Control stepper motors and servo motors. Coordinate motion axes.
- Time-based IO - Precisely monitor digital input state changes. Precisely control digital output state changes.

4.8.6 Communication instructions

Communication Instructions provide for communication using various network protocols and include the following folder groups:

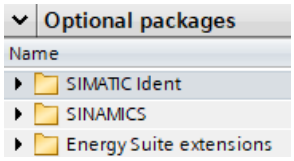


Instructions in these folders allow you to do the following:

- S7 Communication – Read data from or write data to a remote CPU using S7 protocol.
- Open user communication - Establish and terminate communication connections, send and receive data, send emails.
- Others - Exchange data using Modbus TCP protocol (client or server) over the PROFINET interface.
- Communication Processor - Control serial communications such as point-to-point (PtP), Universal Serial Interface Protocol (USS), and Modbus Remote Terminal Unit (Modbus RTU).

4.8.7 Optional instructions

Optional Instructions provide additional functionality and include the following folder groups:



Instructions in these folders allow you to do the following:

- SIMATIC Ident - Interface with Siemens radio-frequency (RF) and optical identification systems.
- SINAMICS - Control Siemens variable-frequency drives (VFD).
- Energy Suite extensions - Calculate energy data. Create an energy report as a data log.

Communication 5

5.1 Overview

The S7-1200 G2 offers several types of communication between CPUs and programming devices, HMIs, and other CPUs.

PROFINET

PROFINET (www.us.profinet.com) (PN) is used for exchanging data through the STEP 7 program with other communications partners through Ethernet.

For the S7-1200 G2, PROFINET supports 31 IO devices with a maximum of 512 submodules as well as the following:

- S7 communication (Page 179)
- Open User Communication with the following protocols:
  - User Datagram Protocol (Page 150) (UDP)
  - ISO on TCP (Page 150) (RFC 1006)
  - Transport Control Protocol (Page 149) (TCP)

PROFINET IO controller

As an IO controller using PROFINET IO, the CPU communicates with up to 31 PN devices on the local PN network.

CPU-to-CPU S7 communication

You can create a communication connection to a partner station and use the PUT and GET instructions (Page 179) to communicate with S7 CPUs. For more information on using PUT/GET, see the "S7 connections using PUT and GET instructions" chapter in the TIA Portal Information System.

Network security

⚠ WARNING

Avoiding security risks from network attacks

If an attacker can access your networks, the attacker can possibly read and write data.

For example, I/O exchange through PROFINET, PUT/GET (Page 179), T-Block, and communication modules (CMs) have no security features. You must protect these forms of communication.

If you fail to protect these forms of communication, death or severe personal injury can result.

For security information and recommendations, see the "Operational Guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html)" white paper on the Siemens Industrial Cybersecurity Web site.

5.2 Secure communication

S7-1200 G2 CPUs implement secure communication between PLCs and the TIA Portal, SIMATIC Automation Tool, and HMIs. This implementation uses the industry standard TLS 1.3 (Transport Layer Security) protocol. The S7-1200 G2 CPU does not support legacy PG/PC communication.

Advantages of secure communication

Secure communication offers the following advantages:

- Confidentiality: Ensures that data remains confidential and cannot be accessed by unauthorized individuals.
- Integrity: Guarantees that the received message has not been modified during transmission.
- End point authentication: Verifies the identity of the communication partner.

Today, networked industrial machinery and control systems with sensitive data are at high risk and consequently pose high security requirements for data exchange.

Protection through firewall, VPN connection, or a security module, was common in the past and remains common. In addition to physical security, secure communication supports the transfer of data to external communication partners in encrypted form.

The CPU uses X.509 certificates (Page 135) to provide secure communication between the CPU and clients. Clients such as STEP 7 and the SIMATIC Automation Tool might require that you trust the certificate that is in the CPU. Be aware of the certificate you download to a CPU so that you can trust it when prompted.

Additional information

You can find additional details about the implementation of secure communication in the TIA Portal Information System. In particular, additional information about certificates is in the following TIA Portal Information System topics:

- Confidentiality through encryption
- Managing certificates with STEP 7
- Examples for the management of certificates
- Authenticity and integrity through signatures

5.3 Communication protocols and ports used by Ethernet communication

The specified ports are the standard port numbers that the S7-1200 G2 CPU uses. Many communication protocols and implementations enable you to use other port numbers. The following tables show different layers, protocols, and ports used in the S7-1200 G2 CPU.

Table 5-1 Transport layer ports and protocols by S7-1200 G2

Port(s)	Direction	Protocol	Application	Description	Default setting/notes
25	Outbound	TCP	SMTP	SMTP is used for sending e-mails.	Default: Deactivated. Can be enabled via TMAIL_C instruction in the STEP 7 program.
68	Outbound	UDP	DHCP	The IP address suite is obtained from a DHCP server during the startup of the PROFINET interface.	Default: Deactivated. Can be changed in the CPU properties
102	Inbound/ Outbound	TCP	ISO-on-TCP	ISO-on-TCP (according to RFC 1006). The S7 protocol uses ISO-on-TCP according to RFC 1006 for PG/HMI communication with TIA Portal.	Default: Activated. This function cannot be deactivated.
123	Outbound	UDP	NTP	NTP is used for synchronization of the CPU system time with the time of an NTP server.	Default: Deactivated. Can be enabled in the CPU properties.
161	Inbound	UDP	SNMP	SNMP is used for reading and setting network management data (SNMP managed Objects) by the SNMP Manager.	Default: Deactivated. Can be enabled via data record in the STEP 7 project or in CPU Properties. Provides customizable community strings to limit access.
443	Inbound	TCP	HTTPS	HTTPS is used for secure communication with the CPU-internal web server over TLS.	Default: Deactivated. Can be enabled by enabling the Web server in the CPU properties.
465, 587	Outbound	TCP	SMTPS	SMTPS is used for sending e-mails over secure connections.	Default: Deactivated. Can be enabled via TMAIL_C instruction in the STEP 7 program.

Port(s)	Direction	Protocol	Application	Description	Default setting/notes
502	Inbound/ Outbound	TCP	Modbus	Modbus/TCP is used by MB_CLIENT/MB_SERVER instructions in the STEP 7 program.	Default: Deactivated. Can be activated via Modbus instructions in the STEP 7 project. Port 502 is the default port for Modbus, but can be configured to other values via the Modbus instructions in the STEP 7 program.
6514, 514	Outbound	TCP (6514) UDP (514)	Syslog Client	The Syslog client of the CPU is used for transferring syslog messages to a server.	Default: Deactivated. Can be enabled in the CPU properties. You can configure the forwarding of syslog messages to a syslog server in the CPU properties. The collection of system logging events within a CPU cannot be disabled. Port 6514 is the default value for Syslog servers in STEP 7. Port 514 is the standard port for UDP Syslog servers, but it is not the default value even if you select UDP in the STEP 7 project configuration.
34964	Inbound/ Outbound	UDP	PROFINET Context Manager	The PROFINET Context Manager provides an endpoint mapper in order to establish an application relation (PROFINET AR).	Default: Enabled (UDP port open). This function cannot be deactivated.

Table 5-2 Port ranges that could be used by Open User Communication (OUC) and other protocols.

Port Range	Direction	Protocol	Application	Description
1-1999	Varies	TCP/UDP	OUC	This port range can be used to limited extent, excluding already used ports.
2000-5000	Varies	TCP/UDP	OUC	This is the recommended port range for OUC.
5001-49151	Varies	TCP/UDP	OUC	This port range can be used to limited extent, excluding already used ports.
49152-65535	Outbound	TCP/UDP	Varies	This is the Dynamic port area used for active connection end point if the application does not determine the local port number.

You define these communication parameters in the STEP 7 program.

Table 5-3 Protocols used by S7-1200 G2 in the Data Link and Network Layer (Layer 2, 3) of the OSI model.

Protocol	Direction	Ethertype	Description
PROFINET DCP	Inbound/Outbound	0x8892	DCP is used by PROFINET to discover PROFINET devices and provide basic settings. DCP uses the special multicast MAC addresses: 01-0E-CF-00-00-00 and 01-0E-CF-00-00-01.
LLDP	Outbound	0x88CC	LLDP is used by PROFINET to discover and manage neighbor relationships between PROFINET devices. LLDP uses the special multicast MAC address: 01-80-C2-00-00-0E.

Protocol	Direction	Ethertype	Description
PROFINET IO	Inbound/Outbound	0x8892	The PROFINET IO frames are used to transmit IO data cyclically between PROFINET IO controller and IO devices via Ethernet.
ICMP	Inbound	0x0800	Internet Control Message Protocol is used for diagnostic or control purposes.
MRP	Inbound/Outbound	0x88E3	Media Redundancy Protocol enables control of redundant transmission paths in a ring topology. MRP uses the special multicast MAC addresses: 01:15:4E:00:00:01 and 01:15:4E:00:00:02

5.4 Asynchronous communication connections

Overview of communication services

The CPU supports the following communication services:

Communication service	Functionality	Ethernet
PG communication	Commissioning, testing, diagnostics	Yes
HMI communication	Operator control and monitoring	Yes
S7 communication	Data exchange using configured connections	Yes
PROFINET IO	Data exchange between I/O controllers and I/O devices	Yes
Web server	Diagnostics, maintenance, and process data	Yes
SNMP (Page 177) [1] (Simple Network Management Protocol)	Standard protocol for network diagnostics and parameterization	Yes
Open communication over TCP/IP	Data exchange over Industrial Ethernet with TCP/IP protocol (with Open user communication instructions)	Yes
Open communication over ISO on TCP	Data exchange over Industrial Ethernet with ISO on TCP protocol (with Open user communication instructions)	Yes
Open communication over UDP	Data exchange over Industrial Ethernet with UDP protocol (with Open user communication instructions)	Yes

[1] The CPU supports SNMP V1 without TRAPs (alarm frames).

Available connections

The CPU supports a fixed number of maximum simultaneous asynchronous communication connections for PROFINET; you cannot change these values. You can configure the "Free available connections" to increase the number of any category as required by your application.

Some connection types have a fixed number of reserved resources (sometimes called guaranteed). This means that the CPU is guaranteed to support up to the number of reserved resources for the connection type. Additional connections beyond the number of reserved

resources can be made for a connection type, but those connection resources must come from the "dynamic" resources pool.

The dynamic resources (sometimes called Free) are a collection of resources that can be used for any connection type. These resources are used by connections that do not have any reserved resources or by connections that have used up all of their reserved resources.

S7-1200 G2 CPUs have 10 reserved connection resources and 78 dynamic resources for a total of 88 connection resources.

Based upon the allocated connection resources, the following number of connections per CPU are available:

Type	Maximum guaranteed connections	Maximum dynamic connections	Total connections possible[1]
Programming device (PG) communication	4	78	82
Human Machine Interface (HMI) communication	4	78	82
S7 communication	0	78	78
Open User communication	0	78	78
Web communication	2	78	80

[1] Since the dynamic connections are shared, it is not possible to max out all connections simultaneously.

For an example, the CPU has four available PG connection resources. Depending on the current PG functions in use, the PG might actually use one, two, three, or four of its available connection resources. You can always use one PG.

NOTE

Web server connections: The CPU provides connections for multiple Web browsers. The number of browsers that the CPU can simultaneously support depends upon how many connections a given Web browser requests/utilizes and the number of dynamic connection resources available in the CPU.

NOTE

The Open user communication, S7 connection, HMI, programming device, and Web server communication connections can utilize multiple connection resources based upon the features currently being used.

5.5 Supported certificates

Secure communication services require certificates with certain security parameters.

You can create or select these certificates from the following areas in the TIA Portal "General" tab of the CPU "Properties" window:

- "Web server > Security": Use for the generation and assignment of Web server certificates.
- "Protection & Security > Connection mechanisms": Use for the generation or assignment of PLC communication or Secure PG/PC and HMI communication certificates.
- "Protection & Security > Certificate manager": Use for the generation or assignment of all types of certificates. The default setting for the creation of certificates is TLS certificates for Secure Open User Communication (Secure OUC).

For more information on generating and assigning certificates or certificate parameters, refer to the TIA Portal Information System.

5.6 PROFINET

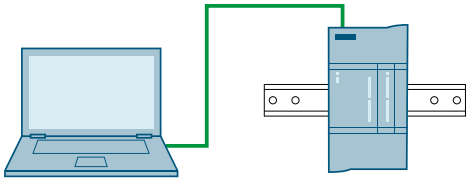
5.6.1 CPU communication

The CPU can communicate with the following devices:

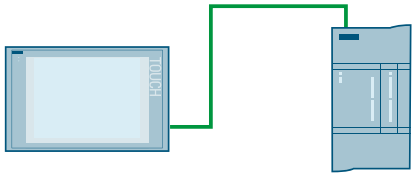
- Other CPUs
- Programming devices
- HMI devices
- Non-Siemens devices using standard TCP communications protocols

Example connections are as follows:

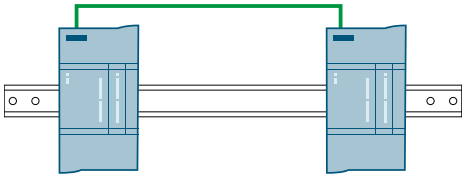
Programming device connected to the CPU (Page 156)



HMI connected to the CPU (Page 160)



A CPU connected to another CPU (Page 161)

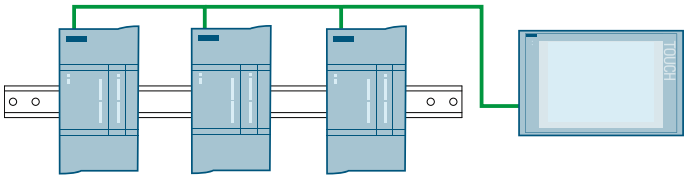


Ethernet switching

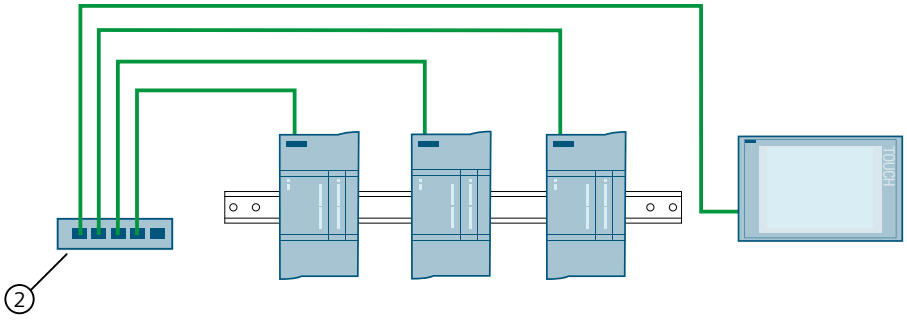
The S7-1200 G2 CPUs have a built-in 2-port Ethernet switch. You can use these built-in switches to create a network.

Example connections are as follows:

Multiple CPUs connected to an HMI device using the built-in 2-port Ethernet switch



Multiple CPUs connected to an HMI device using an external ethernet switch

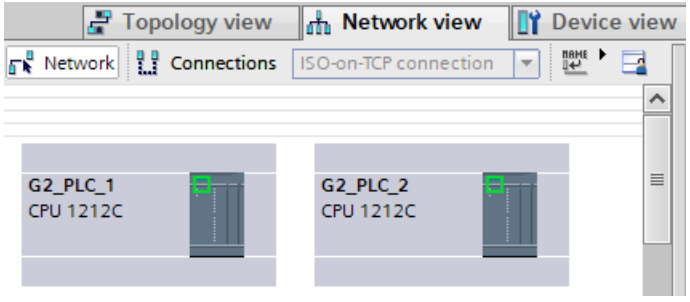


② External Ethernet switch

5.6.2 Creating a network connection

Use the "Network view" of Device configuration to create the network connections between the devices in your project.

1. Select "Network view" to display the devices to be connected.

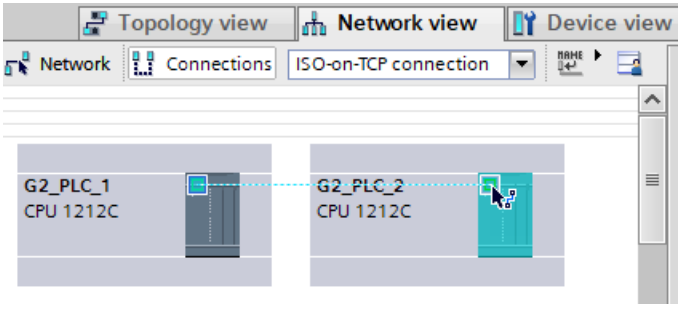


2. Select the "Connections" tab in the toolbar of Network view and choose your connection type from the dropdown menu.

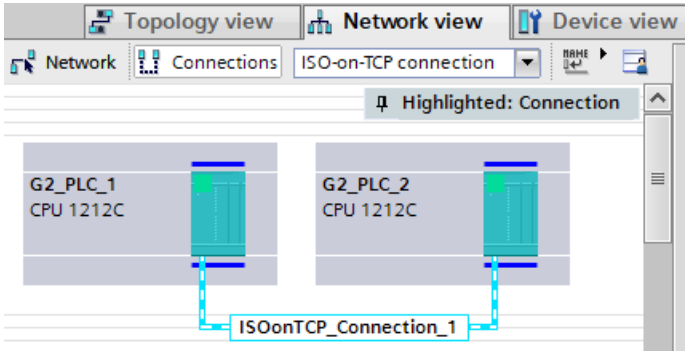
   Note: the S7-1200 G2 supports the following connections:

   – S7 connection (Page 179)
   – ISO-on-TCP connection (Page 150)
   – TCP connection (Page 149)
   – UDP connection (Page 150)
   – HMI connection (Page 160) (PLC to an HMI)

3. Select the port on one device and drag the connection to the port on the second device.



4. Release the mouse button to create the network connection.



After creating the network connection, use the "Properties" tab of the inspector window to configure the parameters of the network.

5.6.3 Configuring the Local/Partner connection path

A Local/Partner (remote) connection defines a logical assignment of two communication partners to establish communication services. A connection defines the following:

- Communication partners involved (one active, one passive)
- Type of connection (for example, a PLC, HMI, or device connection)
- Connection path

Communication partners execute the instructions to set up and establish the communication connection. You use instruction parameters to specify the active and passive communication end point partners. After the STEP 7 program sets up and establishes the connection, the CPU automatically maintains and monitors the connection.

If the connection is terminated (for example, due to a line break), the active partner attempts to re-establish the configured connection. You do not have to execute the communication instruction again.

For more information, see "Using Open User Communication > Connection configuration" and "Using Open User Communication > Connection parameters" in the TIA Portal Information System.

5.6.4 Locating the Ethernet (MAC) address on the CPU

In PROFINET networking, a Media Access Control address (MAC address) is an identifier assigned to the network interface by the manufacturer for identification. A MAC address usually encodes the manufacturer's registered identification number.

The standard (IEEE 802.3) format for printing MAC addresses in human-friendly form is six groups of two hexadecimal digits, separated by hyphens (-) or colons (:), in transmission order, (for example, 01-23-45-67-89-ab or 01:23:45:67:89:ab).

Each CPU is loaded at the factory with a permanent, unique MAC address. You cannot change the MAC address of a CPU.

The MAC address is printed on the front, upper-left corner of the CPU. Note that you have to lower the upper door to see the MAC address information.

The CPU interface is designated as X1, and initially has no IP address, only a factory-installed MAC address. PROFINET communication requires that all devices be assigned a unique IP address.

NOTE

Three sequential MAC addresses are assigned to the CPU:

- The lowest number, the number printed on the CPU, is for the X1 interface.
- The next higher number is for port P1R.
- The highest number is for port P2R.

The low-level protocols (Page 169) require the MAC addresses for P1R and P2R.

5.6.5 Assigning Internet Protocol (IP) addresses

5.6.5.1 Assigning IP addresses to programming and network devices

If the network interface of your programming device connects to a local area network (LAN) with multiple subnets, both the programming device and the CPU must be on the same subnet. You assign the subnet as a combination of the IP address and subnet mask for the device. See your local network administrator for help.

The Network ID of a Class C IP address is the first three octets of the IP address. The network ID of 211.154.184.16, for example, is 211.154.184. This network ID uniquely identifies your IP network. The subnet mask normally has a value of 255.255.255.0. Because your computer is on a plant LAN, however, the subnet mask might have various values, for example, 255.255.254.0, to set up unique subnets. The subnet mask, when combined with the device IP address in a logical AND operation, defines the boundaries of an IP subnet.

NOTE

You must assign unique IP addresses to all devices on your subnet.

⚠ WARNING

Unauthorized access to a CPU

Users with CPU full access or full access (incl. fail-safe) privileges have privileges to read and write PLC variables. Regardless of the access level for the CPU, Web server users can have privileges to modify PLC data and execute functions. Unauthorized access to the CPU can disrupt process operation.

Siemens recommends that you observe the following security practices:

- Enable Access control under "Protection & Security > Access control".
- Do not enable the "Anonymous" user.
- Use strong passwords, as defined in STEP 7.
- Use a secure Virtual Private Network (VPN) to connect to the S7-1200 PLC from a location outside your protected network.
- Perform error-checking and range-checking on your variables in your program logic because Web server or users can change PLC variables to invalid values.

Disruption of process operations can result in death, severe personal injury, and/or property damage.

NOTE

A secondary network adapter card is useful when you do not want your CPU on your company LAN. During initial testing or commissioning tests, this arrangement is particularly useful.

Assigning or checking the IP address of your programming device

To assign or check your programming device's IP address, follow these steps:

1. Open the Control Panel.
2. Navigate to the "Network and Sharing Center".
3. Click "Change adapter settings" in the left column.
4. Right-click the network interface connected to your CPU.
5. Select "Properties" to open the properties dialog.
6. In the properties dialog, select the checkbox for "Internet Protocol Version 4 (TCP/IPv4)".
7. Click the "Properties" button.

8. Select "Obtain an IP address automatically" or to enter a static IP address select "Use the following IP address".

   If you selected "Use the following IP address", set the IP address and subnet mask:

   – Set the IP address to use the same Network ID and same subnet as the CPU. For example, if the CPU IP address is **192.168.0**.1, you could set the IP address to **192.168.0**.200.
   – Select a subnet mask of 255.255.255.0.
   – Leave the default gateway blank.

Consult your network administrator to help you set up a network configuration to allow you to connect to the S7-1200 G2 CPU.

5.6.5.2 Checking the IP address and MAC address of your network interface

To check the MAC and IP addresses of your network interface in STEP 7, follow these steps:

1. In the "Project tree", expand "Online access".
2. Right-click the required network interface, and select "Properties".
3. In the dialog, expand "Configurations", and select "Industrial Ethernet".

The window displays the MAC and IP addresses of the network interface.

5.6.5.3 Assigning an IP address to an online CPU

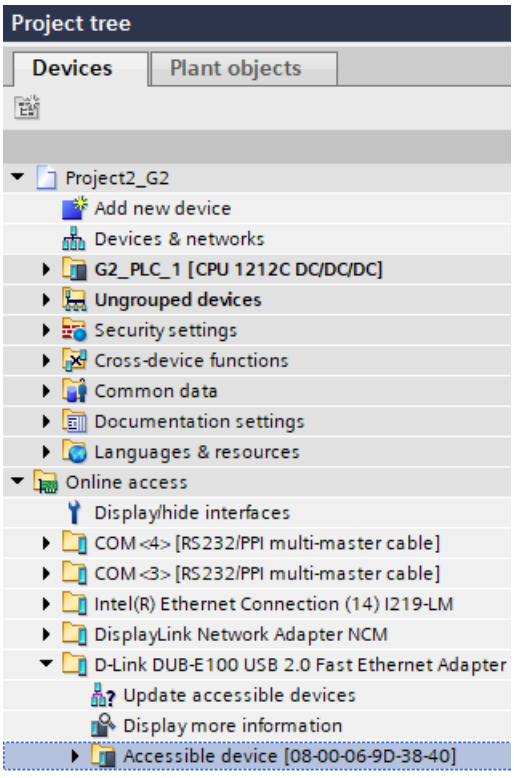
You can assign an IP address to a network device online. This is particularly useful in an initial device configuration.

To verify that the CPU does not have a configured IP address, do the following:

1. In the "Project tree", expand "Online access".
2. Expand the network in which the device is located.

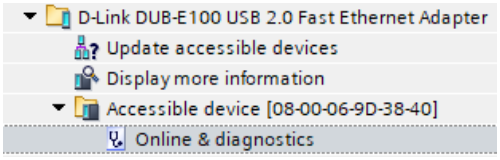
3. Double-click "Update accessible devices".

   If STEP 7 displays a MAC address instead of an IP address, then no IP address has been assigned.



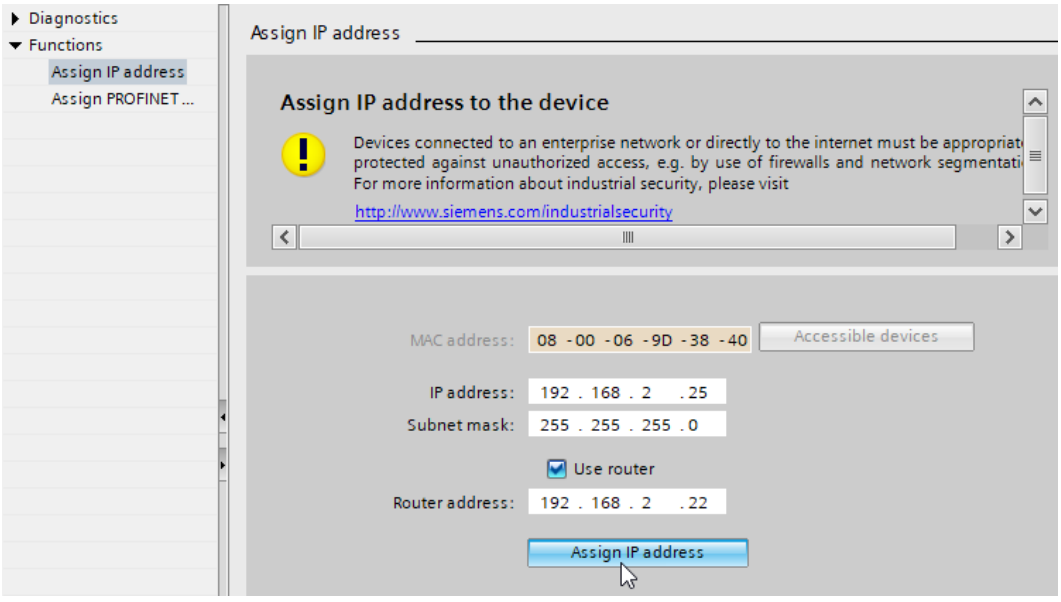
To assign an IP address, follow these steps:

1. Expand the PLC for which you want to assign an IP address.
2. Double-click "Online & diagnostics".

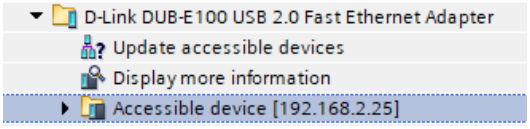


3. In the "Online & diagnostics" dialog, select "Functions > Assign IP address".

4. In the "IP address" field, enter your new IP address, and click "Assign IP address".



To verify that STEP 7 has assigned your new IP address to the CPU, double-click "Update accessible devices". It should now display the IP address that you configured.



5.6.5.4 Configuring an IP address for a CPU in your project

Configuring the PROFINET interface

In the Device configuration (Page 107) of the CPU, you can configure parameters for the PROFINET interface. Click the green PROFINET interface on the CPU and then select the "Properties" tab in the inspector window to display the PROFINET port.

Subnet and Subnet mask

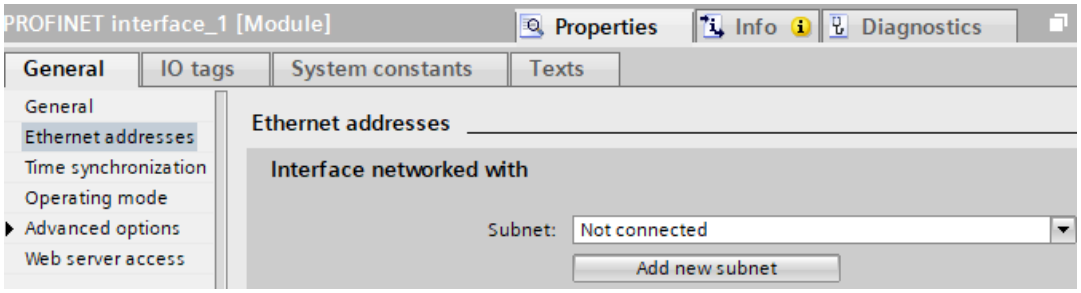
A subnet is a logical grouping of connected network devices. Nodes on a subnet tend to be located in close physical proximity to each other on a Local Area Network (LAN). A mask, known as the subnet mask or network mask, defines the boundaries of an IP subnet.

A subnet mask of 255.255.255.0 is suitable for a small local network. This means that all IP addresses on this network should have the same first three octets, and the various devices on this network are identified by the last octet (8-bit field). An example of this is to assign a subnet mask of 255.255.255.0 and an IP address of 192.168.2.0 through 192.168.2.255 to the devices on a small local network.

The only connection between different subnets is through a router. You must use an IP router if you use more than one subnet.

To set your subnet in your STEP 7 project, follow these steps:

1. In Device configuration, select the "Properties" Tab.
2. Under the "General" tab, select "Ethernet addresses".
3. In the "Interface networked with" section, click "Add new subnet" to create a new subnet. The default "Not connected" provides a local connection. You can choose a previously added subnet from the dropdown menu.



Internet Protocol (IP) address

Each device must also have an Internet Protocol (IP) address. This address allows the device to deliver data on a more complex, routed network. Each IP address is divided into four 8-bit octets and is expressed in a dotted, decimal format (for example, 211.154.184.16). The first part of the IP address is used for the Network ID, and the second part of the address is for the Host ID which is unique for each device on the network. An IP address of 192.168.x.y is a standard designation recognized as part of a private network that is not routed on the Internet.

In your STEP 7 project, you can configure how the IP address is set. In Device configuration, click the "Properties" Tab and select "Ethernet addresses". Choose one of the following options:

- Set IP address in the project
- IP address from DHCP (Dynamic HostConfiguration Protocol) server
- IP address is set directly at the device

Optionally, select "Use router" and enter the router's IP address if your network uses a router.

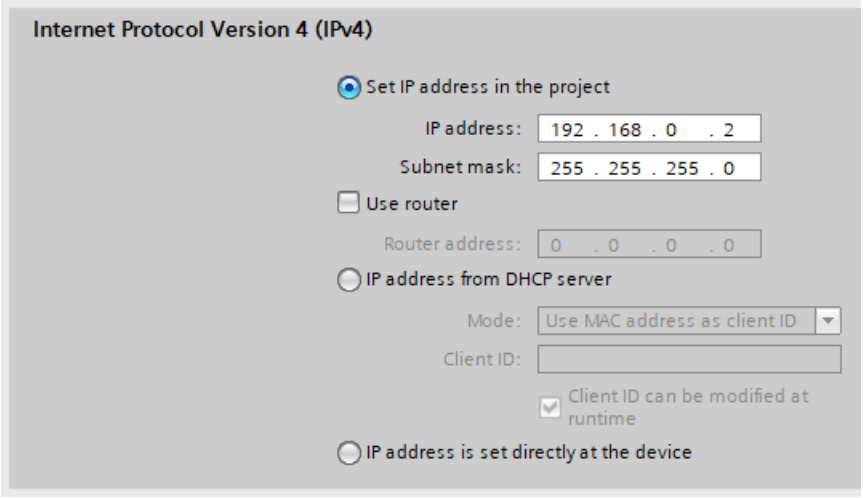


Table 5-4 Parameters for the IP address

Protocol	Parameter	Description
Set IP address in the project	IP address	Assigned IP address for the CPU
	Subnet mask	Assigned subnet mask
Use router		Click the checkbox to indicate the use of an IP router. Routers are the link between LANs. Using a router, a computer in a LAN can send messages to any other networks, which might have other LANs behind them. If the destination of the data is not within the LAN, the router forwards the data to another network or group of networks where it can be delivered to its destination. Routers rely on IP addresses to deliver and receive data packets.
	Router address	Assigned IP address for the router, if applicable
IP address from DHCP server	Mode	An external DHCP server provides the IP address based on either the MAC address of your network interface or an optional client ID. However, if the client ID is not configured, the server will not provide the MAC address as the identification. For more information, see "Assigning addresses via DHCP" in the TIA Portal Information System.
	Client ID	
IP address is set directly at the device		Click the radio button set the IP address set directly at the device.

NOTE

The download operation sets all IP addresses for devices configured as "Set IP address in the project". If the CPU does not have a pre-configured IP address, download to the accessible device with the MAC address of your target device. If your CPU is connected to a router on a network, you must also enter the IP address of the router.

The "IP address is set directly at the device" radio button allows you to change the IP address through a tool such as the SIMATIC Automation Tool, Online & Diagnostics in the TIA Portal (Page 140), or by using the T_CONFIG instruction (Page 151) after the program is downloaded.

⚠ WARNING

Downloading a hardware configuration with "IP address is set directly at the device"

After downloading a hardware configuration with the "IP address is set directly at the device" option enabled, you cannot use communication functions to transition the CPU from RUN to STOP or from STOP to RUN until you set an IP address. User equipment continues to run under these conditions and can result in unexpected equipment and process operations.

Ensure that your CPU IP address(es) are set before using the CPU in an actual automation environment. This can be done by using STEP 7, the SIMATIC Automation Tool, or an attached HMI device in conjunction with the T_CONFIG instruction.

Unexpected equipment and process operations can cause death, severe personal injury, or property damage if proper precautions are not taken.

⚠ WARNING

Condition in which PROFINET network might stop

Changing the IP address of a CPU online or from the STEP 7 program can create a condition where the PROFINET network might stop. If the CPU's IP address is changed to one outside the subnet, the PROFINET network loses communication, and all data exchange stops. User equipment might be configured to keep running under these conditions. Loss of PROFINET communication can result in unexpected machine or process operations.

If an IP address must be changed, ensure that the new IP address lies within the subnet.

Unexpected machine or process operations can cause death, severe personal injury, or property damage if proper precautions are not taken.

Configuring the PROFINET port

By default, the CPU configures port(s) of the PROFINET interface for autonegotiation, a feature that allows connected devices to automatically determine and configure the best possible parameters for communication. For autonegotiation to function properly, you must configure both stations to autonegotiate. If one station has a fixed configuration (for example, full-duplex at 100 Mbps) and the other station is set to autonegotiate, then autonegotiation fails, resulting in half-duplex operation.

To overcome this limitation of autonegotiation, the S7-1200 G2 provides an option to disable autonegotiation. When you disable autonegotiation, the S7-1200 G2 is automatically configured for full-duplex operation at 100 Mbps.

To set the transmission rate and duplex to a fixed value for each port, follow these steps:

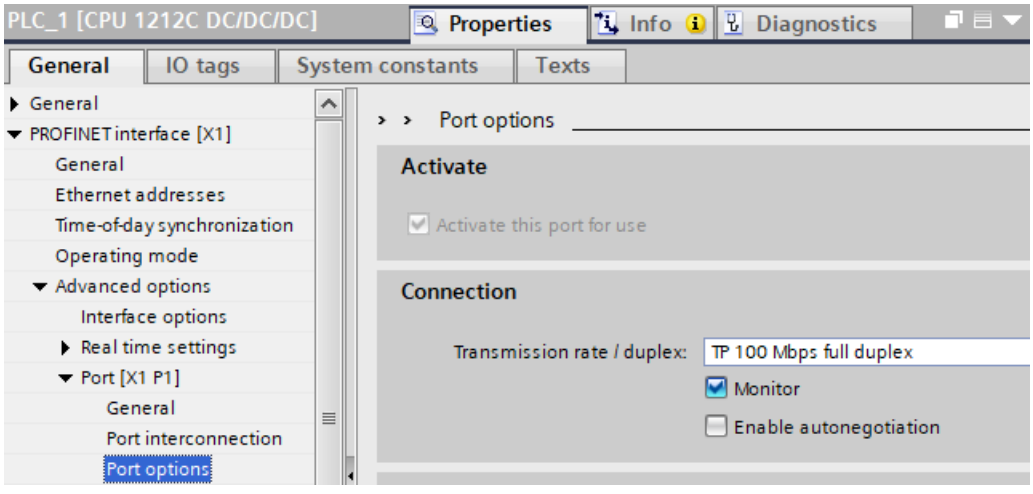
1. Select Advanced options and the port you need to configure. Then, select Port options.
2. In the Connection, Transmission rate / duplex field, select one of the following:
   - Automatic: The CPU and the peer device determine the port's transmission rate and duplex by autonegotiation.
   - TP 100 Mbps full-duplex: If you disable autonegotiation, the port operates at 100 Mbps full-duplex. If you enable autonegotiation, the port can operate at 100 Mbps full-duplex or another transmission rate / duplex that is autonegotiated between the CPU and the peer device. This places a message in the diagnostics buffer if "Monitor" is selected (see below).

You have the option to select the following parameters:

- Monitor: When you select this checkbox, the CPU places a message in the diagnostics buffer if any of the following occur at the port:
  - A link cannot be established
  - An established link fails
  - You select "TP 100 Mbps full-duplex" as the Transmission rate / duplex, and the CPU establishes a link using autonegotiation with the negotiated transmission rate not equal to 100 Mbps or the negotiated duplex equal to half-duplex.
- Enable autonegotiation: Once you set the Transmission rate / duplex field to full-duplex at 100 Mbps, you can then disable autonegotiation. Deselect the "Enable autonegotiation" checkbox to disable autonegotiation.

NOTE

If you disable autonegotiation, the CPU and the peer device do not negotiate the port's transmission rate and duplex.

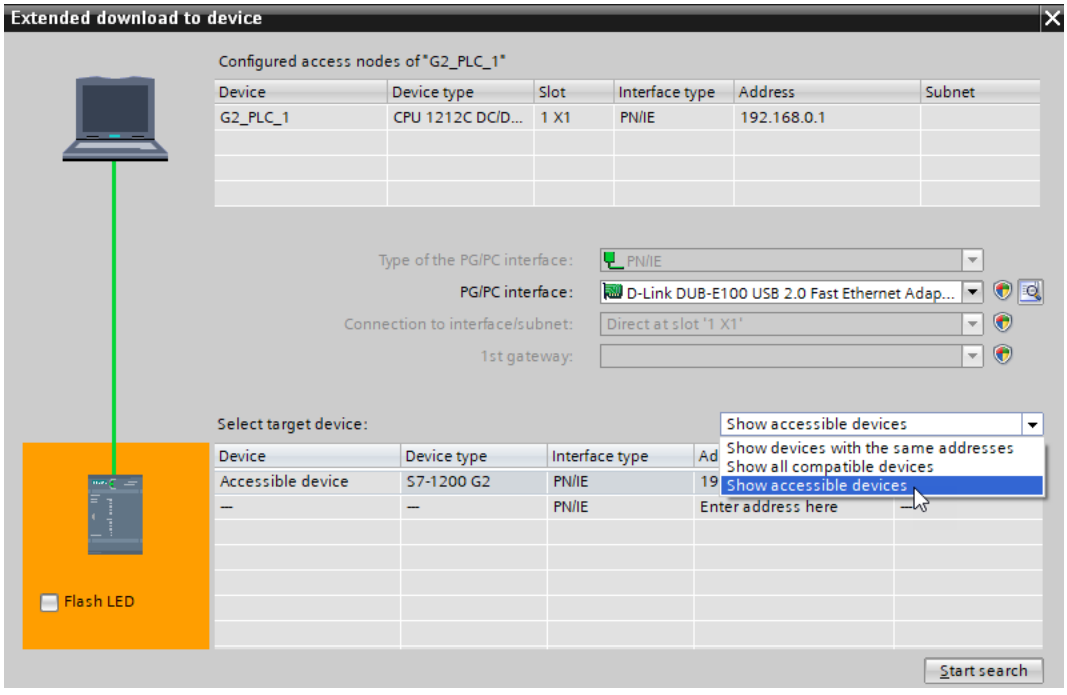


5.6.6 Testing the PROFINET network

After completing the configuration, download the project (Page 118) to the CPU.

Using the "Extended download to device" dialog to test for connected network devices

The S7-1200 G2 CPU "Download to device" function and its "Extended download to device" dialog show all accessible network devices and whether unique IP addresses have been assigned to all devices. To display all accessible and available devices with their assigned MAC or IP addresses, select "Show accessible devices" from the "Select target device" dropdown menu.



If the required network device is not in this list, communications to that device have been interrupted. The device and network must be investigated for hardware and/or configuration errors.

5.6.7 PROFINET device startup time, naming, and address assignment

PROFINET IO can extend the startup time for your system (Configuration time). More devices and slow devices impact the amount of time it takes to switch to RUN.

On your PROFINET network, you can have a maximum of 31 PROFINET IO devices, reducing to 30 devices if the CPU is an I-Device and 29 if the CPU is a shared I-Device.

All PROFINET devices must have a Device name and an IP Address.

Each station (or IO Device) starts up independently on startup, and this affects the overall CPU startup time. If you set the "Configuration time" too low, there might not be a sufficient overall CPU startup time for all stations to complete startup. If this situation occurs, false station errors will result.

The default Configuration time is 60,000 ms (1 minute). You can configure this in CPU Properties > Startup > Configuration time.

PROFINET address assignment at system startup

The controller broadcasts the names of the devices to the network, and the devices respond with their MAC addresses. The controller then assigns an IP address to the device using the PROFINET DCP protocol:

- If the MAC address has a configured IP address, then the station performs startup.
- If the MAC address does not have a configured IP address, STEP 7 assigns the address that is configured in the project, and the station then performs startup.

If there is a problem with this process, a station error occurs and no startup takes place. This situation causes the configurable time-out value to be exceeded.

5.6.8 Configuring Network Time Protocol (NTP) synchronization

The Network Time Protocol (NTP) is widely used to synchronize the clocks of computer systems to Internet time servers. In NTP mode, the CPU sends time-of-day queries at regular intervals (in the client mode) to the NTP server in the subnet (LAN). Based on the replies from the server, the NTP determines the most reliable and most accurate time and synchronizes the time of day on the querying module.

⚠ WARNING

Risk of network attacks through Network Time Protocol (NTP) synchronization

If an attacker can access your networks through Network Time Protocol (NTP) synchronization, the attacker can possibly disrupt control of your process by shifting the CPU system time.

The S7-1200 G2 CPU disables the NTP client feature by default. When you enable the NTP feature, then only the IP addresses that you configure can act as NTP servers. You must configure the NTP feature to allow CPU system time corrections from remote servers.

The S7-1200 G2 CPU supports "time of day" interrupts and clock instructions that depend upon accurate CPU system time. If you configure NTP and accept time synchronization from a server, you must ensure that the server is a trusted source. Failure to do so can cause a security breach that allows an unknown user to disrupt control of your process by shifting the CPU system time.

For security information and recommendations, see the "Operational Guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html)" white paper on the Siemens Industrial Cybersecurity Web site.

Disruptions to process control can cause death, severe injury, or property damage.

The advantage of NTP mode is that it allows the time to be synchronized across subnets.

For more information on configuring the NTP in your STEP 7 program, refer to "Time-of-day synchronization with NTP" in the TIA Portal Information System.

5.6.9 Open user communication

5.6.9.1 Protocols

The integrated PROFINET interface of the CPU supports multiple communications standards over an Ethernet network:

- Transport Control Protocol (TCP) (Page 149)
- ISO on TCP (Page 150)
- User Datagram Protocol (UDP) (Page 150)

Table 5-5 Protocols and communication instructions for each

Protocol	Usage examples	Entering data in the receive area	Communication instructions	Addressing type
TCP (Page 149)	CPU-to-CPU communication Transport of frames	Ad hoc mode (Page 151)	Only TRCV_C and TRCV	Assigns port numbers to the Local (active) and Partner (passive) devices
		Data reception with specified length	TSEND_C, TRCV_C, TCON, TCONSettings, TDISCON, TSEND, TRCV, T_RESET, and T_DIAG	
ISO on TCP (Page 150)	CPU-to-CPU communication Message fragmentation and reassembly	Ad hoc mode	Only TRCV_C and TRCV	Assigns TSAPs to the Local (active) and Partner (passive) devices
		Protocol-controlled	TSEND_C, TRCV_C, TCON, TCONSettings, TDISCON, TSEND, TRCV, T_RESET, and T_DIAG	
UDP (Page 150)	CPU-to-CPU communication STEP 7 program communications	User Datagram Protocol	TUSEND and TURCV	Assigns port numbers to the Local (active) and Partner (passive) devices, but is not a dedicated connection

5.6.9.2 TCP, ISO on TCP, and UDP

TCP

Transport Control Protocol (TCP) is a standard protocol described by RFC 793: Transmission Control Protocol (https://www.rfc-editor.org/info/rfc793). The primary purpose of TCP is to provide reliable connection service between pairs of processes. Most of the user application protocols, such as TELNET and FTP, commonly use TCP. This protocol offers the following features and capabilities:

- Offers an efficient communications protocol that is closely tied to the hardware
- Allows for the handling of data amounts up to 8192 bytes.
- Provides extensive facilities for applications, notably error recovery, flow control, and reliability
- Operates as a connection-oriented protocol
- Offers flexibly for integration with third-party systems that exclusively support TCP
- Provides routing capabilities
- Supports only static data lengths
- Acknowledges messages

- Addresses applications using port numbers
- Requires programming effort for data management due to the SEND / RECEIVE programming interface

ISO on TCP

International Organization for Standardization on Transport Control Protocol, commonly known as "ISO on TCP", is described by RFC 1006 (https://www.rfc-editor.org/info/rfc1006) as a mechanism that enables ISO applications to be ported to the TCP/IP network. This protocol has the following features and capabilities:

- Offers an efficient communications protocol that is closely tied to the hardware
- Allows for the handling of medium-sized to large data amounts (up to 8192 bytes)
- Provides routing capabilities; can be used in WAN
- Supports dynamic data lengths
- Requires programming effort for data management due to the SEND / RECEIVE programming interface

In contrast to TCP, the messages feature an end-of-data identification and are message-oriented.

Using Transport Service Access Points (TSAPs), TCP protocol allows multiple connections to a single IP address (up to 64K connections). With RFC 1006, TSAPs uniquely identify these communication end point connections to an IP address.

UDP

UDP is a standard protocol described by RFC 768: User Datagram Protocol (https://www.rfc-editor.org/info/rfc768). UDP is a simpler transport control protocol than TCP that provides a mechanism for one application to send a datagram to another; however, delivery of data is not guaranteed. UDP has the following features and capabilities:

- Offers a quick communications protocol
- Allows for the handling of small-sized to medium data amounts (up to 2048 bytes)
- Provides a thin layer that yields low overheads
- Offers flexibly for integration with many third-party systems
- Provides routing capabilities
- Uses port numbers to direct the datagrams
- Requires the application to take responsibility for error recovery and security as messages are unacknowledged
- Requires programming effort for data management due to the SEND / RECEIVE programming interface

UDP supports broadcast communication. To use broadcast, you must configure the IP address portion of the ADDR configuration. For example: A CPU with an IP address of 192.168.2.10 and subnet mask of 255.255.255.0 would use a broadcast address of 192.168.2.255.

For further information, see "Configuring connections > Creating UDP/FDL connections with broadcast/multicast" in the TIA Portal Information System.

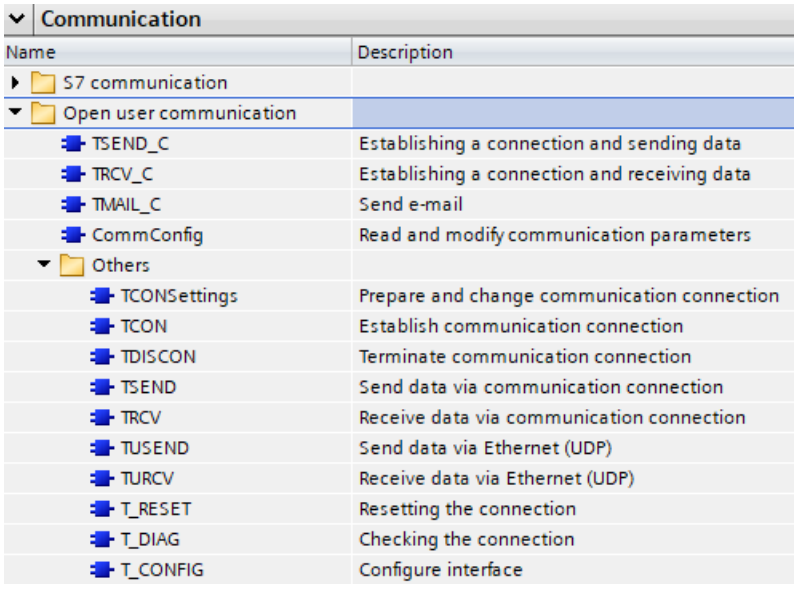
5.6.9.3 Ad hoc mode

Typically, TCP and ISO on TCP receive data packets of a specified length, ranging from 1 to 8192 bytes. However, the TRCV_C and TRCV communication instructions also provide an "ad hoc" communications mode that can receive data packets of a variable length from 1 to 1460 bytes.

For further information on using these instructions in ad hoc mode, see "TRCV_C: Receive information via Ethernet" and "TRCV: Receive data via communication connection" in the TIA Portal Information System

5.6.9.4 Instructions

Open user communication instructions provide for communication using various network protocols and include the following folder groups:



To find more information about each instruction and its use, follow these steps:

1. Open a program block to display the Instruction task card.
2. Expand an instruction group.
3. Do one of the following:
   - Select the individual instruction and press F1.
   - Hover over an individual instruction to reveal a TIA Portal tooltip. If you click the tooltip, or continue to hover over the instruction, a cascading tooltip provides a link to the corresponding instruction topic in the TIA Portal Information System.

You can also access the instructions under "Programming a PLC > Instructions" in the TIA Portal Information System.

NOTE

Choosing an instruction by PLC family

If the TIA Portal Information System presents an instruction differently within the tooltips or table of contents based on PLC family, follow the S7-1500 option for the instruction topic.

5.6.9.5 Connection IDs for the Open user communication instructions

Create an instance DB to configure the communications channel (or connection) between the devices by inserting the TSEND_C, TRCV_C or TCON instructions into STEP 7. To configure the parameters for the connection, utilize the Properties of the instruction. One of these parameters is the connection ID, which must be unique for the CPU. Ensure that each connection you create has a different DB and connection ID. Also, note the following:

- Both the local CPU and the partner CPU can use the same connection ID number for the same connection, but the connection ID numbers are not required to match. The connection ID number is relevant only for the Open user communication instructions within the user program of the individual CPU.
- You can use any number in the range of 1 to 4095 for the connection ID of the CPU. However, configuring the connection IDs sequentially from "1" provides an easy method for tracking the number of connections in use for a specific CPU. Alternatively, you can use the TCONSettings instruction to request a connection ID from the CPU.

  NOTE

  Each TSEND_C, TRCV_C, or TCON instruction in STEP 7 creates a new connection. It is important to use the correct connection ID for each connection.

For more information, see the following topics in the Open User Communication chapter of the TIA Portal Information System:

- TCON: Establish communication connection (S7-1200, S7-1500)
- TSEND_C: Establishing a connection and sending data
- TRCV_C: Establishing a connection and receiving data

5.6.9.6 Parameters for the OUC connection

The TSEND_C, TRCV_C, and TCON instructions require connection-related parameters to connect to the partner device. The TCON_Param structure assigns these parameters for the TCP, ISO-on-TCP, and UDP protocols. Use the "Configuration" tab of the "Properties" of the instruction to specify these parameters. If the "Configuration" tab is not accessible, provide the TCON_Param structure in the instruction parameters.

For more information, see the following topics in the "Using Open User Communication > Connection parameters" area of the TIA Portal Information System:

- Connection parameters with structure according to TCON_Param
- Connection parameters with structure according to TCON_IP_v4
- Connection parameters in accordance with TCON_QDN (S7-1500)
- Connection parameters in accordance with TCON_QDN_SEC (S7-1500)

- Connection parameters according to TCON_IP_V4_SEC (S7-1500)
- Connection parameters with structure according to TCON_IP_RFC

NOTE

If you specify the address of a device as an FQDN via the connection types of TCON_QDN or TCON_QDN_SEC, you need to configure a DNS server (Page 153).

NOTE

Connection types of TCON_QDN_SEC and TCON_IP_V4_SEC use TLS for security (Page 153).

5.6.9.7 Transport Layer Security (TLS)

TLS is Transport Layer Security in the application layer of data communications. TLS increases security and privacy in communication between the S7-1200 G2 CPU and other devices.

5.6.9.8 Configuring DNS

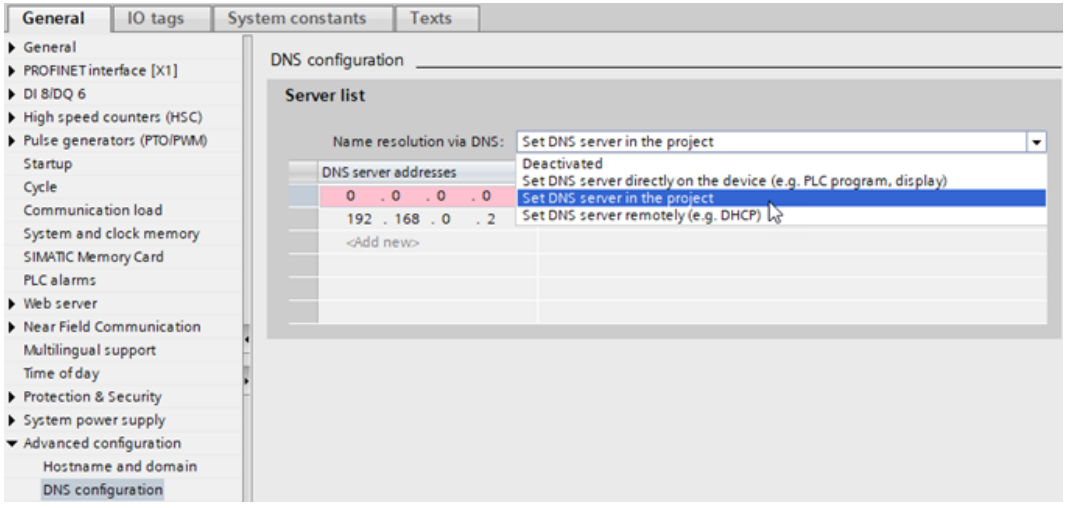
A DNS server might be required when the module itself, a communications partner, or for example an FTP server should be reachable via the host name (FQDN). If you specify the address of a connection partner as FQDN, configure a DNS server. In this case, the IP address of the connection partner is obtained via the configured DNS server.

To use DNS, you must have at least one DNS server in your network, and you must configure at least one DNS server for the S7-1200 G2 CPU.

To configure a DNS server, follow these steps:

1. From the Device view for your S7-1200 G2 CPU, navigate to "Properties > General".
2. Navigate to "Advanced configuration > DNS configuration" to display the configuration pane.

3. Select "Set DNS servers in the project" in the dropdown menu.



4. In the Server list table, click "<Add new>" and enter the IP address of your DNS server.

5.6.9.9 Configuring an OUC connection in the TIA Portal

For complete information on configuring an Open User Communication connection in STEP 7, see the following topics and chapters under "Using Open User Communication" in the TIA Portal Information System:

- Basics of Open User Communication
- Connection configuration
- Connection parameters

5.6.9.10 Common parameters for instructions

REQ input parameter

Many of the OUC instructions use the REQ input to initiate the operation on a low to high transition. The REQ input must be high (TRUE) for one execution of an instruction, but the REQ input can remain TRUE for as long as you choose. The instruction does not initiate another operation until it has been executed with the REQ input FALSE so that the instruction can reset the history state of the REQ input. This is required so that the instruction can detect the low to high transition to initiate the next operation.

When you place one of these instructions in your program, STEP 7 prompts you to identify the instance DB. Use a unique DB for each instruction call. This ensures that each instruction properly handles inputs such as REQ.

ID input parameter

The ID parameter is a reference to the "Local ID (hex)" on the "Network view" of "Devices and networks" in STEP 7 and is the ID of the network that you want to use for this communication block. The ID must be identical to the associated parameter ID in the local connection description.

DONE, NDR, BUSY, ERROR, and STATUS output parameters

The following parameters are common to the OUC instructions and provide outputs describing the completion status:

Table 5-6 Open User Communication instruction output parameters

Parameter	Data type	Default	Description
DONE	Bool	FALSE	Is set TRUE for one execution to indicate that the last request completed without errors; otherwise, FALSE.
NDR	Bool	FALSE	Is set TRUE for one execution to indicate that the requested action has completed without error and new data has been received; otherwise, FALSE.
BUSY	Bool	FALSE	Is set TRUE when active to indicate that: • The job is not yet complete. • A new job cannot be triggered. Is set FALSE when job is complete.
ERROR	Bool	FALSE	Is set TRUE for one execution to indicate that the last request completed with errors, with the applicable error code in STATUS; otherwise, FALSE.
STATUS	Word	0	Is set to a status value as follows: • If the DONE or NDR bit is set, then STATUS is set to 0 or to an informational code. • If the ERROR bit is set, then STATUS is set to an error code. • If none of the above bits are set, then the instruction returns status results that describe the current state of the function. STATUS retains its value for the duration of the execution of the function.

NOTE

Note that DONE, NDR, and ERROR are set for one execution only.

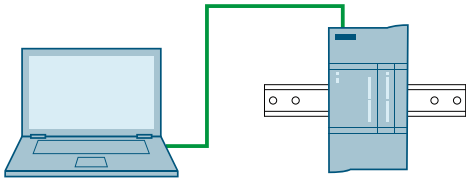
5.6.9.11 Restricted TSAPs or port numbers for passive ISO and TCP communication

If you use the TCON instruction to set up and establish a passive communications connection, do not use the following restricted port addresses:

- ISO TSAP (passive):
  - 01.00, 01.01, 02.00, 02.01, 03.00, 03.01
  - 10.00, 10.01, 11.00, 11.01, ... BF.00, BF.01
- TCP port (passive) and UDP port (passive):
  - 20, 21, 25, 80, 102, 443, 5001, 34962, 34963, 34964, 49152 to 65535

5.6.10 Communication with a programming device

A CPU can communicate with a STEP 7 programming device on a network.



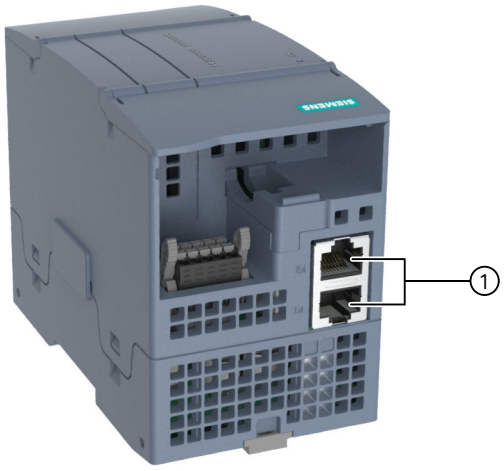
5.6.10.1 Establishing the hardware communications connection

PROFINET interfaces establish the physical connections between a programming device and a CPU. Since Auto-Cross-Over functionality is built into the CPU, either a standard or crossover Ethernet cable can be used for the interface. An Ethernet switch is not required to connect a programming device directly to a CPU.

Follow the steps below to create the hardware connection between a programming device and a CPU:

1. Install the CPU (Page 30).
2. Plug the Ethernet cable into one of the two PROFINET ports located on the top left of the CPU.

3. Connect the Ethernet cable to the programming device.

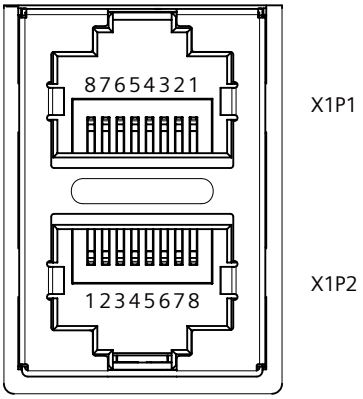


① PROFINET ports

PROFINET interface X1 port pinouts

S7-1200 G2 CPUs connect to the PROFINET network using standard female RJ45 jacks. All S7-1200 G2 CPUs have dual-ports, but one interface. The connector pinout is the same for all CPUs.

The dual-ports of S7-1200 G2 CPUs have a standard Ethernet MDI-X pin configuration as follows:

Pin	Signal name	Description	RJ45 female jack pinout
1	TD+	Transmit data	
2	TD-		
3	RD+	Receive data	
4	GND	Ground	
5	GND		
6	RD-	Receive data	
7	GND	Ground	
8	GND		

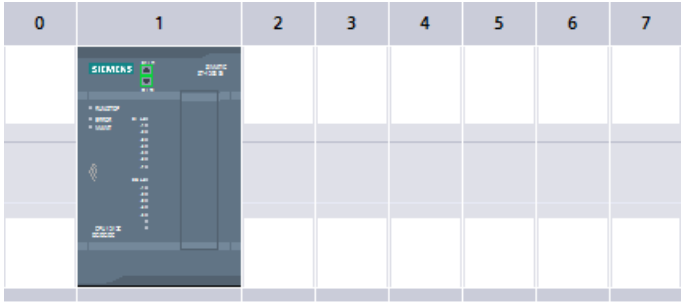
NOTE

All S7-1200 G2 CPUs are dual-port CPUs with no crossover between pins. There is an internal Ethernet switch in the units: The TD+/- and RD+/- pairs are not crossed over internally.

5.6.10.2 Configuring the devices

If you have already created a project with a CPU, open your project in STEP 7.

If not, create a project and insert a CPU (Page 108) into the rack.



Autonegotiation

If the port's configuration enables autonegotiation, the S7-1200 G2 CPU automatically detects the cable type and swaps the transmit/receive lines, if needed. If the port's configuration disables autonegotiation, the CPU also disables this automatic swap. You configure a port's autonegotiation setting (Page 142) in the TIA Portal's port options dialog. This is a port-specific advanced option for the PROFINET interface (X1) of the CPU's properties.

5.6.10.3 Testing the PROFINET network

After completing the configuration, download the project to the CPU. The download operation sets all IP addresses for devices configured as "Set IP address in the project".

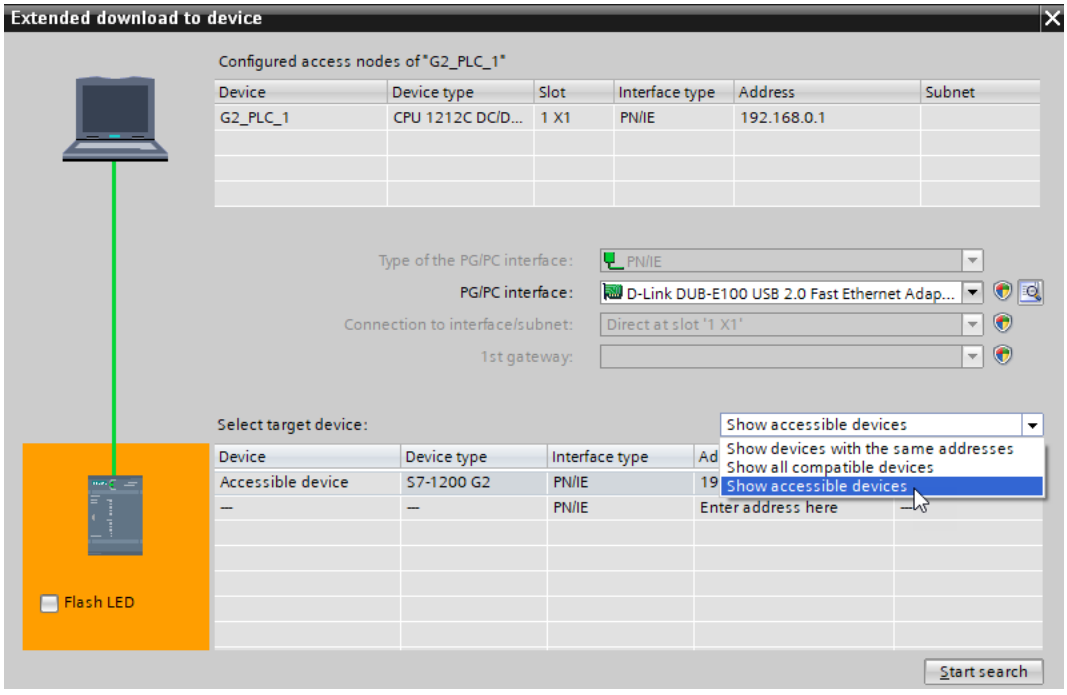
Assigning an IP address to an online CPU

The CPU does not have a pre-configured IP address. You must manually assign an IP address for the CPU in one of the following ways:

- Assign an IP address to an online CPU (Page 140).
- Assign IP address for a CPU in your project (Page 142). You must configure the IP address, save the configuration, and download it to the CPU.

Using the "Extended download to device" dialog to test for connected network devices

The CPU "Download to device" function and its "Extended download to device" dialog can show all accessible network devices and whether or not unique IP addresses have been assigned to all devices. To display all accessible and available devices with their assigned MAC or IP addresses, select "Show all accessible devices" from the dropdown menu.



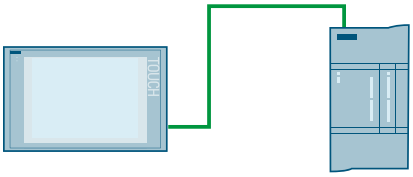
If the required network device is not in this list, communications to that device have been interrupted for some reason. Check the device and network for hardware or configuration errors.

5.6.10.4 Assigning Internet Protocol (IP) addresses

In a PROFINET network, each device must have an Internet Protocol (IP) address. This address allows the device to deliver data on a more complex, routed network:

- If you have programming or other network devices that use a network interface connected to your plant LAN or an Ethernet-to-USB adapter connected to an isolated network, you must assign IP addresses to them. Refer to "Assigning IP addresses to programming and network devices" (Page 138) for more information.
- You can also assign an IP address to a CPU or network device online (Page 140). This is particularly useful in an initial device configuration.
- After you have configured your CPU or network device in your project, you can configure parameters for the PROFINET interface to include its IP address. Refer to "Configuring an IP address for a CPU in your project" (Page 142) for more information.

The S7-1200 G2 CPU supports PROFINET communications connections to HMIs.



Consider the following requirements when setting up communications between CPUs and HMIs:

Configuration/Setup:

- The PROFINET port of the CPU must be configured to connect with the HMI.
- The HMI must be setup and configured.
- The HMI configuration information is part of the CPU project and can be configured and downloaded from within the project.
- The HMI driver must be selected from the Device wizard. The S7-1200 G2 CPU uses the "SIMATIC S7-1500" driver to communicate with Basic or Comfort HMIs, and the "SIMATIC S7-1200/1500" driver to communicate with Unified panels.

NOTE

All S7-1200 G2 CPUs feature one PROFINET interface equipped with two ports that operate as an Ethernet switch.

Configuring communication between the HMI and a CPU

To configure communication between the HMI and a CPU, do the following:

1. Establish the hardware communications connection (Page 156). A PROFINET interface establishes the physical connection between an HMI and a CPU. Since Auto-Cross-Over functionality is built into the CPU, you can use either a standard or crossover Ethernet cable for the interface. An Ethernet switch is not required to connect an HMI and a CPU.
2. Configure the device (Page 158).
3. Configure the logical network connections between an HMI and a CPU (Page 136).
4. Configure an IP address in your project (Page 142). You must configure IP addresses for the HMI and the CPU.
5. Test the PROFINET network (Page 158). You must download the configuration for each CPU and HMI device.

Supported HMI connection mechanisms

You can configure your HMI communication preferences in the "Device configuration" for your CPU under "Protection & Security > Connection mechanisms". The S7-1200 G2 supports the following HMI connection mechanisms based on panel type:

Panel type	S7-1200 G2 supported HMI connection mechanisms
Basic Panel	GET/PUT (Page 179)
	Secure PG/PC and HMI Communication
Comfort Panel	GET/PUT
	Secure PG/PC and HMI Communication
Unified Panel	GET/PUT
	Secure PG/PC and HMI Communication
	Standard Modbus TCP/IP (Page 186)

Supported HMI tags and subscriptions

The CPU supports 2000 tags per HMI and up to 250 HMI subscriptions.

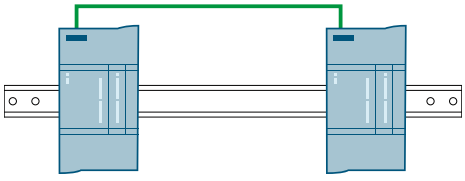
See also

Supported certificates (Page 135)

5.6.11 PLC-to-PLC communication

A CPU can communicate with another CPU on a network.

One way to configure two CPUs to communicate with each other is by using the TSEND_C and TRCV_C instructions.



Consider the following when setting up communications between two CPUs:

- Configuration/Setup
- Supported functions: Reading/Writing data to a peer CPU
- No Ethernet switch is required for one-to-one communications; an Ethernet switch is required for more than two devices in a network unless the devices have a built in switch.

Configuring communication between two CPUs

To configure communication between two CPUs, follow these steps:

1. Establish the hardware communications connection (Page 156). A PROFINET interface establishes the physical connection between two CPUs. Since Auto-Cross-Over functionality is built into the CPU, you can use either a standard or crossover Ethernet cable for the interface. An Ethernet switch is not required to connect the two CPUs.
2. Configure the devices (Page 158). You must configure two CPUs in your project.
3. Configure the logical network connections between two CPUs (Page 136).
4. Configure an IP address in your project (Page 142). You must configure IP addresses for two CPUs (for example, PLC_1 and PLC_2).
5. Configure transmit (send) and receive parameters (Page 163). You must configure TSEND_C and TRCV_C instructions in both CPUs to enable communications between them.
6. Test the PROFINET network (Page 158). You must download the configuration for each CPU.

5.6.11.1 Configuring connection parameters

Configuring connection parameters

To specify the connection parameters, select any part of the instruction and do the following:

1. In the inspector window of STEP 7, select the "Properties" tab
2. Select the "Configuration" tab at right.
3. Select "Connection parameter".

Refer to "Configuring the Local/Partner connection path (Page 137)" for more information on each parameter.

Defining TSAPs (Transport Service Access Points) or Ports

If you configure a communication connection in your STEP 7 program, STEP 7 automatically assigns the TSAP.

If you are using TBlocks, you can edit the TSAP fields in the "Address Details" section of the Connection parameters dialog or directly in the connection parameter Data block .

For detailed information on defining the TSAP parameters, refer to the TIA Portal Information System.

5.6.11.2 Configuring transmit (send) and receive parameters

Communication blocks (for example, TSEND_C and TRCV_C) are used to establish a connection between two CPUs. Before the CPUs can engage in PROFINET communications, you must configure parameters for transmitting (or sending) messages and receiving messages.

For more information on Configuring the TSEND_C and TRCV_C instructions, see the following topics under Open User Communication in the TIA Portal Information System:

- TSEND_C: Establishing a connection and sending data
- TRCV_C: Establishing a connection and receiving data

5.6.12 Configuring a CPU and PROFINET IO device

5.6.12.1 Adding a PROFINET IO device

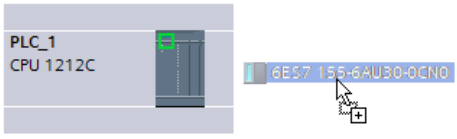
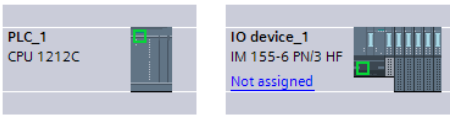
CPU-to-PROFINET IO device communication allows for data transmission and reception with specified length.

To add PROFINET IO devices in your STEP 7 program, follow these steps:

1. From the "Project tree", double click to select "Device configuration" for your CPU.
2. In the center window, select the "Network view" tab.
3. From the "Hardware catalog" pane at right, select the PROFINET IO device (sorted by part number).
4. Drag and drop the selected IO device into the "Network view" inspector window.

For example, expand the following containers in the hardware catalog to add an ET 200SP IO device: Distributed I/O, ET 200SP, Interface modules, and PROFINET. You can then select the interface module from the list of ET 200SP devices and add the ET 200SP IO device.

Table 5-7 Adding an ET 200SP IO device to the device configuration

Insert the IO device	Result
	

You can now connect the PROFINET IO device to the CPU:

1. Right-click the "Not assigned" link on the device and select "Assign new IO controller" from the context menu to display the "Select IO controller" dialog.
2. Select your CPU (in this example, "S7-1200 G2") from the list of IO controllers in the project.
3. Click "OK" to create the network connection.

You can also go to the "Devices and networks" window and use the "Network view" to create the network connections between the devices in your project:

1. To create a PROFINET connection, click the green (PROFINET) box on the first device, and drag a line to the PROFINET box on the second device.
2. Release the mouse button to configure the PROFINET connection.

Refer to "Device Configuration: Configuring the CPU for communication (Page 118)" for more information.

5.6.12.2 Assigning CPUs and device name

Network connections between the devices also assign the PROFINET IO device to the CPU, which is required for that CPU to control the device. To change this assignment, click the PLC name shown on the PROFINET IO device. Use the dialog box to disconnect the PROFINET IO device from the current CPU and reassign it to another CPU. Alternatively, you can leave the PROFINET IO device unassigned.

To connect with the CPU, you must assign a name to the devices on your PROFINET network. If you have not assigned a name to the devices, or if you need to change a device's name, use the "Network view" option. Select the PROFINET IO device and right-click to choose "Assign device name".

NOTE

You must assign the same name to each PROFINET IO device in both the STEP 7 project and the PROFINET network.

You can use one of the following tools to assign the device name in the PROFINET network:

- STEP 7 "Online & diagnostics" tool
- PRONETA commissioning, configuration, and diagnostics tool
- SIMATIC Automation Tool

If a name is missing or does not match in either location, the PROFINET IO data exchange mode will not run.

Refer to the chapter "Assigning a PROFINET device name" in the TIA Portal Information System for more information.

5.6.12.3 Assigning Internet Protocol (IP) addresses

In a PROFINET network, each device must have an Internet Protocol (IP) address. Note the following:

- If you have programming or other network devices that use an onboard adapter interface connected to your plant LAN or an Ethernet-to-USB adapter card connected to an isolated network, you must assign IP addresses to them. Refer to "Assigning IP addresses to programming and network devices" (Page 138) for more information.
- You can also assign an IP address to a CPU or network device online. This is particularly useful in an initial device configuration. Refer to "Assigning an IP address to a CPU online" (Page 140) for more information.
- After you have configured your CPU or network device in your project, you can configure parameters for the PROFINET interface to include its IP address. Refer to "Configuring an IP address for a CPU in your project" (Page 142) for more information.

5.6.12.4 Configuring the IO cycle time

The CPU supplies a PROFINET IO device with new data within an IO cycle time period. The update time can be separately configured for each device and determines the time interval in which data is transmitted from the CPU to and from the device.

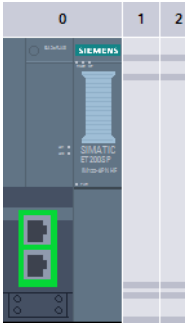
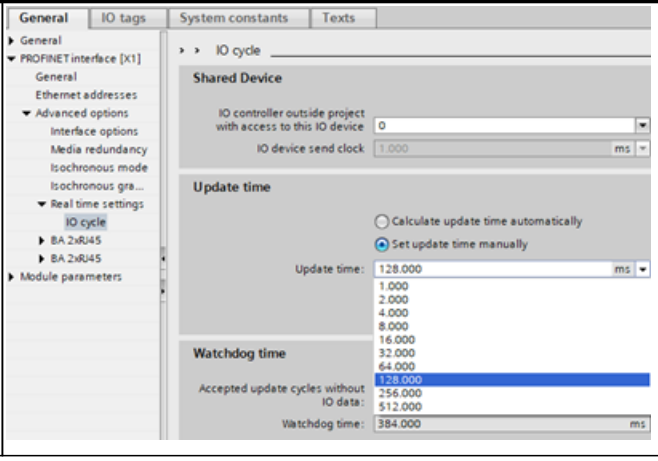
STEP 7 calculates the IO cycle update time automatically in the default setting for each device of the PROFINET network, taking into account the volume of data to be exchanged and the number of devices assigned to this controller. If you do not want to have the update time calculated automatically, you can change this setting.

To access the IO cycle parameters, click a PROFINET port on the ET 200SP IO device. From Properties dialog, select "Advanced options > Realtime settings > IO cycle".

Define the IO cycle "Update time" with the following selections:

- To have a suitable update time calculated automatically, select "Calculate update time automatically".
- To set the update time yourself, select "Set update time manually" and choose the required update time in ms from the dropdown menu.

Table 5-8 Configuring the ET 200SP PROFINET IO cycle time

ET 200SP PROFINET IO device	ET 200SP PROFINET IO cycle dialog
	

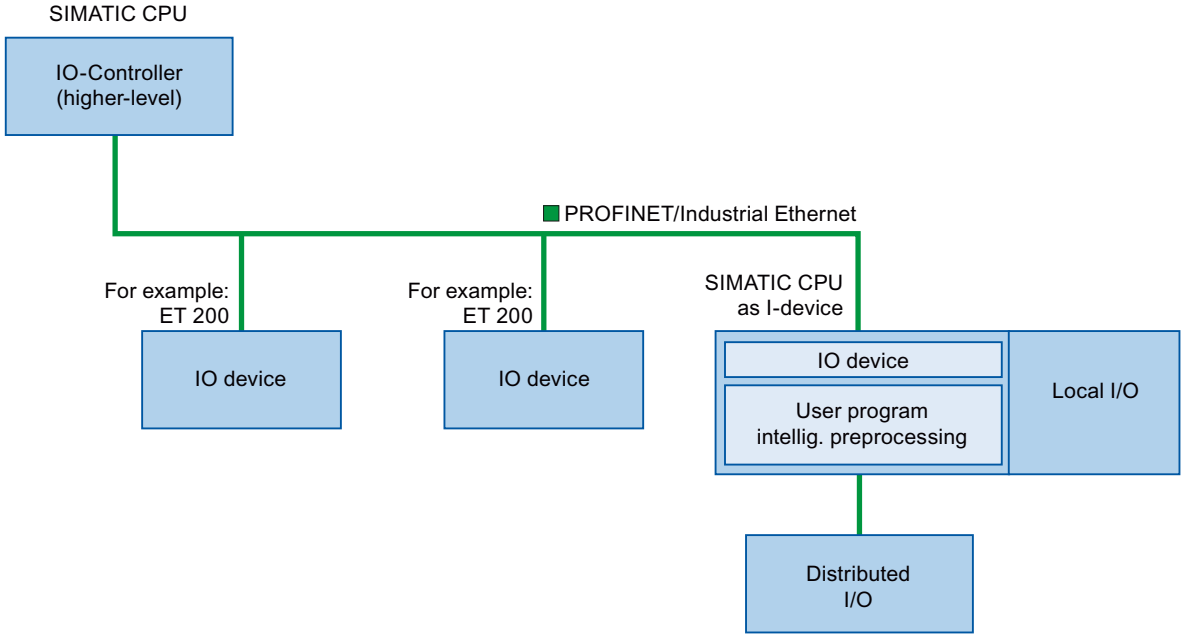
5.6.13 Configuring a CPU and PROFINET I-device

5.6.13.1 I-device functionality

A CPU with I-device functionality is called an "I-device".

The "I-device" (intelligent IO device) functionality of a CPU facilitates data exchange with an IO controller and operation of the CPU as an intelligent preprocessing unit of subprocesses, for example. The I-device is linked as an IO device to a "higher-level" IO controller.

STEP 7 handles the preprocessing on the CPU. The process values acquired in the local or distributed (PROFINET IO) I/O are preprocessed by STEP 7 and made available through a PROFINET IO interface to the CPU of a higher-level station.



5.6.13.2 Properties and advantages of the I-device

The I-device allows you to separate STEP 7 automation projects between creators and users, with the GSD file serving as the interface between these projects. This establishes a connection to standard IO controllers through a standardized interface. Additionally, the I-device has a deterministic PROFINET IO system for real-time communication through the PROFINET IO interface.

Advantages

The I-device offers the following advantages:

- Simple linking of IO controllers
- Real-time communication between IO controllers
- Relieving the IO controller by distributing the computing capacity to I-devices
- Lower communications load by processing process data locally

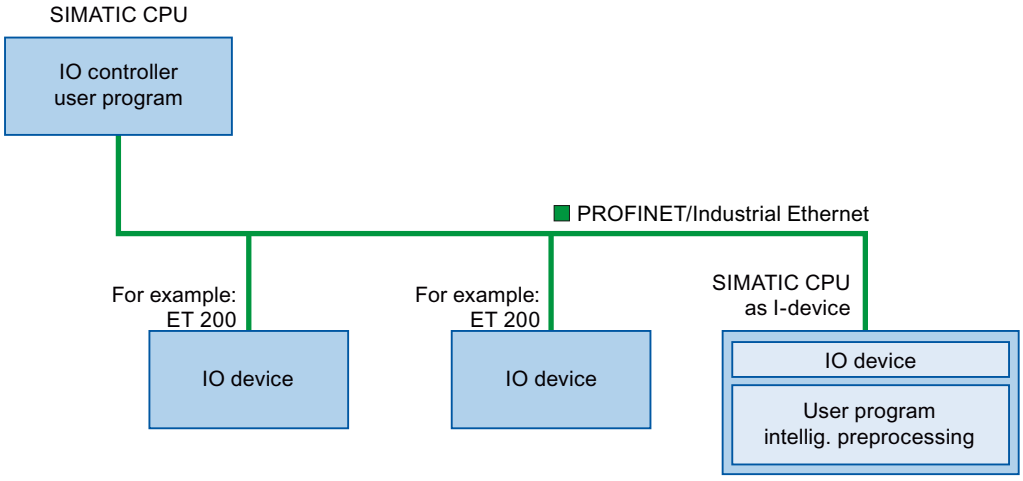
- Manageable solution design that includes the following:
  - Distributed processing: Divide complex automation tasks into smaller subprocesses for increased manageability and simplified subtasks.
  - Separating subprocesses: You can subdivide complicated, widely distributed and extensive processes into subprocesses with manageable interfaces by using I-devices. Store these subprocesses in separate STEP 7 projects and later merge them into a single master project.
  - Know-how protection: Deliver components with a GSD file for the I-device interface description instead of a STEP 7 project. This approach protects your program and eliminates the need for program publication.

5.6.13.3 Characteristics of an I-device

An I-device is included in an IO system like a standard IO device.

I-device without lower-level PROFINET IO system

The I-device does not have its own distributed I/O. The configuration and parameter assignment of the I-devices in the role of an IO device is the same as for a distributed I/O system (for example, ET 200).

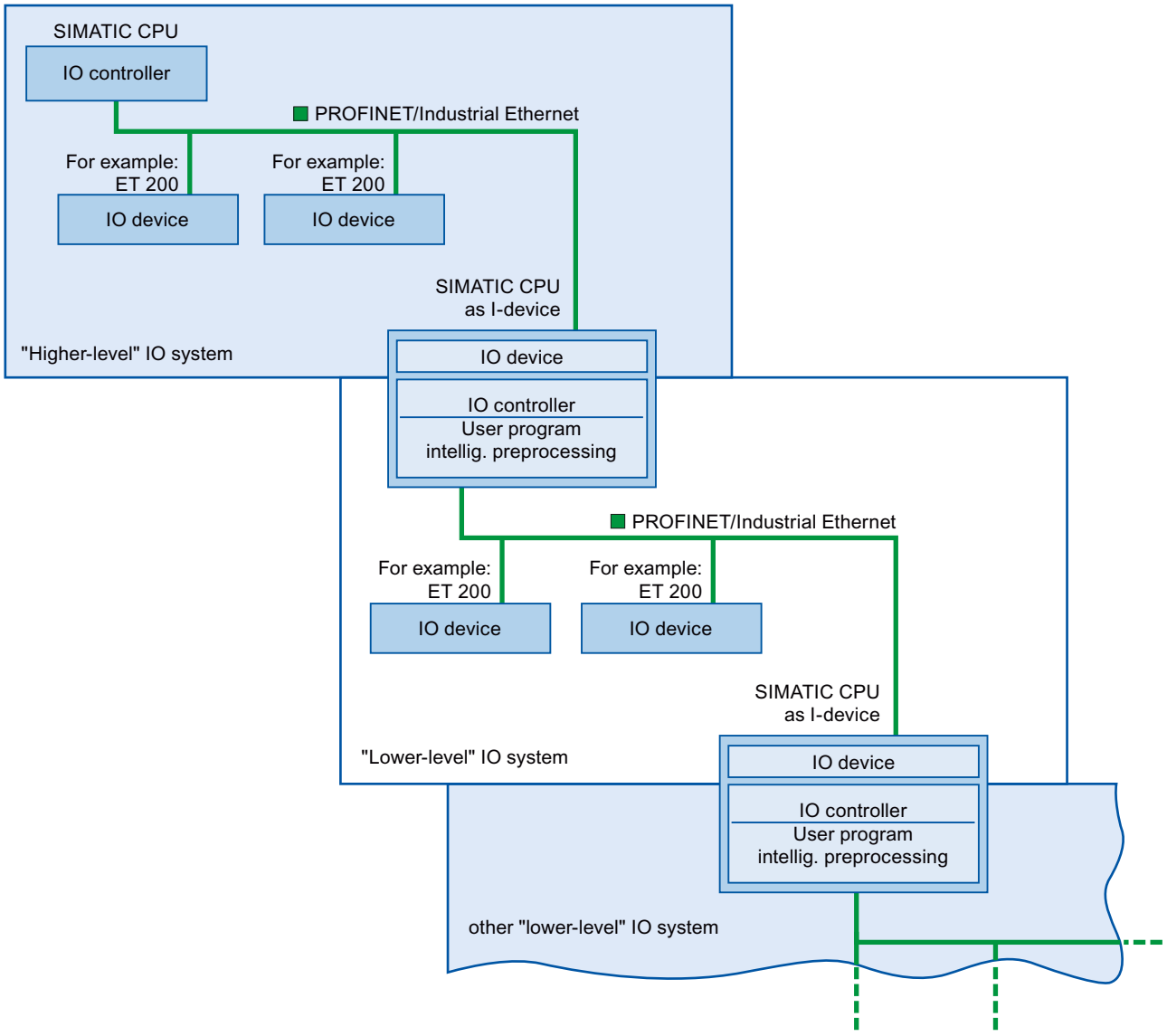


I-device with lower-level PROFINET IO system

Depending on the configuration, an I-device can also be an IO controller on a PROFINET interface in addition to having the role of an IO device.

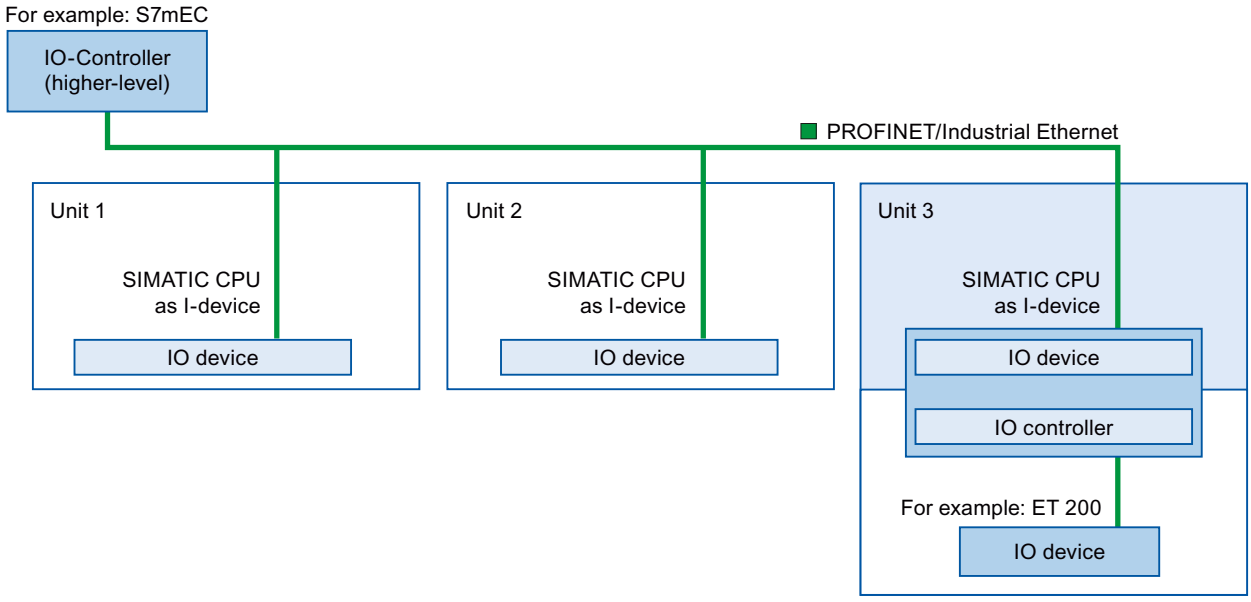
This means that the I-device can be part of a higher-level IO system through its PROFINET interface and as an IO controller can support its own lower-level IO system.

The lower-level IO system can, in turn, contain I-devices. This makes hierarchically structured IO systems possible.



Example: I-device as IO device and IO controller

This example explains the use of an I-device as IO device and IO controller in a print process. The I-device controls a unit (a subprocess). One unit is used, for example, to insert additional sheets such as flyers or brochures in a package of printed material.



Unit 1 and unit 2 each consist of an I-device with local I/O. The I-device along with the distributed I/O system (for example, ET 200) forms unit 3.

The STEP 7 program on the I-device is responsible for preprocessing the process data. For this task, the STEP 7 program of the I-device requires default settings (for example, control data) from the higher-level IO controller. The I-device provides the higher-level IO controller with the results (for example, status of its subtask).

5.6.13.4 Data exchange between higher- and lower-level IO system

Transfer areas are an interface to the STEP 7 program of the I-device CPU. The CPU processes the inputs and sets the outputs.

The data for communication between IO controller and I-device is available in the transfer areas. A transfer area contains an information unit that is exchanged consistently between IO controller and I-device (Page 172).

Input transfer areas behave differently upon network loss between controller and I-device

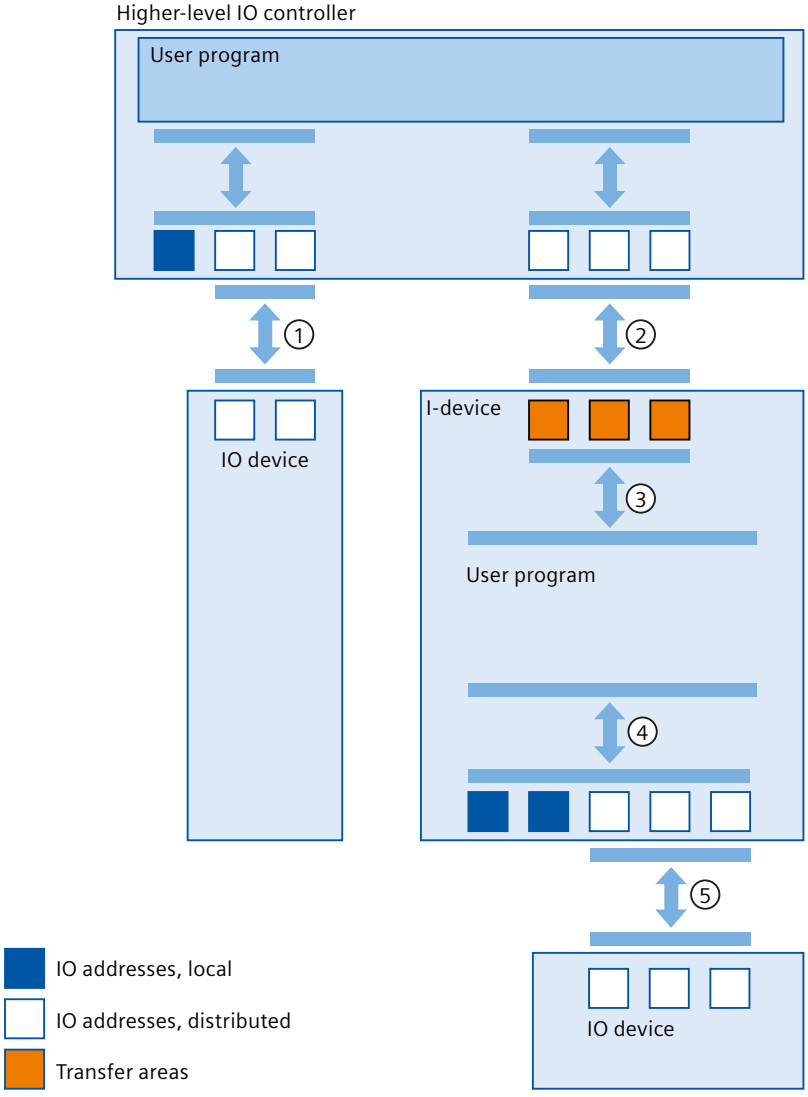
On the controller, the CPU writes zero to the input transfer areas upon network loss. On the I-device, the input transfer areas retain their last values.

You can configure your system to avoid this condition for the general I-device case (non-shared I-device). To do this, clear the input transfer areas for the I-device in a "Rack or Station Failure OB" for a coming event. Follow these steps:

1. Add a "Rack or Station Failure OB (Page 67)" to your project.
2. Add logic to the OB to write the values of the inputs for the I-device to zero when the startup variable of LADDR indicates the value of the I-device hardware ID and the startup variable of Event_Class indicates a "coming" event:
   - You can find the I-device hardware ID in the Default tag table in the "System constants" tab. The hardware ID is a type of "HW_Device", and the name of the tag indicates that it is an I-device (for example, "Local~PROFINET_interface_1~IODevice").
   - A value of "16#39" in the Event_Class indicates a "coming" event. If the "Event_Class" input variable contains the value of "16#39", this indicates that the "Rack or Station Failure OB" is now active (as opposed to being cleared).

Data exchange flow

The data exchange between the higher- and lower-level IO system is as follows:



① **Data exchange between higher-level IO controller and IO-device** through PROFINET.

② **Data exchange between higher-level IO controller and I-device** through PROFINET.
The data exchange between a higher-level IO controller and an I-device is based upon the conventional IO controller / IO device relationship.
For the higher-level IO controller, the transfer areas of the I-devices represent submodules of a preconfigured station.
The output data of the IO controller is the input data of the I-device. Similarly, the input data of the IO controller is the output data of the I-device.

③ **Transfer relationship between the STEP 7 program and the transfer area**
STEP 7 and the transfer area exchange input and output data.

④ **Data exchange between the STEP 7 program and the I/O of the I-device**
STEP 7 and the local / distributed I/O exchange input and output data.

⑤ **Data exchange between the I-device and a lower-level IO device** through PROFINET.

5.6.13.5 Configuring the I-device

You have two possibilities for configuration:

- Configuration of an I-device within a project
- Configuration of an I-device that is used in another project or in another engineering system

STEP 7 allows you to configure an I-device for another project or for another engineering system by exporting a configured I-device to a GSD file. You import the GSD file in other projects or engineering systems as with other GSD files. The transfer areas for the data exchange, among other data, are stored in this GSD file.

NOTE

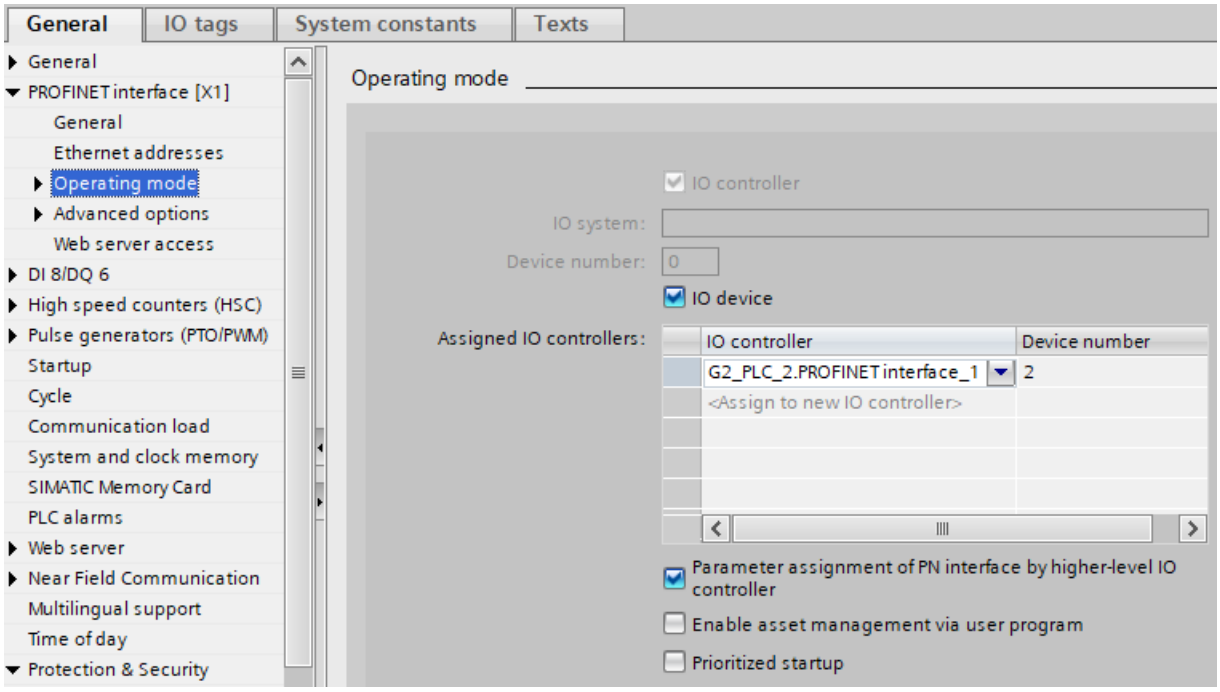
When you use the S7-1200 G2 as a shared I-device and as a controller, ensure that you increase the PROFINET I-device and PROFINET IO update times to alleviate the communications performance impact. The system is very stable and works well when you select 2 ms for the update time of a single PROFINET device time and you select 2 ms for the update time of a single PROFINET IO time.

Configuration of an I-device within a project

1. Drag-and-drop a PROFINET CPU from the hardware catalog into the network view.
2. Drag-and-drop the second PROFINET CPU, which can also be configured as an IO device, from the hardware catalog into the network view. This device is configured as an I-device (for example, CPU 1212C).
3. Click the device in the Device view to display the "Properties" tab view.
4. In the left column, select and expand the PROFINET interface for the I-device and select the "Operating Mode" category.
5. In the inspector window, select the checkbox for "IO device".

6. Choose the IO controller in the "Assigned IO controller" drop-down list.

   After you have chosen the IO controller, the network view displays the networking and the IO system between both devices.

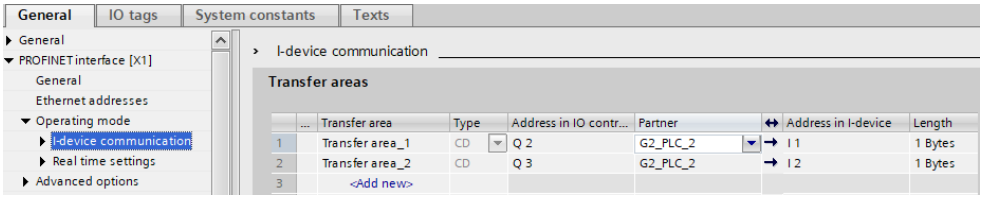


7. With the "Parameter assignment of PN interface by higher-level IO controller" checkbox, you specify whether the interface parameters will be assigned by the Idevice or by a higher-level IO controller.

   If you operate the I-device with a lower-level IO system, then the parameters of the I-device PROFINET interface (for example, the port parameter) cannot be assigned with the higher-level IO controller.

8. Configure the transfer areas. The transfer areas are found in the area navigation section "I-device communication":

   – Click in the first field of the "Transfer area" column. STEP 7 assigns a default name, which you can change.
   – Type of communication relation is set to CD (Communication Direction) by default.
   – Addresses are automatically preset; you can correct addresses if necessary, and determine the length of the transfer area which is to be consistently transferred.



9. A separate entry is created under "I-device communication" for each transfer area. If you select one of these entries, you can adjust the details of the transfer area, or correct them and comment on them.

NOTE

If you configure an S7-1200 G2 as an I-device, the maximum size of a transfer area is 1024 input or output bytes. There are possible constraining factors depending on local I/O as well as address space limitations on the controlling device.

Configuring an I-device with a GSD file

If you use an I-device in another project, or if the I-device is used in another engineering system, you must configure the higher-level IO controller and the I-device as follows:

1. Configure the transfer areas so the I-device creates a new GSD file. This GSD file represents the configured I-device in other projects. For further information, see the topic "Installing the GSD file" in the TIA Portal Information System.
2. Assign a name for the I-device proxy as well as a description in the fields provided.
3. Click the "Export" button in the "I-device communication" section of the Inspector window.

To test, import the GSD file, for example, in another project.

5.6.14 Shared device functionality

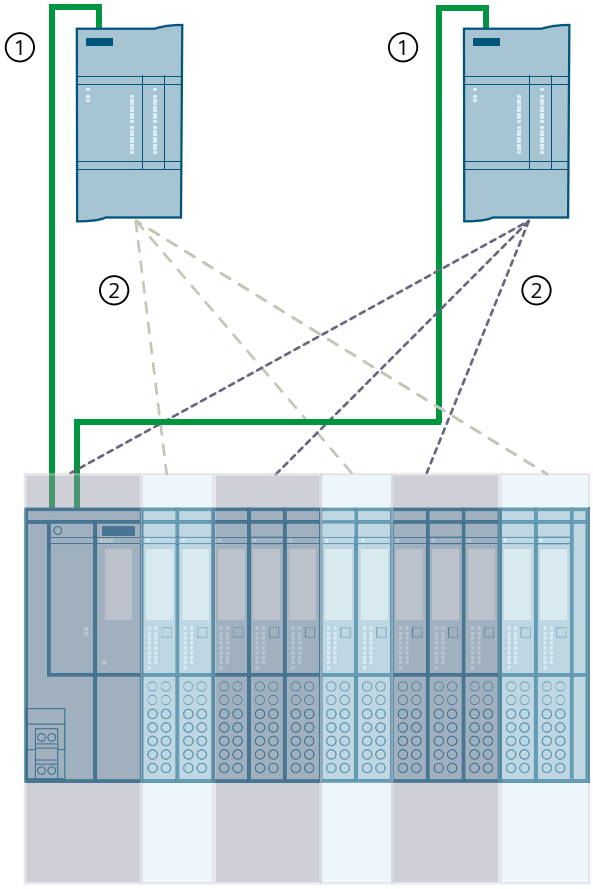
Large or widely distributed systems might use multiple IO controllers.

By default, one IO controller manages each IO module of an IO device. The "Shared Device" function allows you to divide the modules or submodules of an IO device among different IO controllers.

Configuration

When you configure an S7-1200 G2 CPU as an I-device, it enables the support of shared I-device functionality for up to two IO controllers. If both the IO controllers and the I-device are SIMATIC CPUs, configure them within a single STEP 7 project. For further guidance, see "Configuring a project-internal shared device" in the TIA Portal Information System.

If one or both IO controllers are non-SIMATIC CPUs, use a GSD file for the configuration process. For detailed instructions, see "Configuring Shared Device (GSD configuration)" in the TIA Portal Information System.



① PROFINET
② Logical assignment

Further information

For more detailed information on shared device functionality, see "Configuring PROFINET IO > Configuring Shared Devices" in the TIA Portal Information System.

5.6.15 Media Redundancy Protocol (MRP)

The S7-1200 G2 CPUs support Media Redundancy Protocol (MRP) functionality and MRP ring setup as either a "Manager" or a "Client":

Media Redundancy Protocol	CPU as a Client	CPU as a Manager or Manager (Auto)
Functionality	Must operate in an MRP ring by forwarding MRP packets over its interface and reporting connection breaks to a manager in the network.	Must send MRP packets around the network, detect open ports in the ring, and manage blocked ports. Manager (Auto) only: Negotiate manager status with other potential managers.
Ring setup	Forwards test frames instead of making the check itself.	Uses test frames to check and make sure the ring is not interrupted.

Use the MRP protocol and configuration parameters to initialize MRP client and manager operation.

For further information, see the "Configuring media redundancy" chapter in the TIA Portal Information System.

5.6.16 Media Redundancy with Planned Duplication of frames (MRPD)

The MRP extension "Media Redundancy with Planned Duplication of frames" (MRPD) provides the advantage that, in the case of a failure of a device or a line in the ring, all other devices continue to be supplied with IO data without interruption and with short update times. MRPD is based on IRT and MRP. To realize media redundancy with short update times, the PROFINET devices participating in the ring send their data in both directions. The devices receive this data at both ring ports so that there is no reconfiguration time.

For detailed information see "Media Redundancy with Planned Duplication of frames (MRPD)" in the TIA Portal Information System.

Requirements for media redundancy with MRPD

- All the devices of the ring must support MRPD. Terminal devices at the switch that cyclically exchange IRT data with a ring component must also support MRPD.
  MRPD support is listed in the device information in the STEP 7 hardware catalog (Devices & networks).
- You have configured MRP for all the devices of the ring.
- You have assigned the MRP role "Not device in the ring" to devices that are not located in the ring.
- You have configured IRT for all the involved components.

Configuring MRPD

You do not have to activate MRPD in STEP 7. The function is available automatically as soon as all the requirements for MRPD are fulfilled.

5.6.17 Isochronous Real-Time PROFINET (IRT)

The S7-1200 G2 CPUs support Isochronous Real-Time PROFINET (IRT).

IRT is a transmission method by which PROFINET devices are synchronized with very high accuracy. A sync master specifies the clock to which sync slaves are synchronized. An IO controller or an IO device can have the role of sync master.

Sync master and sync slaves are always devices in a sync domain. Bandwidth is reserved within the sync domain for IRT communication. Real-time and non-real-time communication (TCP/IP communication) is possible outside of the reserved bandwidth.

PROFINET with IRT is especially suited for the following:

- High performance and deterministics for large quantity structures with regard to user data communications (productive data).
- High performance even with many devices in the line topology with regard to user data communications (productive data).
- Parallel transmission of production and TCP/IP data over wire, and securing the forwarding of production data when data volume is high by reserving transmission bandwidth.

For detailed information on IRT and configuring PROFINET with IRT, see "Configuring IRT communication" in the TIA Portal Information System

5.6.18 SNMP

Simple Network Management Protocol (SNMP) is an Internet standard protocol for collecting and organizing information about managed devices on IP networks and for modifying that information to change device behavior. Devices that typically support SNMP include routers, switches, servers, workstations, printers, modem racks, and more.

Network management systems use SNMP to monitor network-attached devices for conditions that warrant administrative attention. SNMP uses various services and tools for detection and diagnostics of the network topology. You can find information about the properties of devices capable of SNMP in the Management Information Base (MIB) files. You must have the required rights to access the MIB files.

SNMP exposes management data in the form of variables on the managed systems, which describe the system configuration. Managing applications can query (and sometimes set) these variables.

SNMP uses the UDP transport protocol and has two network components:

- SNMP manager: Monitors the network nodes
- SNMP client: Collects the various network-specific information in the individual network nodes and stores it in a structured form in the Management Information Base (MIB). You can use this data to perform detailed network diagnostics.

For security reasons, SNMP is disabled by default on S7-1200 G2 CPUs, preventing read and write access of SNMP variables. You must enable SNMP to remotely view and edit SNMP variables.

After enabling SNMP, certain conditions might require you to disable it. Examples of these conditions include the following:

- The security settings in your network do not allow the use of SNMP.
- You use your own SNMP solution (for example, with your own communications instructions).

If SNMP is disabled on the device, some functions and tools that rely on access to SNMP variables are unavailable or inoperable. For example, topology detection in TIA Portal is inoperable, and some functions of the SIMATIC Automation Tool V4.x and prior, are inoperable.

NOTE

Restoring the CPU to factory defaults disables SNMP.

Enabling and disabling SNMP from the device configuration

To enable or disable SNMP follow these steps:

1. From the Project Tree, under the CPU, double-click Device configuration.
2. From the General tab of the device properties, expand Advanced configuration and select SNMP.
3. To enable SNMP, select the "Activate SNMP" checkbox or to disable SNMP, deselect it.
4. Enter a Read-only community string or use the default (public) and enter a Read-write community string or use the default (private).

   NOTE

   To share SNMP data between the STEP 7 project and the PLC, the community name entered in the STEP 7 project must match the community name entered for the host when creating the SNMP database connection.

5. Download the configuration to the CPU.

Enabling and disabling SNMP from the STEP 7 program

For detailed information on enabling and disabling SNMP from your STEP 7 program, see the following areas in the TIA Portal Information System:

- Configuring SNMP
- Activating and deactivating SNMP
- Disabling SNMP: Full program example

5.7 S7 communication

5.7.1 PUT and GET (Write and read from a remote CPU)

You can use the PUT and GET instructions to communicate with S7 CPUs through PROFINET connections. This is only possible if the "Permit access with PUT/GET communication from remote partner" function is activated for the partner CPU in the "Protection & Security" property of the local CPU properties:

- Accessing data in a remote CPU: An S7-1200 G2 CPU can only use absolute addresses in the ADDR_x input field to address variables of remote CPUs (S7-200/300/400/1200).
- Accessing data in a standard DB: An S7-1200 G2 CPU can only use absolute addresses in the ADDR_x input field to address DB variables in a standard DB of a remote S7 CPU.
- Accessing data in an optimized DB: An S7-1200 G2 CPU cannot access DB variables in an optimized DB of a remote S7-1200 G2 CPU.
- Accessing data in a local CPU: An S7-1200 G2 CPU can use either absolute or symbolic addresses as inputs to the RD_x or SD_x input fields of the PUT or GET instruction, respectively.

Enabling PUT/GET access

PUT/GET operation is not automatically enabled.

To enable PUT/GET access, follow these steps:

1. In the Project tree under "Security settings" > "Users and roles", click the checkbox to enable the Anonymous user.
2. In the "Roles" tab, click "Add new role" and give it a name.
3. From the "Roles" tab, click the "Runtime rights" tab and select your PLC from the dropdown menu at left.
4. Assign at least one of the following function rights for your PLC:
   - HMI access
   - Read Access
   - Full access
5. Select the "Users" tab in the top right and click the checkbox beside the new role to assign it to the Anonymous user.
6. In the CPU's "Device configuration" inspector window, select the "Properties" tab > "Protection & Security > Connection mechanisms" and click the checkbox to "Permit access with PUT/GET communication from remote partner".

WARNING

Avoiding security risks from network attacks

If an attacker can access your networks, the attacker can possibly read and write data.

For example, I/O exchange through PROFINET, PUT/GET, T-Block, and communication modules (CMs) have no security features. You must protect these forms of communication.

If you fail to protect these forms of communication, death or severe personal injury can result.

For security information and recommendations, see the "Operational Guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html)" white paper on the Siemens Industrial Cybersecurity Web site.

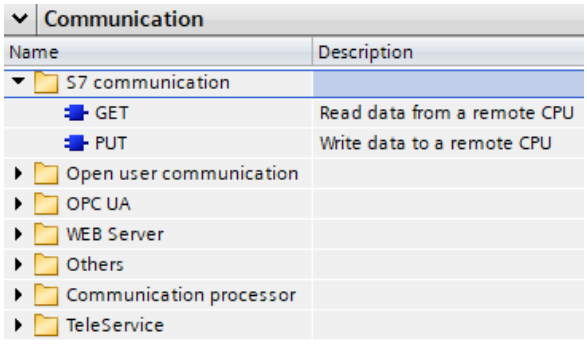
Protocol

The protocol for S7 communication and communication instructions are as follows:

Protocol	Usage examples	Entering data in the receive area	Communication instructions	Addressing type
S7 communication	CPU-to-CPU communication Read/write data from/to a CPU	Data transmission and reception with specified length	PUT and GET	Assigns TSAPs to the Local (active) and Partner (passive) devices

Instructions

The S7 communication PUT and GET instructions allow you to read and write data from a remote CPU:



For detailed information about the PUT and GET instructions, see the "S7 communication (S7-1200, S7-1500)" chapter in the TIA Portal Information System.

5.7.2 Creating an S7 connection

You must have permission to access remote connection partners with PUT/GET instructions.

By default, the "Permit access with PUT/GET communication from remote partner" option is disabled. In this case, read and write access to CPU data is only possible for communication connections that require configuration or programming both for the local CPU and for the communication partner.

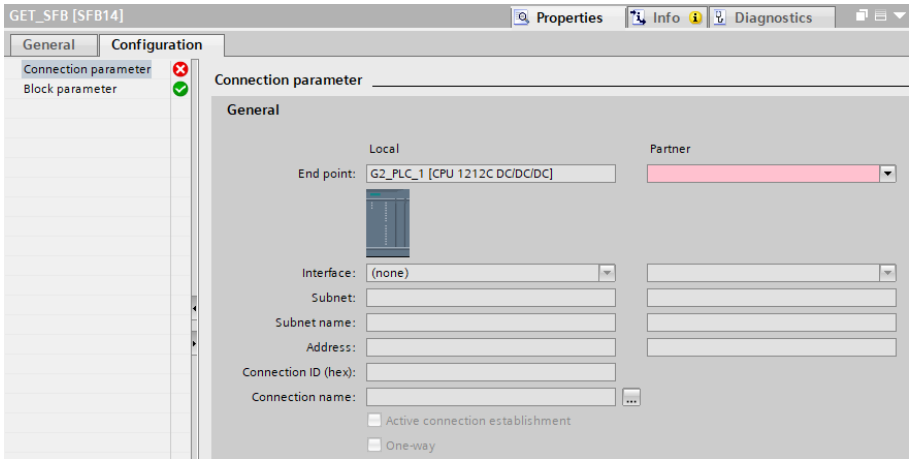
For detailed information, see the "Configuring S7 connections (S7-1200)" chapter in the TIA Portal Information System.

5.7.3 PUT/GET connection parameter assignment

The PUT/GET instructions connection parameter assignment is a user aid for configuring CPU-to-CPU S7 communication connections.

After inserting a PUT or GET instruction, the Properties tab for the instruction displays the connection parameter assignment dialog for the GET/PUT instructions.

The "Connection parameters" dialog allows you to configure the necessary S7 connection and to configure the parameter "Connection ID" that is referenced by the GET/PUT block parameter "ID". The dialog has information about the local endpoint and allows you to define the local interface. You can also define the partner end point.



The "Block parameters" dialog allows you to configure the additional block parameters.

Table 5-9 Connection parameter: General definitions

Parameter		Definition
Connection parameter: General	End point	"Local End point": Name assigned to the Local CPU "Partner End point": Name assigned to the Partner (remote) CPU Note: In the "Partner End point" dropdown list, the system displays all potential S7 connection partners of the current project as well as the option "unspecified". An unspecified partner represents a communication partner which is not currently in the STEP 7 project (for example, a third party device communication partner).
	Interface	Name assigned to the interfaces Note: You can change the connection by changing the Local and Partner interfaces
	Subnet	Type of subnet

Parameter		Definition
Connection parameter: General	Subnet name	Name assigned to the subnets
	Address	Assigned IP addresses Note: You can specify the remote address of a third party device for an "unspecified" communication partner.
	Connection ID (hex)	ID number: Automatically generated by the GET/PUT connection parameter assignment
	Connection name	Local and Partner CPU data storage location: Automatically generated by the GET/PUT connection parameter assignment
	Active connection establishment	Checkbox to select Local CPU as the active connection
	One-way	Checkbox to specify a one-way or two-way connection; read-only Note: In a PROFINET GET/PUT connection, both the local and partner devices can act as a server or a client. This allows a two-way connection, and the "One-way" checkbox is unchecked.

5.7.3.1 Connection ID parameter

You can change the system-defined connection IDs in one of the following ways:

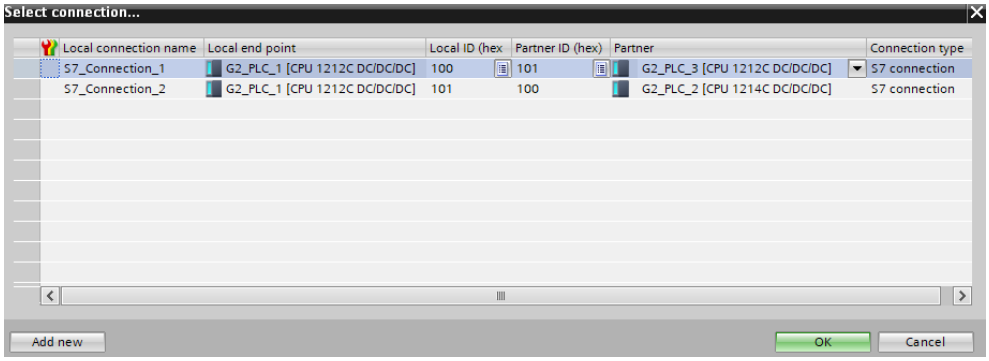
- Change the current ID directly on the GET/PUT instruction. If the new ID belongs to an already existing connection, the connection is changed.
- Change the current ID directly on the GET/PUT instruction, but the new ID does not already exist. A new S7 connection is created by the system.
- Change the current ID through the "Connection overview" dialog: Your input is synchronized with the ID-parameter on the corresponding GET/PUT instruction.

NOTE

The parameter "ID" of the GET/PUT instruction is not a connection name, but a numerical expression, which is written like the following example: W#16#1

5.7.3.2 Connection name parameter

The connection name is editable through the "Select connection" dialog. This dialog offers all the available S7 connections that could be selected as an alternative for the current GET/PUT communication. You can create a new connection in this table. Click the button to the right of the "Connection name" field to start the "Select connection" dialog.



5.8 Diagnostic events for distributed I/O

As shown in the following table, the CPU supports diagnostics that can be configured for the components of the distributed I/O system. Each of these errors generates a log entry in the diagnostics buffer.

Table 5-10 Handling of diagnostic events for PROFINET

Type of error	Diagnostic information for the station?	Entry in the diagnostics buffer?	CPU operating mode
Diagnostic error	Yes	Yes	Stays in RUN mode
Rack or station failure	Yes	Yes	Stays in RUN mode
I/O access error [1]	No	Yes	Stays in RUN mode
Peripheral access error [2]	No	Yes	Stays in RUN mode
Pull / plug event	Yes	Yes	Stays in RUN mode

[1] I/O access error example cause: Reading inputs or writing outputs for a module that has been removed or not communicating.

[2] Peripheral access error example cause: Reading peripheral inputs or writing peripheral outputs for a module that has been removed or not communicating.

Use the GET_DIAG instruction for each station to obtain the diagnostic information. This will allow you to programmatically handle the errors encountered on the device and if desired take the CPU to STOP mode. This method requires you to specify the hardware device from which to read the status information.

The GET_DIAG instruction uses the "L address" (LADDR) of the station to obtain the health of the entire station. This L Address can be found within the Network Configuration view and by selecting the entire station rack, the L Address is shown in the Properties Tab of the station. The LADDR for each individual module is either in the properties for the module in the device configuration or in the default tag table for the CPU.

5.9 What to do when you cannot access the CPU by the IP address

In case you cannot reach a CPU by the IP address, you can set an emergency (temporary) IP address for the CPU. The emergency IP address enables you to re-establish communication with the CPU in order to download a device configuration with a valid IP address.

Reasons why you might need an emergency IP address

Your CPU might be inaccessible if someone downloaded a project with one of the following problems:

- The IP address of the PROFINET interface of the CPU is a duplicate of another device on the network.
- The subnet is incorrect for the CPU.
- The subnet mask makes the CPU unreachable.

In these cases, the CPU is no longer accessible from STEP 7.

Assigning an emergency IP address

You can assign an emergency IP address under the following conditions:

- The device configuration in STEP 7 has "Set IP address in the project" for the IP protocol.
- The CPU is in STOP mode.

Under these conditions, you can use a DCP tool to set the IP address of the device to an emergency IP address. The SIMATIC Automation Tool, for example, has a DCP Set IP address command. You can set an emergency IP address regardless of the protection level of the CPU. After you set a temporary IP address with a DCP tool, the Maintenance LED on the CPU turns on. The Diagnostics Buffer also includes an entry indicating that you enabled an emergency address of an Ethernet interface.

Restoring an IP address after assigning an emergency IP address

The diagnostics buffer informs you when you have enabled or disabled an emergency IP address. You can reset the emergency IP address by powering the CPU off and on.

After you have assigned an emergency IP address, you can then download a STEP 7 project with a valid IP address for the CPU. After you download the project, power cycle the CPU.

5.10 Modbus communication

Modbus function codes

A CPU operating as a Modbus TCP client can read/write both data and I/O states in a remote Modbus TCP server. Remote data can be read and then processed in your program logic.

A CPU operating as a Modbus TCP server allows a supervisory device to read/write both data and I/O states in CPU memory. A Modbus TCP client can write new values into server CPU memory that is available to your program logic.

⚠ WARNING

Avoiding security risks from network attacks

If an attacker can access your networks, the attacker can possibly read and write data.

For example, I/O exchange through PROFINET, PUT/GET (Page 179), T-Block, and communication modules (CMs) have no security features. You must protect these forms of communication.

If you fail to protect these forms of communication, death or severe personal injury can result.

For security information and recommendations, see the "Operational Guidelines (https://www.siemens.com/global/en/products/services/cert/news/operational-guidelines-for-industrial-security.html)" white paper on the Siemens Industrial Cybersecurity Web site.

Table 5-11 Read data functions: Read remote I/O and program data

Modbus function code	Read server functions - standard addressing
01	Read output bits: 1 to 2000 bits per request
02	Read input bits: 1 to 2000 bits per request
03	Read holding registers: 1 to 125 words per request
04	Read input words: 1 to 125 words per request

Table 5-12 Write data functions: Write remote I/O and modify program data

Modbus function code	Write server functions - standard addressing
05	Write one output bit: 1 bit per request
06	Write one holding register: 1 word per request
15	Write one or more output bits: 1 to 1968 bits per request
16	Write one or more holding registers: 1 to 123 words per request

Modbus function code 23 can write and read one or more holding registers: 1 to 121/125 (Write/Read) words per request.

Modbus network station addresses

In a Modbus TCP network, each device is uniquely addressed using its IP address and port number. To establish a connection, enter these details into the appropriate configuration field. The Modbus protocol then uses this address information to access and communicate with devices over the network.

Modbus memory addresses

The actual number of available Modbus memory addresses depends on the CPU model, how much work memory exists, and how much CPU memory is used by other program data. The table below gives the nominal value of the address range.

Table 5-13 Modbus memory addresses

Station		Address range
TCP station	Standard memory address	10K
	Extended memory address	64K

5.10.1 Modbus TCP

5.10.1.1 Overview

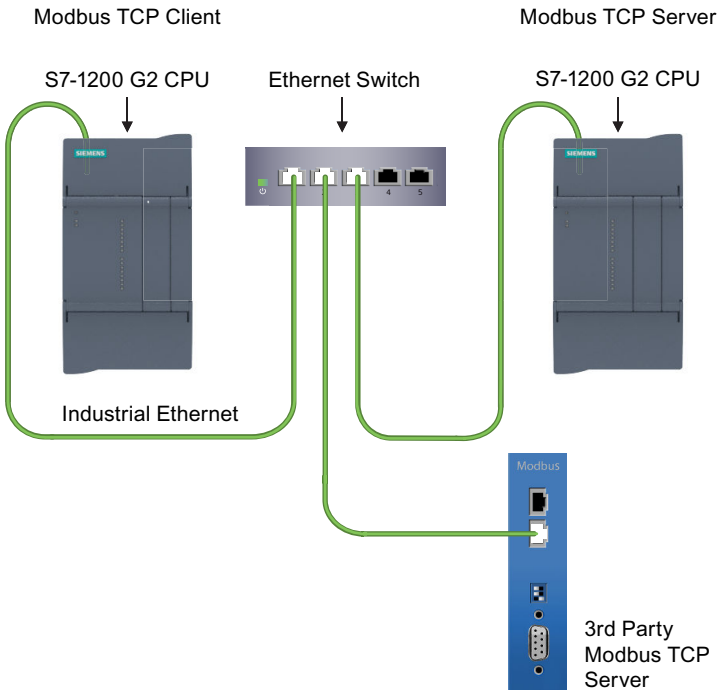
Modbus TCP (Transmission Control Protocol) is a standard network communication protocol that uses the PROFINET connector on the CPU for TCP/IP communication.

Modbus TCP uses Open User Communication (OUC) connections as a Modbus communication path. Multiple client-server connections can exist in addition to the connection between STEP 7 and the CPU. Mixed client and server connections are supported up to the maximum number of connections allowed by the CPU model (Page 133).

Each MB_SERVER connection must use a unique instance DB and port number. Only one connection per port number is supported. Each MB_SERVER (with its unique instance DB, IP address, and port number) must be executed individually for each connection.

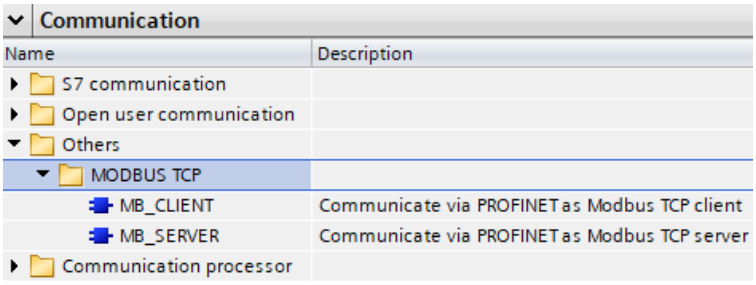
A Modbus TCP client must control the client-server connection with the DISCONNECT parameter. The basic Modbus client actions are shown below:

1. Initiate a connection to a particular server IP address and port number.
2. Initiate client transmission of a Modbus message and receive the server responses.
3. Initiate the disconnection of client and server to enable connection with a different server.



5.10.1.2 Modbus TCP instructions and versions

The Modbus TCP instructions provide the capability to communicate between Modbus TCP clients, Modbus TCP servers, and third-party Modbus TCP devices through a switch. These can be found in the following folders:



For more information on the Modbus TCP instructions and their uses, search the TIA Portal Information System on "MB_CLIENT" and "MB_SERVER" for the MODBUS (TCP) V4.0 and later library.

NOTE

Choosing an instruction by PLC family

If the TIA Portal Information System presents an instruction differently based on PLC family, follow the S7-1500 option for the instruction topic.

Near Field Communication (NFC) 6

Near Field Communication (NFC) allows you to scan a tag in your CPU and access information via the S7-1200 G2 NFC application (Page 188) (app) from an Apple® iPhone® device. Open the app and place your iPhone near the NFC symbol on the front surface of the S7-1200 G2 CPU to scan the NFC tag (Page 190). After the scan is complete, you can read information from the CPU and perform several maintenance operations on the CPU as NFC writes.

By default, NFC is disabled in a new STEP 7 project. If you want to use NFC in your STEP 7 project, you must enable (Page 189) it in the project before downloading the project to your CPU. Note that, if you disable NFC in your STEP 7 project and perform a new download to the CPU, the CPU clears the data on the NFC tag.

Installing (Page 188) the S7-1200 G2 NFC app on your iPhone allows you to read information from the CPU and write operations to the CPU. The supported options for interaction vary based on certain CPU conditions. For more information on which Read/Write commands are supported under the various CPU conditions, see CPU conditions for Read/Write commands (Page 192).

⚠ WARNING

Risks when using a cellular phone in close proximity to the S7-1200 G2 CPU

Using a cellular phone in close proximity to the S7-1200 G2 system with cellular and Wi-Fi communications active could cause unpredictable behavior.

To reduce any influence of a cellular phone on the S7-1200 G2 system, and to ensure proper operation of your CPU, place the phone in "Airplane mode" to disable cellular and Wi-Fi before bringing the phone into proximity (<10 cm) of the CPU.

Failure to comply with these guidelines can cause damage or unpredictable operation which could result in severe personal injury, property damage, and/or death.

⚠ WARNING

Risks when operating a cellular phone in a hazardous or explosive environment

Do not use a cellular phone in a hazardous or explosive environment unless the phone has been approved for use in such environments.

Failure to comply with these guidelines can cause damage or unpredictable operation which could result in death or severe personal injury and/or property damage.

6.1 Installing and setting up the NFC app

From the App Store®, search for, download, and install the free S7-1200 G2 NFC app by Siemens. The following icon is associated with the app:

Note: If your iPhone or iOS version is not compatible, then the S7-1200 G2 NFC app will not download. Refer to the application requirements in the App Store for device version and iOS version compatibility with the S7-1200 G2 NFC app.

Tap the settings icon to customize the appearance and language for the S7-1200 G2 NFC app.

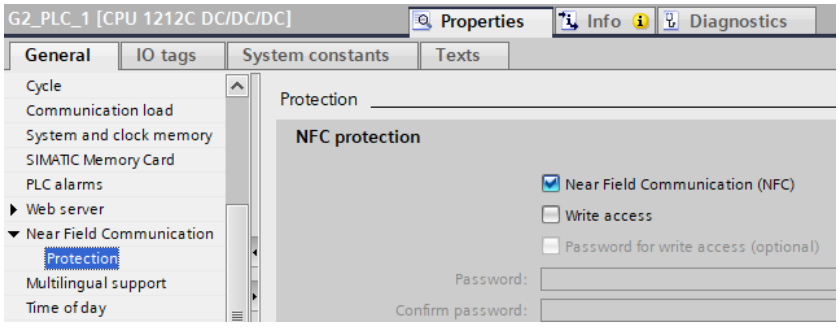
To access the S7-1200 G2 NFC app's security information, tap the icon in the lower right corner and tap "Security information".

6.2 Enabling NFC and optional settings in STEP 7

To use the S7-1200 G2 NFC app to read accurate data from your CPU, you must enable Near Field Communication in STEP 7.

To enable the NFC and optional settings in STEP 7, follow these steps:

1. Select "Device configuration" from the project tree.
2. From the "Properties" tab, navigate to "Near Field Communication > Protection".
3. Click the checkbox to enable Near Field Communication (NFC).



4. Optional: Click the checkbox to "Write access".
5. If you have selected "Write access", you can configure a "Password for write access".
6. Download your project to the CPU.

NOTE

If you make changes in your STEP 7 project and download to the CPU, always perform a new NFC scan to ensure your changes are up-to-date in the NFC app.

Write access privileges

If your CPU is powered on and configured in your STEP 7 project with NFC and write access also enabled in the project, you can use the S7-1200 G2 NFC app to perform write operations to the CPU. With write access, you can do the following:

- Change the CPU operating mode
- Perform a memory reset
- Set the CPU time of day clock based on the iPhone time
- Edit the CPU IP address, subnet, and gateway
- Edit the CPU PROFINET name

NOTE

You cannot use the S7-1200 G2 NFC app to perform write operations to a powered off CPU. See the CPU conditions for Read/Write commands (Page 192) for more information.

You have the option to enable write access with or without enabling and setting a password. If you select the optional "Write password" and set a password in your STEP 7 project configuration, the app will prompt you to enter the password to perform a write operation.

⚠ WARNING

Enabling write access without a password

If you enable write access without enabling and setting a write password, unauthorized users could modify CPU data and execute functions. Unauthorized access to the CPU can disrupt process operation.

To reduce the risk of disrupting process operation, enable "Write password" and set a strong password as defined in STEP 7.

Failure to comply with these guidelines could result in severe personal injury, property damage, and/or death.

6.3 Scanning a device with the S7-1200 G2 NFC app

You can use the S7-1200 G2 NFC app to scan an S7-1200 G2 CPU.

To scan and identify a CPU, do the following:

1. Press the "Read" icon in the bottom, center of the S7-1200 G2 NFC app. The “Ready to Scan” pop-up will guide you to "Hold phone close to the front of the CPU".
2. Hold your smartphone within 1cm of the symbol on the CPU. Hold in place until you receive a blue circle and checkmark icon with the message, "NFC read was successful". Note that a scan times out within 60 seconds if the S7-1200 G2 NFC app does not read a compatible NFC tag.

The new device information shows on the main screen and in "Settings > Recent Devices Scanned".

Known issue

AirDrop® is an iPhone feature that allows users to exchange data between two iPhones using NFC. If you have the S7-1200 G2 NFC app open to the "Ready to Scan" screen on one iPhone and bring another iPhone close by, AirDrop causes you receive the blue checkmark icon with the "NFC read was successful" message when, in fact, the application did not read from the S7-1200 G2 device. Scan the NFC tag on your S7-1200 G2 CPU without another iPhone in close proximity to achieve a successful read.

Troubleshooting

If you are having trouble scanning your device, refer to Troubleshooting (Page 193) for help.

6.4 Working with devices in the S7-1200 G2 NFC app

You can select, update, and remove devices in the S7-1200 G2 NFC app.

Selecting a device

By default, the main screen only displays the last scanned device. To select another scanned device, tap "Settings > Recent Devices Scanned" and select the device from the list.

Updating a device

Rescan the device to update the scan date and timestamp. This does not change your previously specified app settings.

Removing a device

To remove a device, do the following:

1. Tap the settings icon
2. Select "Recent Devices Scanned".
3. Swipe left and select "Delete" for the device you want to delete.

6.5 CPU conditions for Read/Write commands

The S7-1200 G2 NFC app supports various commands for reading information from the CPU, writing commands to perform operations, and writing IP suite data and PROFINET names to the CPU. Use the key below to identify your specific CPU use condition:

CPU is powered on:

1. Configured in STEP 7, NFC and write access enabled for the CPU
2. Configured in STEP 7, NFC enabled for the CPU, write access not enabled for the CPU.
3. Configured in STEP 7, NFC is not enabled for the CPU
4. Not configured in STEP 7

CPU is powered off:

5. Configured in STEP 7, NFC is enabled for the CPU
6. Configured in STEP 7, NFC is not enabled for the CPU
7. Not configured in STEP 7

Use the following table to determine which commands are supported in the S7-1200 G2 NFC app for each CPU use condition:

S7-1200 G2 NFC App Button	Operation	Condition						
		1	2	3	4	5	6	7
 Allows you to view specific device information for the CPU and its connected CB/SBs and CM/SMs.	Device type	Read	Read	--	Read	Read	--	Read
	Article number	Read	Read	--	Read	Read	--	Read
	Hardware version	Read	Read	--	Read	Read	--	Read
	Serial number (SN)	Read	Read	--	Read	Read	--	Read
	Firmware version	Read	Read	--	Read	Read	--	Read
	Slot number	Read	Read	--	Read	Read	--	Read
	MAC address	Read	Read	--	Read	Read	--	Read
	IP address, Subnet, Gateway, PROFINET name	Read/ Write	Read	--	Read/ Write	Read	--	Read
	Webserver on/off	Read	Read	--	Read	Read	--	--
	TIA Portal version	Read	Read	--	Read	Read	--	--
	SD card info	Read	Read	--	Read	--	--	--
 Allows you to read/write operations.	Operating mode	Read/ Write	Read	--	Read	--	--	--
	Reset memory	Write	--	--	Write	--	--	--
	Set Time of Day	Write	--	--	Write	--	--	--
	Configured vs actual device diagnostics	Read	Read	--	Read	Read	--	Read

S7-1200 G2 NFC App Button	Operation	Condition						
		1	2	3	4	5	6	7
 Allows you to read diagnostics.	Cycle times	Read	Read	--	Read	--	--	--
	CPU memory usage	Read	Read	--	Read	--	--	--
	Diagnostic buffer	Read	Read	--	Read	--	--	--

6.6 Troubleshooting

If you are having trouble, reference the following troubleshooting guide:

Issue	Possible cause	Potential corrective action
Scan does not complete	Phone is too far away from the CPU.	Move the phone closer to the CPU or tap the phone lightly against the NFC marking on the CPU and hold until you receive confirmation of a successful read.
	Phone was moved away from the CPU too quickly.	The amount of data transferred from the CPU to the S7-1200 G2 NFC app on a read affects the read time. Be sure to keep the phone in place for at least 5 seconds to allow time for the to read to complete.
	The target CPU does not have NFC enabled in STEP 7.	Activate NFC in your STEP 7 device configuration and download the new project configuration to the CPU.
	The NFC enabled project in STEP 7 has not been downloaded to the CPU.	Download the project configuration to the CPU.
	You have read from a device that is not equipped with NFC capabilities.	The S7-1200 G2 is currently the only CPU enabled with the digital NFC tag and available for use with the NFC app.
	The NFC tag in the device is damaged or defective.	Check the diagnostics log to confirm a detected hardware issue. If one exists, replace the CPU.
Receiving "Unsupported Device" message	A hardware component was released after the NFC app.	Update the NFC app.
	You scanned an NFC tag in an incompatible device.	Only scan Siemens S7-1200 G2 devices with the S7-1200 G2 NFC app.
Password is not accepted	You have entered an Incorrect password.	Check the password you set when you enabled NFC protection in STEP 7 for the target CPU and re-enter your password.

Issue	Possible cause	Potential corrective action
Password is not accepted	You have forgotten your password.	In STEP 7, navigate to Properties > NFC > Enable NFC protection, reset the password (Page 189), and download the project to your CPU. If you do not have access to the STEP 7 project, request that the project owner provides or resets the NFC protection password.
	You have downloaded a new configuration to the CPU with NFC protection disabled	Use your iPhone to re-read your CPU's NFC tag.
Changing the IP address or PROFINET name using the S7-1200 G2 NFC app does not work	You configured IP address and/or PROFINET name in your STEP 7 project.	Configuring your IP address and/or PROFINET name in your STEP 7 project disables writes to those areas from the S7-1200 G2 NFC app. To configure those settings with the app, delete them from your STEP 7 project and download the new project configuration to the CPU.

Web server

7

The S7-1200 G2 CPU Web server provides a Web API for you to develop custom Web pages that can read and write process data. The S7-1200 G2 Web API implements the functionality of the S7-1500 Web API, which is documented in the chapter **Web pages > Application Programming Interface (API)** of this Web server manual (https://support.industry.siemens.com/cs/ww/en/view/59193560).

Differences from the S7-1500 Web API

The Web server manual describes the Web API functionality for S7-1500 CPUs and other controllers. This functionality is available for S7-1200 G2 CPUs, with the following exceptions and differences:

- The S7-1200 G2 CPU does not provide standard Web pages. You have the flexibility to design the pages you need for your purposes.
- The number of concurrent API sessions is 30.
- The S7-1200 G2 does not support the following API methods:
  - Plc.CreateBackup
  - Plc.RestoreBackup

Default page for Web application

You can use the following methods to set a default page for Web pages that you create with the Web API:

- WebServer.SetDefaultPage
- WebApp.SetDefaultPage

If you have not created a Web application and configured a default page, the Web browser returns a 404 error. For information on configuring and setting default pages, refer to the Web server manual (https://support.industry.siemens.com/cs/ww/en/view/59193560)

Examples

Refer to the online examples for developing Web pages. The examples demonstrate a variety of functions.

Additional information

With the functionality of the Web API, S7-1200 G2 does not support the former AWP commands for developing user-defined Web pages.

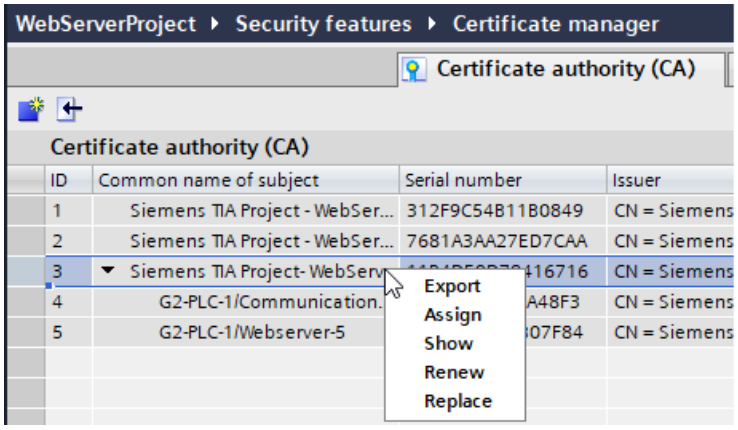
The Web API does not include a method for updating firmware.

7.1 Certificate requirements for the Web server

To communicate with the S7-1200 G2 Web API using a web browser, you must have a trusted Certificate Authority (CA) installed on your programming device. The trusted Certificate Authority (CA) enables secure communications over HTTPs.

The process includes the following tasks:

- Protecting the TIA Portal project from Security settings > Settings > Protect this project, as described in the TIA Portal Information System, Activating project protection topic
- Selecting "Use global security settings for certificate manager" for your CPU in the device configuration properties, Protection & Security > Certificate manager
- Creating a PLC communication certificate (Page 135)
- Enabling the Web server in the device configuration of the CPU (Page 114)
- Using the Security settings > Security features > Certificate manager to install or export the PLC communication certificate and Web server certificate, as described in the TIA Portal Information System, Certificate manager chapter



- Following the FAQ (https://support.industry.siemens.com/cs/ww/en/view/103528224) beginning with Step 2 to install, store, and trust the certificates you installed or exported from the TIA Portal project.

References

For additional information on managing certificates for the Web server, refer to the TIA Portal Information System and these documents:

- Web server manual (https://support.industry.siemens.com/cs/ww/en/view/59193560)
- How to install a certificate for the Web server (https://support.industry.siemens.com/cs/ww/en/view/103528224)

These documents are applicable to S7-1500 CPUs, but most of the content is applicable to S7-1200 G2 CPUs.

Motion control

8

8.1 Introducing S7-1200 G2 Motion Control

Motion Control allows users to accomplish specific tasks that require movement of tools or materials, such as bottling, machining, or welding.

Machines and production lines must increasingly be adapted to different formats, sizes, product types, and production processes. S7-1200 G2 Motion Control offers a precise, dynamic and easy-to-implement solution.

Motion Control instructions control drives with PROFIdrive capability, drives with analog setpoint interface, and servo motors in accordance with the PLCopen standard. The axis control panel and comprehensive online and diagnostic functions support commissioning and optimization of drives. S7-1200 G2 Motion Control is fully integrated into the S7-1200 G2 CPU.

Achieving motion control

You can achieve Motion Control with the S7-1200 G2 CPU using the following concepts:

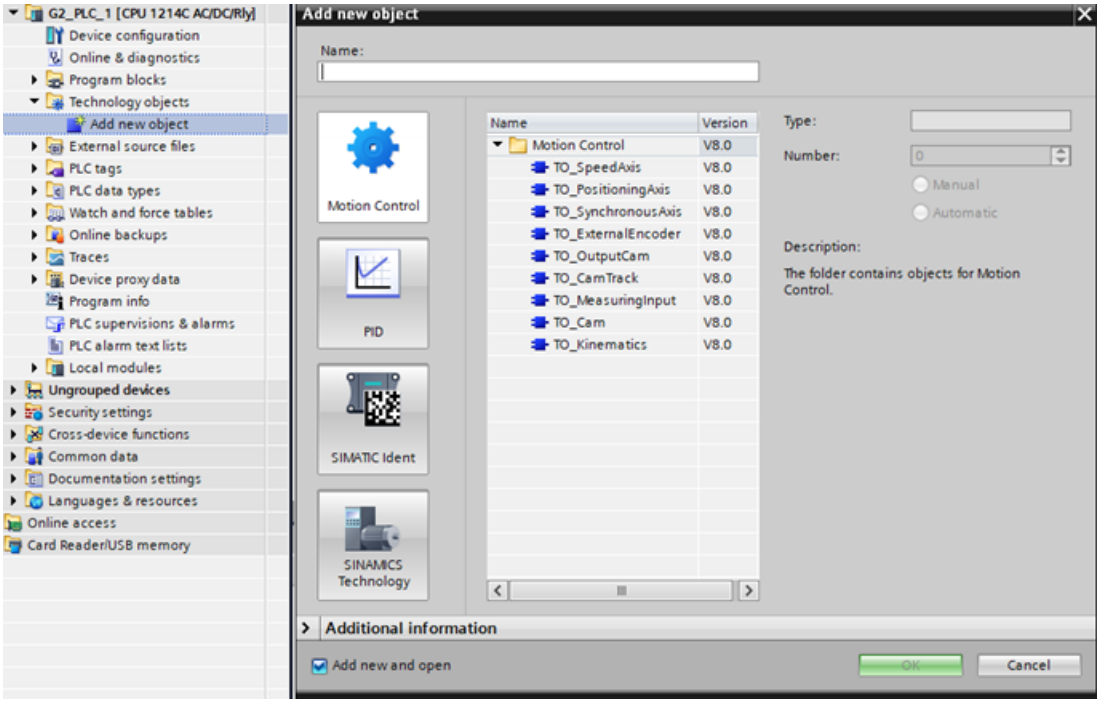
- Technology Objects serve as links to the drive and allow for configuration of dynamic behavior.
- Motion Control instructions allow you to control each Technology Object.
- Organization Blocks execute the Motion Control instructions of the user program in a structured manner.

8.2 Motion Control Technology Objects (TOs)

In S7-1200 G2 Motion Control, the technology objects (TO) represent control elements of Motion Control, such as a position axis or an output cam. A TO establishes a logical relationship between the user program and the physical device and defines the motion profile by allowing for parameterization, such as setting limits like acceleration, deceleration, and jerk. This information is stored in a corresponding technology data block (DB), where you can read information about the status of the motion control job, such as speed, position, or error status.

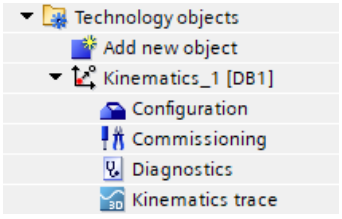
Creating a new TO

You can add a TO to your STEP 7 project by selecting "Add new object" under the Technology objects folder in the project tree.



Configuration and commissioning

Within STEP 7, multiple tools exist to help configure, commission, and debug TOs in your motion control project.



Motion resources

When you create a motion control TO, that TO draws from a pool of resources which represents the resources available within the CPU for motion tasks. There are two pools, one each for Motion Control and Extended Motion Control. If you exceed the number of resources available from either pool, an error occurs when you compile your program in the TIA Portal.

The costs associated with each TO are additive in some cases. For example, implementing a three-axis Cartesian Portal solution requires one Kinematics TO, costing 30 Extended Motion

Control resources, and three PositioningAxis TOs, costing 80 Motion Control resources each. In this case, the total cost is 30 Extended resources and 240 Motion resources.

You can find more information about motion resources in the Technical Specifications (Page 229).

Supported TOs

The S7-1200 G2 CPU provides varying levels of support for a range of Motion Control TOs, as described in the table below:

TO	Supported	Motion Control resources required (out of 800 provided by the CPU)	Extended Motion Control resources required (out of 40 provided by the CPU)
TO_SpeedAxis	✓	40	
TO_PositioningAxis	✓	80	
TO_SynchronousAxis	✓	160	
TO_ExternalEncoder	✓	80	
TO_OutputCam	✓	20	
TO_CamTrack	✓	160	
TO_MeasuringInput	✓	40	
TO_Cam	Partially supported		2
TO_Kinematics	Partially supported		30

You can find help on programming each Motion Control TO in the TIA Portal Information System, as defined for the S7-1500/S7-1500T. These TOs are equivalent in S7-1200 G2.

8.3 Motion Control instructions

The STEP 7 program calls the Motion Control (MC) instructions and acts upon configured TOs. These blocks exist within the motion library as function blocks (FB) and create a data instance when they are placed into the user program in STEP 7.

You can use MC instructions to accomplish motion tasks of varying complexity, such as setting a constant velocity, moving a tool to a desired position, or synchronizing two axes.

Supported instructions

The following MC instructions are available for the S7-1200 G2 CPU:

MC instruction	Motion Control	Extended Motion Control
MC_Power	✓	
MC_Reset	✓	
MC_Home	✓	
MC_Halt	✓	
MC_MoveAbsolute	✓	
MC_MoveRelative	✓	
MC_MoveVelocity	✓	
MC_MoveJog	✓	
MC_Stop	✓	
MC_SetAxisSTW	✓	
MC_SaveAbsoluteEncoderData	✓	
MC_SetSensor		✓
MC_MeasuringInput	✓	
MC_MeasuringInputCyclic	✓	
MC_AbortMeasuringInput	✓	
MC_OutputCam	✓	
MC_CamTrack	✓	
MC_GearIn	✓	
MC_PhasingRelative		✓
MC_PhasingAbsolute		✓
MC_CamIn		✓
MC_GearOut		✓
MC_CamOut		✓
MC_InterpolateCam		✓
MC_GetCamLeadingValue		✓
MC_GetCamFollowingValue		✓
MC_GroupInterrupt		✓
MC_GroupContinue		✓
MC_GroupStop		✓
MC_MoveLinearAbsolute		✓

MC instruction	Motion Control	Extended Motion Control
MC_MoveLinearRelative		✓
MC_MoveCircularAbsolute		✓
MC_MoveCircularRelative		✓

You can find help on programming each MC instruction in the TIA Portal Information System, as defined for the S7-1500/S7-1500T. These instructions are equivalent in S7-1200 G2.

8.4 Motion Control Organization Blocks (OBs)

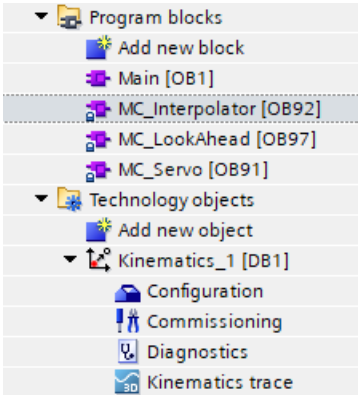
You can use an organization block (OB) to control how the CPU executes STEP 7 programs and handles interrupts and events. For Motion Control, this might mean executing closed-loop position control algorithms of TOs, monitoring and generating setpoints, or executing logic to create the desired movement of the axis.

Generated OBs

There are two types of OBs related to motion control. User OBs allow you to enter your motion control logic. Compiler-generated OBs are protected blocks and cannot be edited.

Supporting OBs

STEP 7 creates supporting organization blocks (OB) when you create a TO in your project.



G2-supported OBs

The S7-1200 G2 CPU provides support for the following Motion Control OBs:

- MC_PreServo (Page 71) - the CPU calls MC_PreServo immediately before MC_Servo, allowing you to make adjustments before the Servo logic executes.
- MC_Servo (Page 69) - performs calculations required to control the speed and position of axes. This block is protected.
- MC_PostServo (Page 72) - the CPU calls MC_PostServo immediately after MC_Servo executes, allowing you to modify outputs.

- MC_PreInterpolator - the CPU calls MC_PreInterpolator immediately before MC_Interpolator executes, allowing you to adjust inputs used by MC_Interpolator. These inputs will be IPO-synchronous.
- MC_Interpolator (Page 69) - evaluates Motion Control instructions, generates setpoints, and monitors inputs. This block is protected.
- MC_LookAhead (Page 72) - calculates motion processing for the Kinematics TO. This block is protected.

You can find help on programming each Motion Control OB in the TIA Portal Information System, as defined for the S7-1500/S7-1500T. These OBs are equivalent in S7-1200 G2.

8.5 Differences between S7-1200 G2 and S7-1500/S7-1500T

S7-1200 G2 Motion Control is similar In function to that of the S7-1500/1500T, with the following notable additions:

- Support for a subset of Extended Motion Control
- Support for a subset of Kinematics devices
  - Kinematics Cartesian Portal up to 3D with Orientation
- Support for Camming is limited to Points
- Support for library versions V8.0 and greater
- Support for single core only

S7-1200 G2 Motion Control is similar In function to that of the S7-1500/1500T, with the following notable differences:

- No support for PTO-based motion control
- No support for Kinematics Zones
- No support for User Defined Kinematics

8.5.1 Adapting Motion Control to S7-1200 G2

S7-1200 G2 motion control differs from that of the S7-1200. The S7-1200 G2 CPU uses Motion Control based upon the same technology used by the S7-1500/S7-1500T. However, the S7-1200 G2 does not use Basic Motion Control, while the S7-1200 does. For these reasons, you cannot load an S7-1200 project with motion control into an S7-1200 G2 CPU.

You must manually port your S7-1200 motion control projects into S7-1200 G2. Consider the following when performing this migration:

- The TOs are different
  - Pulse Train Output (PTO) is not supported.
  - TO_CommandTable is not supported.
  - Configuration interfaces in STEP 7 differ.
- The MC library is different
  - You will need to drop and replace new blocks from the new library.
  - The behavior of most blocks is the same across libraries.
  - Some MC instructions no longer exist.

NOTE

This is not a comprehensive list of differences.

8.6 Additional information

Siemens offers additional support for S7-1200 G2 Motion Control.

See also

You can learn more about Motion Control topics through the STEP 7 Help System.

You can also refer to the family of Motion Control V8.0 manuals available through Siemens Industry Online Support (https://support.industry.siemens.com/cs/start?lc=en-US).

PID

9

9.1 PID functionality

STEP 7 provides the following PID instructions for the S7-1200 G2 CPU:

- The PID_Compact instruction is used to control technical processes with continuous or PWM input variables.
- The PID_3Step instruction is used to control motor-actuated devices, such as valves that require discrete signals for open- and close actuation or analog signal for specification of the target position.
- The PID_Temp instruction provides a universal PID controller that allows handling of the specific requirements of temperature control.

NOTE

Changes that you make to the PID configuration and download in RUN do not take effect until the CPU transitions from STOP to RUN mode. Changes that you make in the "PID parameters" dialog might not take effect immediately.

All three PID instructions (PID_Compact, PID_3Step, and PID_Temp) can calculate the proportional, integral, and derivative parameters for your controlled system during pretuning. You can also use fine tuning to tune the parameters further. You do not need to manually determine the parameters.

NOTE

Execute the PID instruction at constant intervals of the sampling time, preferably in a cyclic OB. Do not execute the PID instruction in the main program cycle OB, such as OB 1.

The sampling time of the PID algorithm represents the time between two calculations of the output value (control value). The sampling time of the PID algorithm is calculated during self-tuning and rounded to a multiple of the cycle time. All other functions of PID instruction are executed at every call.

PID algorithm

The output value for the PID controller consists of three components:

- P (proportional): When calculated with the "P" component, the output value is proportional to the difference between the setpoint and the process value (input value).
- I (integral): When calculated with the "I" component, the output value increases in proportion to the duration and value of the difference between the setpoint and the process value (input value) to correct the difference.
- D (derivative): When calculated with the "D" component, the output value increases as a function of the rate of change of the difference between the setpoint and the process value (input value). The process value is corrected to the setpoint as quickly as possible.

The PID controller uses the following formula to calculate the output value for the PID_Compact and PID_Temp instructions.

$$y = K_p \left[(b \cdot w - x) + \frac{1}{T_I \cdot s} (w - x) + \frac{T_D \cdot s}{a \cdot T_D \cdot s + 1} (c \cdot w - x) \right]$$

y	Output value	x	Process value
w	Setpoint value	s	Laplace operator
K_p	Proportional gain (P, I, D components)	a	Derivative delay coefficient (D component)
T_I	Integral action time (I component)	b	Proportional action weighting (P component)
T_D	Derivative action time (D component)	c	Derivative action weighting (D component)

The PID controller uses the following formula to calculate the output value for the PID_3Step instruction.

$$\Delta y = K_p \cdot s \cdot \left[(b \cdot w - x) + \frac{1}{T_I \cdot s} (w - x) + \frac{T_D \cdot s}{a \cdot T_D \cdot s + 1} (c \cdot w - x) \right]$$

y	Output value	x	Process value
w	Setpoint value	s	Laplace operator
K_p	Proportional gain (P, I, D components)	a	Derivative delay coefficient (D component)
T_I	Integral action time (I component)	b	Proportional action weighting (P component)
T_D	Derivative action time (D component)	c	Derivative action weighting (D component)

See also

For a comprehensive explanation of PID functions and instructions, see the "SIMATIC S7-1200, S7-1500 PID control" Function Manual (https://support.industry.siemens.com/cs/us/en/view/108210036), or find more information in the TIA Portal Information System.

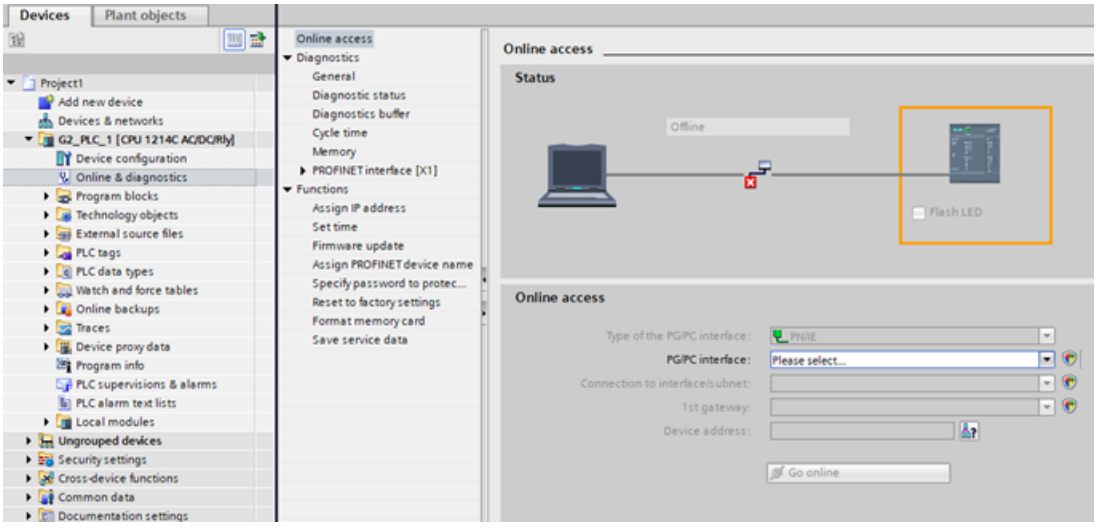
Online and diagnostic tools

10

10.1 Overview

TIA Portal enables you to set diagnostic parameters and modify settings for the online behavior of your S7-1200 G2 CPU by using the tools listed below. You can update firmware, monitor cycle time and memory usage, and monitor or modify values in the CPU, in addition to other valuable functions.

To configure these parameters, select the CPU in the Project tree and select "Online & diagnostics" from the drop-down menu.



Tool	Description
Online access	
Online access	You can establish an online connection between the programming device and CPU for loading programs and project engineering data. For protected CPUs, you must enter either the access level CPU password or a user and user password. User roles and passwords are part of User Management and Access Control (UMAC) (Page 106) in the STEP 7 project.
Diagnostics	
General	Displays general information about the modules in your project.
Diagnostic status	Displays the status of diagnostic processes.
Diagnostics buffer (Page 84)	Use the diagnostics buffer to review the recent activity in the CPU. The diagnostics buffer is accessible from "Online & diagnostics" for an online CPU in the Project tree. It contains the following entries: • Diagnostic events • Changes in the CPU operating mode (transitions to STOP or RUN mode)

Tool	Description
Cycle time	You can monitor the cycle time of an online CPU. After connecting to the online CPU, open the Online tools task card to view the relevant measurements.
Memory	You can monitor the memory usage of an online CPU. After connecting to the online CPU, open the Online tools task card to view the relevant measurements.
PROFINET interface	You can use the PROFINET interface to view MAC addresses, IP Addresses, and Port settings.
Functions	
Assign IP address	After accessing "Online & diagnostics" from the Project tree for an online CPU, you can display or change the IP address.
Set time	You can display or set the time and date parameters of the online CPU.
Firmware update	You can update the firmware of a connected CPU from the TIA Portal online and diagnostics tools using one of two methods: • Updating from the CPU in the project • Updating from the accessible devices in the project tree
Assign PROFINET device name	The devices on your PROFINET network must have an assigned name before you can connect with the CPU. Use the "Devices & networks" editor to assign names to your PROFINET devices if the devices have not already been assigned a name, or if the name of the device is to be changed.
Set password for protection of PLC configuration data	The "Protection of confidential PLC configuration data" feature allows you to protect each CPU in your project individually. From the device configuration, you can enable this protection and set a password for the "protection of confidential PLC configuration data". Clients such as TIA Portal and the SIMATIC Automation Tool can only access the confidential data in the PLC through use of the password. You can also use the security wizard to enable this feature and set the password for the "protection of confidential PLC configuration data".
Reset to factory settings	You can reset an S7-1200 G2 CPU to its original factory settings under the following conditions: • The CPU has an online connection. • The CPU is in STOP mode. If you reset the CPU to factory defaults, the CPU time will be reset to its default value.
Format memory card	You can format the memory card in a connected CPU from the TIA Portal online and diagnostic tools.
Save service data	In the event of servicing, the SIEMENS Customer Support requires information about the state of a module of your system for diagnostic purposes. If such a case occurs in your system, Customer Support can ask you to save the service data of the module and send the resulting file to them.

You can learn more about the above Tool properties by referring to the related topics in the TIA Portal Information System.

10.2 Status LEDs

The CPU and the I/O modules use LEDs to provide information about the operating state of the CPU and status of the devices.

Status LEDs on a CPU

The CPU provides the following status indicators:

- STOP/RUN
  - Solid yellow indicates STOP mode
  - Solid green indicates RUN mode
  - Flashing (alternating green and yellow) indicates that the CPU is in the STARTUP operating state
- ERROR
  - Flashing red indicates an error, such as an internal error in the CPU, an error with the memory card, or a configuration error (mismatched modules)
  - Flashing red for three seconds indicates a temporary error. An example is if the real time clock (RTC) resets to the default time due to a power loss. Another example would be the failure of an NFC transaction.
  - Defective state:

    - STOP (ON), ERROR (Blinking), MAINT (Blinking)
- MAINT (Maintenance) is ON whenever maintenance is required, or if the NFC tag is defective while NFC is enabled in Device Configuration.

You can also use the LED instruction to determine the status of the LEDs.

Table 10-1 Status LEDs for a CPU

Description	RUN/STOP Green / Yellow	ERROR Red	MAINT Yellow
CPU power off	Off	Off	Off
CPU power up	Flashing (alternating yellow and green)[1]	Flashing[1]	Flashing[1]
STARTUP state	Flashing (alternating yellow and green)[1]	-	Off
Firmware update in progress	Flashing (yellow)	-	-
Firmware update complete	-	-	Flashing
STOP state	On (yellow)	-	-
RUN state	On (green)	-	-
Missing program memory card (if External Load Memory used)	On (yellow)	Flashing	-
Memory card evaluation	Flashing (yellow)	-	-

1 When power is applied to the CPU, all three system-status indicators flash such that ERROR and MAINT are both ON when RUN/STOP is yellow and both OFF when RUN/STOP is green.

2 Cyclically; three seconds Flashing, one second pause.

3 For each NFC transaction failure between CPU and NFC tag, the ERROR LED flashes three times.

Description	RUN/STOP Green / Yellow	ERROR Red	MAINT Yellow
Error	On (either yellow or green)	Flashing	-
Forced I/O	On (either yellow or green)	-	On
NFC defective, NFC enabled in configuration	On (either yellow or green)	-	On
NFC transaction failure	On (either yellow or green)	Flashing (3x)[3]	-
Defective hardware (Page 212)	On (yellow)	On	Off
LED test or defective CPU firmware (Page 212)	Flashing (alternating yellow and green)	Flashing	Flashing
Unknown or incompatible version of CPU configuration (Page 212)	On (yellow)	Flashing	Flashing
Flash LED (Online access feature to identify CPU)[2]	Flashing (alternating yellow and green)	Flashing	Flashing
Internal Load Memory was erased	Flashing (yellow)	Off	Flashing
Internal Load Memory is empty	Flashing (3 seconds) (yellow)	Off	Flashing (3 seconds)

1 When power is applied to the CPU, all three system-status indicators flash such that ERROR and MAINT are both ON when RUN/STOP is yellow and both OFF when RUN/STOP is green.

2 Cyclically; three seconds Flashing, one second pause.

3 For each NFC transaction failure between CPU and NFC tag, the ERROR LED flashes three times.

Status LEDs for onboard I/O

Each CPU shall provide an I/O channel indicator for each onboard digital input and output, according to the table below:

Description	Digital I/O Channel (Green)
CPU power off	Off
Input or output point is Off	Off
Input or output point is On	On

Status LEDs for communication on the CPU

The CPU also provides two LEDs that indicate the status of the PROFINET communications. These LEDs are visible from the top of the CPU near the PROFINET connectors. Each PROFINET port has one LED which behaves according to the table below:

Description	PROFINET port (Green)
CPU power off	Off
Link down (no connection established)	Off
Link up (connection established)	On
Communication activity	Flashing

Status LEDs on a Signal Module (SM) and a Signal Board (SB)

Each digital or analog SM/SB provides a DIAG LED that indicates the status of the module or board:

- Green indicates that the module or board is operational
- Red indicates that the module or board is defective or non-operational

Each digital module or board provides an I/O Channel LED for each of the digital inputs and outputs.

- Green indicates the channel is ON
- OFF indicates the channel is OFF

Each analog module or board provides an I/O Channel LED for each of the analog inputs and outputs.

- Green indicates that the channel has been configured and is active
- Red indicates an error condition of the individual analog input or output

Each analog SB/SM provides an I/O Channel LED for each of the analog inputs and outputs, according to the following table:

Table 10-2 Status LEDs for an analog signal board (SB) or analog signal module (SM)

Description	DIAG (Green/Red)	Analog I/O Channel (Green/Red)
I/O bus power off, user power either on or off	Off	Off
I/O bus power on, user power off		
• Power fault diagnostic is enabled	Flashing (red)	Off
• Power fault diagnostic is disabled	On (green)	On (green)
STARTUP, but not yet logged into the CPU	Flashing (red)	Off

[1] Flashing the LED is only possible when the firmware is operational.

[2] The red DIAG LED acts like a summary fault indication which includes module errors and channel errors with channel diagnostics enabled.

Description	DIAG (Green/Red)	Analog I/O Channel (Green/Red)
Logged in, but not yet configured	Flashing (green)	Off
Module configured with no errors	On (green)	On (green), all enabled channels
Error[1] [2]		
• Module error	Flashing (red)	Flashing (red), all channels
• Channel error with channel diagnostic enabled	Flashing (red)	Flashing (red), affected channel
• Channel error with channel diagnostic disabled	On (green)	On (green), affected channel
Firmware update is running	Flashing (green)	Off

[1] Flashing the LED is only possible when the firmware is operational.

[2] The red DIAG LED acts like a summary fault indication which includes module errors and channel errors with channel diagnostics enabled.

Each digital SB/SM provides an I/O Channel LED for each of the digital inputs and outputs, according to the following table:

Table 10-3 Status LEDs for a digital signal board (SB) or digital signal module (SM)

Description	DIAG (Green/Red)	Digital I/O Channel (Green)
I/O bus power off, user power either on or off	Off	Off
I/O bus power on, user power off		
• Power fault diagnostic is enabled	Flashing (red)	Off
• Power fault diagnostic is disabled	On (green)	Off
STARTUP, but not yet logged into the CPU	Flashing (red)	Off
Logged in, but not yet configured	Flashing (green)	Off
Module configured with no errors		
• Input or output point is Off	On (green)	Off
• Input or output point is On	On (green)	On
Error	Flashing (red)	Off
Firmware update is running	Flashing (green)	Off

10.3 CPU error behavior

"Unknown or incompatible version of CPU configuration" error

The diagnostics buffer can report an "Unknown or incompatible version of CPU configuration" error, which can occur in one of the following ways:

- Attempting to load an invalid project.
- Attempting to download a project with different protection of confidential PLC configuration data (Page 206) between the CPU and the project

If you reached this state by using an invalid version transfer card (Page 96), follow these steps to recover:

1. Remove the transfer card.
2. Perform a STOP to RUN transition.
3. Reset the memory (MRES) or cycle power.

If you reach this state by using an invalid project on a program card (Page 99), reset the CPU to factory settings (Page 206) using the "Format memory card" option .

If your reach this state from a mismatch between the CPU and the project for the protection of confidential PLC configuration data, use the Online & Diagnostics tools (Page 206) to set the online CPU's password for protection of confidential PLC configuration data to the password in the project, or delete it from the online CPU.

After you recover the CPU from the error condition, you can download a valid program.

S7-1200 G2 behavior following a fatal error

If the CPU firmware detects a fatal error, it attempts a defect-mode restart, and if successful, signals the defective mode by continually flashing the STOP/RUN, ERROR and MAINT LEDs.

If the CPU successfully completes the defect-mode restart, the CPU performs these actions:

- Sets the CPU and signal board outputs to the configured value
- Sets the outputs of local rack signal modules and distributed I/O to the selection for "Reaction to CPU STOP" in the device configuration of the digital outputs of the module

If the defect-mode restart fails, (for example, due to a hardware fault), the STOP and ERROR LEDs are ON and the MAINT LED is OFF.

⚠ WARNING

Operation in defect state cannot be guaranteed

Control devices can fail in an unsafe condition, resulting in unexpected operation of controlled equipment.

Use an emergency stop function, electromechanical overrides or other redundant safeguards that are independent of the PLC.

Such unexpected operations can result in death or serious injury to personnel, and/or damage to equipment.

10.4 Analog module diagnostics

Analog modules have multiple diagnostics depending on the module and channel type. You can separately enable or disable these diagnostics for each module and channel by using the TIA Portal under the project's device configuration/general properties of the module.

Power supply errors are reported as follows:

Power supply error	Error reported
Analog module with a power supply diagnostic error reports:	Overflow: 32767 for all input channels
	Missing power supply diagnostic, if enabled for output modules

You can enable these diagnostics separately by channel and type for each channel. See the table below:

Channel type	Error reported
Voltage input	Overflow: 32767
	Underflow: -32768
Current input (0 to 20 mA)	Overflow: 32767
	Underflow: -32768
Current input (4 to 20 mA) (for < 1.185 mA input)	Broken wire: 32767
	Overflow: 32767
Voltage output (for > 0.5 V output)	Short circuit diagnostic, if enabled
Current output (for > 1.0 mA output)	Open circuit diagnostic, if enabled

An analog input module with a diagnostic error on any channel reports 32767 or -32768 on that channel even if the diagnostics is not enabled. Analog input channels report 32767 when deactivated.

10.5 Comparing offline and online CPUs

You can compare the code blocks in an online CPU with the code blocks in your project. If the code blocks of your project do not match the code blocks of the online CPU, the "Compare" editor allows you to synchronize your project with the online CPU by downloading the code blocks of your project to the CPU, or by deleting blocks from the project that do not exist in the online CPU.

NOTE

Read access required on protected CPU for the Offline/Online compare operations

For TIA Portal, the "HMI access" security level is insufficient to perform the Offline/Online compare operations. You must have "Read access" or "Full access", to do Offline/Online compare operations.

See also Protection & Security in CPU properties (Page 114).

You can learn more about comparing offline/online CPUs, as well as their related topologies in your network, by referring to the TIA Portal Information System.

10.6 Monitoring and modifying values in the CPU

10.6.1 Overview of the online monitoring and modification tools

TIA Portal provides online tools for monitoring the CPU:

- You can display or monitor the current values of the tags. The monitoring function does not change the program sequence. It presents you with information about the program sequence and the data of the program in the CPU.
- You can also use other functions to control the sequence and the data of the user program:
  - You can modify the value for the tags in the online CPU to see how the user program responds.
  - You can force a peripheral output (such as Q0.1:P or "Start":P) to a specific value.

NOTE

Always exercise caution when using control functions. These functions can influence the execution of the user/system program.

Table 10-4 Online capabilities of the TIA Portal editors

Editor	Monitor	Modify	Force
Watch table	Yes	Yes	No
Force table	Yes	No	Yes
Program editor	Yes	Yes	No
Tag table	Yes	No	No
DB editor	Yes	Yes	No

You can learn more about online tools for monitoring the CPU by referring to the related topics in the TIA Portal Information System.

10.6.2 Watch tables for monitoring the user program

A watch table allows you to perform monitoring and control functions on data points as the CPU executes your program. These data points can be process image (I or Q), M, DB or physical inputs (I_:P), depending on the monitor or control function. You cannot accurately monitor the physical outputs (Q_:P) because the monitor function can only display the last value written from Q memory and does not read the actual value from the physical outputs.

The monitoring function does not change the program sequence. It presents you with information about the program sequence and the data of the program in the CPU.

Control functions enable the user to control the sequence and the data of the program. You must exercise caution when using control functions. These functions can influence the execution of the user/system program. The two control functions are Modify and Force.

With the watch table, you can perform the following online functions:

- Monitoring the status of the tags
- Modifying values for the individual tags

You can learn more about using a watch table for monitoring and modifying values in the CPU by referring to the related topics in the TIA Portal Information System.

10.6.3 Using the force table

A force table provides a "force" function that overwrites the value for an input or output point to a specified value for the peripheral input or peripheral output address. The CPU applies this forced value to the input process image prior to the execution of the user program and to the output process image before the outputs are written to the modules.

You can learn more about forcing values in the CPU with the Force function by referring to the related topics in the TIA Portal Information System.

10.7 Downloading in RUN mode

10.7.1 Overview

The CPU supports "Download in RUN mode". This capability allows you to download program changes while the program is running.

⚠ WARNING

Risks when downloading in RUN mode

When you download changes to the CPU in RUN mode, the changes immediately affect process operation. Changing the program in RUN mode can result in unexpected system operation.

Only authorized personnel who understand the effects of RUN mode changes on system operation should perform a download in RUN mode.

Unexpected system operation can cause death or serious injury to personnel, and/or damage to equipment.

The "Download in RUN mode" feature allows you to make changes to a program and download them to your CPU without switching to STOP mode:

- You can make minor changes to your current process without having to shut down (for example, change a parameter value).
- You can debug a program more quickly with this feature (for example, invert the logic for a normally open or normally closed switch).

You can make the following program block and tag changes and download them in RUN mode:

- Create, overwrite, and delete Functions (FC), Function Blocks (FB), and Tag tables.
- Create, delete, and overwrite Data Blocks (DB) and instance data blocks for Function Blocks (FB). You can add to DB structures and download them in RUN mode. The CPU can maintain the values of existing block tags and initialize the new data block tags to their initial values, or the CPU can set all data block tags to initial values, depending on your configuration settings.
- Create, overwrite, modify, and delete Organization Blocks (OB).

You can download a maximum number of 20 blocks in RUN mode at one time. If you need to download more than 20 blocks, you must place the CPU in STOP mode.

If you download changes to a running process, you must think through the possible safety consequences to machines and machine operators before you download.

NOTE

If the CPU is in RUN mode and program changes have been made, TIA Portal always tries to download in RUN first. If you do not want this to happen, you must put the CPU into STOP.

If the changes made are not supported in "Download in RUN", TIA Portal prompts you that the CPU must go to STOP.

10.7.2 Prerequisites for "Download in RUN mode"

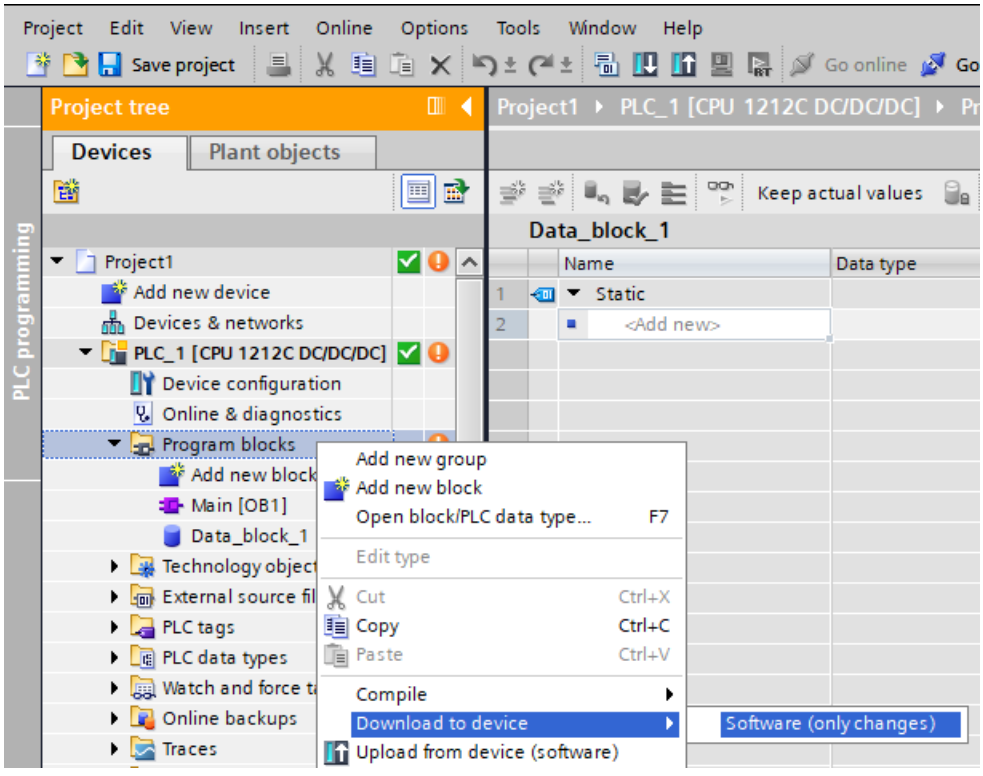
To be able to download your program changes to a CPU that is in RUN mode, you must meet these prerequisites:

- Your program blocks must compile successfully.
- You must have successfully established communication between the CPU and the programming device.

10.7.3 Changing your program in RUN mode

To change the program in RUN mode, you must first ensure that the CPU and program meet the prerequisites (Page 216), and then follow these steps:

1. To download your program in RUN mode, select one of the following methods:
   - Select the "Download to device" command from the "Online" menu.
   - Click the "Download to device" button in the toolbar.
   - In the "Project tree", right-click "Program blocks" and select the "Download to device > Software (only changes)" command.



   If the program compiles successfully, TIA Portal starts to download the program to the CPU.

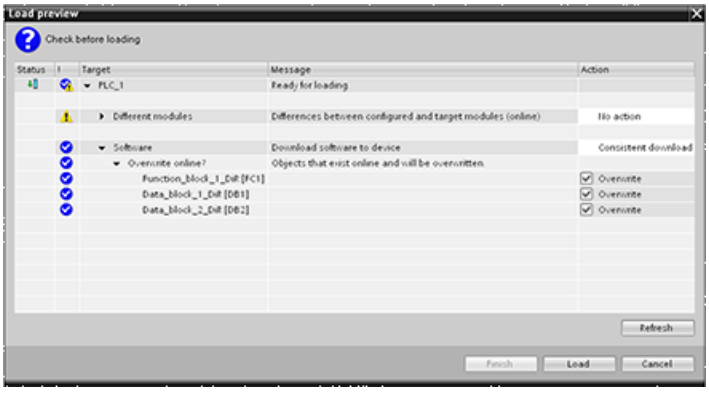
2. When TIA Portal prompts you to load your program or cancel the operation, click "Load" to download the program to the CPU.

10.7.4 Downloading selected blocks

From the Program blocks folder, you can select a single block or a selection of blocks for downloading.

If you select a single block for downloading, then the only option in the "Action" column is "Consistent download".
You can expand the category line to be sure what blocks are to be loaded. In this example, a small change was made to the offline block, and no other blocks need to be loaded.

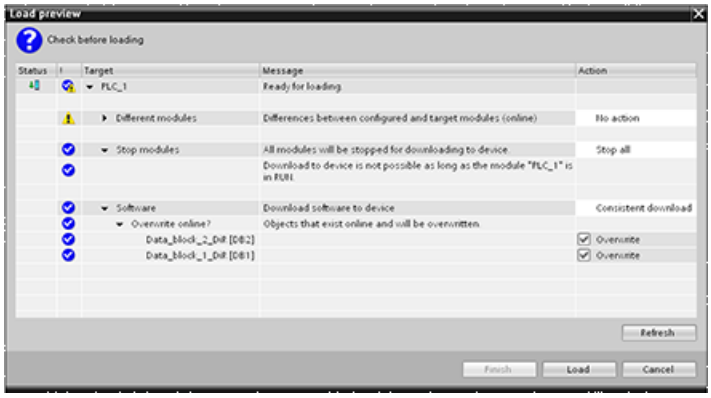
In this example, more than one block is needed for downloading.



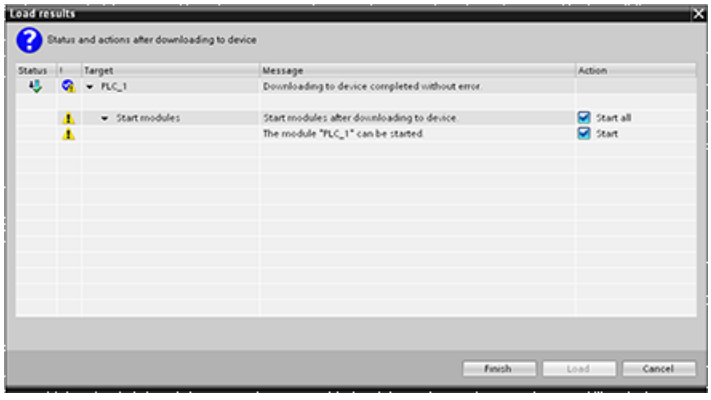
NOTE

You can download a maximum number of 20 blocks in RUN mode at one time. If you need to download more than 20 blocks, you must place the CPU in STOP mode.

If you attempt to download in RUN, but the system detects that this is not possible prior to the actual download, then the Stop modules category line appears in the dialog.

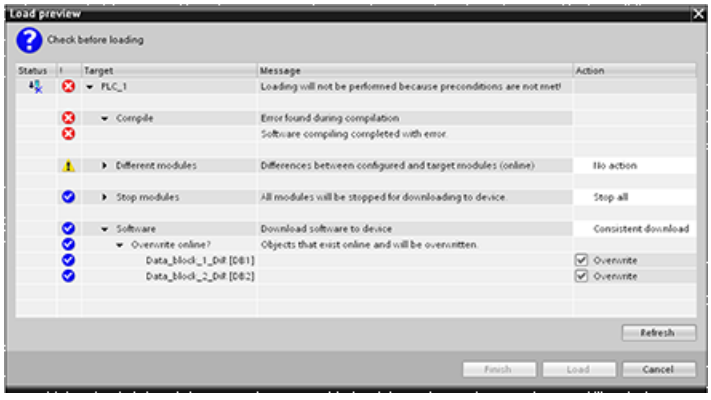


Click the "Load" button, and the "Load results" dialog appears. Click the "Finish" button to complete the download.



10.7.5 Downloading a single selected block with a compile error in another block

If you attempt a consistent download with a compile error in another block, then the dialog indicates an error, and the load button is disabled.



You must correct the compile error in the other block. Then, the "Load" button becomes active.

10.7.6 Modifying and downloading existing tags in RUN mode

The Download in Run feature allows you to add and modify tags in data blocks and function blocks and then download the changed block to the CPU in RUN mode.

Download without reinitialization

Each DB and FB has an amount of reserved memory, which you can use for adding tags to the block that you can subsequently download in RUN mode. By default, the initial size of the memory reserve is 100 bytes. You can add additional tags to your data up to the size of the memory reserve and download the extended block to the CPU in RUN mode. You can also increase the memory reserve if you need more memory for additional tags in your block. If you add more tags than the amount of memory you have allocated, you cannot download the extended block to the CPU in RUN mode.

The "Download without reinitialization" feature allows you to extend a data block by adding more data block tags and download the extended data block in RUN mode. In this way, you can add tags to a data block and download it without reinitializing your program. The CPU retains the values of the existing data block tags and initializes the newly-added tags to their start values.

To enable this function for an online project with a CPU in RUN mode, follow these steps:

1. From the Program blocks folder in the TIA Portal project tree, right-click the block and select "Properties".
2. Click "Download without reinitialization" and select the "Enable download without reinitialization for retentive tags" checkbox in the block editor to enable the function.
3. Click "OK" on the prompt to confirm your choice.
4. Add tags to the block interface and download the block in RUN mode. You can add and download as many new tags as your memory reserve allows.

If you have added more bytes to your block than you have configured for the memory reserve, TIA Portal displays an error when you attempt to download the block in RUN mode. You must edit the block properties to increase the amount. You cannot delete existing entries or modify the “Memory reserve” of the block while the “Download without reinitialization” function is enabled. To disable the "Download without reinitialization" function, follow these steps:

1. From the Program blocks folder in the TIA Portal project tree, right-click the block and select "Properties".
2. Click "Download without reinitialization" and de-select the "Enable download without reinitialization for retentive tags" checkbox in the block editor to disable the function.
3. Click "OK" on the prompt to confirm your choice.
4. Download the block. On the download dialog, you must select "reinitialize" in order to download the extended block.

The download then reinitializes all existing and new block tags to their start values.

Downloading retentive block tags

Downloading retentive block tags in RUN mode requires the allocation of a retentive memory reserve. To configure this retentive memory reserve, follow these steps:

1. From the Program blocks folder in the TIA Portal project tree, right-click the block and select "Properties" from the context menu.
2. Select the "Download without reinitialization" property.
3. Select the check box for "Enable download without reinitialization for retentive tags".
4. Configure the number of bytes available for the retentive memory reserve.
5. Click "OK" to save your changes.
6. Add retentive data block tags to the data block and download the data block in RUN mode.

To add and download as many new retentive data block tags as your retentive memory reserve allows, click "Activate memory reserve" on the toolbar. For more information, refer to "Basic information on loading block extensions without reinitialization" in the TIA Portal Information System.

If you have added more retentive bytes to your data block than you have configured for the retentive memory reserve, TIA Portal displays an error when you attempt to download the block in RUN mode. You can only add retentive block tags up to the retentive memory reserve in order to be able to download them in RUN mode.

When you download the extended retentive block tags, the tags contain their current values.

Configuring amount of reserved memory for new blocks

The default memory reserve size for new data blocks is 100 bytes. When you create a new block, it has 100 bytes available in reserve. If you want the memory reserve size to be different for new blocks, you can change the setting in the PLC programming settings:

1. From TIA Portal, select the **Options > Settings** menu command.
2. From the Settings dialog, expand "PLC programming" and select "General".
3. In the "Download without reinitialization" section, enter the number of bytes for the memory reserve.

When you create new blocks, TIA Portal uses the memory reserve configuration that you entered for the new blocks.

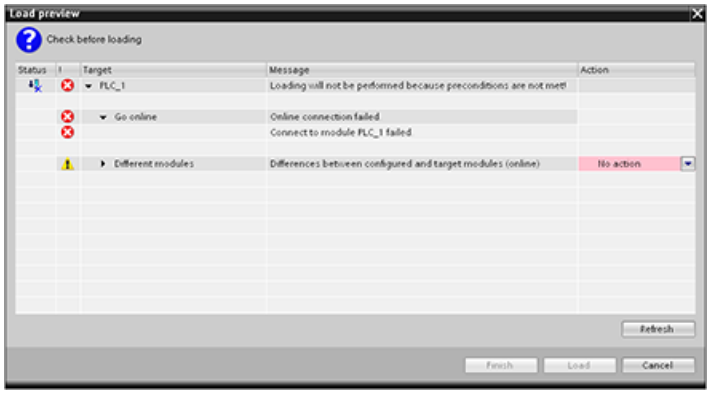
Restrictions

The following restrictions apply to editing and downloading blocks in RUN mode:

- Extending the block interface by adding new tags and downloading in RUN mode is only available for optimized blocks.
- You cannot change the structure of a block and download the changed block in RUN mode without reinitializing. Adding new members to a Struct tag, changing tag names, array sizes, data types, or retentive status all require that you reinitialize the block if you download it in RUN mode. The only modifications to existing block tags that you can perform and still download the block in RUN mode without reinitialization are changes to start values (data blocks), default values (function blocks) or comments.
- You cannot download more new block tags in RUN mode than the memory reserve can accommodate.
- You cannot download more new retentive block tags in RUN mode than the retentive memory reserve can accommodate.

10.7.7 System reaction if the download process fails

During the initial Download in RUN operation, if a network connection failure occurs, STEP 7 displays the following "Load preview" dialog:



10.7.8 Considerations when downloading in RUN mode

Before downloading the program in RUN mode, consider the effect of a RUN-mode modification on the operation of the CPU for the following situations:

- If you deleted the control logic for an output, the CPU maintains the last state of the output until the next power cycle or transition to STOP mode.
- If you deleted a high-speed counter or pulse output functions which were running, the high-speed counter or pulse output continues to run until the next power cycle or transition to STOP mode.
- Any logic that is conditional on the state of the first scan bit will not be executed until the next power cycle or transition from STOP to RUN mode. The first scan bit is set only by the transition to RUN mode and is not affected by a download in RUN mode.
- The current values of data blocks (DBs) and/or tags can be overwritten.

Requirements

Before you can download your program in RUN mode, the program must compile with no errors, and the communication between TIA Portal and the CPU must be error-free.

You can make the following changes in program blocks and tags and download them in RUN mode:

- Create, overwrite, and delete Functions (FCs), Function Blocks (FBs), and Tag tables.
- Create and delete Data Blocks (DBs); however, DB structure changes cannot be overwritten. Initial DB values can be overwritten. You cannot download a Web server DB (control or fragment) in RUN mode.
- Create, overwrite, and delete Organization Blocks (OBs).

You can download a maximum number of 20 blocks in RUN mode at one time. If you need to download more than 20 blocks, you must place the CPU in STOP mode.

Once you initiate a download, you cannot perform other tasks in TIA Portal until the download completes.

Instructions that might fail due to "Download in RUN mode"

The following instructions might experience a temporary error when download in RUN mode changes are being activated in the CPU. The error occurs when the instruction is initiated while the CPU is preparing to activate the downloaded changes. During this time, the CPU suspends initiation of user-program access to the Load Memory, while it completes in-progress user program access to Load Memory. This is done so that downloaded changes can be activated consistently.

Instruction	Response while Activation is Pending
DataLogCreate	STATUS = W#16#80C0, ERROR = TRUE
DataLogOpen	STATUS = W#16#80C0, ERROR = TRUE
DataLogWrite	STATUS = W#16#80C0, ERROR = TRUE
DataLogClose	STATUS = W#16#80C0, ERROR = TRUE
DataLogNewFile	STATUS = W#16#80C0, ERROR = TRUE
DataLogClear	STATUS = W#16#80C0, ERROR = TRUE
DataLogDelete	STATUS = W#16#80C0, ERROR = TRUE
READ_DBL	RET_VAL = W#16#82C0
WRIT_DBL	RET_VAL = W#16#82C0
CREATE_DB	RET_VAL = W#16#80C0
DELETE_DB	RET_VAL = W#16#80C0
RTM	RET_VAL = W#16#80C0

In all cases the RLO output from the instruction will be false when the error occurs. The error is temporary. If it occurs, the instruction should be retried later.

If one of the above instructions fails to execute because a download in RUN mode was in process, retry the failed instruction in a subsequent execution of that OB. If you retry the instruction in the same OB execution, it will fail.

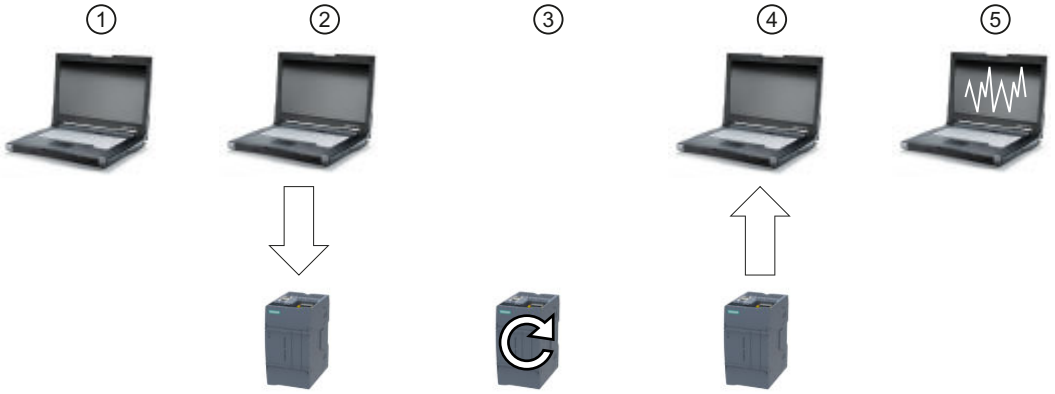
10.8 Tracing and recording CPU data on trigger conditions

TIA Portal provides trace and logic analyzer functions with which you can configure variables for the PLC to trace and record. You can then upload the recorded trace measurement data to your programming device and use TIA Portal tools to analyze, manage, and graph your data. You use the Traces folder in the TIA Portal project tree to create and manage traces.

NOTE

The trace measurement data is available only within the TIA Portal project and is not available for processing by other tools.

The following figure shows the various steps of the trace feature:



① Configure the trace in the trace editor of TIA Portal You can configure the following options:
- Data values to record
- Recording duration
- Recording frequency
- Trigger condition

② Transfer the trace configuration from TIA Portal to the PLC.

③ The PLC executes the program, and when the trigger condition occurs, begins recording the trace data.

④ Transfer the recorded values from the PLC to TIA Portal.

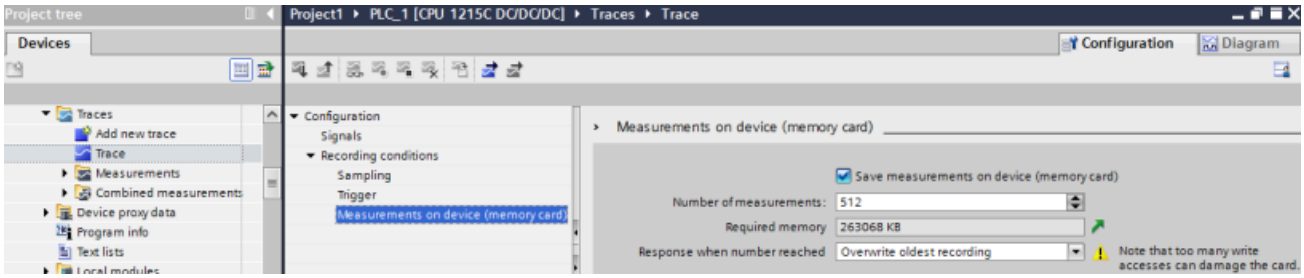
⑤ Use the tools in TIA Portal to analyze, graphically display, and save the data.

The S7-1200 G2 supports four trace jobs with a maximum of 16 variables captured per trigger event. Each trace job provides 512 Kbytes of RAM for the recording of trace values and associated overhead, for example variable addresses and time stamps.

Saving trace measurements to the memory card

The S7-1200 G2 CPU can only save trace measurements to the SIMATIC memory card. If you do not have a memory card in your CPU, the CPU will log a diagnostics buffer entry if the program attempts to save trace measurements. The CPU limits the space allocated to trace measurements such that 1 MB of external load memory must always be available. If a trace measurement would require more memory than the maximum allowance, the CPU will not save the measurement and will log a diagnostics buffer entry.

In addition, if you select "Overwrite oldest recording" in TIA Portal, the continual writing can reduce the lifetime of load memory. When you select "Overwrite oldest recording", the CPU replaces the oldest measurement with the newest measurement after it has stored the configured number of trace measurements, and continues tracing and saving measurements. Overwriting the oldest measurements is useful in capturing intermittent problems.



The CPU supports a maximum of 1000 trace measurement results. During the time that the CPU is saving the trace measurements to external load memory, the CPU does not check the trigger condition for the trace job. Once the CPU finishes saving the trace measurements, the CPU resumes checking for trigger conditions.

Access to examples

See the TIA Portal Information System for details about how to program a trace, how to download the configuration, upload the trace data, and display the data in the logic analyzer. You can find detailed examples there in the "Using online and diagnostics functions > Using the trace and logic analyzer function" chapter.

In addition, the online manual "Industry Automation SINAMICS/SIMATIC Using the trace and logic analyzer function" (https://support.industry.siemens.com/cs/us/en/view/64897128) is an excellent reference.

10.9 Determining the type of wire break condition from an SM 1231 module

As described in the topic Analog module diagnostics (Page 213), the SM 1231 module returns an analog input value of 32767 (16#7FFF) for both a wire break condition or an overflow condition. These conditions apply to the module only and not the channel. If you want to determine which of these two conditions occurred, you can include logic in your STEP 7 program to make the determination. The method to determine the condition type consists of these tasks:

- Create a Diagnostic error interrupt OB to be called whenever there is an incoming or outgoing diagnostic event.
- Include a call to the RALRM instruction.
- Set up an array of bytes for the AINFO parameter, which includes the information about the condition type.
- Evaluate bytes 32 and 33 of the AINFO structure of the RALRM_DB when the CPU triggers the Diagnostic Interrupt OB..

Creating a Diagnostic error interrupt OB

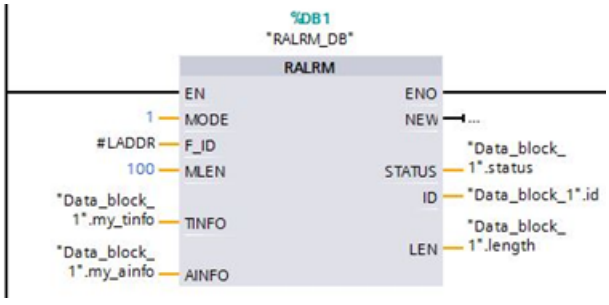
To be able to determine when a wire break condition occurs, create a Diagnostic error interrupt OB. The CPU calls this OB whenever an incoming or outgoing diagnostic event occurs.

When the CPU calls the Diagnostic error interrupt OB, the input parameter LADDR will contain the hardware identifier for the module with the error. You can find the hardware identifier for the SM 1231 module in the STEP 7 device configuration for the SM 1231 module.

Calling the RALRM instruction

To program the RALRM instruction call, follow these steps:

1. Add a call to RALRM in your STEP 7 program.
2. Set the F_ID input parameter to the hardware identifier in the LADDR parameter of the Diagnostic error interrupt OB.
3. Use an array of bytes for the TINFO and AINFO input parameters. Use an array size of 34 bytes or greater.



Interpreting AINFO after a diagnostic interrupt has occurred

The AINFO byte array will contain the information about the module diagnostics after the Diagnostic error interrupt OB executes.

Bytes 0 - 25 are header information. The bytes pertaining to the module diagnostic are as follows:

Byte	Description	
26 and 27	Word value 16#8000 - indicates the diagnostic is a PROFINET style diagnostic	
28 and 29	Word containing channel number responsible for this diagnostic	
30	Bit pattern aaabb000 that indicates the type of channel (aaa) and type of error (bb)	
	aaa	bb
	000: reserved	00: reserved
	001: input channel	01: incoming error
	010: output channel	10: outgoing error

Byte	Description	
30	011: input/output channel	11: outgoing error, other errors present
31	Indication of data format 0: Free data format 1: Bit 2: Two bits 3: Four bits 4: Byte 5: Word (two bytes) 6: Double word (four bytes) 7: Two double words (eight bytes)	
32 and 33	Word that defines the type of error: 16#0000: reserved 16#0001: short circuit 16#0002: undervoltage 16#0003: overvoltage 16#0004: overload 16#0005: over temperature 16#0006: wire break 16#0007: high limit exceeded 16#0008: low limit exceeded 16#0009: error	

For example, consider bytes 26 - 33 of this AINFO structure:

29		my_ainfo[26]	Byte	16#0	16#80
30		my_ainfo[27]	Byte	16#0	16#00
31		my_ainfo[28]	Byte	16#0	16#00
32		my_ainfo[29]	Byte	16#0	16#00
33		my_ainfo[30]	Byte	16#0	16#28
34		my_ainfo[31]	Byte	16#0	16#05
35		my_ainfo[32]	Byte	16#0	16#00
36		my_ainfo[33]	Byte	16#0	16#07

- The Word at bytes 26 and 27 is 16#8000, which indicates that this is a PROFINET style diagnostic.
- The Word at bytes 28 and 29 indicates this is a diagnostic for channel 0 or the module.
- Byte 30 is 16#28, which when interpreted as the bit pattern aaa bb 00 is 001 01 000. This value indicates that this diagnostic is for an input channel and is an incoming error.
- Byte 31 is 5, which indicates a Word value
- The word value at bytes 32 and 33 is 16#0007, which indicates high limit exceeded.

By capturing the AINFO information from a Diagnostic error interrupt event, you can thus determine the nature of the diagnostic event.

Technical specifications

A

A.1 General technical specifications

Standards compliance

The S7-1200 G2 automation system design conforms with the following standards and test specifications. The test criteria for the S7-1200 G2 automation system are based on these standards and test specifications.

NOTE

Some S7-1200 G2 devices are not certified to all the following standards, and certification status can change without notice. Most certification approval markings are listed on the device or packaging. You are responsible for determining whether the devices in your system meet the required certifications for your application. For additional information on the certifications of a specific device, consult with a local Siemens representative or visit the Siemens Industry Online Support Web site (https://support.industry.siemens.com/). Device certificates can be downloaded from the Siemens Industry Online Support Web site.

CE approval

The S7-1200 G2 automation system satisfies requirements and safety related objectives according to the EC directives listed below, and conforms to the harmonized European standards (EN) for the programmable controllers listed in the Official Journals of the European Community.

- 2014/30/EU "Electromagnetic Compatibility" (EMC Directive)
- 2014/53/EU "Radio Equipment" (RED Directive)
- 2014/34/EU "Equipment and protective systems intended for use in potentially explosive atmospheres" (ATEX Directive)
- 2011/65/EU "Restriction of the use of certain hazardous substances in electrical and electronic equipment" (RoHS Directive)
- 2006/42/EC "Machinery Directive" for S7-1200 G2 F-CPU, F-SM, and F-SB modules

EU declarations of conformity for the respective authorities are available from:

Siemens AG
Digital Industries
Factory Automation
P.O. Box 1963
D-92209 Amberg

The EU declarations of conformity are also available for download from the Siemens Industry Online Support Web site (https://support.industry.siemens.com/), under the keyword "Declaration of Conformity".

Radio Equipment Directive (RED) compliance

The S7-1200 G2 automation system complies with the Radio Equipment Directive (RED) 2014/53/EU. The RED defines NFC tags as radio equipment. The frequency 13.56 MHz is regulated under ETSI EN 300 330 v2.1.1.

UK Conformity Assessed marking

The S7-1200 G2 automation system complies with the designated British standards (BS) for programmable controllers published in the official consolidated list of the British Government. The S7-1200 G2 automation system meets the requirements and protection targets of the following regulations and related amendments:

- Electromagnetic Compatibility Regulations 2016 (EMC)
- Radio Equipment Regulations 2017
- Equipment and Protective Systems Intended for use in Potentially Explosive Atmospheres Regulations 2016 (ATEX)
- Regulations on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2012 (RoHS)
- Supply of Machinery (Safety) Regulations 2008 for S7-1200 G2 F-CPU, F-SM, and F-SB modules

UK Declarations of Conformity for the respective authorities are available from:

Siemens AG
Digital Industries
Factory Automation
P.O. Box 1963
D-92209 Amberg

The UK Declaration of Conformity is also available for download from the Siemens Industry Online Support Web site (https://support.industry.siemens.com/) under the keyword "Declaration of Conformity".

cULus approval

Underwriters Laboratories Inc. complying with:

- Underwriters Laboratories, Inc.: UL 61010-1, Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use; Part 1: General Requirements and UL 61010-2-201, Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use - Part 2-201: Particular Requirements for Control Equipment.
- Canadian Standards Association: CAN/CSA-C22.2 No. 61010-1-12, Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use - Part 1: General Requirements and CSA C22.2 No. 61010-2-201, Safety Requirements for Electrical Equipment for Measurement, Control, and Laboratory Use - Part 2-201: Particular Requirements for Control Equipment.

NOTE

The SIMATIC S7-1200 G2 series meets the CSA standard.
The cULus logo indicates that the S7-1200 G2 has been examined and certified by Underwriters Laboratories (UL) to the standards referenced above.

cULus HAZ. LOC. approval

Underwriters Laboratories Inc. in accordance with:

- ANSI/ISA 12.12.01
- CAN/CSA C22.2 No. 213 (Hazardous Location) APPROVED for use in Class I, Division 2, Group A, B, C, D T4C; Class I, Zone 2, Group IIC T4 Installation Instructions for cULus haz.loc.
- WARNING – Explosion Hazard – Do not disconnect while circuit is live unless area is known to be non-hazardous.
- WARNING – Explosion Hazard – Substitution of components can impair suitability for Class I, Division 2 or Zone 2.
- This equipment is suitable for use in Class I, Division 2, Groups A, B, C, D; Class I, Zone 2, Group IIC; or non-hazardous locations.

IMPORTANT EXCEPTION: Some models are de-rated for Ta = 60 °C. See the Technical Specifications of each device for derating information.

ATEX approval

According to EN 60079-7 (Electrical apparatus for potentially explosive atmospheres – Part 7: Increased safety “e”), EN IEC 60079-0 (Electrical apparatus for potentially explosive gas atmospheres – Part 0: General requirements), and IEC 60079-15 (Electrical apparatus for potentially explosive atmospheres - Part 15: Equipment protection by type of protection "n").

II 3 G Ex ec IIC T4 Gc (some models are II 3 G Ex ec nC IIC T4 Gc, see product marking) (Page 239)

UL 24 ATEX 3237X

Special conditions of use:

- The equipment shall only be used in an area of not more than pollution degree 2, as defined in EN 60664-1.
- The equipment shall be installed in an enclosure that provides a degree of protection not less than IP54 in accordance with EN 60079-7.
- Transient protection shall be provided that is set at a level not exceeding 140% of the peak rated voltage value at the supply terminals to the equipment.

IECEx approval

According to IEC 60079-7 (Explosive atmospheres – Part 7: Equipment protection by increased safety “e”), IEC 60079-0 (Explosive atmospheres – Part 0: Equipment – General requirements), and IEC 60079-15 (Electrical apparatus for potentially explosive atmospheres - Part 15: Equipment protection by type of protection "n").

II 3 G Ex ec IIC T4 Gc (some models are II 3 G Ex ec nC IIC T4 Gc, see product marking) (Page 239)

IECEx UL 24.0044X

Specific conditions of use:

- The equipment shall only be used in an area of not more than pollution degree 2, as defined in IEC 60664-1.
- The equipment shall be installed in an enclosure that provides a degree of protection not less than IP54 in accordance with EN IEC 60079-0.
- Transient protection shall be provided that is set at a level not exceeding 140% of the peak rated voltage value at the supply terminals to the equipment.

UKEX approval

According to EN 60079-7 (Explosive atmospheres – Part 7: Equipment protection by increased safety “e”), EN IEC 60079-0 (Explosive atmospheres – Part 0: Equipment – General requirements), and IEC 60079-15 (Electrical apparatus for potentially explosive atmospheres - Part 15: Equipment protection by type of protection "n").

II 3 G Ex ec IIC T4 Gc (some models are II 3 G Ex ec nC IIC T4 Gc, see product marking) (Page 239)

UL 24UKEX2991X

Specific conditions of use:

- The equipment shall only be used in an area of not more than pollution degree 2, as defined in EN 60664-1.
- The equipment shall be installed in an enclosure that provides a degree of protection not less than IP54 in accordance with EN 60079-7.
- Transient protection shall be provided that is set at a level not exceeding 140% of the peak rated voltage value at the supply terminals to the equipment.

CCCEx approval

According to GB/T 3836.1 (Explosive atmospheres – Part 1: Equipment – General requirements),GB/T 3836.3 (Explosive atmospheres – Part 3: Equipment protection by increased safety “e”), and GB/T 3836.8 (Explosive atmospheres – Part 8: Equipment protection by type of protection "n" see product marking) (Page 239)

Specific conditions of safety use:

- The equipment shall only be used in an area of at least pollution degree 2, as defined in GB/T 16935.1.
- The equipment shall be installed in an enclosure that provides a degree of protection not less than IP54 in accordance with GB/T 3836.3.
- Transient protection shall be provided that is set at a level not exceeding 140% of the peak value at the supply terminals to the equipment.

Australia and New Zealand - RCM Mark (Regulatory Compliance Mark)

The S7-1200 G2 automation system satisfies the requirements of AS/NZS 2064 standards (Class A).

Eurasian Customs Union approval

EAC (Eurasian Conformity): Declaration of Conformity according to Technical Regulation of Customs Union (TR CU)

Industrial environments

The S7-1200 G2 automation system is designed for use in industrial environments.

Table A-1 Industrial environments

Application field	Emission requirements	Immunity requirements
Industrial	EN 61000-6-4	EN 61000-6-2

Environmental conditions

The S7-1200 G2 automation system is suitable for use in weather-proof, fixed locations. The operating conditions are based on requirements of IEC 61131-2:2017.

Table A-2 Shipping and storage

Environmental conditions – Shipping and storage conditions (TTH4 and STH4)	
EN 60068-2-1, Test Ab, Cold EN 60068-2-2, Test Dc, Dry heat	-40 °C to 70 °C
EN 60068-2-30, Test Db, Damp heat	25 °C to 55 °C, 95% RH
EN 60068-2-14, Test Na, Temperature shock	-40 °C to 70 °C, dwell time 3 hours, 2 cycles
EN 60068-2-31, Free fall	0.3 m, 5 times, product packaging
Atmospheric pressure	1140 to 540 hPa (corresponding to an altitude of -1000 to 5000 m)

Table A-3 Climatic ambient conditions

Environmental conditions – Climatic ambient operating conditions (OTH4)	
Ambient temperature (Inlet Air 25 mm below unit)	-20 °C to 40 °C Max. specifications -20 °C to 60 °C With derating For vertical mounting see individual device specifications. Minimum temperature for Fail-safe SMs/SBs is 0 °C.
	95% non-condensing humidity
Atmospheric pressure	1140 to 540 hPa (corresponding to an altitude from -1000 to 5000 m) For altitudes above 2000 m, the maximum permissible ambient temperature must be derated: >2000 m 0.9 factor, >3000 m 0.8 factor, >4000 m 0.7 factor. 5000 m is max allowed altitude.
Effects on the availability of modules at altitude	The higher cosmic radiation present during operation at altitudes above 2000 m affect the failure rate of electronic components. This is what is called a soft-error rate. In rare cases, this can result in a transition of modules to the safe state, especially for fail-safe modules. However, the functional safety of the modules is fully retained.
Concentration of contaminants	SO_2: < 0.5 ppm; H_2S: < 0.1 ppm; RH < 60% non-condensing
EN 60068-2-14, Test Nb (Temperature change)	-20 °C to 60 °C, dwell time 3 hours, 5 cycles
EN 60068-2-78, Test Cab (Damp heat)	30 °C, 95% RH, 16 hours
EN 60068-2-27 (Shock)	15 g, 11 ms pulse, 6 shocks in each of 3 axes (when panel mounted)
EN 60068-2-6 (Sinusoidal vibration)	3.5 mm from 5 to 8.4 Hz, 1g from 8.4 to 150 Hz 10 sweeps each axis, 1 octave per minute (when panel or DIN rail mounted) Note: In high vibration applications, Siemens recommends panel mounting or the use of a Siemens DIN Rail with DIN Rail End Retainers to secure devices.

Electromagnetic compatibility

Electromagnetic Compatibility (EMC) is the ability of an electrical device to operate as intended in an electromagnetic environment and to operate without emitting levels of electromagnetic interference (EMI) that can disturb other electrical devices in the vicinity.

Table A-4 Immunity

Electromagnetic compatibility - Immunity per EN 61000-6-2	
EN 61000-4-2 Electrostatic discharge	8 kV air discharge to all surfaces 6 kV contact discharge to exposed conductive surfaces
EN 61000-4-3 Radiated, radio-frequency, electro-magnetic field immunity test	80 MHz to 1000 MHz, 10 V/m, 80% AM (1 kHz) 1.4 GHz to 6 GHz, 3 V/m, 80% AM (1 kHz)
EN 61000-4-4 Fast transient bursts	2 kV, 5 kHz with coupling network to AC and DC system power 2 kV, 5 kHz with coupling clamp to I/O
EN 61000-4-5 Surge immunity	AC systems - 2 kV common mode, 1 kV differential mode DC systems - 1 kV common mode, 0.5 kV differential mode
EN 61000-4-6 Conducted disturbances	150 kHz to 80 MHz, 10 V RMS, 80% AM at 1 kHz
EN 61000-4-11 Voltage dips	AC systems 0% for 1 cycle, 40% for 12 cycles, and 70% for 30 cycles at 60 Hz

Table A-5 Emissions

Electromagnetic compatibility - Conducted and radiated emissions per EN 61000-6-4		
Conducted emissions AC power ports	0.15 MHz to 0.5 MHz	< 79 dBµV quasi-peak, < 66 dBµV average
	0.5 MHz to 30 MHz	< 73 dBµV quasi-peak, < 60 dBµV average
Conducted emissions DC power ports	0.15 MHz to 0.5 MHz	< 89 dBµV quasi-peak, < 76 dBµV average
	0.5 MHz to 30 MHz	< 83 dBµV quasi-peak, < 70 dBµV average
Radiated emissions	30 MHz to 230 MHz	< 40 dBµV/m quasi-peak at 10 m
	230 MHz to 1000 MHz	< 47 dBµV/m quasi-peak at 10 m
	1000 MHz to 3000 MHz	< 76 dBµV/m peak, < 56 dBµV/m average at 3 m
	3000 MHz to 6000 MHz	< 80 dBµV/m peak, < 60 dBµV/m average at 3 m

Insulation

The insulation is designed in accordance with the requirements of IEC 61010-2-201.

NOTE

For modules having 24 V DC (SELV / PELV) supply voltage, galvanic isolations are tested with 707 V DC (type test)

Pollution degree / overvoltage category in accordance with IEC 61131-2 and IEC 61000-2-201

- Pollution degree 2
- Overvoltage category II

Protection class according to IEC 61131-2 and IEC 61010-2-201

- Protection class II

Degree of protection

- IP20 Mechanical Protection, EN 60529
- Protects against finger contact with high voltage as tested by standard probe. External protection required for dust, dirt, water and foreign objects of < 12.5 mm in diameter.

Rated voltages

The rated voltages are:

- 24 V DC
- 120/240 V AC

⚠ WARNING

Risks when turning on output power

When a mechanical contact turns on output power to the S7-1200 G2 CPU, or any digital expansion module, it sends a “1” signal to the digital outputs for approximately 50 microseconds.

This could cause unexpected machine or process operation, which could result in death or serious injury to personnel and/or damage to equipment.

You must plan for the "1" signal to the digital outputs.

Reverse voltage protection

Reverse voltage protection circuitry is provided on each terminal pair of +24 V DC power or user input power for CPUs, signal modules (SMs), and signal boards (SBs). It is still possible to damage the system by wiring different terminal pairs in opposite polarities.

Some of the 24 V DC power input ports in the S7-1200 G2 system are interconnected, with a common logic circuit connecting multiple M terminals. For example, the following circuits are interconnected when designated as “not isolated”: the 24 V DC power supply of the CPU, the sensor power of the CPU, the power input for the relay coil of an SM, and the power supply for a non-isolated analog input. All non-isolated M terminals must connect to the same external reference potential.

⚠ WARNING

Risks when connecting non-isolated M terminals to different reference potentials.

Connecting non-isolated M terminals to different reference potentials causes unintended current flows that can cause damage or unpredictable operation in the PLC and any connected equipment.

Always ensure that all non-isolated M terminals in an S7-1200 G2 system are connected to the same reference potential.

Failure to comply with these guidelines could cause damage or unpredictable operation, which can result in death or severe personal injury and/or property damage.

DC Outputs

Short-circuit protection circuitry is not provided for DC outputs on CPUs, signal modules (SMs), and signal boards (SBs).

Relay electrical service life

The typical performance data estimated from sample tests is shown below. Actual performance can vary depending upon your specific application. An external protection circuit that is adapted to the load enhances the service life of the contacts. Normally closed contacts have a typical service life of about one-third that of normally open contacts under inductive and lamp load conditions.

Table A-6 Typical performance data

Data for selecting an actuator			
Continuous thermal current	2 A max.		
Switching capacity and life of the contacts			
For ohmic load	Voltage	Current	Number of operating cycles (typical)
	24 V DC	2.0 A	0.1 million
	24 V DC	1.0 A	0.2 million
	24 V DC	0.5 A	1.0 million
	48 V AC	1.5 A	1.5 million
	60 V AC	1.5 A	1.5 million
	120 V AC	2.0 A	1.0 million
	120 V AC	1.0 A	1.5 million
	120 V AC	0.5 A	2.0 million
	230 V AC	2.0 A	1.0 million
	230 V AC	1.0 A	1.5 million
	230 V AC	0.5 A	2.0 million
For inductive load (according to IEC 947-5-1 DC13/AC15)	Voltage	Current	Number of operating cycles (typical)
	24 V DC	2.0 A	0.05 million
	24 V DC	1.0 A	0.1 million

Data for selecting an actuator			
For inductive load (according to IEC 947-5-1 DC13/AC15)	24 V DC	0.5 A	0.5 million
	24 V AC	1.5 A	1.0 million
	48 V AC	1.5 A	1.0 million
	60 V AC	1.5 A	1.0 million
	120 V AC	2.0 A	0.7 million
	120 V AC	1.0 A	1.0 million
	120 V AC	0.5 A	1.5 million
	230 V AC	2.0 A	0.7 million
	230 V AC	1.0 A	1.0 million
	230 V AC	0.5 A	1.5 million
Activating a digital input	Possible		
Switching frequency			
Mechanical	Max. 10 Hz		
At ohmic load	Max. 1 Hz		
At inductive load (according to IEC 947-5-1 DC13/AC15)	Max. 0.5 Hz		
At lamp load	Max. 1Hz		

Internal CPU memory retention

The CPU performs operations to extend the life of the internal memory devices that contain the application data. Below is the life expectancy of the internal memory.

- Lifetime of retentive data and data log data: 10 years
- Power down retentive data, write cycle endurance: 2 million cycles
- Data log data, write cycle endurance: 500 million data log entries

NOTE

Effect of data logs on internal CPU memory

Each data log write consumes at a minimum 2 KB of memory. If your program writes small amounts of data frequently, it is consuming at least 2 KB of memory on each write. A better implementation would be to accumulate the small data items in a data block (DB), and to write the data block to the data log at less frequent intervals.

If your program writes many data log entries at a high frequency, consider using a replaceable SD memory card.

Use of cellular phones

You can read information from the CPU and write operations to the CPU from the Near Field Communication (NFC) (Page 188) tag by placing your iPhone near the NFC symbol on the S7-1200 G2 CPU.

All S7-1200 G2 CPUs and modules have a scannable QR code lasered on the housing. Use your smartphone's camera to read the QR code. The QR code provides a direct link to the Siemens Industrial Online Support information for your device.

⚠ WARNING

Risks when using a cellular phone in close proximity to the S7-1200 G2 CPU

Using a cellular phone in close proximity to an S7-1200 G2 system with cellular and Wi-Fi communications active can cause unpredictable behavior.

To reduce any influence of a cellular phone on the S7-1200 G2 system, and to ensure proper operation of your CPU, place the phone in "Airplane mode" to disable cellular and Wi-Fi before bringing the phone into proximity (<10 cm) of the CPU.

Failure to comply with these guidelines can cause damage or unpredictable operation which could result in severe personal injury, property damage, and/or death.

⚠ WARNING

Risks when operating a cellular phone in a hazardous or explosive environment

Do not use a cellular phone in a hazardous or explosive environment unless the phone has been approved for use in such environments.

Failure to comply with these guidelines can cause damage or unpredictable operation which could result in severe personal injury, property damage, and/or death.

A.2 Protection methods

The S7-1200 G2 automation system is covered by two protection methods:

Article numbers covered by II 3 G Ex ec IIC T4 Gc / Ex ec IIC T4 Gc	Article numbers covered by II 3 Ex ec nC IIC T4 Gc / Ex ec nC IIC T4 Gc
6ES7212-1AG50-0XB0	6ES7212-1HG50-0XB0
6ES7214-1AH50-0XB0	6ES7212-1BG50-0XB0
6ES7212-1AF50-0XB0	6ES7214-1HH50-0XB0
6ES7214-1AF50-0XB0	6ES7214-1BH50-0XB0
6ES7221-1BH50-0XB0	6ES7212-1HF50-0XB0
6ES7222-5BH50-0XB0	6ES7214-1HF50-0XB0
6ES7223-5BH50-0XB0	6ES7222-5HH50-0XB0
6ES7232-4HF50-0XB0	6ES7223-5PH50-0XB0
6ES7221-3BF50-0XB0	6ES7231-4HF50-0XB0
6ES7222-5BF50-0XB0	6ES7233-4HF50-0XB0
6ES7223-7BF50-0XB0	6ES7231-4HD50-0XB0
6ES7223-7AF50-0XB0	6ES7233-4HD50-0XB0
6ES7232-4HD50-0XB0	

A.3 CPU 1212C

A.3.1 General specifications and features

Table A-7 General

Technical data	**CPU 1212C AC/DC/Relay**	**CPU 1212C DC/DC/Relay**	**CPU 1212C DC/DC/DC**
Article number	6ES7212-1BG50-0XB0	6ES7212-1HG50-0XB0	6ES7212-1AG50-0XB0
Dimensions W x H x D	70 x 125 x 100 mm		
Weight (product/shipping)	373 grams / 420 grams	333 grams / 380 grams	319 grams / 366 grams
Power dissipation	4.0 W	3.0 W	
Current available for expansion devices	1000 mA max. (5 V DC)		
Current available on sensor supply	300 mA (24 V DC sensor power, current limited)		
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]		
	Vertical mounting -20 °C to 50 °C[2]		Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum		

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-8 CPU features

Technical data	**Description**	
User memory	Work Memory	150 Kbytes (Program) 500 Kbytes (Data)
	Load Memory	8 Mbytes (Internal) 32 Gbytes (using SD card)
	Retentive Memory	20 Kbytes
Onboard digital I/O	8 inputs / 6 outputs	
Process image size	1024 bytes of inputs (I) / 1024 bytes of outputs (Q)	
Bit memory size	8192 bytes (M)	
Temporary (local) memory	Per priority class, max.	64 Kbytes
	Per block, max.	16 Kbytes
Communication module expansion	3 max. (must connect to the right of the CPU or to the right of another CM)	
Signal module expansion (SM plus CM)	6 max.	
Signal board or Communication board expansion	1 max.	
High-speed counters	Max. number of high-speed counters	8 (any CPU or SB digital input)
	Max. rate, CPU inputs Ia.0 to Ia.5	100 kHz (80 kHz in quadrature mode)

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

Technical data	Description	
High-speed counters	Max. rate, CPU inputs Ia.6 to Ia.7	30 kHz (20 kHz in quadrature mode)
	Max. rate, SB inputs	See SB specifications
Pulse outputs[1]	Max. number of pulse outputs	8 (any CPU or SB digital output)
	Max. rate, CPU outputs Qa.0 to Qa.3	100 kHz
	Max. rate, CPU outputs Qa.4 to Qa.5	20 kHz
	Max. rate, SB outputs	See SB specifications
Pulse catch inputs	Yes, each onboard CPU digital input and SB digital input	
Time delay interrupts	20 total with 1 ms resolution	
Cyclic interrupts	20 total with 1 us resolution	
Edge interrupts	Rising and falling for each onboard CPU digital input and SB digital input	
Memory card (Page 333)	SIMATIC memory card (optional).	
Motion control	Available Resources	800
	Required Resources	40 per speed-controlled axis
		80 per positioning axis
		160 per synchronous axis
		80 per external encoder
		20 per output cam
		160 per cam track
		40 per measuring input
	Available Extended Resources	40
	Required Extended Resources	2 per cam (1000 points)
		30 for each set of kinematics
PID	PID Compact	Yes, universal PID controller with integrated optimization
	PID 3Step	Yes, PID controller with integrated optimization for valves
	PID Temp	Yes, PID controller with integrated optimization for temperature
Real time clock	Accuracy	+/- 60 seconds per month
	Retention time, super capacitor	20 days typical at 40 °C, 12 days minimum at 40 °C

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

A.3.2 Performance

Table A-9 Performance

Type of instruction[1]	Direct addressing (I, Q, and M)	DB accesses
Boolean	0.037 µs/instruction	
Move_Bool	0.067 µs/instruction	0.066 µs/instruction
Move_Word	0.027 µs/instruction	0.030 µs/instruction
Move_Real	0.027 µs/instruction	0.030 µs/instruction
Add_Real	0.119 µs/instruction	0.074 µs/instruction

[1] Many variables affect measured times. The above performance times are for the fastest instructions in each category and error-free programs.

A.3.3 Blocks, timers, and counters

Table A-10 Blocks, times, and counters

Element	Description	
Blocks	Type	OB, FB, FC, DB
	Max. number of elements	4000; Blocks (OB, FB, FC, DB) and UDTs
	Max. OB, FB, FC size	64 Kbytes
	Max. DB size (Optimized)	500 Kbytes Work Memory 16 Mbytes Load Memory
	Max. DB size (Non-optimized)	64 Kbytes (DBs with absolute addressing)
	Address range for FBs and FCs	1 to 65535
	Address range for DBs	1 to 59999
	Nesting depth per priority class[1]	24 (OB plus 23 more levels)
	Monitoring	Status of 8 code blocks can be monitored simultaneously.
Number of OBs per event class	Program cycle	100
	Startup	100
	Time delay interrupt	20 (one per event)
	Cyclic interrupt	20 (one per event)
	Hardware interrupt	50
	Time error interrupt	1
	Diagnostic error interrupt	1
	Pull or plug of modules	1
	Rack or station failure	1
	Time of day	20 (one per event)
	Synchronous Cycle	1
	Status	1
	Update	1
	Profile	1

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

Element	Description	
Number of OBs per event class	MC-Interpolator	1
	MC-Servo	1
	MC-PreServo	1
	MC-PostServo	1
	MC-LookAhead	1
	MC-PreInterpolator	1
	Programming error	1
	I/O access error	1
Timers	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon time type
	IEC_TIMER	16 bytes
	IEC_LTIMER	28 bytes
Counters	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon count type
	IEC_SCOUNTER, IEC_USCOUNTER	3 bytes
	IEC_COUNTER, IEC_UCOUNTER	6 bytes
	IEC_DCOUNTER, IEC_UDCOUNTER	12 bytes
	IEC_LCOUNTER, IEC_ULCOUNTER	24 bytes
Runtime Meters	Quantity	16

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

A.3.4 Communications

Table A-11 Communications

Technical data	Description
Number of ports	2 with an integrated switch
Type	Ethernet (RJ-45 connector)
Connections	88 connections max. (integrated into CPU) 10 reserved for ES/HMI/web
Data rates	100 Mb/s
Isolation (external signal to logic)	Transformer isolated, 1500 V AC (type test)[1]
Cable type	CAT5e shielded
Interfaces	1 PROFINET
	0 PROFIBUS

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
PROFINET Protocols	PROFINET IO controller	Yes
	PROFINET IO device	Yes
	SIMATIC communication	Yes
	Open IE communication	Yes
	Web server	Yes
	Media redundancy	Yes
PROFINET IO controller services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	Yes
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes
	MRPD	Yes – Requires an IRT sync domain
	PROFIenergy	Yes (per user program)
	Prioritized startup	Yes (max. 16 PROFINET devices)
	Number of connectable I/O devices, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of submodules, max.	512
	Number of IO devices that you can connect for RT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of in line IO devices that you can connect for RT, max.	31
	Number of IO devices that you can connect for IRT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of IO devices that can be activ-ated/deactivated simultaneously, max.	8
	The minimum update time depends on the communication component set for PROFINET IO, on the number of IO devices, and the quantity of configured user data.	RT Send clock: 1 ms to 512 ms IRT Send clock: 1 ms to 512 ms (1 ms resolution)
PROFINET I-Device	Number of connections, max.	2
PROFINET I-Device services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	No
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes
	PROFIenergy	Yes (per user program)
	Shared device	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
PROFINET I-Device services	Number of IO controllers with shared device, max.	2
SIMATIC communication	S7 communication as server	Yes
	S7 communication as client	Yes
	User data per job, max.	See TIA Portal information system (S7 communication, user data size)
Open IE communication	TCP/IP	Yes, 8 Kbytes max. data length Several passive connections per port
	ISO-on-TCP (RFC1006)	Yes, 8 Kbytes max. data length
	UDP	Yes, 2048 bytes max. data length 1472 bytes max. for UDP broadcast
	DHCP	Yes
	SNMP	Yes
	DCP	Yes
	LLDP	Yes
Near Field Communication (NFC)	Yes, with the S7-1200 G2 NFC app	
S7 message functions	Number of login stations for message functions, max.	32
	Program alarms	Yes
	Number of configurable program messages, max.	5000
	Number of loadable program messages in RUN, max.	2500
	Number of simultaneously active program alarms	600 program alarms 100 alarms for system diagnostics 160 for motion technology objects
Test commissioning functions	Joint commission (Team Engineering)	Yes, parallel online access possible for up to 5 engineering systems
	Program status	Yes, up to 8 blocks simultaneously (in total across all ES clients)
	Single step	No
	Breakpoints	No
	SIMATIC Controller Profiling	Yes
Monitor/modify	Variables	Inputs/outputs, memory bits, DBs, distributed I/Os, timers, counters
	Number of monitor variables, max.	200 per job
	Number of modify variables, max.	200 per job
Force	Variables	Peripheral inputs/outputs
	Number of variables, max.	200
Trace	Number of configurable traces	4
	Variables captured per trace, max.	16

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
Trace	Data captured per trace, max.	512 KB
Diagnostics buffer	Number of entries, max.	500
	Retentive	100

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

A.3.5 Power supply and sensor power

Table A-12 Power supply

Technical data	CPU 1212C AC/DC/Relay	CPU 1212C DC/DC/Relay	CPU 1212C DC/DC/DC
Rated voltage	120/240 V AC	24 V DC	
Voltage range	85 to 264 V AC	20.4 to 28.8 V DC	
Reverse voltage protection	--	Yes	
Line frequency	47 to 63 Hz	--	
Input current (CPU only)	70 mA at 120 V AC 38 mA at 240 V AC	185 mA at 24 V DC	125 mA at 24 V DC
Input current (with all accessories)	330 mA at 120 V AC 200 mA at 240 V AC	765 mA at 24 V DC	700 mA at 24 V DC
Inrush current	20 A max. at 264 V AC	12 A max. at 28.8 V DC	
I^2t	0.8 A^2 s	0.5 A^2 s	
Isolation (input power to logic)	1500 V AC	Not isolated	
Ground leakage (AC line to functional earth)	0.5 mA max.	--	
Hold up time (loss of power)	20 ms at 120 V AC 80 ms at 240 V AC	10 ms at 24 V DC	
Internal fuse	3 A, 250 V, slow blow not user replaceable		

Table A-13 Sensor power

Technical data	CPU 1212C AC/DC/Relay	CPU 1212C DC/DC/Relay	CPU 1212C DC/DC/DC
Rated voltage	24 V DC		
Voltage range	20.4 to 28.8 V DC	L+ minus 4 V DC min.	
Output current rating	300 mA max. (short-circuit protected)		
Ripple noise (<10 MHz)	< 1 V peak to peak max.	Same as input line	
Isolation (CPU logic to sensor power)	Not isolated		
Cable length	500 m shielded		
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)		

A.3.6 Digital inputs and outputs

Table A-14 Digital inputs

Technical data	CPU 1212C AC/DC/Relay	CPU 1212C DC/DC/Relay	CPU 1212C DC/DC/DC
Number of inputs	8		
Assignment	Ia.0 to Ia.5 (high-speed) Ia.6 to Ia.7 (standard)		
Type	Sink/Source (IEC Type 1 sink)		
Rated voltage	24 V DC at 6 mA, nominal (high-speed) 24 V DC at 4 mA, nominal (standard)		
Continuous permissible voltage	30 V DC, max. at 8 mA, max. (high-speed) 30 V DC, max. at 6 mA, max. (standard)		
Logic 1 signal	15 V DC min. at 2.5 mA		
Logic 0 signal	5 V DC max. or 0.5 mA		
Isolation (field side to logic)	707 V DC (type test)		
Isolation groups	1		
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0		
HSC clock input rates (Logic 1 level = 15 to 26 V DC)	Single phase: 100 kHz (Ia.0 to Ia.5) Single phase: 30 kHz (Ia.6 to Ia.7) Quadrature phase: 80 kHz (Ia.0 to Ia.5) Quadrature phase: 20 kHz (Ia.6 to Ia.7)		
Cable length	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs		
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)		

Table A-15 Digital outputs

Technical data	CPU 1212C AC/DC/Relay	CPU 1212C DC/DC/Relay	CPU 1212C DC/DC/DC
Number of outputs	6		
Assignment	Qa.0 to Qa.5		Qa.0 to Qa.3 (high-speed) Qa.4 to Qa.5 (standard)
Type	Relay, dry contact		Solid state – MOSFET (sourcing)
Rated voltage	--		24 V DC
Voltage range	5 to 30 V DC or 5 to 250 V AC		20.4 to 28.8 V DC
Logic 1 signal at max. current	--		20 V DC min.
Logic 0 signal with 10 kΩ load	--		0.1 V DC max.
Current	2.0 A max.		0.5 A max.
Minimum load[1]	125 mW DC / 500 mW AC		--
Lamp load	30 W DC / 200 W AC		5 W

[1] When using relays at minimum load, avoid ambient temperatures below 0 °C.

[2] For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

[3] Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

Technical data	**CPU 1212C AC/DC/Relay**	**CPU 1212C DC/DC/Relay**	**CPU 1212C DC/DC/DC**
ON state resistance	0.2 Ω max. when new		0.6 Ω max.
Leakage current per point	--		10 µA max.
Overload protection	No		
Isolation (field side to logic)	4200 V DC for 5 seconds + 1600 V DC for 1 minute (type test)		500 V AC for 1 minute (type test)
Isolation (coil to logic)	None		--
Isolation resistance	100 MΩ min. when new		--
Isolation between open contacts	750 V AC for 1 minute		--
Isolation groups	1		1
Current per common	12 A max. (10 A max. per pin)		3 A max.
Inductive clamp voltage	--		L+ minus 40 V, 1 W dissipation
Switching delay (Qa.0 to Qa.3)	10 ms max.		1.0 µs max., OFF to ON 3.0 µs max., ON to OFF
Switching delay (Qa.4 to Qa.5)	10 ms max.		50 µs max., OFF to ON 200 µs max., ON to OFF
Maximum relay switching frequency	1 Hz		--
Pulse Train Output (PTO) rate	Not recommended[2]		100 kHz max. (Qa.0 to Qa.3) 20 kHz max. (Qa.4 to Qa.5) 2 Hz min.[3]
Lifetime mechanical (no load)	10000000 open/close cycles		--
Lifetime contacts at rated load	100000 open/close cycles		--
Behavior on RUN to STOP	Last value or substitute value (default value 0)		
Control of a digital input	Yes		
Parallel outputs for redundant load control	Yes (with same common)		
Parallel outputs for increased load	No		
Cable length	500 m shielded, 150 m unshielded		
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)		

[1] When using relays at minimum load, avoid ambient temperatures below 0 °C.

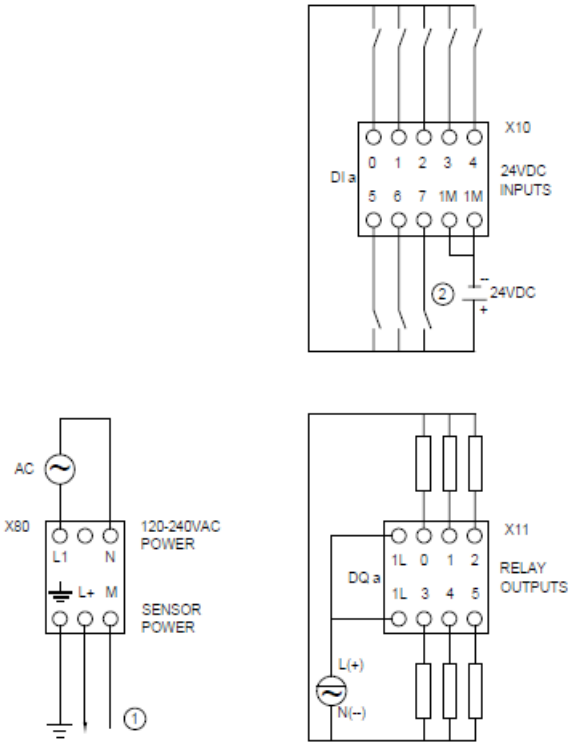
[2] For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

[3] Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

A.3.7 Wiring diagrams

The wiring diagrams and pin connector locations are shown below:

CPU 1212C AC/DC/Relay



X80: AC power wiring terminal (Orange, Type-A keying)						
AC power	L1		N			
Pin #	1	3	5			
Pin #	2	4	6			
Sensor power	GND	L+	M			
X10: DC input wiring terminal (Gray, No keying)						
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	
Pin #	1	3	5	7	9	
Pin #	2	4	6	8	10	
Signal	DI a.5	DI a.6	DI a.7	1M	1M	
X11: Relay output wiring terminal (Orange, Type-A keying)						
Signal	1L	DQ a.0	DQ a.1	DQ a.2		
Pin #	1	3	5	7		
Pin #	2	4	6	8		
Signal	1L	DQ a.3	DQ a.4	DQ a.5		

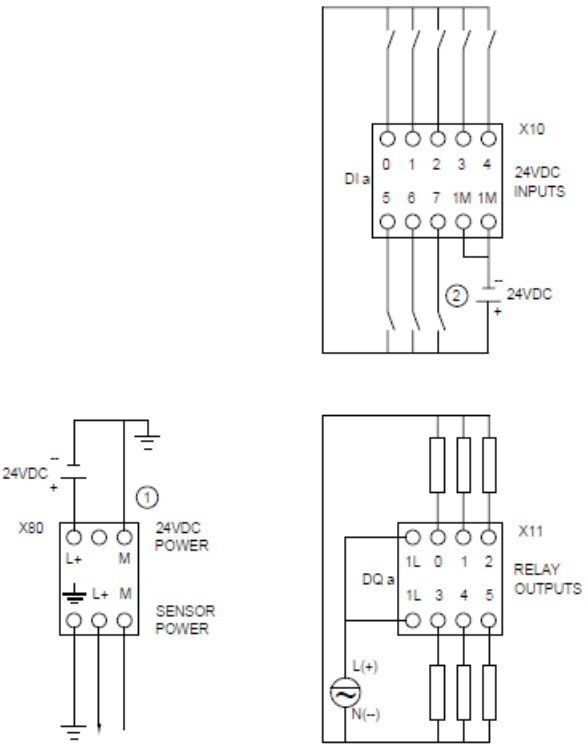
① For additional noise immunity, jumper the Sensor Power "M" to Chassis Ground on the connector.

② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

NOTE

You can connect either the L1 or N (L2) terminal to a voltage source up to 240 V AC. The N terminal can be considered L2 and is not required to be grounded. No polarization is required for L1 and N (L2) terminals.

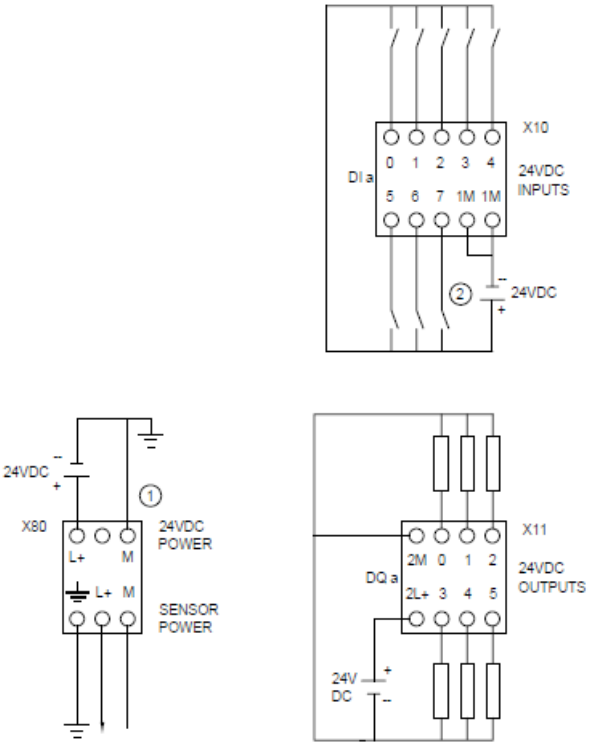
CPU 1212C DC/DC/Relay



X80: DC power wiring terminal (Gray, No keying)						
DC power	L+		M			
Pin #	1	3	5			
Pin #	2	4	6			
Sensor power	GND	L+	M			
X10: DC input wiring terminal (Gray, No keying)						
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	
Pin #	1	3	5	7	9	
Pin #	2	4	6	8	10	
Signal	DI a.5	DI a.6	DI a.7	1M	1M	
X11: Relay output wiring terminal (Orange, Type-A keying)						
Signal	1L	DQ a.0	DQ a.1	DQ a.2		
Pin #	1	3	5	7		
Pin #	2	4	6	8		
Signal	1L	DQ a.3	DQ a.4	DQ a.5		

① For additional noise immunity, jumper the 24 V DC Power “M” to Chassis Ground on the connector.
② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

CPU 1212C DC/DC/DC



X80: DC power wiring terminal (Gray, No keying)					
DC power	L+		M		
Pin #	1	3	5		
Pin #	2	4	6		
Sensor power	GND	L+	M		
X10: DC input wiring terminal (Gray, No keying)					
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4
Pin #	1	3	5	7	9
Pin #	2	4	6	8	10
Signal	DI a.5	DI a.6	DI a.7	1M	1M
X11: DC output wiring terminal (Gray, No keying)					
Signal	2M	DQ a.0	DQ a.1	DQ a.2	
Pin #	1	3	5	7	
Pin #	2	4	6	8	
Signal	2L+	DQ a.3	DQ a.4	DQ a.5	

① For additional noise immunity, jumper the 24 V DC Power "M" to Chassis Ground on the connector.
② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.4 CPU 1212FC

A.4.1 General specifications and features

Table A-16 General

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Article number	6ES7212-1HF50-0XB0	6ES7212-1AF50-0XB0
Dimensions W x H x D	70 x 125 x 100 mm	
Weight (product/shipping)	333 grams / 380 grams	319 grams / 366 grams
Power dissipation	3.0 W	
Current available for expansion devices	1000 mA max. (5 V DC)	
Current available on sensor supply	300 mA (24 V DC sensor power, current limited)	

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Safety class (highest)	PL e (performance level according to ISO 13849-1) SIL 3 (safety integrity level according to IEC 61508)	
Probability of failure	Low demand mode: PFDavg in accordance with SIL 3 < 2.00E-05 High demand/continuous mode: PFH in accordance with SIL 3 < 1.00E-09 (altitude -1000 m to 3000 m) < 2.00E-09 (altitude >3000 m to 5000 m) For service life of 20 years and repair time of 100 hours	
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]	
	Vertical mounting -20 °C to 50 °C[2]	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum	

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-17 CPU features

Technical data	**Description**	
User memory	Work Memory	200 Kbytes (Program) 500 Kbytes (Data)
	Load Memory	8 Mbytes (Internal) 32 Gbytes (using SD card)
	Retentive Memory	20 Kbytes
Onboard digital I/O	8 inputs / 6 outputs	
Process image size	1024 bytes of inputs (I) / 1024 bytes of outputs (Q)	
Bit memory size	8192 bytes (M)	
Temporary (local) memory	Per priority class, max.	64 Kbytes
	Per block, max.	16 Kbytes
Communication module expansion	3 max. (must connect to the right of the CPU or to the right of another CM)	
Signal module expansion (SM plus CM)	6 max.	
Signal board or Communication board expansion	1 max.	
High-speed counters	Max. number of high-speed counters	8 (any CPU or SB digital input)
	Max. rate, CPU inputs Ia.0 to Ia.5	100 kHz (80 kHz in quadrature mode)
	Max. rate, CPU inputs Ia.6 to Ia.7	30 kHz (20 kHz in quadrature mode)
	Max. rate, SB inputs	See SB specifications
Pulse outputs[1]	Max. number of pulse outputs	8 (any CPU or SB digital output)
	Max. rate, CPU outputs Qa.0 to Qa.3	100 kHz

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

Technical data	Description	
Pulse outputs[1]	Max. rate, CPU outputs Qa.4 to Qa.5	20 kHz
	Max. rate, SB outputs	See SB specifications
Pulse catch inputs	Yes, each onboard CPU digital input and SB digital input	
Time delay interrupts	20 total with 1 ms resolution	
Cyclic interrupts	20 total with 1 us resolution	
Edge interrupts	Rising and falling for each onboard CPU digital input and SB digital input	
Memory card (Page 333)	SIMATIC memory card (optional).	
Motion control	Available Resources	800
	Required Resources	40 per speed-controlled axis
		80 per positioning axis
		160 per synchronous axis
		80 per external encoder
		20 per output cam
		160 per cam track
		40 per measuring input
	Available Extended Resources	40
	Required Extended Resources	2 per cam (1000 points)
		30 for each set of kinematics
PID	PID Compact	Yes, universal PID controller with integrated optimization
	PID 3Step	Yes, PID controller with integrated optimization for valves
	PID Temp	Yes, PID controller with integrated optimization for temperature
Real time clock	Accuracy	+/- 60 seconds per month
	Retention time, super capacitor	20 days typical at 40 °C, 12 days minimum at 40 °C

1 For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

A.4.2 Performance

Table A-18 Performance

Type of instruction[1]	Direct addressing (I, Q, and M)	DB accesses
Boolean	0.037 µs/instruction	
Move_Bool	0.067 µs/instruction	0.066 µs/instruction
Move_Word	0.027 µs/instruction	0.030 µs/instruction
Move_Real	0.027 µs/instruction	0.030 µs/instruction
Add_Real	0.119 µs/instruction	0.074 µs/instruction

1 Many variables affect measured times. The above performance times are for the fastest instructions in each category and error-free programs.

A.4.3 Blocks, timers, and counters

Table A-19 Blocks, times, and counters

Element	Description	
Blocks	Type	OB, FB, FC, DB
	Max. number of elements	4000; Blocks (OB, FB, FC, DB) and UDTs
	Max. OB, FB, FC size	64 Kbytes
	Max. DB size (Optimized)	500 Kbytes Work Memory 16 Mbytes Load Memory
	Max. DB size (Non-optimized)	64 Kbytes (DBs with absolute addressing)
	Address range for FBs and FCs	1 to 65535
	Address range for DBs	1 to 59999
	Nesting depth per priority class[1]	24 (OB plus 23 more levels)
	Monitoring	Status of 8 code blocks can be monitored simultaneously.
Number of OBs per event class	Program cycle	100
	Startup	100
	Time delay interrupt	20 (one per event)
	Cyclic interrupt	20 (one per event)
	Hardware interrupt	50
	Time error interrupt	1
	Diagnostic error interrupt	1
	Pull or plug of modules	1
	Rack or station failure	1
	Time of day	20 (one per event)
	Synchronous Cycle	1
	Status	1
	Update	1
	Profile	1
	MC-Interpolator	1
	MC-Servo	1
	MC-PreServo	1
	MC-PostServo	1
	MC-LookAhead	1
	MC-PreInterpolator	1
	Programming error	1
	I/O access error	1
Timers	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon time type

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

Element	Description	
Timers	IEC_TIMER	16 bytes
	IEC_LTIMER	28 bytes
Counters	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon count type
	IEC_SCOUNTER, IEC_USCOUNTER	3 bytes
	IEC_COUNTER, IEC_UCOUNTER	6 bytes
	IEC_DCOUNTER, IEC_UDCOUNTER	12 bytes
	IEC_LCOUNTER, IEC_ULCOUNTER	24 bytes
Runtime Meters	Quantity	16

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

A.4.4 Communications

Table A-20 Communications

Technical data	Description	
Number of ports	2 with an integrated switch	
Type	Ethernet (RJ-45 connector)	
Connections	88 connections max. (integrated into CPU) 10 reserved for ES/HMI/web	
Data rates	100 Mb/s	
Isolation (external signal to logic)	Transformer isolated, 1500 V AC (type test)[1]	
Cable type	CAT5e shielded	
Interfaces	1 PROFINET	
	0 PROFIBUS	
PROFINET Protocols	PROFINET IO controller	Yes
	PROFINET IO device	Yes
	SIMATIC communication	Yes
	Open IE communication	Yes
	Web server	Yes
	Media redundancy	Yes
PROFINET IO controller services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	Yes
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
PROFINET IO controller services	MRPD	Yes – Requires an IRT sync domain
	PROFIenergy	Yes (per user program)
	Prioritized startup	Yes (max. 16 PROFINET devices)
	Number of connectable I/O devices, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of submodules, max.	512
	Number of IO devices that you can connect for RT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of in line IO devices that you can connect for RT, max.	31
	Number of IO devices that you can connect for IRT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of IO devices that can be activ-ated/deactivated simultaneously, max.	8
	The minimum update time depends on the communication component set for PROFINET IO, on the number of IO devices, and the quantity of configured user data.	RT Send clock: 1 ms to 512 ms IRT Send clock: 1 ms to 512 ms (1 ms resolution)
PROFINET I-Device	Number of connections, max.	2
PROFINET I-Device services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	No
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes
	PROFIenergy	Yes (per user program)
	Shared device	Yes
	Number of IO controllers with shared device, max.	2
SIMATIC communication	S7 communication as server	Yes
	S7 communication as client	Yes
	User data per job, max.	See TIA Portal information system (S7 com-munication, user data size)
Open IE communication	TCP/IP	Yes, 8 Kbytes max. data length Several passive connections per port
	ISO-on-TCP (RFC1006)	Yes, 8 Kbytes max. data length
	UDP	Yes, 2048 bytes max. data length 1472 bytes max. for UDP broadcast
	DHCP	Yes
	SNMP	Yes
	DCP	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
Open IE communication	LLDP	Yes
Near Field Communication (NFC)	Yes, with the S7-1200 G2 NFC app	
S7 message functions	Number of login stations for message functions, max.	32
	Program alarms	Yes
	Number of configurable program messages, max.	5000
	Number of loadable program messages in RUN, max.	2500
	Number of simultaneously active program alarms	600 program alarms 100 alarms for system diagnostics 160 for motion technology objects
Test commissioning functions	Joint commission (Team Engineering)	Yes, parallel online access possible for up to 5 engineering systems
	Program status	Yes, up to 8 blocks simultaneously (in total across all ES clients)
	Single step	No
	Breakpoints	No
	SIMATIC Controller Profiling	Yes
Monitor/modify	Variables	Inputs/outputs, memory bits, DBs, distributed I/Os, timers, counters
	Number of monitor variables, max.	200 per job
	Number of modify variables, max.	200 per job
Force	Variables	Peripheral inputs/outputs
	Number of variables, max.	200
Trace	Number of configurable traces	4
	Variables captured per trace, max.	16
	Data captured per trace, max.	512 KB
Diagnostics buffer	Number of entries, max.	500
	Retentive	100

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

A.4.5 Power supply and sensor power

Table A-21 Power supply

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Rated voltage	24 V DC	
Voltage range	20.4 to 28.8 V DC	
Reverse voltage protection	Yes	
Input current (CPU only)	185 mA at 24 V DC	125 mA at 24 V DC
Input current (with all accessories)	765 mA at 24 V DC	700 mA at 24 V DC
Inrush current	12 A max. at 28.8 V DC	
I^2t	0.5 A^2 s	
Isolation (input power to logic)	Not isolated	
Hold up time (loss of power)	10 ms at 24 V DC	
Internal fuse	3 A, 250 V, slow blow not user replaceable	

Table A-22 Sensor power

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Rated voltage	24 V DC	
Voltage range	L+ minus 4 V DC min.	
Output current rating	300 mA max. (short-circuit protected)	
Ripple noise (<10 MHz)	Same as input line	
Isolation (CPU logic to sensor power)	Not isolated	
Cable length	500 m shielded	
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)	

A.4.6 Digital inputs and outputs

Table A-23 Digital inputs

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Number of inputs	8	
Assignment	Ia.0 to Ia.5 (high-speed) Ia.6 to Ia.7 (standard)	
Type	Sink/Source (IEC Type 1 sink)	
Rated voltage	24 V DC at 6 mA, nominal (high-speed) 24 V DC at 4 mA, nominal (standard)	
Continuous permissible voltage	30 V DC, max. at 8 mA, max. (high-speed) 30 V DC, max. at 6 mA, max. (standard)	
Logic 1 signal	15 V DC min. at 2.5 mA	
Logic 0 signal	5 V DC max. or 0.5 mA	
Isolation (field side to logic)	707 V DC (type test)	

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Isolation groups	1	
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0	
HSC clock input rates (Logic 1 level = 15 to 26 V DC)	Single phase: 100 kHz (Ia.0 to Ia.5) Single phase: 30 kHz (Ia.6 to Ia.7) Quadrature phase: 80 kHz (Ia.0 to Ia.5) Quadrature phase: 20 kHz (Ia.6 to Ia.7)	
Cable length	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs	
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)	

Table A-24 Digital outputs

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Number of outputs	6	
Assignment	Qa.0 to Qa.5	Qa.0 to Qa.3 (high-speed) Qa.4 to Qa.5 (standard)
Type	Relay, dry contact	Solid state – MOSFET (sourcing)
Rated voltage	--	24 V DC
Voltage range	5 to 30 V DC or 5 to 250 V AC	20.4 to 28.8 V DC
Logic 1 signal at max. current	--	20 V DC min.
Logic 0 signal with 10 kΩ load	--	0.1 V DC max.
Current	2.0 A max.	0.5 A max.
Minimum load[1]	125 mW DC / 500 mW AC	--
Lamp load	30 W DC / 200 W AC	5 W
ON state resistance	0.2 Ω max. when new	0.6 Ω max.
Leakage current per point	--	10 µA max.
Overload protection	No	
Isolation (field side to logic)	4200 V DC for 5 seconds + 1600 V DC for 1 minute (type test)	500 V AC for 1 minute (type test)
Isolation (coil to logic)	None	--
Isolation resistance	100 MΩ min. when new	--
Isolation between open contacts	750 V AC for 1 minute	--
Isolation groups	1	1
Current per common	12 A max. (10 A max. per pin)	3 A max.
Inductive clamp voltage	--	L+ minus 40 V, 1 W dissipation
Switching delay (Qa.0 to Qa.3)	10 ms max.	1.0 µs max., OFF to ON 3.0 µs max., ON to OFF

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

2 For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

Technical data	**CPU 1212FC DC/DC/Relay**	**CPU 1212FC DC/DC/DC**
Switching delay (Qa.4 to Qa.5)	10 ms max.	50 µs max., OFF to ON 200 µs max., ON to OFF
Maximum relay switching frequency	1 Hz	--
Pulse Train Output (PTO) rate	Not recommended[2]	100 kHz max. (Qa.0 to Qa.3) 20 kHz max. (Qa.4 to Qa.5) 2 Hz min.[3]
Lifetime mechanical (no load)	10000000 open/close cycles	--
Lifetime contacts at rated load	100000 open/close cycles	--
Behavior on RUN to STOP	Last value or substitute value (default value 0)	
Control of a digital input	Yes	
Parallel outputs for redundant load control	Yes (with same common)	
Parallel outputs for increased load	No	
Cable length	500 m shielded, 150 m unshielded	
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)	

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

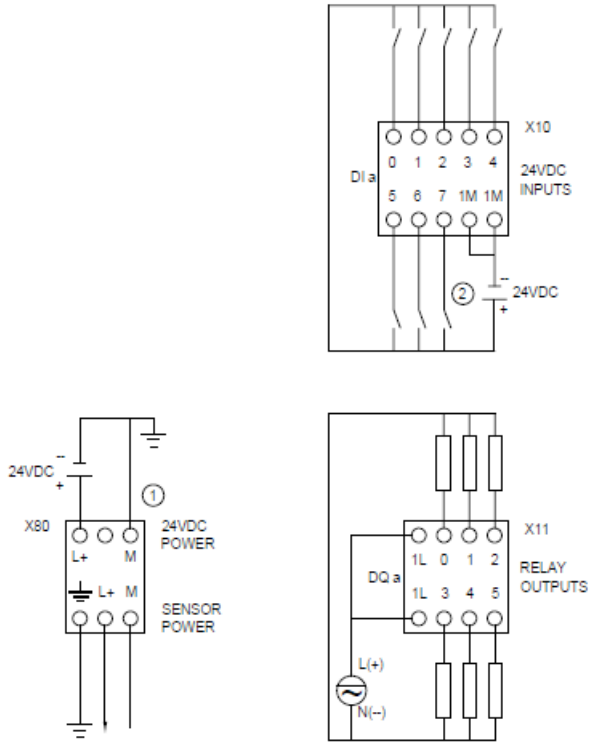
2 For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

A.4.7 Wiring diagrams

The wiring diagrams and pin connector locations are shown below:

CPU 1212FC DC/DC/Relay



X80: DC power wiring terminal (Gray, No keying)

DC power	L+		M
Pin #	1	3	5
Pin #	2	4	6
Sensor power	GND	L+	M

X10: DC input wiring terminal (Gray, No keying)

Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4
Pin #	1	3	5	7	9
Pin #	2	4	6	8	10
Signal	DI a.5	DI a.6	DI a.7	1M	1M

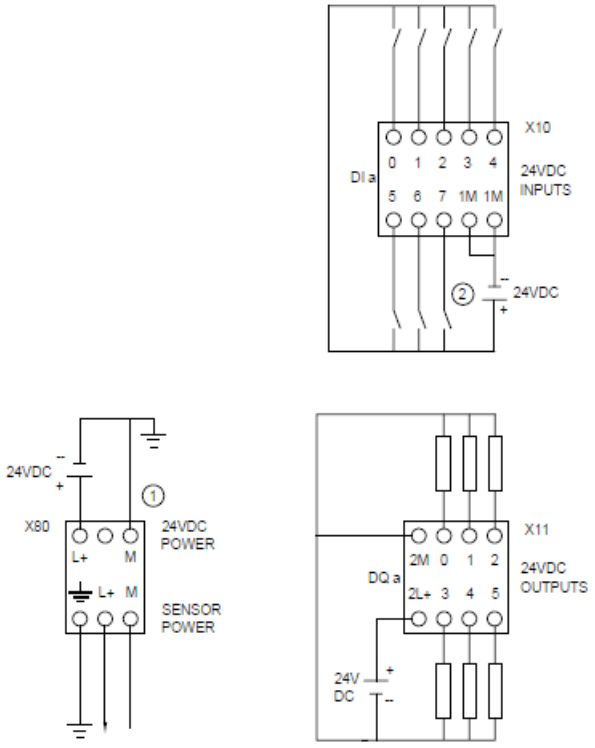
X11: Relay output wiring terminal (Orange, Type-A keying)

Signal	1L	DQ a.0	DQ a.1	DQ a.2
Pin #	1	3	5	7
Pin #	2	4	6	8
Signal	1L	DQ a.3	DQ a.4	DQ a.5

① For additional noise immunity, jumper the 24 V DC Power “M” to Chassis Ground on the connector.

② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

CPU 1212FC DC/DC/DC



X80: DC power wiring terminal (Gray, No keying)					
DC power	L+		M		
Pin #	1	3	5		
Pin #	2	4	6		
Sensor power	GND	L+	M		
X10: DC input wiring terminal (Gray, No keying)					
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4
Pin #	1	3	5	7	9
Pin #	2	4	6	8	10
Signal	DI a.5	DI a.6	DI a.7	1M	1M
X11: DC output wiring terminal (Gray, No keying)					
Signal	2M	DQ a.0	DQ a.1	DQ a.2	
Pin #	1	3	5	7	
Pin #	2	4	6	8	
Signal	2L+	DQ a.3	DQ a.4	DQ a.5	

① For additional noise immunity, jumper the 24 V DC Power "M" to Chassis Ground on the connector.
② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.5 CPU 1214C

A.5.1 General specifications and features

Table A-25 General

Technical data	**CPU 1214C AC/DC/Relay**	**CPU 1214C DC/DC/Relay**	**CPU 1214C DC/DC/DC**
Article number	6ES7214-1BH50-0XB0	6ES7214-1HH50-0XB0	6ES7214-1AH50-0XB0
Dimensions W x H x D	80 x 125 x 100 mm		
Weight (product/shipping)	417 grams / 474 grams	376 grams / 433 grams	352 grams / 409 grams
Power dissipation	4.0 W	3.5 W	
Current available for expansion devices	1600 mA max. (5 V DC)		
Current available on sensor supply	400 mA (24 V DC sensor power, current limited)		

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]		
	Vertical mounting -20 °C to 50 °C[2]		Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum		

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-26 CPU features

Technical data	Description	
User memory	Work Memory	250 Kbytes (Program) 750 Kbytes (Data)
	Load Memory	8 Mbytes (Internal) 32 Gbytes (using SD card)
	Retentive Memory	20 Kbytes
Onboard digital I/O	14 inputs / 10 outputs	
Process image size	1024 bytes of inputs (I) / 1024 bytes of outputs (Q)	
Bit memory size	8192 bytes (M)	
Temporary (local) memory	Per priority class, max.	64 Kbytes
	Per block, max.	16 Kbytes
Communication module expansion	3 max. (must connect to the right of the CPU or to the right of another CM)	
Signal module expansion (SM plus CM)	10 max.	
Signal board or Communication board expansion	2 max.	
High-speed counters	Max. number of high-speed counters	8 (any CPU or SB digital input)
	Max. rate, CPU inputs Ia.0 to Ia.5	100 kHz (80 kHz in quadrature mode)
	Max. rate, CPU inputs Ia.6 to Ib.5	30 kHz (20 kHz in quadrature mode)
	Max. rate, SB inputs	See SB specifications
Pulse outputs[1]	Max. number of pulse outputs	8 (any CPU or SB digital output)
	Max. rate, CPU outputs Qa.0 to Qa.3	100 kHz
	Max. rate, CPU outputs Qa.4 to Qb.1	20 kHz
	Max. rate, SB outputs	See SB specifications
Pulse catch inputs	Yes, each onboard CPU digital input and SB digital input	
Time delay interrupts	20 total with 1 ms resolution	
Cyclic interrupts	20 total with 1 us resolution	
Edge interrupts	Rising and falling for each onboard CPU digital input and SB digital input	
Memory card (Page 333)	SIMATIC memory card (optional).	
Motion control	Available Resources	800

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

Technical data	Description	
Motion control	Required Resources	40 per speed-controlled axis
		80 per positioning axis
		160 per synchronous axis
		80 per external encoder
		20 per output cam
		160 per cam track
		40 per measuring input
	Available Extended Resources	40
	Required Extended Resources	2 per cam (1000 points)
		30 for each set of kinematics
PID	PID Compact	Yes, universal PID controller with integrated optimization
	PID 3Step	Yes, PID controller with integrated optimization for valves
	PID Temp	Yes, PID controller with integrated optimization for temperature
Real time clock	Accuracy	+/- 60 seconds per month
	Retention time, super capacitor	20 days typical at 40 °C, 12 days minimum at 40 °C

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

A.5.2 Performance

Table A-27 Performance

Type of instruction[1]	Direct addressing (I, Q, and M)	DB accesses
Boolean	0.037 µs/instruction	
Move_Bool	0.067 µs/instruction	0.066 µs/instruction
Move_Word	0.027 µs/instruction	0.030 µs/instruction
Move_Real	0.027 µs/instruction	0.030 µs/instruction
Add_Real	0.119 µs/instruction	0.074 µs/instruction

[1] Many variables affect measured times. The above performance times are for the fastest instructions in each category and error-free programs.

A.5.3 Blocks, timers, and counters

Table A-28 Blocks, times, and counters

Element	Description	
Blocks	Type	OB, FB, FC, DB
	Max. number of elements	4000; Blocks (OB, FB, FC, DB) and UDTs
	Max. OB, FB, FC size	64 Kbytes
	Max. DB size (Optimized)	500 Kbytes Work Memory 16 Mbytes Load Memory
	Max. DB size (Non-optimized)	64 Kbytes (DBs with absolute addressing)
	Address range for FBs and FCs	1 to 65535
	Address range for DBs	1 to 59999
	Nesting depth per priority class[1]	24 (OB plus 23 more levels)
	Monitoring	Status of 8 code blocks can be monitored simultaneously.
Number of OBs per event class	Program cycle	100
	Startup	100
	Time delay interrupt	20 (one per event)
	Cyclic interrupt	20 (one per event)
	Hardware interrupt	50
	Time error interrupt	1
	Diagnostic error interrupt	1
	Pull or plug of modules	1
	Rack or station failure	1
	Time of day	20 (one per event)
	Synchronous Cycle	1
	Status	1
	Update	1
	Profile	1
	MC-Interpolator	1
	MC-Servo	1
	MC-PreServo	1
	MC-PostServo	1
	MC-LookAhead	1
	MC-PreInterpolator	1
	Programming error	1
	I/O access error	1
Timers	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon time type

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

Element	Description	
Timers	IEC_TIMER	16 bytes
	IEC_LTIMER	28 bytes
Counters	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon count type
	IEC_SCOUNTER, IEC_USCOUNTER	3 bytes
	IEC_COUNTER, IEC_UCOUNTER	6 bytes
	IEC_DCOUNTER, IEC_UDCOUNTER	12 bytes
	IEC_LCOUNTER, IEC_ULCOUNTER	24 bytes
Runtime Meters	Quantity	16

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

A.5.4 Communications

Table A-29 Communications

Technical data	Description	
Number of ports	2 with an integrated switch	
Type	Ethernet (RJ-45 connector)	
Connections	88 connections max. (integrated into CPU) 10 reserved for ES/HMI/web	
Data rates	100 Mb/s	
Isolation (external signal to logic)	Transformer isolated, 1500 V AC (type test)[1]	
Cable type	CAT5e shielded	
Interfaces	1 PROFINET	
	0 PROFIBUS	
PROFINET Protocols	PROFINET IO controller	Yes
	PROFINET IO device	Yes
	SIMATIC communication	Yes
	Open IE communication	Yes
	Web server	Yes
	Media redundancy	Yes
PROFINET IO controller services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	Yes
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
PROFINET IO controller services	MRPD	Yes – Requires an IRT sync domain
	PROFIenergy	Yes (per user program)
	Prioritized startup	Yes (max. 16 PROFINET devices)
	Number of connectable I/O devices, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of submodules, max.	512
	Number of IO devices that you can connect for RT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of in line IO devices that you can connect for RT, max.	31
	Number of IO devices that you can connect for IRT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of IO devices that can be activated/deactivated simultaneously, max.	8
	The minimum update time depends on the communication component set for PROFINET IO, on the number of IO devices, and the quantity of configured user data.	RT Send clock: 1 ms to 512 ms IRT Send clock: 1 ms to 512 ms (1 ms resolution)
PROFINET I-Device	Number of connections, max.	2
PROFINET I-Device services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	No
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes
	PROFIenergy	Yes (per user program)
	Shared device	Yes
	Number of IO controllers with shared device, max.	2
SIMATIC communication	S7 communication as server	Yes
	S7 communication as client	Yes
	User data per job, max.	See TIA Portal information system (S7 communication, user data size)
Open IE communication	TCP/IP	Yes, 8 Kbytes max. data length Several passive connections per port
	ISO-on-TCP (RFC1006)	Yes, 8 Kbytes max. data length
	UDP	Yes, 2048 bytes max. data length 1472 bytes max. for UDP broadcast
	DHCP	Yes
	SNMP	Yes
	DCP	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
Open IE communication	LLDP	Yes
Near Field Communication (NFC)	Yes, with the S7-1200 G2 NFC app	
S7 message functions	Number of login stations for message functions, max.	32
	Program alarms	Yes
	Number of configurable program messages, max.	5000
	Number of loadable program messages in RUN, max.	2500
	Number of simultaneously active program alarms	600 program alarms 100 alarms for system diagnostics 160 for motion technology objects
Test commissioning functions	Joint commission (Team Engineering)	Yes, parallel online access possible for up to 5 engineering systems
	Program status	Yes, up to 8 blocks simultaneously (in total across all ES clients)
	Single step	No
	Breakpoints	No
	SIMATIC Controller Profiling	Yes
Monitor/modify	Variables	Inputs/outputs, memory bits, DBs, distributed I/Os, timers, counters
	Number of monitor variables, max.	200 per job
	Number of modify variables, max.	200 per job
Force	Variables	Peripheral inputs/outputs
	Number of variables, max.	200
Trace	Number of configurable traces	4
	Variables captured per trace, max.	16
	Data captured per trace, max.	512 KB
Diagnostics buffer	Number of entries, max.	500
	Retentive	100

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

A.5.5 Power supply and sensor power

Table A-30 Power supply

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Rated voltage	120/240 V AC	24 V DC	
Voltage range	85 to 264 V AC	20.4 to 28.8 V DC	
Reverse voltage protection	--	Yes	
Line frequency	47 to 63 Hz	--	
Input current (CPU only)	80 mA at 120 V AC 44 mA at 240 V AC	245 mA at 24 V DC	145 mA at 24 V DC
Input current (with all accessories)	480 mA at 120 V AC 275 mA at 240 V AC	1100 mA at 24 V DC	1000 mA at 24 V DC
Inrush current	20 A max. at 264 V AC	12 A max. at 28.8 V DC	
I^2t	0.8 A^2 s	0.5 A^2 s	
Isolation (input power to logic)	1500 V AC	Not isolated	
Ground leakage (AC line to functional earth)	0.5 mA max.	--	
Hold up time (loss of power)	20 ms at 120 V AC 80 ms at 240 V AC	10 ms at 24 V DC	
Internal fuse	3 A, 250 V, slow blow not user replaceable		

Table A-31 Sensor power

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Rated voltage	24 V DC		
Voltage range	20.4 to 28.8 V DC	L+ minus 4 V DC min.	
Output current rating	400 mA max. (short-circuit protected)		
Ripple noise (<10 MHz)	< 1 V peak to peak max.	Same as input line	
Isolation (CPU logic to sensor power)	Not isolated		
Cable length	500 m shielded		
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)		

A.5.6 Digital inputs and outputs

Table A-32 Digital inputs

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Number of inputs	14		
Assignment	Ia.0 to Ia.5 (high-speed) Ia.6 to Ib.5 (standard)		
Type	Sink/Source (IEC Type 1 sink)		
Rated voltage	24 V DC at 6 mA, nominal (high-speed) 24 V DC at 4 mA, nominal (standard)		

Technical data	**CPU 1214C AC/DC/Relay**	**CPU 1214C DC/DC/Relay**	**CPU 1214C DC/DC/DC**
Continuous permissible voltage	30 V DC, max. at 8 mA, max. (high-speed) 30 V DC, max. at 6 mA, max. (standard)		
Logic 1 signal	15 V DC min. at 2.5 mA		
Logic 0 signal	5 V DC max. or 0.5 mA		
Isolation (field side to logic)	707 V DC (type test)		
Isolation groups	1		
Current per common	20 A mix. (10 A max. per pin)		5 A max.
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0		
HSC clock input rates (Logic 1 level = 15 to 26 V DC)	Single phase: 100 kHz (Ia.0 to Ia.5) Single phase: 30 kHz (Ia.6 to Ib.5) Quadrature phase: 80 kHz (Ia.0 to Ia.5) Quadrature phase: 20 kHz (Ia.6 to Ib.5)		
Cable length	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs		
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)		

Table A-33 Digital outputs

Technical data	**CPU 1214C AC/DC/Relay**	**CPU 1214C DC/DC/Relay**	**CPU 1214C DC/DC/DC**
Number of outputs	10		
Assignment	Qa.0 to Qb.1		Qa.0 to Qa.3 (high-speed) Qa.4 to Qb.1 (standard)
Type	Relay, dry contact		Solid state – MOSFET (sourcing)
Rated voltage	--		24 V DC
Voltage range	5 to 30 V DC or 5 to 250 V AC		20.4 to 28.8 V DC
Logic 1 signal at max. current	--		20 V DC min.
Logic 0 signal with 10 kΩ load	--		0.1 V DC max.
Current	2.0 A max.		0.5 A max.
Minimum load[1]	125 mW DC / 500 mW AC		--
Lamp load	30 W DC / 200 W AC		5 W
ON state resistance	0.2 Ω max. when new		0.6 Ω max.
Leakage current per point	--		10 µA max.
Overload protection	No		
Isolation (field side to logic)	4200 V DC for 5 seconds + 1600 V DC for 1 minute (type test)		500 V AC for 1 minute (type test)
Isolation (coil to logic)	None		--
Isolation resistance	100 MΩ min. when new		--

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

2 For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

Technical data	**CPU 1214C AC/DC/Relay**	**CPU 1214C DC/DC/Relay**	**CPU 1214C DC/DC/DC**
Isolation between open contacts	750 V AC for 1 minute		--
Isolation groups	1		1
Current per common	20 A max. (10 A. max. per pin)		5 A. max.
Inductive clamp voltage	--		L+ minus 40 V, 1 W dissipation
Switching delay (Qa.0 to Qa.3)	10 ms max.		1.0 µs max., OFF to ON 3.0 µs max., ON to OFF
Switching delay (Qa.4 to Qa.5)	10 ms max.		50 µs max., OFF to ON 200 µs max., ON to OFF
Maximum relay switching frequency	1 Hz		--
Pulse Train Output (PTO) rate	Not recommended[2]		100 kHz max. (Qa.0 to Qa.3) 20 kHz max. (Qa.4 to Qb.1) 2 Hz min.[3]
Lifetime mechanical (no load)	10000000 open/close cycles		--
Lifetime contacts at rated load	100000 open/close cycles		--
Behavior on RUN to STOP	Last value or substitute value (default value 0)		
Control of a digital input	Yes		
Parallel outputs for redundant load control	Yes (with same common)		
Parallel outputs for increased load	No		
Cable length	500 m shielded, 150 m unshielded		
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)		

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

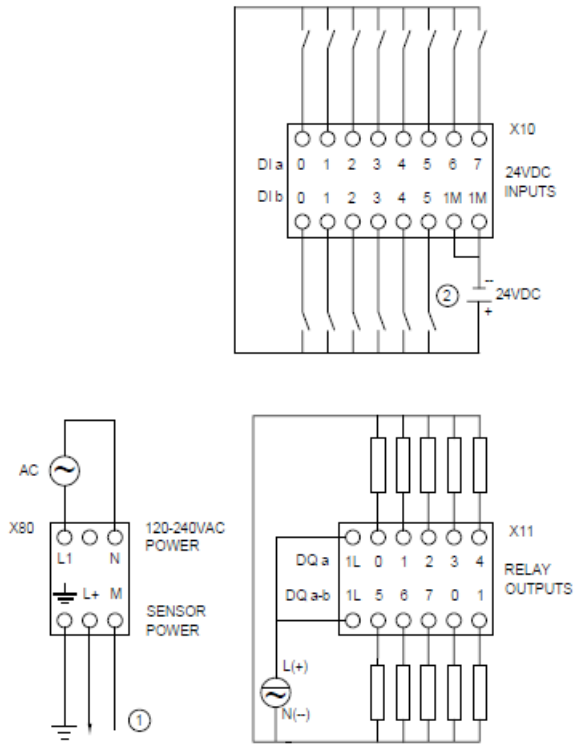
2 For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

A.5.7 Wiring diagrams

The wiring diagrams and pin connector locations are shown below:

CPU 1214C AC/DC/Relay

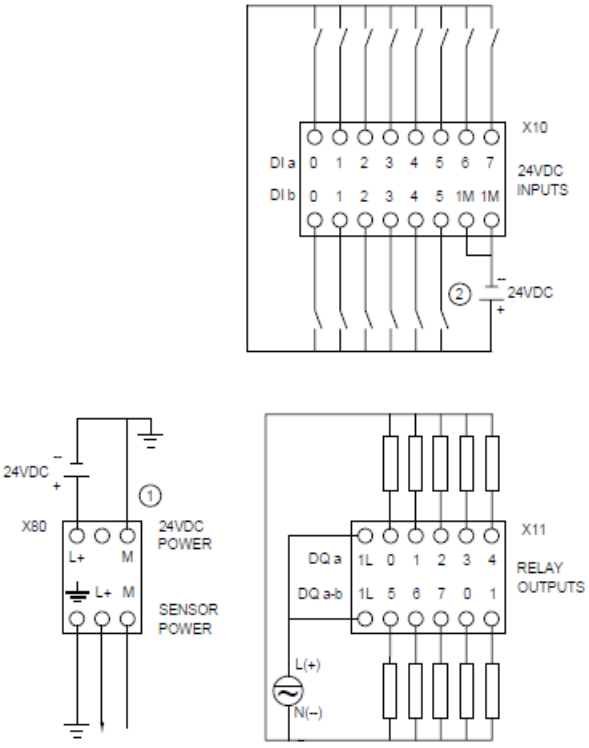


X80: AC power wiring terminal (Orange, Type-A keying)								
AC power	L1		N					
Pin #	1	3	5					
Pin #	2	4	6					
Sensor power	GND	L+	M					
X10: DC input wiring terminal (Gray, No keying)								
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	DI a.5	DI a.6	DI a.7
Pin #	1	3	5	7	9	11	13	15
Pin #	2	4	6	8	10	12	14	16
Signal	DI b.0	DI b.1	DI b.2	DI b.3	DI b.4	DI b.5	1M	1M
X11: Relay output wiring terminal (Orange, Type-A keying)								
Signal	1L	DQ a.0	DQ a.1	DQ a.2	DQ a.3	DQ a.4		
Pin #	1	3	5	7	9	11		
Pin #	2	4	6	8	10	12		
Signal	1L	DQ a.5	DQ a.6	DQ a.7	DQ b.0	DQ b.1		

① For additional noise immunity, jumper the Sensor Power “M” to Chassis Ground on the connector.

② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

CPU 1214C DC/DC/Relay



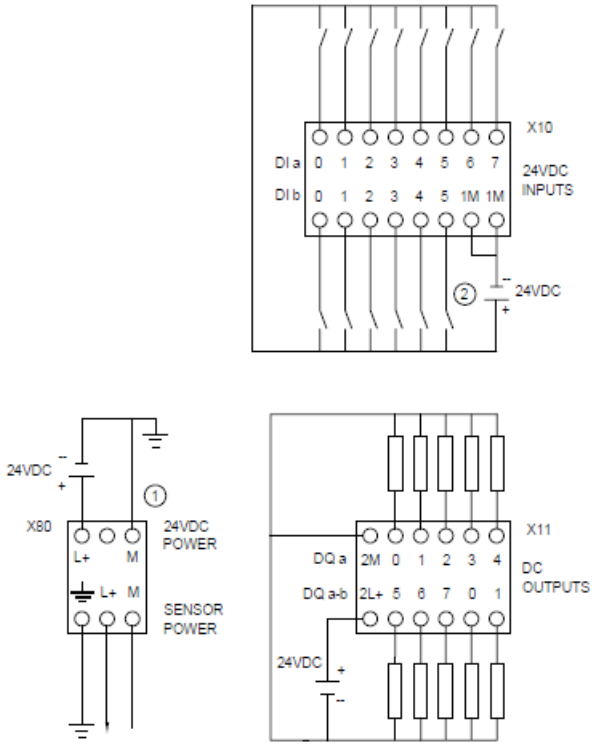
X80: DC power wiring terminal (Gray, No keying)				
DC power	L+		M	
Pin #	1	3	5	
Pin #	2	4	6	
Sensor power	GND	L+	M	

X10: DC input wiring terminal (Gray, No keying)								
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	DI a.5	DI a.6	DI a.7
Pin #	1	3	5	7	9	11	13	15
Pin #	2	4	6	8	10	12	14	16
Signal	DI b.0	DI b.1	DI b.2	DI b.3	DI b.4	DI b.5	1M	1M

X11: Relay output wiring terminal (Orange, Type-A keying)							
Signal	1L	DQ a.0	DQ a.1	DQ a.2	DQ a.3	DQ a.4	
Pin #	1	3	5	7	9	11	
Pin #	2	4	6	8	10	12	
Signal	1L	DQ a.5	DQ a.6	DQ a.7	DQ b.0	DQ b.1	

① For additional noise immunity, jumper the 24 V DC Power “M” to Chassis Ground on the connector.
② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

CPU 1214C DC/DC/DC



X80: DC power wiring terminal (Gray, No keying)								
DC power	L+		M					
Pin #	1	3	5					
Pin #	2	4	6					
Sensor power	GND	L+	M					
X10: DC input wiring terminal (Gray, No keying)								
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	DI a.5	DI a.6	DI a.7
Pin #	1	3	5	7	9	11	13	15
Pin #	2	4	6	8	10	12	14	16
Signal	DI b.0	DI b.1	DI b.2	DI b.3	DI b.4	DI b.5	1M	1M
X11: DC output wiring terminal (Gray, No keying)								
Signal	2M	DQ a.0	DQ a.1	DQ a.2	DQ a.3	DQ a.4		
Pin #	1	3	5	7	9	11		
Pin #	2	4	6	8	10	12		
Signal	2L+	DQ a.5	DQ a.6	DQ a.7	DQ b.0	DQ b.1		

① For additional noise immunity, jumper the 24 V DC Power "M" to Chassis Ground on the connector.
② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.6 CPU 1214FC

A.6.1 General specifications and features

Table A-34 General

Technical data	**CPU 1214FC DC/DC/Relay**	**CPU 1214FC DC/DC/DC**
Article number	6ES7214-1HF50-0XB0	6ES7214-1AF50-0XB0
Dimensions W x H x D	80 x 125 x 100 mm	
Weight (product/shipping)	376 grams / 433 grams	352 grams / 409 grams
Power dissipation	3.5 W	
Current available for expansion devices	1600 mA max. (5 V DC)	
Current available on sensor supply	400 mA (24 V DC sensor power, current limited)	

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Technical data	**CPU 1214FC DC/DC/Relay**	**CPU 1214FC DC/DC/DC**
Safety class (highest)	PL e (performance level according to ISO 13849-1) SIL 3 (safety integrity level according to IEC 61508)	
Probability of failure	Low demand mode: PFDavg in accordance with SIL 3 < 2.00E-05 High demand/continuous mode: PFH in accordance with SIL 3 < 1.00E-09 (altitude -1000 m to 3000 m) < 2.00E-09 (altitude >3000 m to 5000 m) For service life of 20 years and repair time of 100 hours	
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]	
	Vertical mounting -20 °C to 50 °C[2]	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum	

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-35 CPU features

Technical data	**Description**	
User memory	Work Memory	300 Kbytes (Program) 750 Kbytes (Data)
	Load Memory	8 Mbytes (Internal) 32 Gbytes (using SD card)
	Retentive Memory	20 Kbytes
Onboard digital I/O	14 inputs / 10 outputs	
Process image size	1024 bytes of inputs (I) / 1024 bytes of outputs (Q)	
Bit memory size	8192 bytes (M)	
Temporary (local) memory	Per priority class, max.	64 Kbytes
	Per block, max.	16 Kbytes
Communication module expansion	3 max. (must connect to the right of the CPU or to the right of another CM)	
Signal module expansion (SM plus CM)	10 max.	
Signal board or Communication board expansion	2 max.	
High-speed counters	Max. number of high-speed counters	8 (any CPU or SB digital input)
	Max. rate, CPU inputs Ia.0 to Ia.5	100 kHz (80 kHz in quadrature mode)
	Max. rate, CPU inputs Ia.6 to Ib.5	30 kHz (20 kHz in quadrature mode)
	Max. rate, SB inputs	See SB specifications
Pulse outputs[1]	Max. number of pulse outputs	8 (any CPU or SB digital output)
	Max. rate, CPU outputs Qa.0 to Qa.3	100 kHz

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

Technical data	Description	
Pulse outputs[1]	Max. rate, CPU outputs Qa.4 to Qb.1	20 kHz
	Max. rate, SB outputs	See SB specifications
Pulse catch inputs	Yes, each onboard CPU digital input and SB digital input	
Time delay interrupts	20 total with 1 ms resolution	
Cyclic interrupts	20 total with 1 us resolution	
Edge interrupts	Rising and falling for each onboard CPU digital input and SB digital input	
Memory card (Page 333)	SIMATIC memory card (optional).	
Motion control	Available Resources	800
	Required Resources	40 per speed-controlled axis
		80 per positioning axis
		160 per synchronous axis
		80 per external encoder
		20 per output cam
		160 per cam track
		40 per measuring input
	Available Extended Resources	40
	Required Extended Resources	2 per cam (1000 points)
		30 for each set of kinematics
PID	PID Compact	Yes, universal PID controller with integrated optimization
	PID 3Step	Yes, PID controller with integrated optimization for valves
	PID Temp	Yes, PID controller with integrated optimization for temperature
Real time clock	Accuracy	+/- 60 seconds per month
	Retention time, super capacitor	20 days typical at 40 °C, 12 days minimum at 40 °C

[1] For CPU models with relay outputs, you must install a signal board (SB) containing digital outputs to use the pulse outputs.

A.6.2 Performance

Table A-36 Performance

Type of instruction[1]	Direct addressing (I, Q, and M)	DB accesses
Boolean	0.037 µs/instruction	
Move_Bool	0.067 µs/instruction	0.066 µs/instruction
Move_Word	0.027 µs/instruction	0.030 µs/instruction
Move_Real	0.027 µs/instruction	0.030 µs/instruction
Add_Real	0.119 µs/instruction	0.074 µs/instruction

[1] Many variables affect measured times. The above performance times are for the fastest instructions in each category and error-free programs.

A.6.3 Blocks, timers, and counters

Table A-37 Blocks, times, and counters

Element	Description	
Blocks	Type	OB, FB, FC, DB
	Max. number of elements	4000; Blocks (OB, FB, FC, DB) and UDTs
	Max. OB, FB, FC size	64 Kbytes
	Max. DB size (Optimized)	500 Kbytes Work Memory 16 Mbytes Load Memory
	Max. DB size (Non-optimized)	64 Kbytes (DBs with absolute addressing)
	Address range for FBs and FCs	1 to 65535
	Address range for DBs	1 to 59999
	Nesting depth per priority class[1]	24 (OB plus 23 more levels)
	Monitoring	Status of 8 code blocks can be monitored simultaneously.
Number of OBs per event class	Program cycle	100
	Startup	100
	Time delay interrupt	20 (one per event)
	Cyclic interrupt	20 (one per event)
	Hardware interrupt	50
	Time error interrupt	1
	Diagnostic error interrupt	1
	Pull or plug of modules	1
	Rack or station failure	1
	Time of day	20 (one per event)
	Synchronous Cycle	1
	Status	1
	Update	1
	Profile	1
	MC-Interpolator	1
	MC-Servo	1
	MC-PreServo	1
	MC-PostServo	1
	MC-LookAhead	1
	MC-PreInterpolator	1
	Programming error	1
	I/O access error	1
Timers	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon time type

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

Element	Description	
Timers	IEC_TIMER	16 bytes
	IEC_LTIMER	28 bytes
Counters	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size depends upon count type
	IEC_SCOUNTER, IEC_USCOUNTER	3 bytes
	IEC_COUNTER, IEC_UCOUNTER	6 bytes
	IEC_DCOUNTER, IEC_UDCOUNTER	12 bytes
	IEC_LCOUNTER, IEC_ULCOUNTER	24 bytes
Runtime Meters	Quantity	16

[1] Safety programs use 2 nesting levels; the user program, therefore, has a nesting depth of 22 in safety programs.

A.6.4 Communications

Table A-38 Communications

Technical data	Description	
Number of ports	2 with an integrated switch	
Type	Ethernet (RJ-45 connector)	
Connections	88 connections max. (integrated into CPU) 10 reserved for ES/HMI/web	
Data rates	100 Mb/s	
Isolation (external signal to logic)	Transformer isolated, 1500 V AC (type test)[1]	
Cable type	CAT5e shielded	
Interfaces	1 PROFINET	
	0 PROFIBUS	
PROFINET Protocols	PROFINET IO controller	Yes
	PROFINET IO device	Yes
	SIMATIC communication	Yes
	Open IE communication	Yes
	Web server	Yes
	Media redundancy	Yes
PROFINET IO controller services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	Yes
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	Description	
PROFINET IO controller services	MRPD	Yes – Requires an IRT sync domain
	PROFIenergy	Yes (per user program)
	Prioritized startup	Yes (max. 16 PROFINET devices)
	Number of connectable I/O devices, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of submodules, max.	512
	Number of IO devices that you can connect for RT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of in line IO devices that you can connect for RT, max.	31
	Number of IO devices that you can connect for IRT, max.	31 (30 if I-Device is used, 29 if shared I-Device is used)
	Number of IO devices that can be activated/deactivated simultaneously, max.	8
	The minimum update time depends on the communication component set for PROFINET IO, on the number of IO devices, and the quantity of configured user data.	RT Send clock: 1 ms to 512 ms IRT Send clock: 1 ms to 512 ms (1 ms resolution)
PROFINET I-Device	Number of connections, max.	2
PROFINET I-Device services	PG/OP communication	Yes
	S7 routing	No
	Isochronous mode	No
	Open IE communication	Yes
	IRT	Yes
	MRP	Yes
	PROFIenergy	Yes (per user program)
	Shared device	Yes
	Number of IO controllers with shared device, max.	2
SIMATIC communication	S7 communication as server	Yes
	S7 communication as client	Yes
	User data per job, max.	See TIA Portal information system (S7 communication, user data size)
Open IE communication	TCP/IP	Yes, 8 Kbytes max. data length Several passive connections per port
	ISO-on-TCP (RFC1006)	Yes, 8 Kbytes max. data length
	UDP	Yes, 2048 bytes max. data length 1472 bytes max. for UDP broadcast
	DHCP	Yes
	SNMP	Yes
	DCP	Yes

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Technical data	**Description**	
Open IE communication	LLDP	Yes
Near Field Communication (NFC)	Yes, with the S7-1200 G2 NFC app	
S7 message functions	Number of login stations for message functions, max.	32
	Program alarms	Yes
	Number of configurable program messages, max.	5000
	Number of loadable program messages in RUN, max.	2500
	Number of simultaneously active program alarms	600 program alarms 100 alarms for system diagnostics 160 for motion technology objects
Test commissioning functions	Joint commission (Team Engineering)	Yes, parallel online access possible for up to 5 engineering systems
	Program status	Yes, up to 8 blocks simultaneously (in total across all ES clients)
	Single step	No
	Breakpoints	No
	SIMATIC Controller Profiling	Yes
Monitor/modify	Variables	Inputs/outputs, memory bits, DBs, distributed I/Os, timers, counters
	Number of monitor variables, max.	200 per job
	Number of modify variables, max.	200 per job
Force	Variables	Peripheral inputs/outputs
	Number of variables, max.	200
Trace	Number of configurable traces	4
	Variables captured per trace, max.	16
	Data captured per trace, max.	512 KB
Diagnostics buffer	Number of entries, max.	500
	Retentive	100

[1] Ethernet port isolation limits hazards during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

A.6.5 Power supply and sensor power

Table A-39 Power supply

Technical data	CPU 1214FC DC/DC/Relay	CPU 1214FC DC/DC/DC
Rated voltage	24 V DC	
Voltage range	20.4 to 28.8 V DC	
Reverse voltage protection	Yes	
Input current (CPU only)	245 mA at 24 V DC	145 mA at 24 V DC
Input current (with all accessories)	1100 mA at 24 V DC	1000 mA at 24 V DC
Inrush current	12 A max. at 28.8 V DC	
I^2t	0.5 A^2 s	
Isolation (input power to logic)	Not isolated	
Hold up time (loss of power)	10 ms at 24 V DC	
Internal fuse	3 A, 250 V, slow blow not user replaceable	

Table A-40 Sensor power

Technical data	CPU 1214FC DC/DC/Relay	CPU 1214FC DC/DC/DC
Rated voltage	24 V DC	
Voltage range	L+ minus 4 V DC min.	
Output current rating	400 mA max. (short-circuit protected)	
Ripple noise (<10 MHz)	Same as input line	
Isolation (CPU logic to sensor power)	Not isolated	
Cable length	500 m shielded	
Cable size	AWG 24 – 16 (0.2 mm^2 – 1.5 mm^2)	

A.6.6 Digital inputs and outputs

Table A-41 Digital inputs

Technical data	CPU 1214FC DC/DC/Relay	CPU 1214FC DC/DC/DC
Number of inputs	14	
Assignment	Ia.0 to Ia.5 (high-speed) Ia.6 to Ib.5 (standard)	
Type	Sink/Source (IEC Type 1 sink)	
Rated voltage	24 V DC at 6 mA, nominal (high-speed) 24 V DC at 4 mA, nominal (standard)	
Continuous permissible voltage	30 V DC, max. at 8 mA, max. (high-speed) 30 V DC, max. at 6 mA, max. (standard)	
Logic 1 signal	15 V DC min. at 2.5 mA	
Logic 0 signal	5 V DC max. or 0.5 mA	
Isolation (field side to logic)	707 V DC (type test)	

Technical data	**CPU 1214FC DC/DC/Relay**	**CPU 1214FC DC/DC/DC**
Isolation groups	1	
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0	
HSC clock input rates (Logic 1 level = 15 to 26 V DC)	Single phase: 100 kHz (Ia.0 to Ia.5) Single phase: 30 kHz (Ia.6 to Ib.5) Quadrature phase: 80 kHz (Ia.0 to Ia.5) Quadrature phase: 20 kHz (Ia.6 to Ib.5)	
Cable length	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs	
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)	

Table A-42 Digital outputs

Technical data	**CPU 1214FC DC/DC/Relay**	**CPU 1214FC DC/DC/DC**
Number of outputs	10	
Assignment	Qa.0 to Qb.1	Qa.0 to Qa.3 (high-speed) Qa.4 to Qb.1 (standard)
Type	Relay, dry contact	Solid state – MOSFET (sourcing)
Rated voltage	--	24 V DC
Voltage range	5 to 30 V DC or 5 to 250 V AC	20.4 to 28.8 V DC
Logic 1 signal at max. current	--	20 V DC min.
Logic 0 signal with 10 kΩ load	--	0.1 V DC max.
Current	2.0 A max.	0.5 A max.
Minimum load[1]	125 mW DC / 500 mW AC	--
Lamp load	30 W DC / 200 W AC	5 W
ON state resistance	0.2 Ω max. when new	0.6 Ω max.
Leakage current per point	--	10 µA max.
Overload protection	No	
Isolation (field side to logic)	4200 V DC for 5 seconds + 1600 V DC for 1 minute (type test)	500 V AC for 1 minute (type test)
Isolation (coil to logic)	None	--
Isolation resistance	100 MΩ min. when new	--
Isolation between open contacts	750 V AC for 1 minute	--
Isolation groups	1	1
Current per common	20 A max. (10 A max. per pin)	5 A max.
Inductive clamp voltage	--	L+ minus 40 V, 1 W dissipation
Switching delay (Qa.0 to Qa.3)	10 ms max.	1.0 µs max., OFF to ON 3.0 µs max., ON to OFF

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

2 For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

Technical data	**CPU 1214FC DC/DC/Relay**	**CPU 1214FC DC/DC/DC**
Switching delay (Qa.4 to Qa.5)	10 ms max.	50 µs max., OFF to ON 200 µs max., ON to OFF
Maximum relay switching frequency	1 Hz	--
Pulse Train Output (PTO) rate	Not recommended[2]	100 kHz max. (Qa.0 to Qa.3) 20 kHz max. (Qa.4 to Qb.1) 2 Hz min.[3]
Lifetime mechanical (no load)	10000000 open/close cycles	--
Lifetime contacts at rated load	100000 open/close cycles	--
Behavior on RUN to STOP	Last value or substitute value (default value 0)	
Control of a digital input	Yes	
Parallel outputs for redundant load control	Yes (with same common)	
Parallel outputs for increased load	No	
Cable length	500 m shielded, 150 m unshielded	
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)	

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

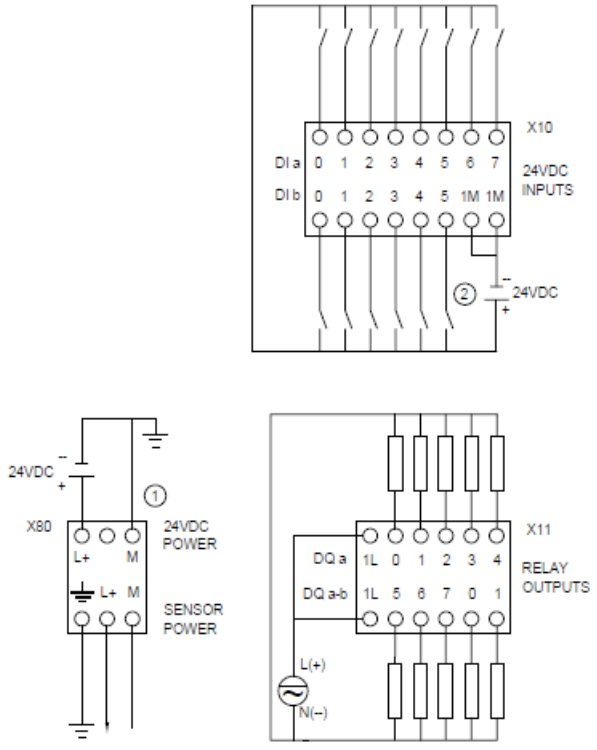
2 For CPU models with relay outputs, you must install a signal board (SB) containing DC digital outputs to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) can improve pulse signal quality and noise immunity.

A.6.7 Wiring diagrams

The wiring diagrams and pin connector locations are shown below:

CPU 1214FC DC/DC/Relay

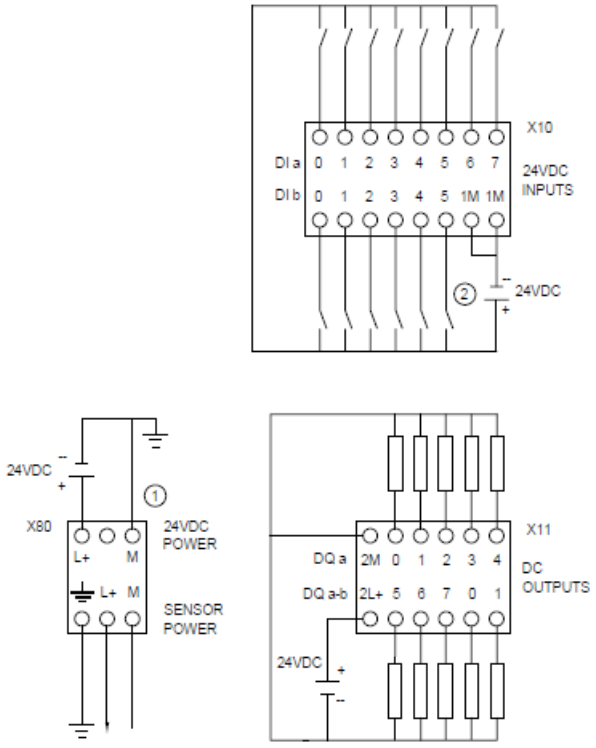


X80: DC power wiring terminal (Gray, No keying)								
DC power	L+		M					
Pin #	1	3	5					
Pin #	2	4	6					
Sensor power	GND	L+	M					
X10: DC input wiring terminal (Gray, No keying)								
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	DI a.5	DI a.6	DI a.7
Pin #	1	3	5	7	9	11	13	15
Pin #	2	4	6	8	10	12	14	16
Signal	DI b.0	DI b.1	DI b.2	DI b.3	DI b.4	DI b.5	1M	1M
X11: Relay output wiring terminal (Orange, Type-A keying)								
Signal	1L	DQ a.0	DQ a.1	DQ a.2	DQ a.3	DQ a.4		
Pin #	1	3	5	7	9	11		
Pin #	2	4	6	8	10	12		
Signal	1L	DQ a.5	DQ a.6	DQ a.7	DQ b.0	DQ b.1		

① For additional noise immunity, jumper the 24 V DC Power “M” to Chassis Ground on the connector.

② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

CPU 1214FC DC/DC/DC



X80: DC power wiring terminal (Gray, No keying)								
DC power	L+		M					
Pin #	1	3	5					
Pin #	2	4	6					
Sensor power	GND	L+	M					
X10: DC input wiring terminal (Gray, No keying)								
Signal	DI a.0	DI a.1	DI a.2	DI a.3	DI a.4	DI a.5	DI a.6	DI a.7
Pin #	1	3	5	7	9	11	13	15
Pin #	2	4	6	8	10	12	14	16
Signal	DI b.0	DI b.1	DI b.2	DI b.3	DI b.4	DI b.5	1M	1M
X11: DC output wiring terminal (Gray, No keying)								
Signal	2M	DQ a.0	DQ a.1	DQ a.2	DQ a.3	DQ a.4		
Pin #	1	3	5	7	9	11		
Pin #	2	4	6	8	10	12		
Signal	2L+	DQ a.5	DQ a.6	DQ a.7	DQ b.0	DQ b.1		

① For additional noise immunity, jumper the 24 V DC Power “M” to Chassis Ground on the connector.
② For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.7 Digital signal modules (SMs)

A.7.1 SM 1221 DI 16x24VDC

Table A-43 General specifications

Technical data	**SM 1221 DI 16x24VDC**
Article number	6ES7221-1BH50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	166 grams / 203 grams
Power dissipation	3.2 W
Current consumption (bus)	90 mA max. (5 V DC)
Current consumption (24 V DC)	4.1 mA / input used
Operating environment	Horizontal mounting -20 °C to 60 °C[1]
	Vertical mounting -20 °C to 50 °C[1]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

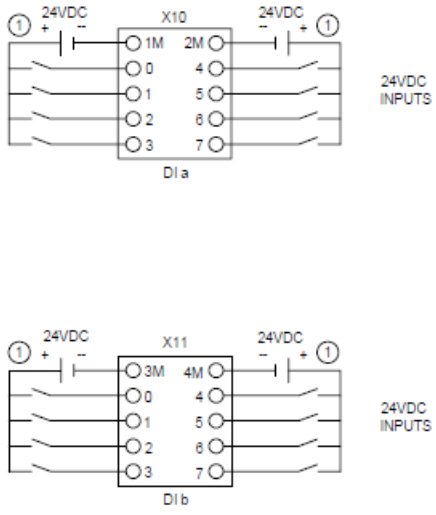
Table A-44 Digital inputs

Technical data	**SM 1221 DI 16x24VDC**
Number of inputs	16
Type	Sink/Source (IEC Type 1 sink)
Rated voltage	24 V DC at 4.1 mA nominal
Continuous permissible voltage	30 V DC max.
Logic 1 signal	15 V DC min. at 2.5 mA
Logic 0 signal	5 V DC max. or 0.5 mA
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	4
Filter times (selectable in groups of 4)	0.2, 0.4, 0.8, 1.6, 3.2, 6.4, and 12.8 ms
Diagnostics	No
Cable length	500 m shielded, 300 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1221 DI 16x24VDC



X10: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
1M	1	2	2M
DI a.0	3	4	DI a.4
DI a.1	5	6	DI a.5
DI a.2	7	8	DI a.6
DI a.3	9	10	DI a.7

X11: Lower User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
3M	1	2	4M
DI b.0	3	4	DI b.4
DI b.1	5	6	DI b.5
DI b.2	7	8	DI b.6
DI b.3	9	10	DI b.7

① For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.7.2 SM 1222 DQ 16x24VDC

Table A-45 General specifications

Technical data	SM 1222 DQ 16x24VDC
Article number	6ES7222-5BH50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	173 grams / 210 grams
Power dissipation	3.5 W
Current consumption (bus)	120 mA max. (5 V DC)
Current consumption (24 V DC)	45 mA
Operating environment	Horizontal mounting -20 °C to 60 °C[1]
	Vertical mounting -20 °C to 50 °C[1]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

Table A-46 Digital outputs

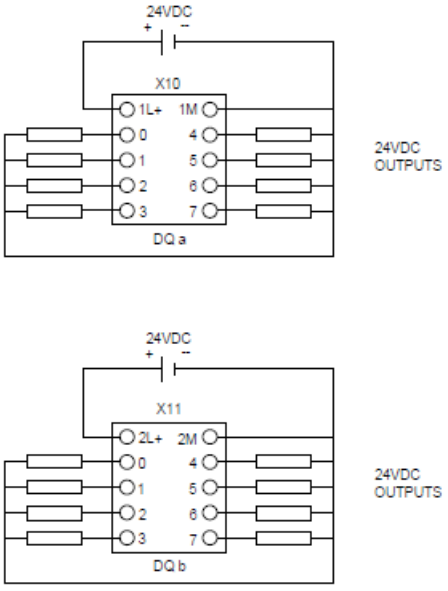
Technical data	SM 1222 DQ 16x24VDC
Number of outputs	16
Type	Solid state – MOSFET (sourcing)
Rated voltage	24 V DC
Voltage range	20.4 to 28.8 V DC
Logic 1 signal at max. current	L+ (-0.5 V)
Logic 0 signal with 10 kΩ load	0.1 V DC max.
Current	0.5 A max.
Lamp load	5 W
ON state resistance	0.6 Ω max.
Leakage current per point	10 µA max.
Overload protection	No
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	2
Current per common	4 A max.
Inductive clamp voltage	L+ minus 40 V, 1 W dissipation
Switching delay	50 µs max. OFF to ON 200 µs max. ON to OFF
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes
Parallel outputs for redundant load control	Yes (with same common)
Parallel outputs for increased load	No

Technical data	SM 1222 DQ 16x24VDC
Diagnostics	24 V DC low voltage
Cable length	500 m shielded, 150 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1222 DQ 16x24VDC



X10: Upper user wiring terminal (Gray, No keying)

Signal	Pin #		Signal
1L+	1	2	1M
DQ a.0	3	4	DQ a.4
DQ a.1	5	6	DQ a.5
DQ a.2	7	8	DQ a.6
DQ a.3	9	10	DQ a.7

X11: Lower user wiring terminal (Gray, No keying)

Signal	Pin #		Signal
2L+	1	2	2M
DQ b.0	3	4	DQ b.4
DQ b.1	5	6	DQ b.5
DQ b.2	7	8	DQ b.6
DQ b.3	9	10	DQ b.7

A.7.3 SM1222 DQ 16xRelay

Table A-47 General specifications

Technical data	SM 1222 DQ 16xRelay
Article number	6ES7222-5HH50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	217 grams / 254 grams
Power dissipation	4.2 W
Current consumption (bus)	115 mA max. (5 V DC)
Current consumption (24 V DC)	10 mA plus 9 mA / relay coil used
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-48 Digital outputs

Technical data	SM 1222 DQ 16xRelay
Number of outputs	16
Type	Relay, mechanical
Voltage range	5 to 30 V DC or 5 to 250 V AC
Current	2.0 A max.
Minimum load[1]	125 mW DC / 500 mW AC
Lamp load	30 W DC / 200 W AC
ON state resistance	0.2 Ω max. when new
Overload protection	No
Isolation (field side to logic)	4200 V DC for 5 seconds + 1600 V DC for 1 minute (type test)
Isolation (coil to logic)	None
Isolation groups	2
Current per common	16 A max. (10 A max. per pin)
Switching delay	10 ms max.
Maximum relay switching frequency	1 Hz
Lifetime mechanical (no load)	10000000 open/close cycles
Lifetime contacts at rated load (N.O. contact)	100000 open/close cycles
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes

[1] When using relays at minimum load, avoid ambient temperatures below 0 °C.

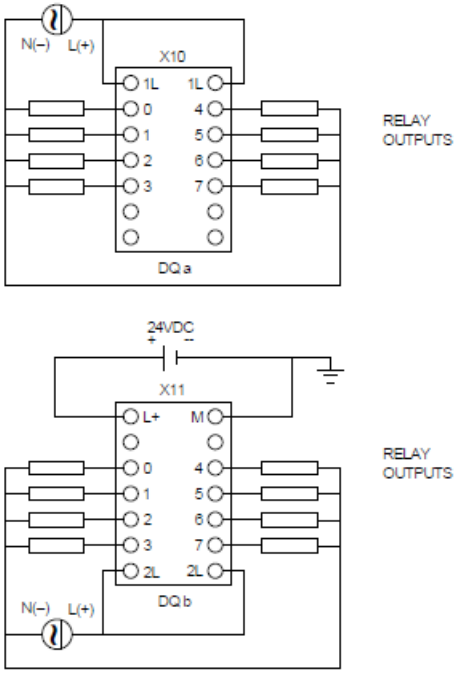
Technical data	SM 1222 DQ 16xRelay
Parallel outputs for redundant load control	Yes (with same common)
Parallel outputs for increased load	No
Diagnostics	24 V DC low voltage
Cable length	500 m shielded, 150 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

[1] When using relays at minimum load, avoid ambient temperatures below 0 °C.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1222 DQ 16xRelay



X10: Upper User Wiring Terminal (Orange, Type-A Keying)

Signal	Pin #		Signal
1L	1	2	1L
DQ a.0	3	4	DQ a.4
DQ a.1	5	6	DQ a.5
DQ a.2	7	8	DQ a.6
DQ a.3	9	10	DQ a.7
	11	12	
	13	14	

X11: Lower User Wiring Terminal (Orange, Type-A Keying)

Signal	Pin #		Signal
L+	1	2	M
	3	4	
DQ b.0	5	6	DQ b.4
DQ b.1	7	8	DQ b.5
DQ b.2	9	10	DQ b.6
DQ b.3	11	12	DQ b.7
2L	13	14	2L

A.7.4 SM 1223 DI 8x24VDC / DQ 8x24VDC

Table A-49 General specifications

Technical data	SM1223 DI 8x24VDC / DQ 8x24VDC
Article number	6ES7223-5BH50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	170 grams / 207 grams
Power dissipation	4.0 W
Current consumption (bus)	110 mA max. (5 V DC)
Current consumption (24 V DC)	60 mA plus 4.1 mA / input used
Operating environment	Horizontal mounting -20 °C to 60 °C[1]
	Vertical mounting -20 °C to 50 °C[1]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

Table A-50 Digital inputs

Technical data	SM 1223 DI 8x24VDC / DQ 8x24VDC
Number of inputs	8
Type	Sink/Source (IEC Type 1 sink)
Rated voltage	24 V DC at 4 mA nominal
Continuous permissible voltage	30 V DC max.
Logic 1 signal	15 V DC min. at 2.5 mA
Logic 0 signal	5 V DC max. or 0.5 mA
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	2
Filter times (selectable in groups of 4)	0.2, 0.4, 0.8, 1.6, 3.2, 6.4, and 12.8 ms
Cable length	500 m shielded, 300 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

Table A-51 Digital outputs

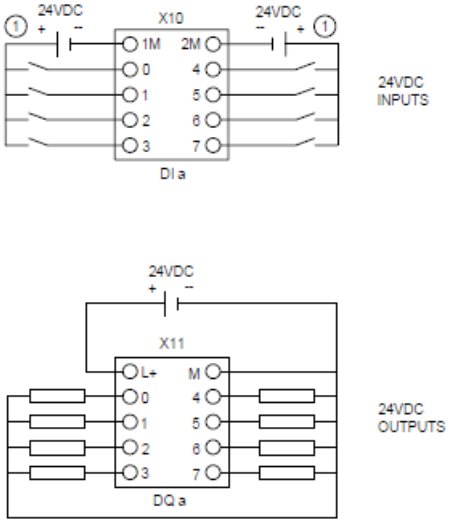
Technical data	SM 1223 DI 8x24VDC / DQ 8x24VDC
Number of outputs	8
Type	Solid state – MOSFET (sourcing)
Rated voltage	24 V DC
Voltage range	20.4 to 28.8 V DC
Logic 1 signal at max. current	L+ (-0.5 V)
Logic 0 signal with 10 kΩ load	0.1 V DC max.
Current	0.5 A max.
Lamp load	5 W

Technical data	**SM 1223 DI 8x24VDC / DQ 8x24VDC**
ON state resistance	0.6 Ω max.
Leakage current per point	10 µA max.
Overload protection	No
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1
Current per common	4 A max.
Inductive clamp voltage	L+ minus 40 V, 1 W dissipation
Switching delay	50 µs max. OFF to ON 200 µs max. ON to OFF
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes
Parallel outputs for redundant load control	Yes (with same common)
Parallel outputs for increased load	No
Diagnostics	24 V DC low voltage
Cable length	500 m shielded, 150 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM1223 DI 8x24VDC / DQ 8x24VDC



X10: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
1M	1	2	2M
DI a.0	3	4	DI a.4
DI a.1	5	6	DI a.5
DI a.2	7	8	DI a.6
DI a.3	9	10	DI a.7

X11: Lower User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
L+	1	2	M
DQ b.0	3	4	DQ b.4
DQ b.1	5	6	DQ b.5
DQ b.2	7	8	DQ b.6
DQ b.3	9	10	DQ b.7

① For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.7.5 SM 1223 DI 8x24VDC / DQ 8xRelay

Table A-52 General specifications

Technical data	SM 1223 DI 8x24VDC / DQ 8xRelay
Article number	6ES7223-5PH50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	194 grams / 231 grams
Power dissipation	4.8 W
Current consumption (bus)	105 mA max. (5 V DC)
Current consumption (24 V DC)	10 mA plus 4.1 mA / input used 9 mA / relay coil used
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-53 Digital inputs

Technical data	SM 1223 DI 8x24VDC / DQ 8xRelay
Number of inputs	8
Type	Sink/Source (IEC Type 1 sink)
Rated voltage	24 V DC at 4 mA nominal
Continuous permissible voltage	30 V DC max.
Logic 1 signal	15 V DC min. at 2.5 mA
Logic 0 signal	5 V DC max. or 0.5 mA
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	2
Filter times (selectable in groups of 4)	0.2, 0.4, 0.8, 1.6, 3.2, 6.4, and 12.8 ms
Cable length	500 m shielded, 300 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

Table A-54 Digital outputs

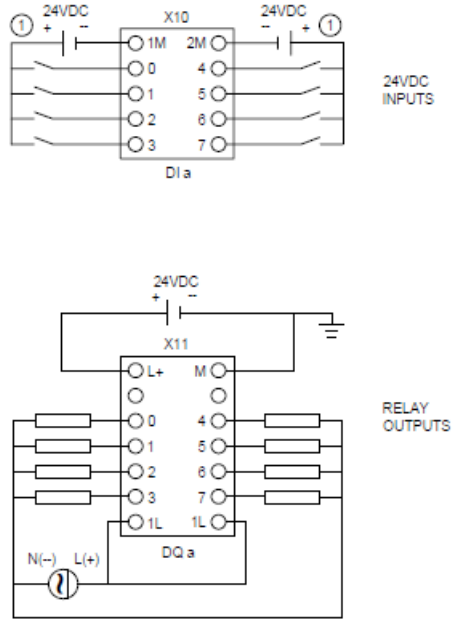
Technical data	**SM 1223 DI 8x24VDC / DQ 8xRelay**
Number of outputs	8
Type	Relay, mechanical
Voltage range	5 to 30 V DC or 5 to 250 V AC
Current	2.0 A max.
Minimum load[1]	125 mW DC / 500 mW AC
Lamp load	30 W DC / 200 W AC
ON state resistance	0.2 Ω max. when new
Overload protection	No
Isolation (field side to logic)	4200 V DC for 5 seconds + 1600 V DC for 1 minute (type test)
Isolation (coil to logic)	None
Isolation groups	1
Current per common	16 A max. (10 A. max per pin)
Switching delay	10 ms max.
Maximum relay switching frequency	1 Hz
Lifetime mechanical (no load)	10000000 open/close cycles
Lifetime contacts at rated load (N.O. contact)	100000 open/close cycles
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes
Parallel outputs for redundant load control	Yes (with same common)
Parallel outputs for increased load	No
Diagnostics	24 V DC low voltage
Cable length	500 m shielded, 150 m unshielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

1 When using relays at minimum load, avoid ambient temperatures below 0 °C.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1223 DI 8x24VDC / DQ 8xRelay



X10: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
1M	1	2	2M
DI a.0	3	4	DI a.4
DI a.1	5	6	DI a.5
DI a.2	7	8	DI a.6
DI a.3	9	10	DI a.7

X11: Lower User Wiring Terminal (Orange, Type-A Keying)

Signal	Pin #		Signal
L+	1	2	M
	3	4	
DQ a.0	5	6	DQ a.4
DQ a.1	7	8	DQ a.5
DQ a.2	9	10	DQ a.6
DQ a.3	11	12	DQ a.7
1L	13	14	1L

① For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.8 Analog signal modules (SMs)

A.8.1 SM 1231 AI 8x14bit

Table A-55 General specifications

Technical data	**SM 1231 AI 8x14bit**
Article number	6ES7231-4HF50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	175 grams / 212 grams
Power dissipation	2.5 W
Current consumption (bus)	75 mA max. (5 V DC)
Current consumption (24 V DC)	45 mA
Operating environment	Horizontal mounting -20 °C to 60 °C[1]
	Vertical mounting -20 °C to 50 °C[1]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

Table A-56 Analog inputs

Technical data	**SM 1231 AI 8x14bit**	
Number of inputs	8	
Type	Voltage or current (differential), selectable in groups of 2	
Range	±10 V, ±5 V, ±2.5 V, 0 to 20 mA or 4 to 20 mA	
Full scale range (data word)	-27648 to 27648 voltage / 0 to 27648 current	
Overshoot/undershoot range (data word)	Voltage: 32511 to 27649 / -27649 to -32512 Current: 32511 to 27649 / 0 to -4864	
Overflow/underflow (data word)	Voltage: 32767 to 32512 / -32513 to -32768 Current 0 to 20 mA: 32767 to 32512 / -4865 to -32768 Current 4 to 20 mA: 32767 to 32512 (values below -4864 indicate open wire)	
Resolution	13 bits plus sign bit	
Maximum withstand voltage/current	±35 V / ±40 mA	
Smoothing	None, weak, medium, or strong	
Noise rejection	400, 60, 50, or 10 Hz	
Input impedance	Before parameterization	>= 1 MΩ
	Voltage	>= 1 MΩ
	Current	< 290 Ω, > 270 Ω
Isolation	Field side to logic	None
	Logic to 24 V DC	None
	Field side to 24 V DC	None
	Channel to channel	None
Accuracy (25 °C / -20 to 60 °C)	±0.1% / ±0.2% of full scale	
Measuring principle	Actual value conversion	

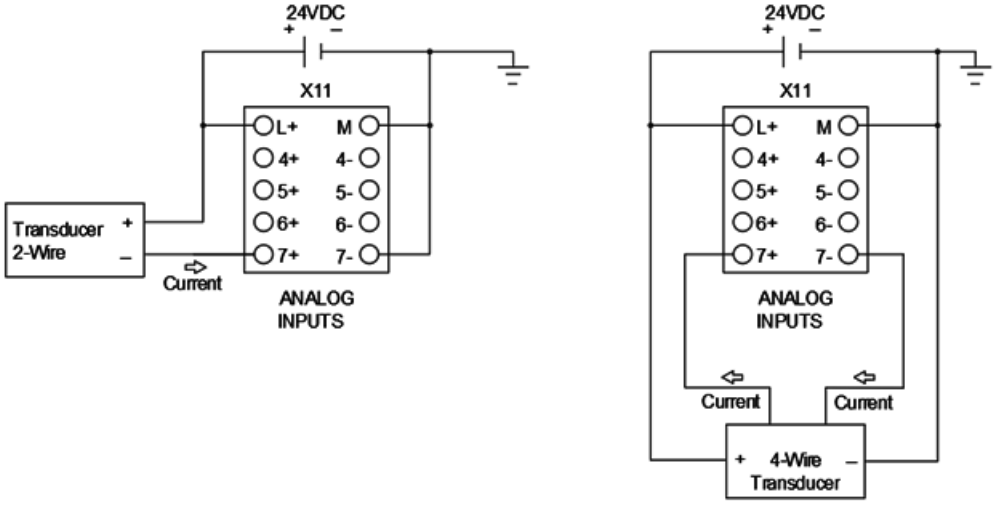
[1] Voltages outside the operational range applied to one channel can cause interference on other channels.

Technical data	SM 1231 AI 8x14bit
Common mode rejection	40 dB, DC to 60 Hz
Operational signal range[1]	Signal plus common mode voltage must be less than +12 V and greater than -12 V
Diagnostics	Overflow/underflow
	24 V DC low voltage
	Open wire, 4 to 20 mA range only (if input is below -4864; 1.185 mA)
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

[1] Voltages outside the operational range applied to one channel can cause interference on other channels.

Current measurement

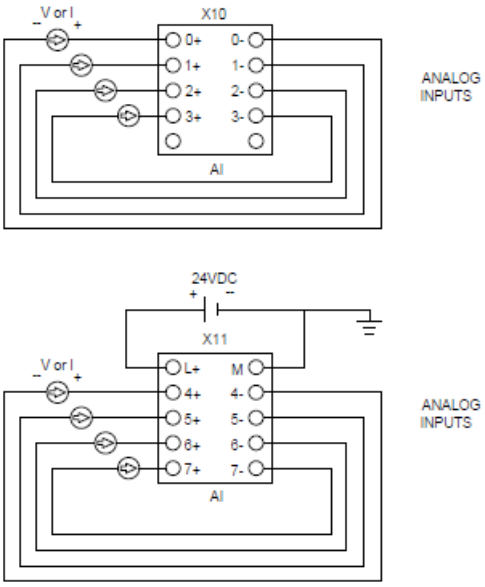
You can implement current measurement with either a 2-wire transducer or a 4-wire transducer as shown below:



Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1231 AI 8x14bit



X10: Upper User Wiring Terminal (Light Gray, Type-B Keying)

Signal	Pin #		Signal
AI 0+	1	2	AI 0-
AI 1+	3	4	AI 1-
AI 2+	5	6	AI 2-
AI 3+	7	8	AI 3-
	9	10	

X11: Lower User Wiring Terminal (Light Gray, Type-B Keying)

Signal	Pin #		Signal
L+	1	2	M
AI 4+	3	4	AI 4-
AI 5+	5	6	AI 5-
AI 6+	7	8	AI 6-
AI 7+	9	10	AI 7-

NOTE

When wiring and configuring analog input channels consider the following:

- Connect the positive input terminal to the negative input terminal on each unused voltage input channel.
- Set unused current input channels to the 0 to 20 mA range and/or disable broken wire error reporting.

Inputs configured for current mode do not conduct loop current if the module is not powered and configured.

Current input channels are operable only when you supply external power to the transmitter.

A.8.2 SM 1232 AQ 8x14bit

Table A-57 General specifications

Technical data	SM 1232 AQ 8x14bit
Article number	6ES7232-4HF50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	173 grams / 210 grams
Power dissipation	5.6 W
Current consumption (bus)	90 mA max. (5 V DC)
Current consumption (24 V DC)	45 mA
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-58 Analog outputs

Technical data	SM 1232 AQ 8x14bit	
Number of outputs	8	
Type	Voltage or current	
Range	±10 V, 0 to 20 mA, or 4 to 20 mA	
Resolution	Voltage: 14 bits Current: 13 bits	
Full scale range (data word)	Voltage: -27648 to 27648 Current: 0 to 27648	
Accuracy (25 °C / -20 to 60 °C)	±0.3% / ±0.6% of full scale	
Settling time (95% of new value)	Voltage: 300 µs (R), 750 µs (1 µF) Current: 600 µs (1 mH), 2 ms (10 mH)	
Load impedance	Voltage: >= 1000 Ω Current: <= 600 Ω	
Maximum output short circuit current	Voltage: <= 24 mA Current: <= 24 mA	
Behavior on RUN to STOP	Last value or substitute value (default value 0)	
Isolation	Field side to logic	None
	24 V to output	None
Diagnostics	Overflow/underflow	
	Short to ground (voltage mode only)[1]	
	Wire break (current mode only)[2]	

[1] Short circuit detection is only possible when the output voltage is less than -0.5 V or greater than +0.5 V.

[2] Wire break detection is only possible when the output current is greater than 1 mA.

Technical data	SM 1232 AQ 8x14bit
Diagnostics	24 V DC low voltage
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 16 (0.2 mm² to 1.5 mm²)

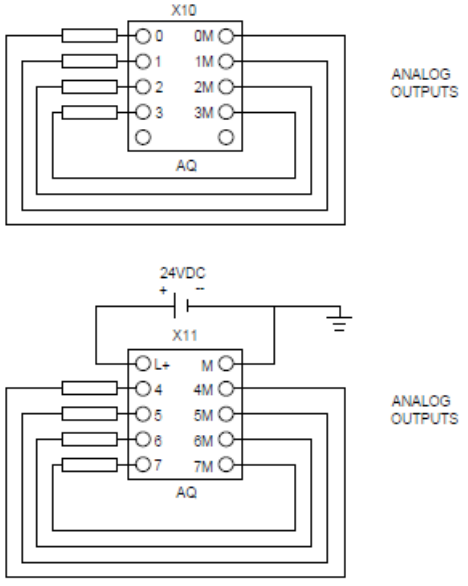
[1] Short circuit detection is only possible when the output voltage is less than -0.5 V or greater than +0.5 V.

[2] Wire break detection is only possible when the output current is greater than 1 mA.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1232 AQ 8x14bit



X10: Upper User Wiring Terminal (Light Gray, Type-B Keying)

Signal	Pin #		Signal
AQ 0	1	2	0M
AQ 1	3	4	1M
AQ 2	5	6	2M
AQ 3	7	8	3M
	9	10	

X11: Lower User Wiring Terminal (Light Gray, Type-B Keying)

Signal	Pin #		Signal
L+	1	2	M
AQ 4	3	4	4M
AQ 5	5	6	5M
AQ 6	7	8	6M
AQ 7	9	10	7M

A.8.3 SM 1233 AI 4x14bit / AQ 4x14bit

Table A-59 General specifications

Technical data	SM 1233 AI 4x14bit / AQ 4x14bit
Article number	6ES7233-4HF50-0XB0
Dimensions W x H x D	30 x 125 x 100 mm
Weight (product/shipping)	174 grams / 211 grams
Power dissipation	4.7 W
Current consumption (bus)	80 mA max. (5 V DC)
Current consumption (24 V DC)	40 mA
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-60 Analog inputs

Technical data	SM 1233 AI 4x14bit / AQ 4x14bit	
Number of inputs	4	
Type	Voltage or current (differential)	
Range	±10 V, ±5 V, ±2.5 V, 0 to 20 mA or 4 to 20 mA	
Full scale range (data word)	-27648 to 27648 voltage / 0 to 27648 current	
Overshoot/undershoot range (data word)	Voltage: 32511 to 27649 / -27649 to -32512 Current: 32511 to 27649 / 0 to -4864	
Overflow/underflow (data word)	Voltage: 32767 to 32512 / -32513 to -32768 Current 0 to 20 mA: 32767 to 32512 / -4865 to -32768 Current 4 to 20 mA: 32767 to 32512 (values below -4864 indicate open wire)	
Resolution	13 bits plus sign bit	
Maximum withstand voltage/current	±35 V / ±40 mA	
Smoothing	None, weak, medium, or strong	
Noise rejection	400, 60, 50, or 10 Hz	
Input impedance	Before parameterization	>= 1 MΩ
	Voltage	>= 1 MΩ
	Current	< 290 Ω, > 270 Ω
Isolation	Field side to logic	None
	Logic to 24 V DC	None
	Field side to 24 V DC	None
	Channel to channel	None

[1] Voltages outside the operational range applied to one channel can cause interference on other channels.

Technical data	**SM 1233 AI 4x14bit / AQ 4x14bit**
Accuracy (25 °C / -20 to 60 °C)	±0.1% / ±0.2% of full scale
Measuring principle	Actual value conversion
Common mode rejection	40 dB, DC to 60 Hz
Operational signal range[1]	Signal plus common mode voltage must be less than +12 V and greater than -12 V
Diagnostics	Overflow/underflow
	24 V DC low voltage
	Open wire, 4 to 20 mA range only (if input is below -4864; 1.185 mA)
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

[1] Voltages outside the operational range applied to one channel can cause interference on other channels.

Table A-61 Analog outputs

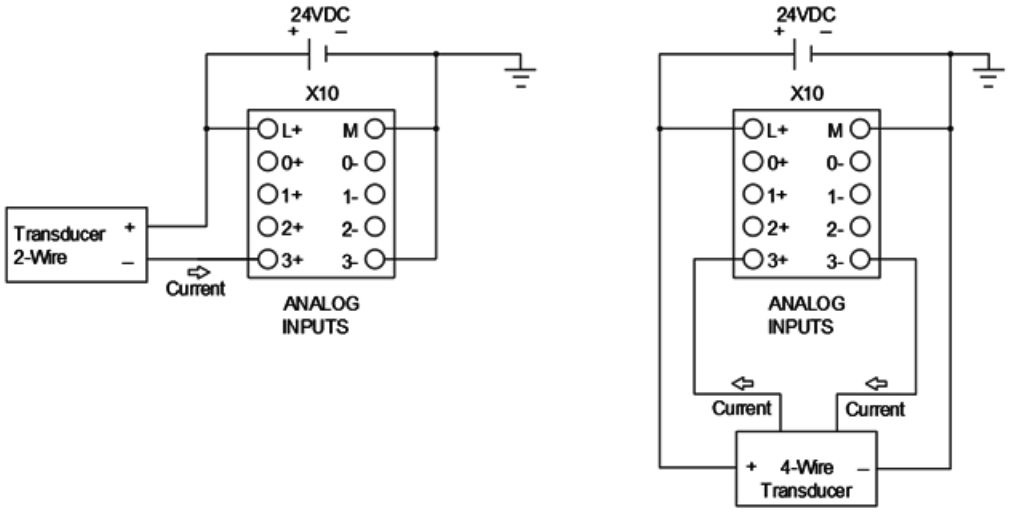
Technical data	**SM 1233 AI 4x14bit / AQ 4x14bit**
Number of outputs	4
Type	Voltage or current
Range	± 10 V, 0 to 20 mA, or 4 to 20 mA
Resolution	Voltage: 14 bits Current: 13 bits
Full scale range (data word)	Voltage: -27648 to 27648 Current: 0 to 27648
Accuracy (25 °C / -20 to 60 °C)	±0.3% / ±0.6% of full scale
Settling time (95% of new value)	Voltage: 300 µs (R), 750 µs (1 µF) Current: 600 µs (1 mH), 2 ms (10 mH)
Load impedance	Voltage: >= 1000 Ω Current: <= 600 Ω
Maximum output short circuit current	Voltage: <= 24 mA Current: <= 24 mA
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Isolation (field side to logic)	None
Isolation (24 V to output)	None
Diagnostics	Overflow/underflow
	Short to ground (voltage mode only)[1]
	Wire break (current mode only)[2]
	24 V DC low voltage
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

[1] Short circuit detection is only possible when the output voltage is less than -0.5 V or greater than +0.5 V.

[2] Wire break detection is only possible when the output current is greater than 1 mA

Current measurement

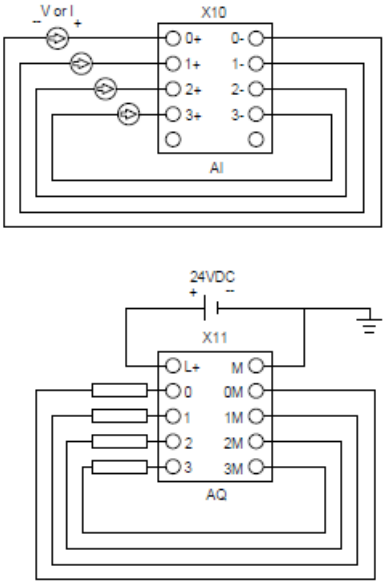
You can implement current measurement with either a 2-wire transducer or a 4-wire transducer as shown below:



Wiring diagram

The wiring diagram and pin connector locations are shown below:

SM 1233 AI 4x14bit / AQ 4x14bit



X10: Upper User Wiring Terminal (Light Gray, Type-B Keying)

Signal	Pin #		Signal
AI 0+	1	2	AI 0-
AI 1+	3	4	AI 1-
AI 2+	5	6	AI 2-
AI 3+	7	8	AI 3-
	9	10	

X11: Lower User Wiring Terminal (Light Gray, Type-B Keying)

Signal	Pin #		Signal
L+	1	2	M
AQ 0	3	4	0M
AQ 1	5	6	1M
AQ 2	7	8	2M
AQ 3	9	10	3M

NOTE

When wiring and configuring analog input channels consider the following:

- Connect the positive input terminal to the negative input terminal on each unused voltage input channel.
- Set unused current input channels to the 0 to 20 mA range and/or disable broken wire error reporting.

Inputs configured for current mode do not conduct loop current if the module is not powered and configured.

Current input channels are operable only when you supply external power to the transmitter.

A.8.4 Step response of the analog inputs

Table A-62 Step response (ms), 0 to full scale measured at 95%

Smoothing selection (sample averaging)	Noise reduction/rejection frequency (Integration time selection)			
	400 Hz (2.5 ms)	60 Hz (16.6 ms)	50 Hz (20 ms)	10 Hz (100 ms)
None (1 cycle): No averaging	4 ms	18 ms	22 ms	100 ms
Weak (4 cycles): 4 samples	9 ms	52 ms	63 ms	320 ms
Medium (16 cycles): 16 samples	32 ms	203 ms	241 ms	1200 ms
Strong (32 cycles): 32 samples	61 ms	400 ms	483 ms	2410 ms

A.8.5 Sample time and update times for the analog inputs

Table A-63 Sample time and update times for the analog inputs, all channels

Rejection frequency (Integration time)	Sample and module update times for all channels			
	400 Hz (2.5 ms)	60 Hz (16.6 ms)	50 Hz (20 ms)	10 Hz (100 ms)
4 channels	0.625 ms	4.17 ms	5 ms	25 ms
8 channels	1.25 ms	4.17 ms	5 ms	25 ms

A.8.6 Measurement ranges of the analog inputs for voltage and current

Table A-64 Analog input representation for voltage

System		Voltage measuring range				
Decimal	Hexadecimal	+/- 10 V	+/- 5 V	+/- 2.5 V	+/- 1.25 V	
32767	7FFF[1]	11.851 V	5.926 V	2.963 V	1.481 V	Overflow
32512	7F00					
32511	7EFF	11.759 V	5.879 V	2.940 V	1.470 V	Overshoot range
27649	6C01					
27648	6C00	10 V	5 V	2.5 V	1.250 V	Rated range
20736	5100	7.5 V	3.75 V	1.875 V	0.938 V	
1	1	361.7 µV	180.8 µV	90.4 µV	45.2 µV	
0	0	0 V	0 V	0 V	0 V	
-1	FFFF					
-20736	AF00	-7.5 V	-3.75 V	-1.875 V	-0.938 V	
-27648	9400	-10 V	-5 V	-2.5 V	-1.250 V	
-27649	93FF					Undershoot

[1] The channel can return 7FFF for one of the following reasons: overflow (as noted in this table), before valid values are available (for example, immediately upon a power up), or if a wire break is detected.

System		Voltage measuring range				
Decimal	**Hexadecimal**	**+/- 10 V**	**+/- 5 V**	**+/- 2.5 V**	**+/- 1.25 V**	
-32512	8100	-11.759 V	-5.879 V	-2.940 V	-1.470 V	range
-32513	80FF					Underflow
-32768	8000	-11.851 V	-5.926 V	-2.963 V	-1.481 V	

[1] The channel can return 7FFF for one of the following reasons: overflow (as noted in this table), before valid values are available (for example, immediately upon a power up), or if a wire break is detected.

Table A-65 Analog input representation for current

System		Current measuring range		
Decimal	**Hexadecimal**	**0 mA to 20 mA**	**4 mA to 20 mA**	
32767	7FFF	> 23.52 mA	> 22.81 mA	Overflow
32511	7EFF	23.52 mA	22.81 mA	Overshoot range
27649	6C01			
27648	6C00	20 mA	20 mA	Nominal range
20736	5100	15 mA	16 mA	
1	1	723.4 nA	4 mA + 578.7 nA	
0	0	0 mA	4 mA	
-1	FFFF			Undershoot range
-4864	ED00	-3.52 mA	1.185 mA	
32767[1]	7FFF		< 1.185 mA	Wire break (4 to 20 mA) (Page 226)
-32768	8000	< -3.52 mA		Underflow (0 to 20 mA)

[1] The wire break value of 32767 (16#7FFF) is always returned regardless of the state of the wire break alarm.

A.8.7 Measurement ranges of the analog outputs for voltage and current

Table A-66 Analog output representation for voltage

System		Voltage output range	
Decimal	**Hexadecimal**	**+/- 10 V**	
32767	7FFF	See note 1	Overflow
32512	7F00	See note 1	
32511	7EFF	11.76 V	Overshoot range
27649	6C01		
27648	6C00	10 V	Rated range
20736	5100	7.5 V	
1	0001	361.7 µV	
0	0000	0 V	
-1	FFFF	-361.7 µV	
-20736	AF00	-7.5 V	
-27648	9400	-10 V	

[1] In an overflow or underflow condition, analog outputs take on the substitute value of the STOP mode.

System		Voltage output range	
Decimal	**Hexadecimal**	**+/- 10 V**	
-27649	93FF		Undershoot range
-32512	8100	-11.76 V	
-32513	80FF	See note 1	Underflow
-32768	8000	See note 1	

[1] In an overflow or underflow condition, analog outputs take on the substitute value of the STOP mode.

Table A-67 Analog output representation for current

System		Current output range		
Decimal	**Hexadecimal**	**0 mA to 20 mA**	**4 mA to 20 mA**	
32767	7FFF	See note 1	See note 1	Overflow
32512	7F00	See note 1	See note 1	
32511	7EFF	23.52 mA	22.81 mA	Overshoot range
27649	6C01			
27648	6C00	20 mA	20 mA	Rated range
20736	5100	15 mA	16 mA	
1	1	723.4 nA	4 mA + 578.7 nA	
0	0	0 mA	4 mA	
-1	FFFF		4 mA to 578.7 nA	Undershoot range
-6912	E500		0 mA	
-6913	E4FF			Not possible. Output value limited to 0 mA.
-32512	8100			
-32513	80FF	See note 1	See note 1	Underflow
-32768	8000	See note 1	See note 1	

[1] In an overflow or underflow condition, analog outputs take on the substitute value of the STOP mode.

A.9 Digital signal boards (SBs)

A.9.1 SB 1221 DI 8x24VDC

Table A-68 General specifications

Technical data	SB 1221 DI 8x24VDC
Article number	6ES7221-3BF50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	26 grams / 53 grams
Power dissipation	2.4 W
Current consumption (bus)	108 mA max. (5 V DC)
Current consumption (24 V DC)	6 mA / input used
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-69 Digital inputs

Technical data	SB 1221 DI 8x24VDC
Number of inputs	8
Type	Sink/Source (IEC Type 1 sink)
Rated voltage	24 V DC at 5.8 mA nominal
Continuous permissible voltage	30 V DC max.
Logic 1 signal	15 V DC min. at 2.5 mA
Logic 0 signal	5 V DC max. or 0.5 mA
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0,12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0
HSC clock input rates (Logic 1 Level = 15 to 26 V DC)	Single phase: 100 kHz max. Quadrature phase: 80 kHz max.
Cable length	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

NOTE

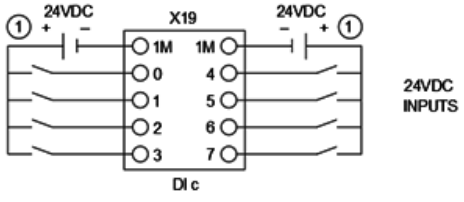
When switching frequencies above 20 kHz, you must have a clean square wave. Consider the following options to improve the signal quality:

- Minimize the cable length.
- Change the driver from a sink or source only to a push-pull driver.
- Change to a higher quality cable.
- Reduce the circuit/components from 24 V to 5 V.
- Add an external load at the input.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1221 DI 8x24VDC



X19: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
1M	1	2	1M
DI c.0	3	4	DI c.4
DI c.1	5	6	DI c.5
DI c.2	7	8	DI c.6
DI c.3	9	10	DI c.7

① For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".

A.9.2 SB 1222 DQ 8x24VDC

Table A-70 General specifications

Technical data	SB 1222 DQ 8x24VDC
Article number	6ES7222-5BF50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	29 grams / 53 grams
Power dissipation	1.0 W
Current consumption (bus)	30 mA max. (5 V DC)
Current consumption (24 V DC)	15 mA
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-71 Digital outputs

Technical data	SB 1222 DQ 8x24VDC
Number of outputs	8
Type	Push-pull
Rated voltage	24 V DC
Voltage range	20.4 to 28.8 V DC
Logic 1 signal at max. current	L+ minus 1.5 V
Logic 0 signal at max. current	1.0 V DC max.
Current	0.1 A max.
Lamp load	--
ON state resistance	4 Ω max.
OFF state resistance	10 Ω max.
Leakage current per point	--
Pulse Train Output (PTO) rate	100 kHz max., 2 Hz min.
Overload protection	Yes
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1
Current per common	0.8 A max.
Inductive clamp voltage	0 V, 1 W dissipation
Switching delay	1.5 µs + 300 ns rise 1.5 µs + 300 ns fall
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes

Technical data	SB 1222 DQ 8x24VDC
Parallel outputs for redundant load control	Yes
Parallel outputs for increased load	No
Diagnostics	24 V DC low voltage
Cable length	500 m shielded, 150 m unshielded, 50 m shielded for PTO outputs
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

NOTE

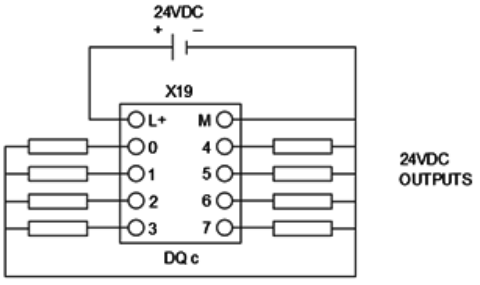
When switching frequencies above 20 kHz, you must have a clean square wave. Consider the following options to improve the signal quality:

- Minimize the cable length.
- Change the driver from a sink or source only to a push-pull driver.
- Change to a higher quality cable.
- Reduce the circuit/components from 24 V to 5 V.
- Add an external load at the input.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1222 DQ 8x24VDC



X19: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
L+	1	2	M
DQ c.0	3	4	DQ c.4
DQ c.1	5	6	DQ c.5
DQ c.2	7	8	DQ c.6
DQ c.3	9	10	DQ c.7

⚠ WARNING

Risk of current leakage from ungrounded connections

Loss of the ground wire connection to the high-speed DQ SBs can allow enough leakage current to activate a DC load resulting in unexpected equipment operation.

Ensure that the M connection wire is securely grounded. If the outputs are used for critical DC load applications, exercise extra caution by using a redundant ground wire to the SB.

Unexpected equipment operation can result in property damage, severe personal injury, and death.

A.9.3 SB 1223 DI 4x24VDC / DQ 4x24VDC

Table A-72 General specifications

Technical data	SB 1223 DI 4x24VDC / DQ 4x24VDC
Article number	6ES7223-7BF50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	28 grams / 55 grams
Power dissipation	1.7 W
Current consumption (bus)	48 mA max. (5 V DC)
Current consumption (24 V DC)	15 mA plus 6 mA / input used
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-73 Digital inputs

Technical data	SB 1223 DI 4x24VDC / DQ 4x24VDC
Number of inputs	4
Type	Sink/Source (IEC Type 1 sink)
Rated voltage	24 V DC at 4 mA nominal
Continuous permissible voltage	30 V DC max.
Logic 1 signal	15 V DC min. at 2.5 mA
Logic 0 signal	5 V DC max. or 0.5 mA
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1 (no isolation inputs to outputs)
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0
HSC clock input rates (Logic 1 Level = 15 to 26 V DC)	Single phase: 100 kHz max. Quadrature phase: 80 kHz max.
Cable length	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

Table A-74 Digital outputs

Technical data	**SB 1223 DI 4x24VDC / DQ 4x24VDC**
Number of outputs	4
Type	Push-pull
Rated voltage	24 V DC
Voltage range	20.4 to 28.8 V DC
Logic 1 signal at max. current	L+ minus 1.5 V
Logic 0 signal at max. current	1.0 V DC max.
Current	0.1 A max.
ON state resistance	4 Ω max.
OFF state resistance	10 Ω max.
Pulse Train Output (PTO) rate	100 kHz max., 2 Hz min.
Overload protection	Yes
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1 (no isolation outputs to inputs)
Current per common	0.4 A max.
Inductive clamp voltage	0 V, 1 W dissipation
Switching delay	1.5 µs + 300 ns rise 1.5 µs + 300 ns fall
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes
Parallel outputs for redundant load control	No
Parallel outputs for increased load	No
Diagnostics	24 V DC low voltage
Cable length	500 m shielded, 150 m unshielded, 50 m shielded for PTO outputs
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

NOTE

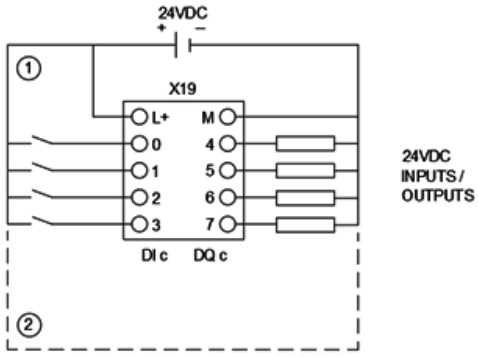
When switching frequencies above 20 kHz, you must have a clean square wave. Consider the following options to improve the signal quality:

- Minimize the cable length.
- Change the driver from a sink or source only to a push-pull driver.
- Change to a higher quality cable.
- Reduce the circuit/components from 24 V to 5 V.
- Add an external load at the input.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1223 DI 4x24VDC / DQ 4x24VDC



X19: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
L+	1	2	M
DI c.0	3	4	DQ c.0
DI c.1	5	6	DQ c.1
DI c.2	7	8	DQ c.2
DI c.3	9	10	DQ c.3

① Wire the input common to (+) when configuring sinking inputs in TIA Portal (shown).
② Wire the input common to (-) when configuring sourcing inputs in TIA Portal.

⚠ WARNING

Risk of current leakage from ungrounded connections

Loss of the ground wire connection to the high-speed DQ SBs can allow enough leakage current to activate a DC load resulting in unexpected equipment operation.

Ensure that the M connection wire is securely grounded. If the outputs are used for critical DC load applications, exercise extra caution by using a redundant ground wire to the SB.

Unexpected equipment operation can result in property damage, severe personal injury, and death.

A.9.4 SB 1223 DI 4x5VDC / DQ 4x5VDC

Table A-75 General specifications

Technical data	SB 1223 DI 4x5VDC / DQ 4x5VDC
Article number	6ES7223-7AF50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	28 grams / 55 grams
Power dissipation	1.0 W
Current consumption (bus)	60 mA max. (5 V DC)
Current consumption (5 V DC)	12 mA plus 15 mA per point used (source)
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-76 Digital inputs

Technical data	SB 1223 DI 4x5VDC / DQ 4x5VDC
Number of inputs	4
Type	Source
Rated voltage	5 V DC at 15 mA nominal
Continuous permissible voltage	6 V DC max.
Logic 1 signal	0 V (20 mA) to L+ minus 2.0 V (5.1 mA) min.
Logic 0 signal	L+ minus 1.0 V (2.2 mA) to L+ (0 mA) max.
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1 (no isolation inputs to outputs)
Filter times (selectable by channel)	µs settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0
HSC clock input rates (Logic 1 Level = 15 to 26 V DC)	Single phase: 200 kHz max. Quadrature phase: 160 kHz max.
Cable length	50 m shielded twisted pair
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

Table A-77 Digital outputs

Technical data	**SB 1223 DI 4x5VDC / DQ 4x5VDC**
Number of outputs	4
Type	Push-pull
Rated voltage	5 V DC
Voltage range	4.25 to 6.0 V DC
Logic 1 signal at max. current	L+ minus 0.7 V
Logic 0 signal at max. current	0.2 V DC max.
Current	0.1 A max.
ON state resistance	7 Ω max.
OFF state resistance	0.2 Ω max.
Pulse Train Output (PTO) rate	200 kHz max., 2 Hz min.
Overload protection	No
Isolation (field side to logic)	707 V DC (type test)
Isolation groups	1 (no isolation outputs to inputs)
Current per common	0.4 A max.
Switching delay	200 ns + 300 ns rise 200 ns + 300 ns fall
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Control of a digital input	Yes
Parallel outputs for redundant load control	No
Parallel outputs for increased load	No
Diagnostics	5 V DC low voltage
Cable length	50 m shielded twisted pair
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

NOTE

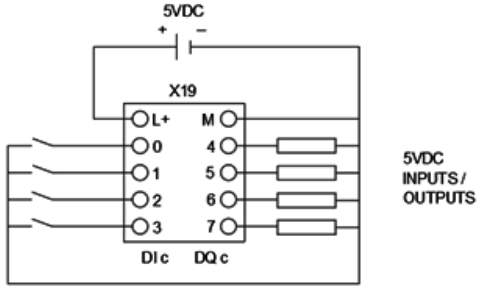
When switching frequencies above 20 kHz, you must have a clean square wave. Consider the following options to improve the signal quality:

- Minimize the cable length.
- Change the driver from a sink or source only to a push-pull driver.
- Change to a higher quality cable.
- Add an external load at the input.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1223 DI 4x5VDC / DQ 4x5VDC



X19: Upper User Wiring Terminal (Gray, No Keying)

Signal	Pin #		Signal
L+	1	2	M
DI c.0	3	4	DQ c.0
DI c.1	5	6	DQ c.1
DI c.2	7	8	DQ c.2
DI c.3	9	10	DQ c.3

A.10 Analog signal boards (SBs)

A.10.1 SB 1231 AI 4x14bit

Table A-78 General specifications

Technical data	SB 1231 AI 4x14bit
Article number	6ES7231-4HD50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	30 grams / 57 grams
Power dissipation	1.4 W
Current consumption (bus)	28 mA max. (5 V DC)
Current consumption (24 V DC)	30 mA
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-79 Analog inputs

Technical data	SB 1231 AI 4x14bit	
Number of inputs	4	
Type	Voltage or current (differential)	
Range	±10 V, ±5 V, ±2.5 V, 0 to 20 mA or 4 to 20 mA	
Full scale range (data word)	-27648 to 27648 voltage / 0 to 27648 current	
Overshoot/undershoot range (data word)	Voltage: 32511 to 27649 / -27649 to -32512 Current: 32511 to 27649 / 0 to -4864	
Overflow/underflow (data word)	Voltage: 32767 to 32512 / -32513 to -32768 Current 0 to 20 mA: 32767 to 32512 / -4865 to -32768 Current 4 to 20 mA: 32767 to 32512 (values below -4864 indicate open wire)	
Resolution	13 bits plus sign bit	
Maximum withstand voltage/current	±35 V / ±40 mA	
Smoothing	None, weak, medium, or strong	
Noise rejection	400, 60, 50, or 10 Hz	
Input impedance	Before parameterization	>= 1 MΩ
	Voltage	>= 1 MΩ
	Current	< 290 Ω, > 270 Ω
Isolation	Field side to logic	None
	Logic to 24 V DC	None
	Field side to 24 V DC	None

[1] The presence of radio frequencies of 500 MHz to 600 MHz can degrade accuracy.

[2] Voltages outside the operational range applied to one channel can cause interference on other channels.

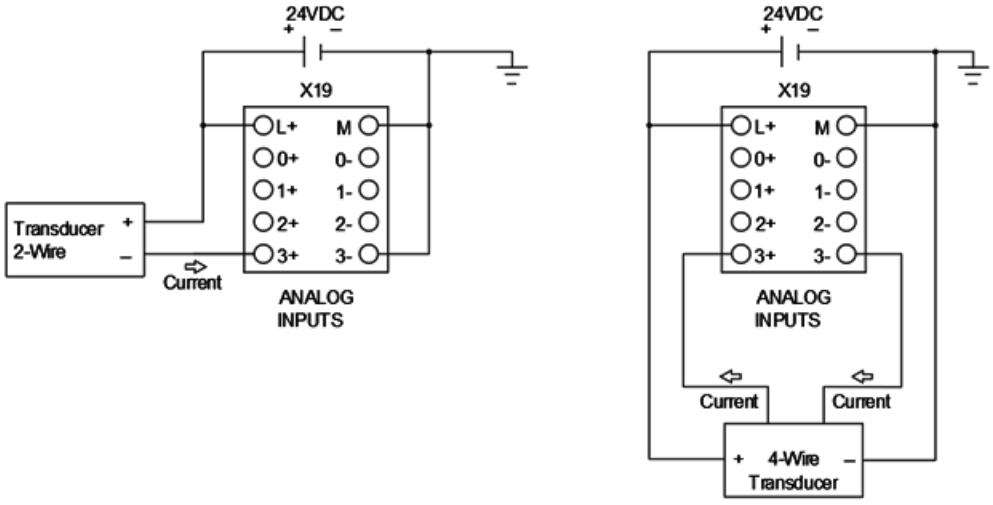
Technical data	**SB 1231 AI 4x14bit**	
Isolation	Channel to channel	None
Accuracy[1](25 °C / -20 to 60 °C)	±0.1% / ±0.2% of full scale	
Measuring principle	Actual value conversion	
Common mode rejection	40 dB, DC to 60 Hz	
Operational signal range[2]	Signal plus common mode voltage must be less than +12 V and greater than -12 V	
Diagnostics	Overflow/underflow	
	24 V DC low voltage	
	Open wire, 4 to 20 mA range only (if input is below -4864; 1.185 mA)	
Cable length	100 m, twisted and shielded	
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)	

1 The presence of radio frequencies of 500 MHz to 600 MHz can degrade accuracy.

2 Voltages outside the operational range applied to one channel can cause interference on other channels.

Current measurement

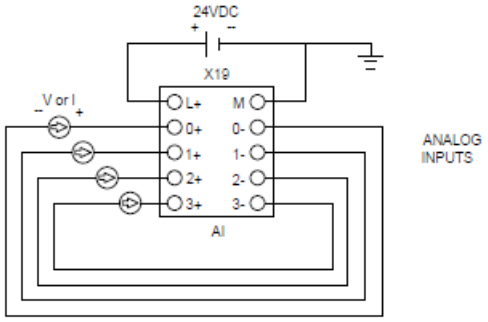
You can implement current measurement with either a 2-wire transducer or a 4-wire transducer as shown below:



Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1231 AI 4x14bit



X19: Upper user wiring terminal (Light gray, No keying)

Signal	Pin #		Signal
L+	1	2	M
AI 0+	3	4	AI 0-
AI 1+	5	6	AI 1-
AI 2+	7	8	AI 2-
AI 3+	9	10	AI 3-

NOTE

When wiring and configuring analog input channels consider the following:

- Connect the positive input terminal to the negative input terminal on each unused voltage input channel.
- Set unused current input channels to the 0 to 20 mA range and/or disable broken wire error reporting.

Inputs configured for current mode do not conduct loop current if the module is not powered and configured.

Current input channels are operable only when you supply external power to the transmitter.

A.10.2 SB 1232 AQ 4x14bit

Table A-80 General specifications

Technical data	SB 1232 AQ 4x14bit
Article number	6ES7232-4HD50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	28 grams / 55 grams
Power dissipation	3.0 W
Current consumption (bus)	25 mA max. (5 V DC)
Current consumption (24 V DC)	30 mA
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-81 Analog outputs

Technical data	SB 1232 AQ 4x14bit
Number of outputs	4
Type	Voltage or current
Range	±10 V, 0 to 20 mA, or 4 to 20 mA
Resolution	Voltage: 14 bits Current: 13 bits
Full scale range (data word)	Voltage: -27648 to 27648 Current: 0 to 27648
Accuracy (25 °C / -20 to 60 °C)	±0.3% / ±0.6% of full scale
Settling time (95% of new value)	Voltage: 300 µs (R), 750 µs (1 µF) Current: 600 µs (1 mH), 2 ms (10 mH)
Load impedance	Voltage: >= 1000 Ω Current: <= 600 Ω
Maximum output short circuit current	Voltage: <= 24 mA Current: <= 24 mA
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Isolation (field side to logic)	None
Isolation (24 V to output)	None
Diagnostics	Overflow/underflow
	Short to ground (voltage mode only)[1]
	Wire break (current mode only)[2]

1 Short circuit detection is only possible when the output voltage is less than -0.5 V or greater than +0.5 V.

2 Wire break detection is only possible when the output current is greater than 1 mA.

Technical data	SB 1232 AQ 4x14bit
Diagnostics	24 V DC low voltage
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

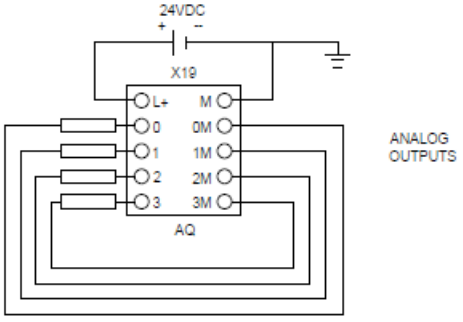
1 Short circuit detection is only possible when the output voltage is less than -0.5 V or greater than +0.5 V.

2 Wire break detection is only possible when the output current is greater than 1 mA.

Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1232 AQ 4 x 14 bit



X19: Upper User Wiring Terminal (Light Gray, No Keying)

Signal	Pin #		Signal
L+	1	2	M
AQ 0	3	4	AQ 0M
AQ 1	5	6	AQ 1M
AQ 2	7	8	AQ 2M
AQ 3	9	10	AQ 3M

A.10.3 SB 1233 AI 2x14bit / AQ 2x14bit

Table A-82 General specifications

Technical data	SB 1233 AI 2x14bit / AQ 2x14bit
Article number	6ES7233-4HD50-0XB0
Dimensions W x H x D	15 x 62 x 63 mm
Weight (product/shipping)	30 grams / 57 grams
Power dissipation	2.0 W
Current consumption (bus)	29 mA max. (5 V DC)
Current consumption (24 V DC)	25 mA
Operating environment	Horizontal mounting -20 °C to 40 °C[1] -20 °C to 60 °C[2]
	Vertical mounting -20 °C to 40 °C[1] -20 °C to 50 °C[2]
	95% relative humidity at 25 °C during operation, without condensation, maximum

[1] Operating temperature range using maximum voltages and maximum specifications

[2] Operating temperature range using rated voltages, 50% of maximum specifications, and alternate I/O active

Table A-83 Analog inputs

Technical data	SB 1233 AI 2x14bit / AQ 2x14bit	
Number of inputs	2	
Type	Voltage or current (differential)	
Range	±10 V, ±5 V, ±2.5 V, 0 to 20 mA or 4 to 20 mA	
Full scale range (data word)	-27648 to 27648 voltage / 0 to 27648 current	
Overshoot/undershoot range (data word)	Voltage: 32511 to 27649 / -27649 to -32512 Current: 32511 to 27649 / 0 to -4864	
Overflow/underflow (data word)	Voltage: 32767 to 32512 / -32513 to -32768 Current 0 to 20 mA: 32767 to 32512 / -4865 to -32768 Current 4 to 20 mA: 32767 to 32512 (values below -4864 indicate open wire)	
Resolution	13 bits plus sign bit	
Maximum withstand voltage/current	±35 V / ±40 mA	
Smoothing	None, weak, medium, or strong	
Noise rejection	400, 60, 50, or 10 Hz	
Input impedance	Before parameterization	>= 1 MΩ
	Voltage	>= 1 MΩ
	Current	< 290 Ω, > 270 Ω
Isolation	Field side to logic	None
	Logic to 24 V DC	None
	Field side to 24 V DC	None
	Channel to channel	None

[1] Voltages outside the operational range applied to one channel can cause interference on other channels.

Technical data	**SB 1233 AI 2x14bit / AQ 2x14bit**
Accuracy (25 °C / -20 to 60 °C)	±0.1% / ±0.2% of full scale
Measuring principle	Actual value conversion
Common mode rejection	40 dB, DC to 60 Hz
Operational signal range[1]	Signal plus common mode voltage must be less than +12 V and greater than -12 V
Diagnostics	Overflow/underflow
	24 V DC low voltage
	Open wire, 4 to 20 mA range only (if input is below -4864; 1.185 mA)
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

[1] Voltages outside the operational range applied to one channel can cause interference on other channels.

Table A-84 Analog outputs

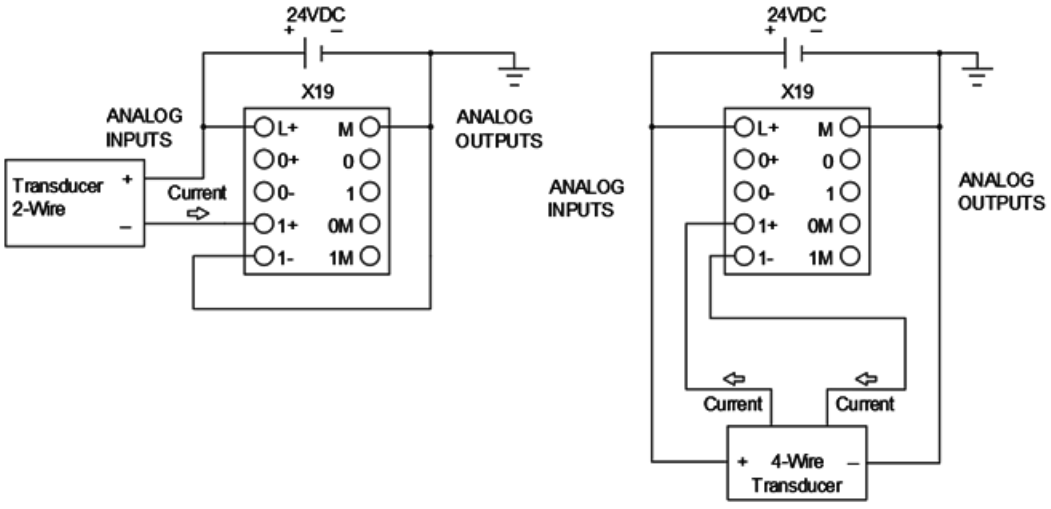
Technical data	**SB 1232 AQ 4x14bit**
Number of outputs	2
Type	Voltage or current
Range	±10 V, 0 to 20 mA, or 4 to 20 mA
Resolution	Voltage: 14 bits Current: 13 bits
Full scale range (data word)	Voltage: -27648 to 27648 Current: 0 to 27648
Accuracy (25 °C / -20 to 60 °C)	±0.3% / ±0.6% of full scale
Settling time (95% of new value)	Voltage: 300 µs (R), 750 µs (1 µF) Current: 600 µs (1 mH), 2 ms (10 mH)
Load impedance	Voltage: >= 1000 Ω Current: <= 600 Ω
Maximum output short circuit current	Voltage: <= 24 mA Current: <= 24 mA
Behavior on RUN to STOP	Last value or substitute value (default value 0)
Isolation (field side to logic)	None
Isolation (24 V to output)	None
Diagnostics	Overflow/underflow
	Short to ground (voltage mode only)[1]
	Wire break (current mode only)[2]
	24 V DC low voltage
Cable length	100 m, twisted and shielded
Cable size	AWG 24 to 18 (0.2 mm^2 to 0.8 mm^2)

[1] Short circuit detection is only possible when the output voltage is less than -0.5 V or greater than +0.5 V.

[2] Wire break detection is only possible when the output current is greater than 1 mA.

Current measurement

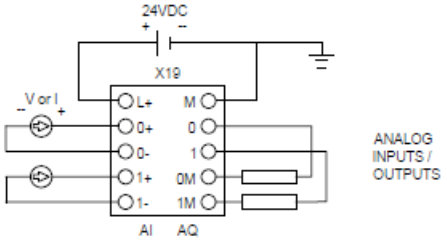
You can implement current measurement with either a 2-wire transducer or a 4-wire transducer as shown below:



Wiring diagram

The wiring diagram and pin connector locations are shown below:

SB 1233 AI 2 x 14 Bit / AQ 2 x 14 Bit



X19: Upper User Wiring Terminal (Light Gray, No Keying)

Signal	Pin #		Signal
L+	1	2	M
AI 0+	3	4	AQ 0
AI 0-	5	6	AQ 1
AI 1+	7	8	AQ 0M
AI 1-	9	10	AQ 1M

NOTE

When wiring and configuring analog input channels consider the following:

- Connect the positive input terminal to the negative input terminal on each unused voltage input channel.
- Set unused current input channels to the 0 to 20 mA range and/or disable broken wire error reporting.

Inputs configured for current mode do not conduct loop current if the module is not powered and configured.

Current input channels are operable only when you supply external power to the transmitter.

A.10.4 Step response of the analog inputs

Table A-85 Step response (ms), 0 to full scale measured at 95%

Smoothing selection (sample averaging)	Noise reduction/rejection frequency (Integration time selection)			
	400 Hz (2.5 ms)	60 Hz (16.6 ms)	50 Hz (20 ms)	10 Hz (100 ms)
None (1 cycle): No averaging	4 ms	18 ms	22 ms	100 ms
Weak (4 cycles): 4 samples	9 ms	52 ms	63 ms	320 ms
Medium (16 cycles): 16 samples	32 ms	203 ms	241 ms	1200 ms
Strong (32 cycles): 32 samples	61 ms	400 ms	483 ms	2410 ms

A.10.5 Sample time and update times for the analog inputs

Table A-86 Sample time and update times

Rejection frequency (Integration time)	Sample and board update times for all channels			
	400 Hz (2.5 ms)	60 Hz (16.6 ms)	50 Hz (20 ms)	10 Hz (100 ms)
2 or 4 channels	0.625 ms	4.17 ms	5 ms	25 ms

A.10.6 Measurement ranges of the analog inputs for voltage and current

Table A-87 Analog input representation for voltage

System		Voltage measuring range				
Decimal	**Hexadecimal**	**+/- 10 V**	**+/- 5 V**	**+/- 2.5 V**	**+/- 1.25 V**	
32767	7FFF[1]	11.851 V	5.926 V	2.963 V	1.481 V	Overflow
32512	7F00					
32511	7EFF	11.759 V	5.879 V	2.940 V	1.470 V	Overshoot range
27649	6C01					
27648	6C00	10 V	5 V	2.5 V	1.250 V	Rated range
20736	5100	7.5 V	3.75 V	1.875 V	0.938 V	
1	1	361.7 µV	180.8 µV	90.4 µV	45.2 µV	
0	0	0 V	0 V	0 V	0 V	
-1	FFFF					
-20736	AF00	-7.5 V	-3.75 V	-1.875 V	-0.938 V	
-27648	9400	-10 V	-5 V	-2.5 V	-1.250 V	
-27649	93FF					Undershoot range
-32512	8100	-11.759 V	-5.879 V	-2.940 V	-1.470 V	
-32513	80FF					Underflow
-32768	8000	-11.851 V	-5.926 V	-2.963 V	-1.481 V	

[1] The channel can return 7FFF for one of the following reasons: overflow (as noted in this table), before valid values are available (for example, immediately upon a power up), or if a wire break is detected.

Table A-88 Analog input representation for current

System		Current measuring range		
Decimal	**Hexadecimal**	**0 mA to 20 mA**	**4 mA to 20 mA**	
32767	7FFF	> 23.52 mA	> 22.81 mA	Overflow
32511	7EFF	23.52 mA	22.81 mA	Overshoot range
27649	6C01			
27648	6C00	20 mA	20 mA	Nominal range
20736	5100	15 mA	16 mA	
1	1	723.4 nA	4 mA + 578.7 nA	
0	0	0 mA	4 mA	
-1	FFFF			Undershoot range
-4864	ED00	-3.52 mA	1.185 mA	
32767[1]	7FFF		< 1.185 mA	Wire break (4 to 20 mA)
-32768	8000	< -3.52 mA		Underflow (0 to 20 mA)

[1] The wire break value of 32767 (16#7FFF) is always returned regardless of the state of the wire break alarm.

A.10.7 Measurement ranges of the analog outputs for voltage and current

Table A-89 Analog output representation for voltage

System		Voltage output range	
Decimal	**Hexadecimal**	**+/- 10 V**	
32767	7FFF	See note 1	Overflow
32512	7F00	See note 1	
32511	7EFF	11.76 V	Overshoot range
27649	6C01		
27648	6C00	10 V	Rated range
20736	5100	7.5 V	
1	0001	361.7 µV	
0	0000	0 V	
-1	FFFF	-361.7 µV	
-20736	AF00	-7.5 V	
-27648	9400	-10 V	
-27649	93FF		Undershoot range
-32512	8100	-11.76 V	
-32513	80FF	See note 1	Underflow
-32768	8000	See note 1	

[1] In an overflow or underflow condition, analog outputs take on the substitute value of the STOP mode.

Table A-90 Analog output representation for current

System		Current output range		
Decimal	**Hexadecimal**	**0 mA to 20 mA**	**4 mA to 20 mA**	
32767	7FFF	See note 1	See note 1	Overflow
32512	7F00	See note 1	See note 1	
32511	7EFF	23.52 mA	22.81 mA	Overshoot range
27649	6C01			
27648	6C00	20 mA	20 mA	Rated range
20736	5100	15 mA	16 mA	
1	1	723.4 nA	4 mA + 578.7 nA	
0	0	0 mA	4 mA	
-1	FFFF		4 mA to 578.7 nA	Undershoot range
-6912	E500		0 mA	
-6913	E4FF			Not possible. Output value limited to 0 mA.
-32512	8100			
-32513	80FF	See note 1	See note 1	Underflow
-32768	8000	See note 1	See note 1	

[1] In an overflow or underflow condition, analog outputs take on the substitute value of the STOP mode.

A.11 Companion products

A.11.1 PM 1207 power module

The PM 1207 is an optional power supply module that you can use to add more power to the SIMATIC S7-1200 G2 system.

Technical data	PM 1207
Article number	6EP3333-4SC00-3AX0 (with EX certification) 6EP3333-4SB00-3AX0 (without EX certification)
Dimensions W x H x D	70 x 125 x 100 mm
Weight (product/shipping)	450 grams / 600 grams
Design format	Matches the S7-1200 G2 shape and color
Input	120 to 240 V AC
Voltage range	85 to 264 V AC
Line frequency	47 to 63 Hz
Input current (full load)	1.1 A at 120 V AC 0.56 A at 240 V AC
Inrush current	43 A max. at 240 V AC
I^2t	1.8 A^2 s
Isolation (input AC to output DC)	3000 V AC
Hold up time (loss of power)	20 ms at 120 V AC 85 ms at 240 V AC
Internal fuse	3.15 A, slow blow, not user replaceable
External miniature circuit breaker recommended	16 A characteristic B or 10 A characteristic C
Output	24 V DC / 5A
UDI diagnostic interface	Yes
Power dissipation	13 W
Current consumption (bus)	Not connected to CPU bus
Operating environment	Horizontal mounting -25 °C to 60 °C[1]
	Vertical mounting -25 °C to 50 °C[1]
	95% relative humidity at 25 °C during operation, without condensation, maximum
Cable size	AWG 24 to 16 (0.2 mm^2 to 1.5 mm^2)

[1] Operating temperature range using maximum voltages and maximum specifications

You can find more information about this module on the product catalog (https://support.industry.siemens.com/cs/us/en/ps) web site.

Ordering information

B

B.1 CPUs

Table B-1 CPUs

CPU models		Article number
CPU 1212C	CPU 1212C AC/DC/RLY	6ES7212-1BG50-0XB0
	CPU 1212C DC/DC/DC	6ES7212-1AG50-0XB0
	CPU 1212C DC/DC/RLY	6ES7212-1HG50-0XB0
CPU 1214C	CPU 1214C AC/DC/RLY	6ES7214-1BH50-0XB0
	CPU 1214C DC/DC/DC	6ES7214-1AH50-0XB0
	CPU 1214C DC/DC/RLY	6ES7214-1HH50-0XB0

Table B-2 Fail-safe CPUs

Fail-safe CPU models		Article number
CPU 1212FC	CPU 1212FC DC/DC/DC	6ES7212-1AF50-0XB0
	CPU 1212FC DC/DC/RLY	6ES7212-1HF50-0XB0
CPU 1214FC	CPU 1214FC DC/DC/DC	6ES7214-1AF50-0XB0
	CPU 1214FC DC/DC/RLY	6ES7214-1HF50-0XB0

B.2 Signal modules (SMs)

Table B-3 Signal modules (SMs)

Signal modules		Article number
Digital input	SM 1221 16 x 24 V DC Input (Sink/Source)	6ES7221-1BH50-0XB0
Digital output	SM 1222 16 x 24 V DC Output (Source)	6ES7222-5BH50-0XB0
	SM 1222 16 x RLY Output	6ES7222-5HH50-0XB0
Digital input / output	SM 1223 8 x 24 V DC Input (Sink/Source) / 8 x 24 V DC Output (Source)	6ES7223-5BH50-0XB0
	SM 1223 8 x 24 V DC Input (Sink/Source) / 8 x RLY Output	6ES7223-5PH50-0XB0
Analog input	SM 1231 8 x Analog Input	6ES7231-4HF50-0XB0
Analog output	SM 1232 8 x Analog Output	6ES7232-4HF50-0XB0
Analog input / output	SM 1233 4 x Analog Input / 4 x Analog Output	6ES7233-4HF50-0XB0

B.3 Signal boards (SBs)

Table B-4 Signal boards (SB)

Signal boards		Article number
Digital input	SB 1221 100 kHz 8 x 24 V DC Input (Sink/Source)	6ES7221-3BF50-0XB0
Digital output	SB 1222 100 kHz 8 x 24 V DC Output (Push-pull)	6ES7222-5BF50-0XB0
Digital input / output	SB 1223 100 kHz 4 x 24 V DC Input (Sink/Source) / 100 kHz 4 x 24 V DC Output (Push-pull)	6ES7223-7BF50-0XB0
	SB 1223 200 kHz 4 x 5 V DC Input (Source) / 200 kHz 4 x 5 V DC Output (Push-pull)	6ES7223-7AF50-0XB0
Analog input	SB 1231 4 x Analog Input	6ES7231-4HD50-0XB0
Analog output	SB 1232 4 x Analog Output	6ES7232-4HD50-0XB0
Analog input / output	SB 1233 2 x Analog Input / 2 x Analog Output	6ES7233-4HD50-0XB0

B.4 Memory cards

SIMATIC memory cards	Description	Article number
Siemens SIMATIC MC	32 GB	6ES7954-8LT04-0AA0
	2 GB	6ES7954-8LP04-0AA0
	256 MB	6ES7954-8LL04-0AA0
	24 MB	6ES7954-8LF04-0AA0
	12 MB	6ES7954-8LE04-0AA0
	4 MB	6ES7954-8LC04-0AA0

Standard memory cards[1]	Description	Article number
Transcend	4 GB, Type SDHC	TS4GSDHC4
	8 GB, Type SDHC	TS8GSDC300S
SanDisk	16 GB, Type SCHC	SDSDBNN-016G-AW6VN
	32 GB, Type SDHC	SDSQUA4-032G-AW6KA
Onn	32 GB, Type SCHC	100006056

[1] You can only use standard memory cards to copy the OSS from the CPU for viewing.

B.5 Spare parts and other hardware

Table B-5 Simulators, spare doors, DIN rails, and end retainer

Item		Article number
Input simulator	Input simulator, 8 position (CPU 1212C, CPU 1212FC)	6ES7274-1XF50-0XA0
	Input simulator, 14 position (CPU 1214C, CPU 1214FC)	6ES7274-1XH50-0XA0
Spare door kit (one pair per kit)	CPU 1212C, CPU 1212FC (70 mm)	6ES7291-1AA50-0XA0
	CPU 1214C, CPU 1214FC (80 mm)	6ES7291-1AB50-0XA0
	SM, CM (30 mm)	6ES7291-1BA50-0XA0
DIN rail	DIN rail 35 mm, length 483 mm	6ES5710-8MA11
	DIN rail 35 mm, length 530 mm	6ES5710-8MA21
	DIN rail 35 mm, length 830 mm	6ES5710-8MA31
	DIN rail 35 mm, length 2000 mm	6ES5710-8MA41
DIN rail end retainer	End retainer thermoplastic, 5.2 mm	8WH9150-0CA00

B.6 Terminal block spare kits

Replacing the terminal block connector

Refer to the tables below and your module specifications to determine the correct terminal block replacement.

NOTE

PLCs require correct wiring to ensure safety and proper operation.

When replacing the terminal block in your S7-1200 G2 CPU or module, it is important that you use the correct terminal block and correct wiring source for your module.

The G2 removable terminal block is designed to prevent you from accidentally placing a high voltage wired terminal block into a low voltage module, or from placing a special voltage wired terminal block into a normal voltage module.

Table B-6 CPU - Terminal block spare kits

CPU (article number)	Use this terminal block spare kit (four per pack)	
	Terminal block description	Terminal block article number
CPU 1212C DC/DC/DC (6ES7212-1AG50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	8 position, tin-plated, gray	6ES7292-2AH50-0XA0
	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
CPU 1212C DC/DC/RLY (6ES7212-1HG50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	8 position, tin-plated, orange	6ES7292-2AH50-0XA3
	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
CPU 1212C AC/DC/RLY (6ES7212-1BG50-0XB0)	6 position, tin-plated, orange	6ES7292-2AF50-0XA3
	8 position, tin-plated, orange	6ES7292-2AH50-0XA3
	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
CPU 1214C DC/DC/DC	6 position, tin-plated, gray	6ES7292-2AF50 0XA0

CPU (article number)	Use this terminal block spare kit (four per pack)	
	Terminal block description	**Terminal block article number**
(6ES7214-1AH50-0XB0)	12 position, tin-plated, gray	6ES7292-2AM50-0XA0
	16 position, tin-plated, gray	6ES7292-2AR50-0XA0
CPU 1214C DC/DC/RLY (6ES7214-1HH50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	12 position, tin-plated, orange	6ES7292-2AM50-0XA3
	16 position, tin-plated, gray	6ES7292-2AR50-0XA0
CPU 1214C AC/DC/RLY (6ES7214-1BH50-0XB0)	6 position, tin-plated, orange	6ES7292-2AF50-0XA3
	12 position, tin-plated, orange	6ES7292-2AM50-0XA3
	16 position, tin-plated, gray	6ES7292-2AR50-0XA0

Table B-7 Fail-safe CPU - Terminal block spare kit

Fail-safe CPU (article number)	Use this terminal block spare kit (four per pack)	
	Terminal block description	**Terminal block article number**
CPU 1212FC DC/DC/DC (6ES7212-1AF50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	8 position, tin-plated, gray	6ES7292-2AH50-0XA0
	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
CPU 1212FC DC/DC/RLY (6ES7212-1HF50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	8 position, tin-plated, orange	6ES7292-2AH50-0XA3
	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
CPU 1214FC DC/DC/DC (6ES7214-1AF50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	12 position, tin-plated, gray	6ES7292-2AM50-0XA0
	16 position, tin-plated, gray	6ES7292-2AR50-0XA0
CPU 1214FC DC/DC/RLY (6ES7214-1HF50-0XB0)	6 position, tin-plated, gray	6ES7292-2AF50 0XA0
	12 position, tin-plated, orange	6ES7292-2AM50-0XA3
	16 position, tin-plated, gray	6ES7292-2AR50-0XA0

Table B-8 SM - Terminal block spare kits

SM (article number)	Use this terminal block spare kit (four per pack)	
	Terminal block description	**Terminal block article number**
SM 1221 16 x 24 V DC Input (Sink/Source) (6ES7221-1BH50-0XB0)	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
SM 1222 16 x 24 V DC Output (Source) (6ES7222-5BH50-0XB0)	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
SM 1222 16 x RLY Output (6ES7222-5HH50-0XB0)	10 position, tin-plated, orange	6ES7292-2AK50-0XA3
	14 position, tin-plated, orange	6ES7292-2AP50-0XA3
SM 1223 8 x 24 V DC Input (Sink/Source) / 8 x 24 V DC Output (Source) (6ES7223-5BH50-0XB0)	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
SM 1223 8 x 24 V DC Input (Sink/Source) / 8 x RLY Output (6ES7223-5PH50-0XB0)	10 position, tin-plated, gray	6ES7292-2AK50-0XA0
	14 position, tin-plated, orange	6ES7292-2AP50-0XA3

SM (article number)	Use this terminal block spare kit (four per pack)	
	Terminal block description	Terminal block article number
SM 1231 8 x Analog Input (6ES7231-4HF50-0XB0)	10 position, gold-plated, light gray	6ES7292-2BK50-0XA4
SM 1232 8 x Analog Output (6ES7232-4HF50-0XB0)		
SM 1233 4 x Analog Input / 4 x Analog Output (6ES7233-4HF50-0XB0)		

Table B-9 SB - Terminal block spare kits

SB (article number)	Use this terminal block spare kit (four per pack)	
	Terminal block description	Terminal block article number
SB 1221 100 kHz DI 8 x DC (6ES7221-3BF50-0XB0)	10 position, tin-plated, gray	6ES7292-4AK50-0XA0
SB 1222 100 kHz DQ 8 x DC (6ES7222-5BF50-0XB0)		
SB 1223 100 kHz DI 4 x DC / DQ 4 x DC (6ES7223-7BF50-0XB0)		
SB 1223 200 kHz 5V DI 4 x DC / DQ 4 x DC (6ES7223-7AF50-0XB0)		
SB 1231 AI 4 (6ES7231-4HD50-0XB0)	10 position, gold plated, light gray	6ES7292-4BK50-0XA4
SB 1232 AQ 4 (6ES7232-4HD50-0XB0)		
SB 1233 AI 2 / AQ 2 (6ES7233-4HD50-0XB0)		

B.7 Programming software

Table B-10 Programming software

SIMATIC software		Article number
Programming software	STEP 7 Basic V20	6ES7822-0AE24-0YA5
	STEP 7 Professional V20	6ES7822-1AE24-0YA5

Safety-relevant symbols

C

C.1 Devices without explosion protection

The following table explains the symbols located on your SIMATIC device, on its packaging, or in the accompanying documentation:

Symbol	Meaning
	General warning sign **Caution/Notice** Read the product documentation. The product documentation contains information about potential risks and enables you to recognize these risks and to implement countermeasures.
	Read the information provided by the product documentation. ISO 7010 M002
	Ensure the device is only installed by an electrically skilled person. IEC 60417 No. 6182
 CABLE SPEC.	Connected mains lines must be designed according to the expected minimum and maximum ambient temperature.
 EMC	The device must be constructed and connected in accordance with EMC regulations.
 230V MODULES	A 230 V device can be exposed to electrical voltages, which can be dangerous. ANSI Z535.2
 24V MODULES	A device of Protection Class III can only be supplied with a protective low voltage according to the standard SELV/PELV. IEC 60417-1-5180 "Class III equipment"
 INDOOR USE ONLY INDUSTRIAL USE ONLY	The device is only approved for the industrial field and only for indoor use.
	An enclosure is required for installing the device. The following are considered to be enclosures: • Standing control cabinet • Modular control cabinet • Terminal boxes • Wall enclosure

C.2 Devices with explosion protection

The following table explains the symbols located on your SIMATIC device, on its packaging, or in the accompanying documentation:

Symbol	Meaning
	General warning sign **Caution/Notice** Read the product documentation. The product documentation contains information about potential risks and enables you to recognize these risks and to implement countermeasures.
	The assigned safety symbol applies to devices **with Ex approval**. Read the product documentation. The product documentation contains information about potential risks and enables you to recognize these risks and to implement countermeasures.
	Read the information provided by the product documentation. ISO 7010 M002
	Ensure the device is only installed by an electrically skilled person. IEC 60417 No. 6182
 F<2N DISPLAY F<4N HOUSING	Observe the mechanical rating of the device.
 CABLE SPEC.	Connected mains lines must be designed according to the expected minimum and maximum ambient temperature.
 EMC	The device must be constructed and connected in accordance with EMC regulations.
 U = 0V	When the device is under voltage, it cannot be installed or removed, or plugged or pulled.
 230V MODULES	A 230 V device can be exposed to electrical voltages, which can be dangerous. ANSI Z535.2
 24V MODULES	A device of Protection Class III can only be supplied with a protective low voltage according to the standard SELV/PELV. IEC 60417-1-5180 "Class III equipment"

Symbol	Meaning
 INDOOR USE ONLY INDUSTRIAL USE ONLY	The device is only approved for the industrial field and only for indoor use.
 ZONE 2 INSIDE CABINET IP54	For Zone 2 potentially explosive atmospheres, the device can only be used when it is installed in an enclosure with a degree of protection ≥ IP54.
 ZONE 22 INSIDE CABINET IP6x	For Zone 22 potentially explosive atmospheres, the device can only be used when it is installed in an enclosure with a degree of protection ≥ IP6x.

Comparison to S7-1200

D

The following tables represent a comparison between S7-1200 and S7-1200 G2:

Major features	S7-1200	S7-1200 G2
Web API Support (Page 195)	Yes (subset)	Yes
Maximum number of concurrent Web API sessions	50	30
iPhone NFC Application (Page 188)	No	Yes
DHCP	No	Yes
DNS	No	Yes
OPC UA Server	Yes	No
Numerous Communication Modules:		
• PROFIBUS	Yes	No
• AS-I Master	Yes	No
• LTE (US and EU)	Yes	No
Configuration control (option handling)	Yes	No
S7 Routing	Yes	No

Features	S7-1200	S7-1200 G2
CPU Variants	1211C, 1212C, 1214C, 1215C, 1217C, 1212FC, 1214FC, 1215FC	1212C 1214C 1212FC 1214FC
Physical Dimensions, W x H x D (mm)	CPU 1211C/1212C: 90 x 100 x 75 CPU 1214C: 110 x 100 x 75 CPU 1215C: 130 x 100 x 75 CPU 1217C: 150 x 100 x 75 SM: 45 or 70 x 100 x 75 CM/CP: 30 x 100 x 75 SB/CB: 38 x 62 x 21	CPU 1212C, CPU 1212FC: 70 x 125 x 100 CPU 1214C, CPU 1214FC: 80 x 125 x 100 SM/CM: 30 or 50 x 125 x 100 SB/CB: 15 x 62 x 63
Built-in Analog	Yes	No, Analogs on optional SBs/SMs
Signal Boards Slots	1 for all CPU variants	CPU 1212C, CPU 1212FC: 1 CPU 1214C, CPU 1214FC: 2
SM/CM/CP	CPU 1211C: 3 CM/CP / 0 SM CPU 1212C: 3 CM/CP / 2 SM CPU 1214C/1215C/1217C: 3 CM/CP / 8 SM	CPU 1212C, CPU 1212FC: 6 total, 3 can be CMs CPU 1214C, CPU 1214FC: 10 total, 3 can be CMs
Module Placement	Left side (CM/CPs) Right side (SMs)	Right side only (CMs must be next to CPU)

Features	S7-1200	S7-1200 G2
Security (Page 114)	Standard Security Measures	Enhanced Security
Number of Ethernet Ports	CPU 1211C/1212C/1214C: 1 port (one interface) CPU 1215C/1217C: 2 switched ports (one interface)	All CPUs: 2 switched ports (one interface)
Load Memory Reporting	ILM only reports program blocks	Reports the size of everything
IRT (Isochronous Real-Time PN) (Page 177)	No Support	HW Support
RT (Real-Time PN)	SW Support	HW Support
Motion Control (Page 197)	Yes	Yes (different)
Number of PROFINET Devices (Page 147)	16	31
Communication Priority	1 (will not interrupt 2 and above)	15 (will not interrupt 16 and above)
Memory Card Evaluation (what happens when you plug a memory card (Page 94))	Evaluates on transition to RUN, power up, and memory reset (MRES)	Evaluates on insertion, power up, and memory reset (MRES)
Work Memory Reporting	Work Memory (included both code and data)	Code Work Memory / Data Work Memory
Cyclic OB (Page 59) (TIA cycle configuration)	milliseconds	microseconds
Synchronous Isochronous Interrupt OB 61	Cyclic only	Tied to Isochronous Scan
Programming Error OB 121 (Page 73) (synchronous)	No	Yes
I/O Access Error OB 122 (Page 74) (synchronous)	No	Yes
Number of User PIP(s) (Page 54)	4	32
Number of Diagnostics buffer (Page 84) Events		
• Visible in the buffer • Retentive	50 50	500 100
Reaction after serious firmware or hardware exception	Attempts defect-mode restart; LEDs show fatal error flash pattern	Attempts defect-mode restart (Page 212); attempts to load device configuration and program; LEDs (Page 208) show fatal error flash pattern;
Alarming configure, display, acknowledge		
• Program alarm wizard • PLC alarms editor • Alarm display • PLC alarm text lists • Central alarm management	No No No Yes No	Yes Yes Yes Yes Yes
Local output substitute values during startup	System automatically sets the output image	System automatically sets the output image
Distributed output substitute values during startup	User must use startup OB to set	User must use startup OB to set
Retentive Memory	14KB	20KB

Features	S7-1200	S7-1200 G2
TIA Languages	LAD, FBD, SCL, and CEM	LAD, FBD, SCL, and CEM
Media Redundancy Protocol (MRP) Support	Yes	Yes
Media Redundancy for Planned Duplication (MRPD) Support	No	Yes
TIA Portal Power Budget Calculation for local rack	No	Yes
Insertion or extraction of modules under power (hot swap)	No	No
EN 60068-2-6 Sinusoidal vibration	DIN rail / Panel mount: 1G/2G	DIN rail / Panel mount: 1G/1G
TOD (End of Month)	Follows START Date and only runs when TOD >= START Date	Ignores START Date and always runs at the end of Month
Enable Outputs in STOP	Allowed when only local IO is configured	Not supported
Backup and restore	Yes	No
CPU clears Temp memory on each OB call		
• Optimized block (OB, FC, or FB)	Yes	Yes
• Non-optimized block (FC or FB)	Yes	No
SIMATIC Controller Profiling (https://support.industry.siemens.com/cs/ww/en/view/109750245)	No	Yes

Instruction set[1] (Page 122)	S7-1200	S7-1200 G2
Legacy instructions		
• FieldRead, FieldWrite	Yes	Superseded by variable array index and multi-dimensional arrays
• CTRL_HSC	Yes	Superseded by CTRL_HSC_EXT
• "Point-to-Point" instructions	Yes	Superseded by "PtP Communication" instructions
• "USS" instructions	Yes	Superseded by "USS communication" instructions
• "MODBUS" instructions	Yes	Superseded by "MODBUS (RTU)" instructions
• TM_MAIL	Yes	Superseded by TMAIL_C
Distributed I/O instructions		
• PROFIBUS[2]	Yes	No
• AS-i control[2]	Yes	No
Communication instructions		
• GPRSComm: CP1242-7	Yes	No

[1] Instruction groups indicate folders in the TIA Portal instruction task card

[2] These instructions are in the Extended instructions > Distributed I/O instructions

Instruction set[1] (Page 122)	**S7-1200**	**S7-1200 G2**
• OPC UA Server	Yes	No
• MODBUS TCP redundancy instructions	Yes	No
Safety instructions		
• RD_ARRAY_I and RD_ARRAY_D	No	Yes
• Range_16	No	Yes
Motion control instructions (Page 197)	Yes	Yes (different)
Alarming Instructions		
• Generate user message	Yes	Yes
• Generate program alarms	No	Yes
• Read status of program alarms	No	Yes
• Copy alarm to DB	No	Yes
• Acknowledge all alarms	No	Yes
• Read alarm resources	No	Yes
PID Instructions		
• Compact PID instructions	Yes	Yes
• Auxiliary functions instructions	Yes	Yes – adds instruction Filter_Universal
Instruction categories (folders in STEP 7 Instructions task card)		
• Process Image	No	Yes
• Module Parameterization	No	Yes
• Cryptography	No	Yes
• Time-based IO (requires IRT and special modules)	No	Yes
• OPC UA	Yes	Future
• Teleservice	Yes	Future (5G)
Miscellaneous instructions in existing categories		
• Move: Array_DB and Symbolic Move instructions	No	Yes
• Convert: REF	No	Yes

1 Instruction groups indicate folders in the TIA Portal instruction task card

2 These instructions are in the Extended instructions > Distributed I/O instructions

Instruction set[1] (Page 122)	S7-1200	S7-1200 G2
• Program Control: INIT_RD and WAIT	No	Yes
• Date and time-of-day: T_COMP and TIME_TCK	No	Yes
• String + Char: S_COMP, JOIN, SPLIT, and GetSymbolForReference	No	Yes
• PROFIEnergy: PE_START_END, PE_CMD, PE_DS3_Write_ET200S, and PE_WOL	No	Yes
• Interrupts: MSK_FLT, DMSK_FLT, READ_ERR, DIS_IRT, and EN_IRT	No	Yes
• Diagnostics:GetClockStatus, and GEN_DIAG	No	Yes
Data consistency for MOVE_BLK and MOVE_BLK_VARIANT	64 bytes	Element size

[1] Instruction groups indicate folders in the TIA Portal instruction task card

[2] These instructions are in the Extended instructions > Distributed I/O instructions

Quantities and default values	S7-1200	S7-1200 G2
Minimum cycle time	Disabled	Enabled (1 ms)
Communication Load	20%	50% See SIMATIC S7-1500, S7-1500R/H, ET 200SP, ET 200pro Cycle and response times (https://support.industry.siemens.com/cs/us/en/view/59193558/-158758826123)
Size of Internal Load Memory	4MB	8 MB
HSC	6	8
PWM/PTO	4	8
Number of CPU connections	68	88
Number of active Trace jobs	2	4
Runtime meters	10	16

Glossary

Autonegotiation

A signaling mechanism and procedure by which two connected devices choose common transmission parameters, such as speed, duplex mode, and flow control

In this process, the connected devices first share their capabilities regarding these parameters and then choose the highest performance transmission mode they both support.

AWG

American Wire Gauge: A standard, predominantly used in North America, that describes the size or diameter of single-stranded, solid, round electrical wire

CB

Communication board: A hardware component used to enable communication between the PLC and other devices or systems

CM

Communication module: A hardware component or device that facilitates communication between different systems, devices, or networks

CTS

Clear to Send: A control signal used in serial communication protocols to coordinate the flow of data between the transmitter and the receiver

When the transmitting device receives a CTS signal, it knows that the receiving device is clear to accept the data transmission.

DNS server

Domain Name System server: A directory of domain names that align with IP addresses

GSD file

General Station Description: Files provide detailed information about the device's capabilities, parameters, and communication properties, allowing the network configuration tool to properly integrate the device into the PROFINET network

IRT

Isochronous Real-Time: A transmission method by which PROFINET devices are synchronized with very high accuracy

MIB file

Management Information Base file: A database used for managing and monitoring network devices in a Simple Network Management Protocol (SNMP) system

NFC

Near Field Communication: A short-range wireless technology that enables devices to exchange data with each other by touching them together or bringing them into close proximity

Optimized DB

Data block with "Optimized block access" selected in the attributes of the Data block properties

An optimized data block maximizes performance, efficiency, and storage utilization.

PID

Proportional-Integral-Derivative: A control loop mechanism that employs feedback, widely used in industrial controls

RTS

Request to Send: A control signal used in serial communication protocols to coordinate the flow of data between the transmitter and the receiver

When the transmitting device sends an RTS signal, it indicates its intention to transmit data and requests permission from the receiving device.

TSAP

Transport Service Access Point: A unique address that identifies a specific communication endpoint within a PLC or other industrial devices

UART

Universal Asynchronous Receiver-Transmitter: A hardware component or interface used to facilitate serial communication between devices

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